General Description

The 843442 is a low jitter, high performance clock generator. The 843442 is designed for use in applications using the SAS and SATA interconnect. The 843442 uses an external, 25MHz, parallel resonant crystal to generate two selectable output frequencies: 75MHz and 150MHz. This silicon based approach provides excellent frequency stability and reliability. The 843442 features down and center spread spectrum (SSC) clocking techniques.

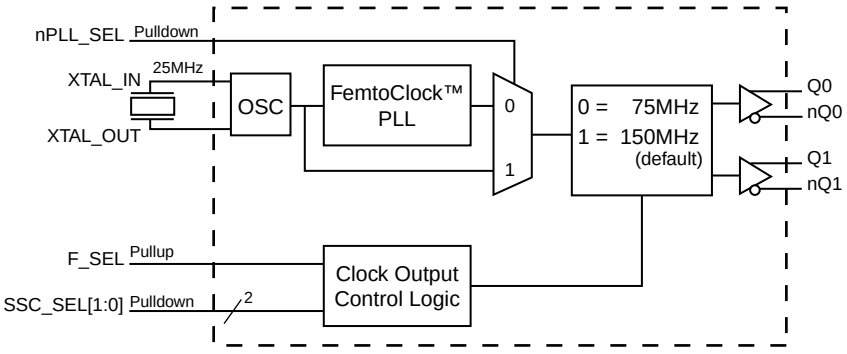
Applications

- SAS/SATA Host Bus Adapters
- SATA Port Multipliers
- SAS I/O Controllers
- TapeDrive and HDD Array Controllers
- SAS Edge and Fanout Expanders
- HDDs and TapeDrives
- Disk Storage Enterprise

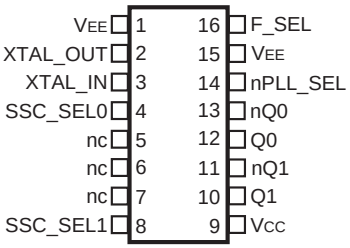
Features

- Designed for use in SAS, SAS-2, and SATA systems
- Center (±0.25%) Spread Spectrum Clocking (SSC)
- Down (-0.23% or -0.5%) SSC
- Two differential 3.3V LVPECL output pairs
- Crystal oscillator interface designed for 25MHz (C_L = 18pF) frequency
- External fundamental crystal frequency ensures high reliability and low aging
- Selectable output frequencies: 75MHz, 150MHz
- Output frequency is tunable with external capacitors
- RMS phase jitter at 150MHz (integrated from 12kHz to 20MHz): 1.07ps (typical)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- **Functional replacement part: 843002AYLF**

Block Diagram



Pin Assignment



843442
16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm package body
G Package
Top View

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Table 1. Pin Descriptions

Number	Name	Type		Description
1, 15	V_{EE}	Power		Negative supply pins.
2, 3	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
4, 8	SSC_SEL0, SSC_SEL1	Input	Pulldown	SSC select pins. See Table 3A. LVCMOS/LVTTL interface levels.
5, 6, 7	nc	Unused		No connect.
9	V_{CC}	Power		Power supply pin.
10, 11	Q1, nQ1	Output		Differential clock outputs. LVPECL interface levels.
12, 13	Q0, nQ0	Output		Differential clock outputs. LVPECL interface levels.
14	nPLL_SEL	Input	Pulldown	PLL Bypass pin. When LOW, selects PLL. When HIGH, bypasses PLL. LVCMOS/LVTTL interface levels.
16	F_SEL	Input	Pullup	Output frequency select pin. See Table 3B. LVCMOS/LVTTL interface levels.

NOTE: *Pullup/Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Tables

Table 3A. SSC_SEL[1:0] Function Table

Inputs		Mode
SSC_SEL1	SSC_SEL0	
0 (default)	0 (default)	SSC Off
0	1	0.5% Down-spread
1	0	0.23% Down-spread
1	1	0.5% Center-spread

Table 3B. F_SEL Function Table

Input	Output Frequency (MHz)
F_SEL	
0	75
1 (default)	150

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Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuos Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	92.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				80	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	F_SEL	V_{CC} = V_{IN} = 3.465V			5	µA
		nPLL_SEL, SSC_SEL[0:1]	V_{CC} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	F_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
		nPLL_SEL, SSC_SEL[0:1]	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA

Table 4C. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		0.9	V

NOTE 1: Output termination with 50Ω to V_{CC} – 2V.

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AC Electrical Characteristics

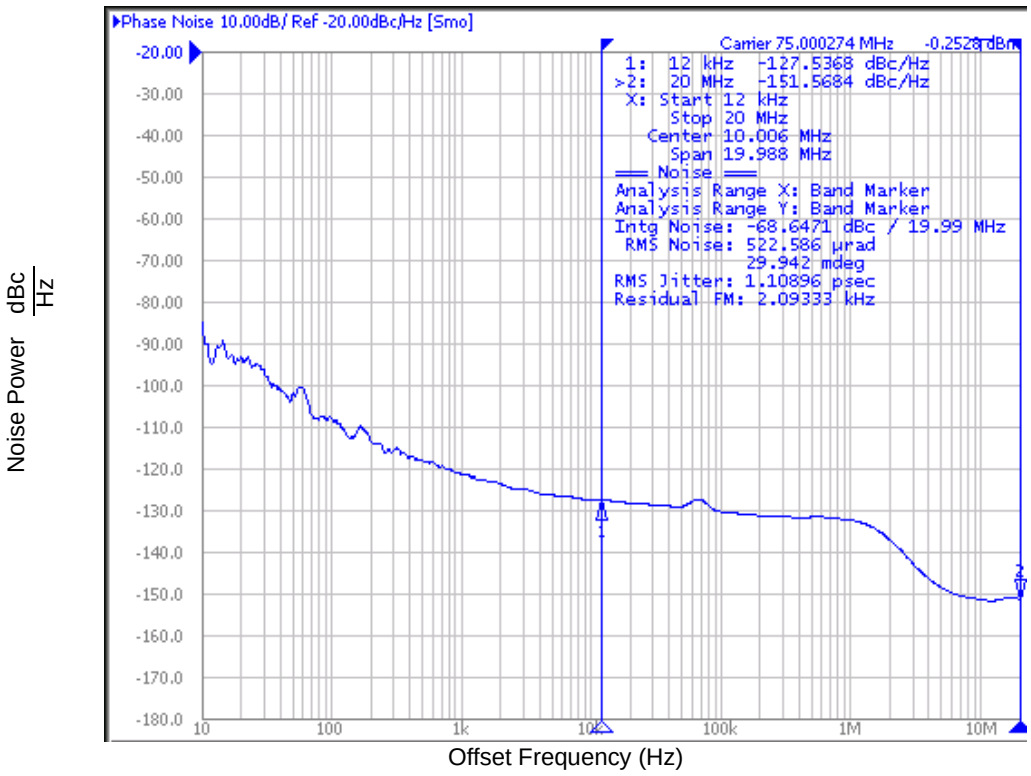
Table 5. AC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL = 0		75		MHz
		F_SEL = 1		150		MHz
$t$jit(Ø)	RMS Phase Jitter (Random); NOTE 1	75MHz, Integration Range: 12kHz – 20MHz		1.10896		ps
		150MHz, Integration Range: 12kHz – 20MHz		1.07375		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	325		650	ps
odc	Output Duty Cycle		48		52	%

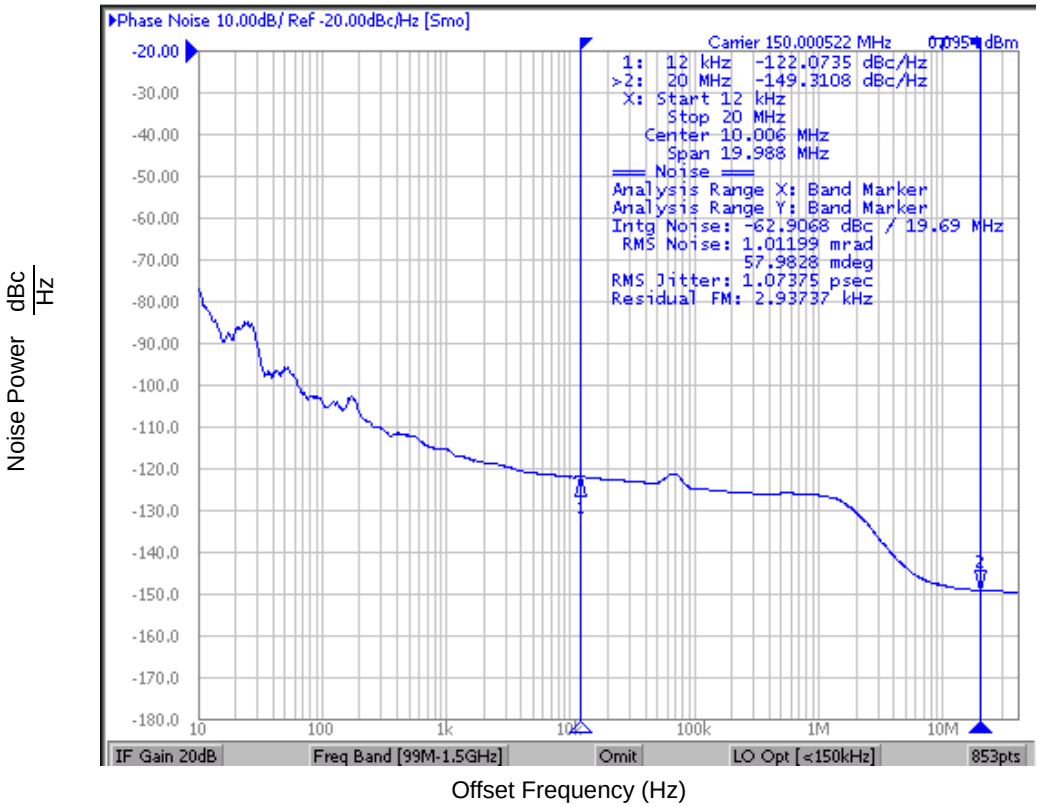
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: See phase noise plot section.

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Typical Phase Noise at 75MHz

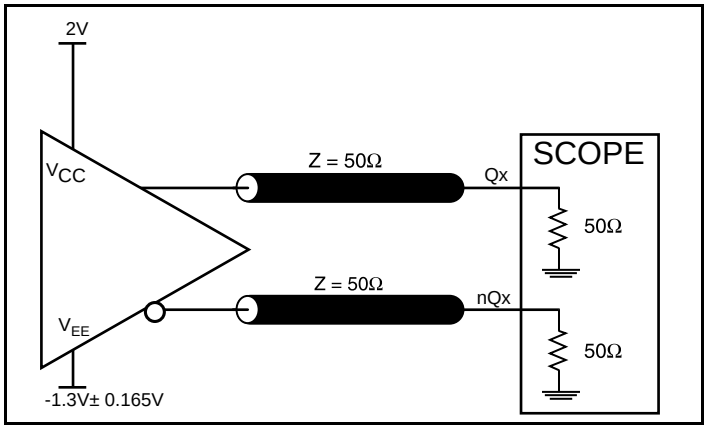


Typical Phase Noise at 150MHz

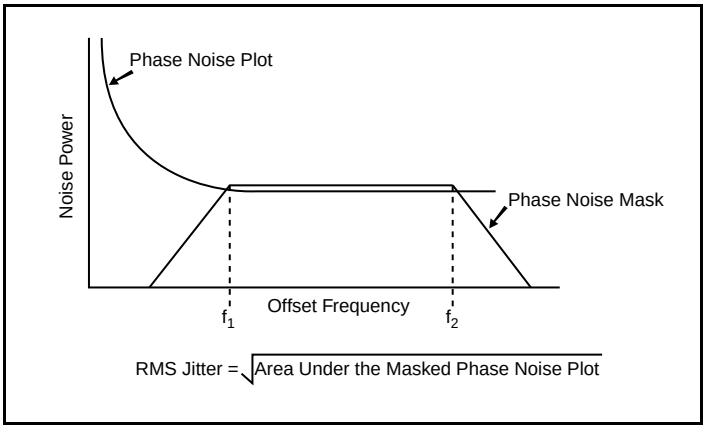


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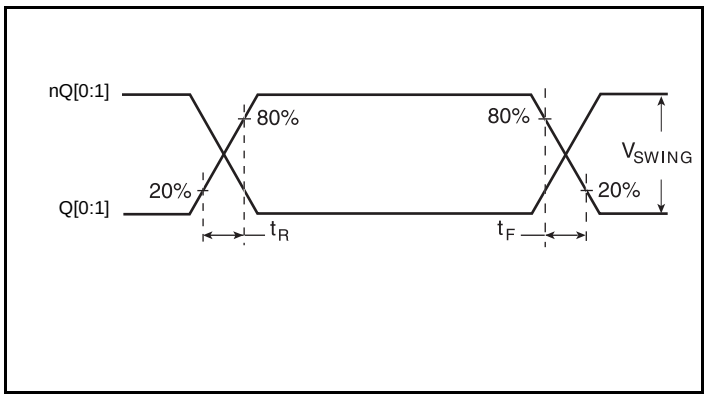
Parameter Measurement Information



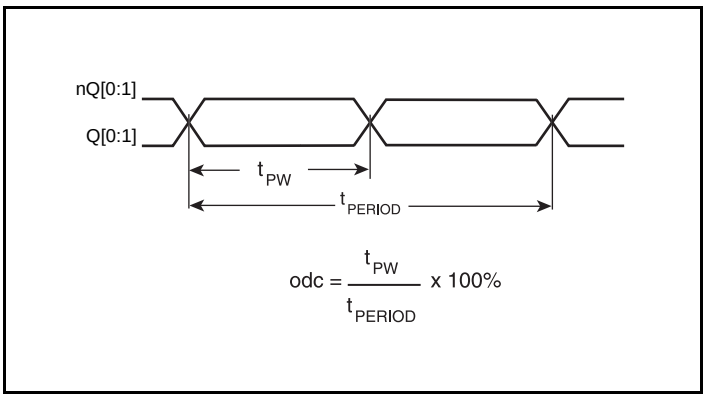
3.3V LVPECL Output Load AC Test Circuit



RMS Phase Jitter



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

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Application Information

Crystal Input Interface

The 843442 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

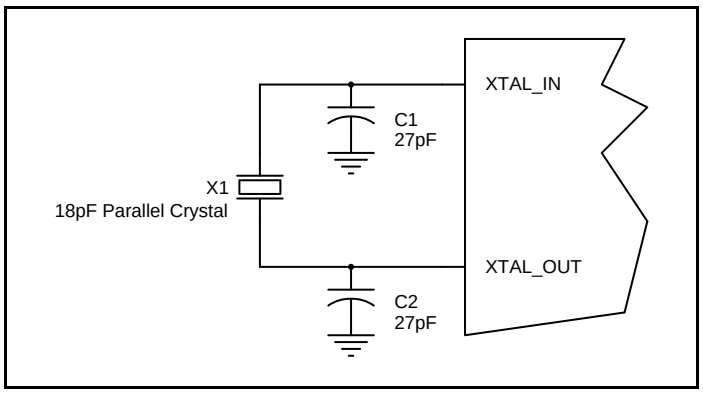


Figure 1. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 2.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

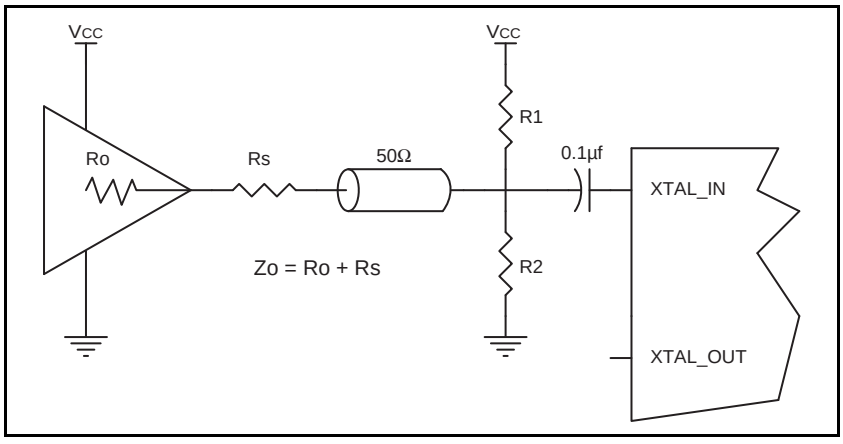


Figure 2. General Diagram for LVCMOS Driver to XTAL Input Interface

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Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups and pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

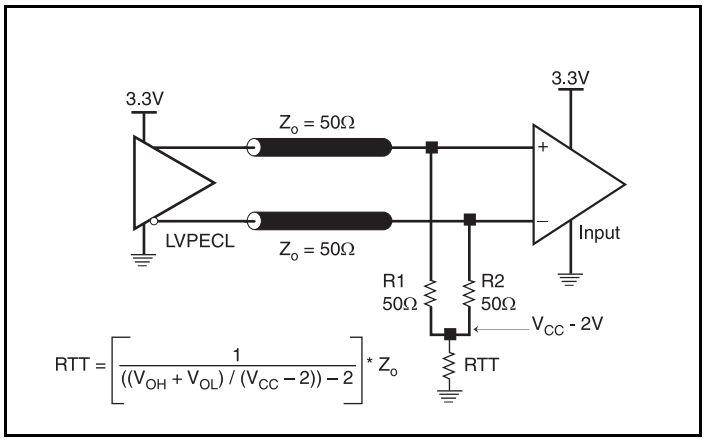


Figure 3A. 3.3V LVPECL Output Termination

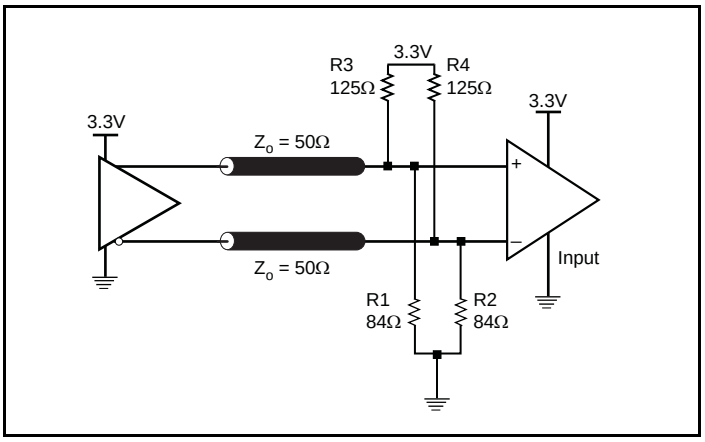


Figure 3B. 3.3V LVPECL Output Termination

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Power Considerations

This section provides information on power dissipation and junction temperature for the 843442.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843442 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 80mA = **277.2mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

Total Power$_{_MAX}$ (3.3V, with all outputs switching) = 277.2mW + 60mW = **337.2mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 92.4°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.337W * 92.4°C/W = 116.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92.4°C/W	88.0°C/W	85.9°C/W

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3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4.*

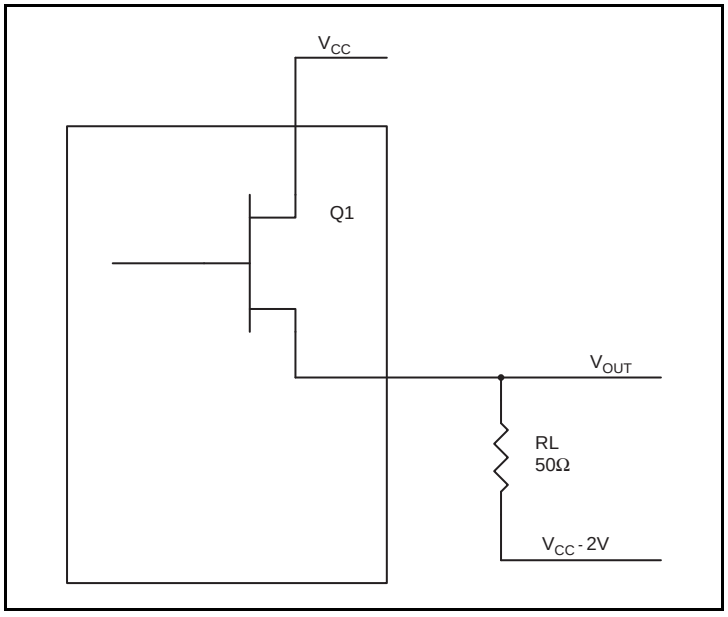


Figure 4. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} =$ **V_{CC_MAX} – 0.9V**
  ($V_{CC_MAX} – V_{OH_MAX}$) = **0.9V**
- For logic low, $V_{OUT} = V_{OL_MAX} =$ **V_{CC_MAX} – 1.7V**
  ($V_{CC_MAX} – V_{OL_MAX}$) = **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd_H = [(V_{OH_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) = [(2V – (V_{CC_MAX} – V_{OH_MAX}))/R_L] * (V_{CC_MAX} – V_{OH_MAX}) =$
$[(2V – 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd_L = [(V_{OL_MAX} – (V_{CC_MAX} – 2V))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) = [(2V – (V_{CC_MAX} – V_{OL_MAX}))/R_L] * (V_{CC_MAX} – V_{OL_MAX}) =$
$[(2V – 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

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Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92.4°C/W	88.0°C/W	85.9°C/W

Transistor Count

The transistor count for 843442 is: 3037

Package Outline and Package Dimensions

Package Outline - G Suffix for 16-Lead TSSOP

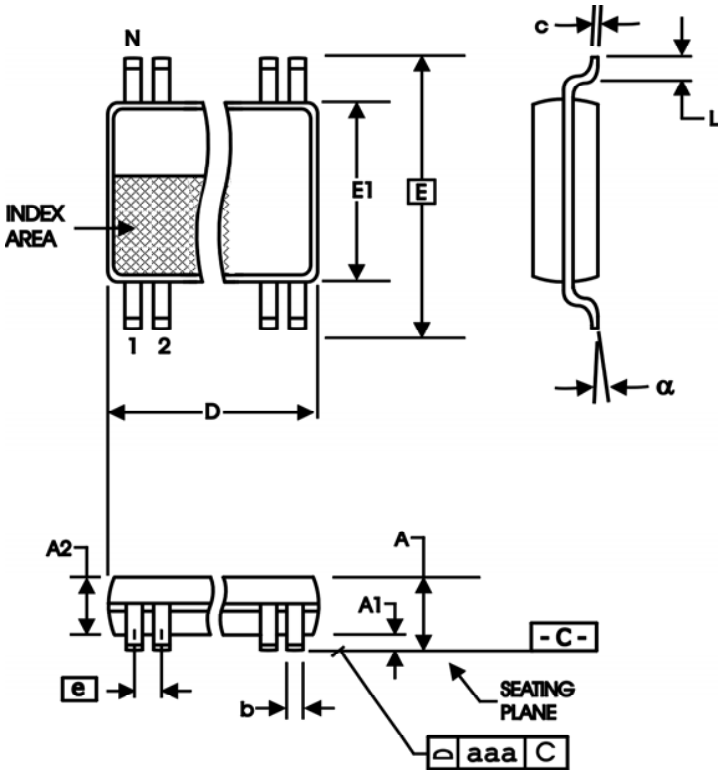


Table 8. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

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Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843442AGILF	43442AIL	16 Lead TSSOP	Tube	-40°C to 85°C
843442AGILFT	43442AIL	16 Lead TSSOP	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
B		1	PDN #CQ-15-04 Product Discontinuance Notice – Last Time buy Expires on August 14, 2016.	08/21/15

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Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com

Tech Support
email: clocks@idt.com

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