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Power Converter Topology and MOSFET Selection for 48-V Telecom Applications

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Introduction

With the recent proliferation of telecommunications equipment, there is more demand than ever for voltage converters that are powered by the nominal 48V telecom supply. Depending on the application and operating environment, the supply voltage range can vary widely. A typical specification can range from a low of 36V to a high of 72- with a 48-V nominal. In some designs, transients in excess of 100V need to be considered. Most of these designs will require input to output isolation of up to 1500V.

Output voltages are frequently 5V and below with 3.3V probably the most common requirement, and 2.5V gaining in popularity. If a processor is on the card, voltages as low as 1.3V are not unlikely. One common approach is to regulate a distributed power bus, say the 5V rail, and then use non-isolated DC/DC converters to generate lower voltages. With the tendency away from 5V, the 3.3V rail is beginning to serve as the distributed bus, although, from the power supply designer's perspective, this is not the most of desirable situations.

Fairchild has recently introduced a family of high voltage MOSFETs ranging from 80- to 200-V drain voltage specifications. This application note will provide information helpful in the proper selection of FETs for primary side switches – available in various types of 48V power converters.

Basic Topologies

There are a nearly endless variety of power converter topologies that can be used for 48V conversion. A large number of considerations will enter into making the final choice. Power level is going to be the main determining factor, although output voltage *and input/output isolation are factors to consider*.

Flyback Converters

Figure 1 shows a basic flyback design using the FDS3670, 100V MOSFET. The circuit illustrated has the advantages of low parts count and simplicity, making it useful for relatively low power levels. Output current is the major limiting factor in flyback designs. The RMS currents in output rectifier(s), transformer secondaries, and output capacitors tend to be large compared to the average output current (i.e., a high crest factor). As such, at high output currents, the secondary side power components tend to get physically large and efficiency suffers. The off-voltage of the primary side power switch is inherently unconstrained in this topology. As this occurs peak voltage is limited by snubbers and/or clamps that generally dissipate power and reduce efficiency. While non-dissipative active clamp schemes have been developed, they are achieved at the expense of significant added complexity.

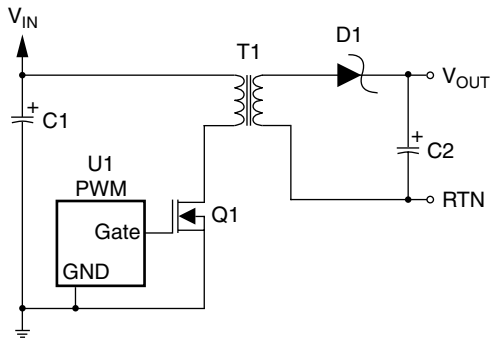

Figure 1. Simplified flyback regulator schematic.

For 36- to 72-V input designs, the FDS3670, 100V MOSFET is the lowest voltage part that should be used. Even then, the drain voltage will have to be carefully controlled with some form of primary side clamp circuit. If the input supply can be expected to experience transient voltages on the order of 100V, the 150V FDS2570 should be considered. It is important to note, two devices would have to be connected in parallel to maintain the same power level that can be achieved with a single FDS3670.

The off-state voltage is determined by the input voltage, output voltage, transformer turns ratio, transformer leakage inductance, and snubber/clamp circuit. Ignoring the effects of leakage inductance, the off voltage is equal to the input voltage plus the output voltage multiplied by the transformer turns ratio. As an example, assuming a 1:1 turns ratio and a 5V output, the off-state drain voltage is equal to Vin plus 5V. The effects of leakage inductance complicate the matter considerably. The energy stored in the leakage inductance is equal to $LI^2/2$, where L is the leakage inductance and I is the peak primary current. This energy appears as a voltage impressed on the various stray capacitances around the circuit. The energy is equal to $CV^2/2$ and, therefore, $V_{pk}=I_{pk}(L/C)^{1/2}$. The problem is complicated by the fact that most of the stray capacitances are nonlinear and vary greatly as a function of the instantaneous voltage applied. As such, an empirical approach to designing the snubbers and clamps is generally used. Figure 2 shows typical waveforms for the flyback regulator. Generally in a 48V application, the maximum useful power level for a flyback design will be around 20 to 30 watts. Above that, consider a single transistor forward converter as shown in Figure 3.

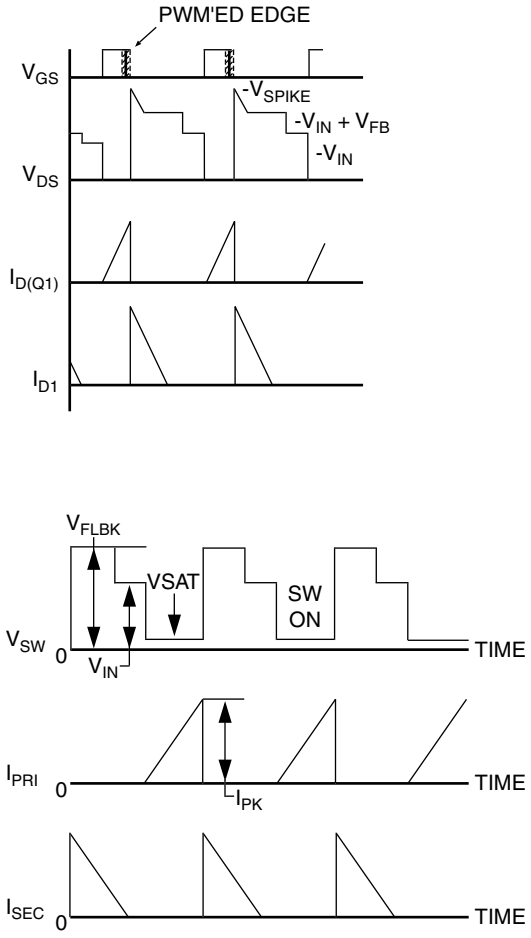

Figure 2. Typical waveforms for the flyback regulator.

Single Transistor Forward Converters

The forward converter achieves much better transformer utilization than the flyback design since in theory, the transformer stores no energy. There is an extra inductor in the output power path and an additional diode as well. Single transistor forward converters are useful in 48V system designs, up to 150 watts or so. A similar problem exists in the forward converter as in the flyback design because the drain voltage is inherently unconstrained. Leakage nductance in the power transformer will produce large *voltage* spikes that must be snubbed or clamped.

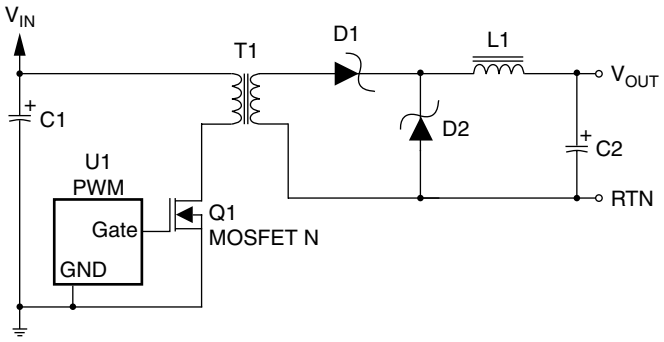

Figure 3. A single transistor forward converter.

Figure 4 shows a design for a typical RCD clamp circuit. The leakage inductance energy is stored in the capacitor, and subsequently burned up in the resistor. The flyback voltage during the primary switch's off state is not forced by the turns ratio as in the flyback design. During the off state the forward output rectifier (D1) essentially disconnects the transformer from the secondary circuit. The resonant effects of the transformer's primary inductance, and the stray capacitance at the switch's drain node control the primary switch drain voltage. This capacitance includes the FET's output capacitance and Miller capacitance, as well as transformer winding capacitances, and reflected secondary rectifier capacitances. Again, the severe nonlinearity of many of these elements leads one to a largely empirical approach to circuit optimization. In general, it is safe to assume that the maximum drain-voltage observed in the off state will be 2.5- to 3-times the input voltage. Therefore, the 200-V FDS2670 is the best choice for these designs. Figure 5 shows the important current and voltage waveforms.

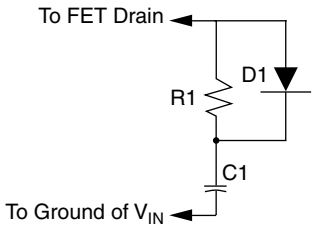

Figure 4. A typical RCD clamp circuit.

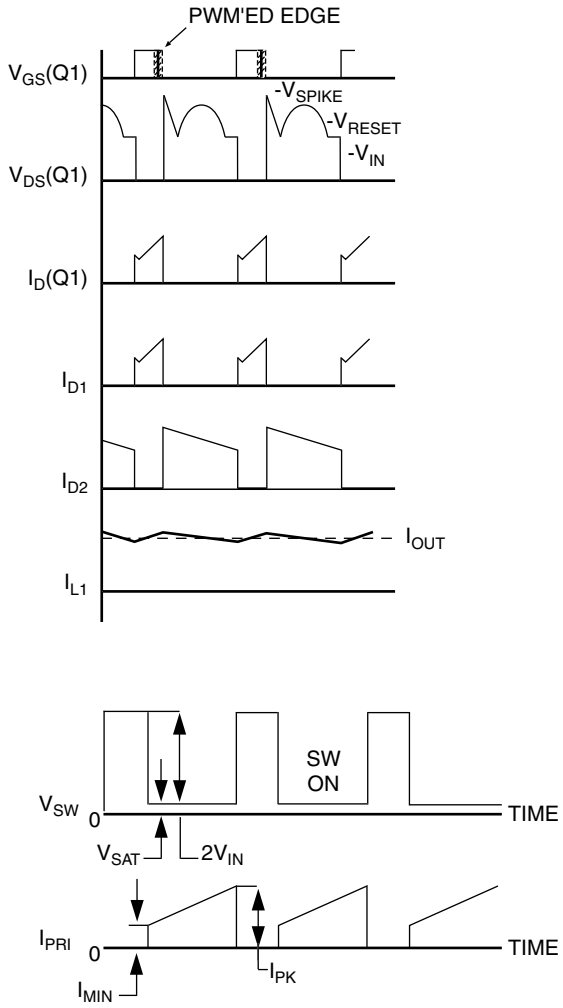

Figure 5. Voltage and current waveforms for a single transistor forward converter.

The average switch current in a Forward converter is equal $P_{OUT}/\eta V_{IN}$ where P_{OUT} is the maximum output power, η is the efficiency, and V_{IN} is the minimum input voltage. With a maximum rating of 3 amps for the FDS2670 and assuming an efficiency of 80%, the maximum output power that can be obtained with a single primary-side FET is approximately 80W. Utilizing two FDS2670 devices in parallel are therefore capable of a theoretical output power of about 160 watts. Note the instantaneous peak switch current is going to be 2.5 to 5 times higher than the average current, depending on the input voltage *range. The wider the input voltage range, the higher the peak switch current.*

Two Transistor Forward Converters

For still higher power levels, up to about 200 watts, the two transistor forward converter of Figure 6 is a good choice. The basics of the circuit's operation are similar to the single transistor design. The difference is that the leakage inductance's energy, and therefore, the drain voltage, is no longer unconstrained. During the off state, the transformer's primary

becomes a current source that forward biases diodes D1 and D2, returning the energy stored in the transformer's primary to the input capacitor. No snubbers or clamps are required, and the maximum off voltage the primary side FET will see is the input voltage, plus a couple of diode drops. Therefore, the 80V FDS3570 is useful in designs that will never have the input exceed of 76V. The 100V FDS3670 will provide a little more design margin if desired. All waveforms are essentially similar to Figure 5 except the FET's drain voltages, which are shown in Figure 7.

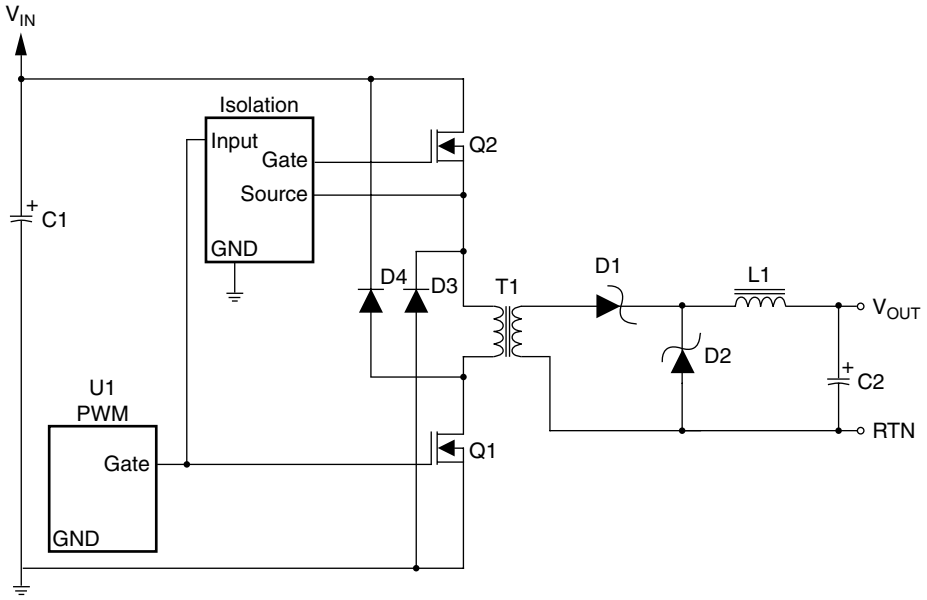

Figure 6. Two transistor forward converter.

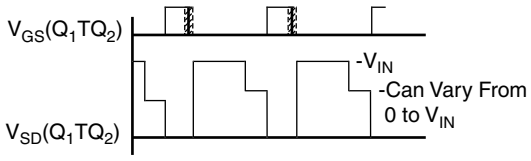

Figure 7. Voltage and current waveforms for two transistor forward converter.

Note that the primary current is the same as the single transistor design example above. However, the FDS3570 has an on-resistance of only 15% than that of the 200V FDS2670 (20*m*Ω vs. 130 mΩ). Even with two transistors in series, the net on-resistance is still much lower than the single high-voltage transistor, *so* a higher power level can be obtained. Efficiency will also be several percentage points higher than the single transistor design since the energy that would be dissipated in snubbers and clamps is, in this case, recovered to the input capacitor. Using the FDS3670's maximum RMS current rating of 9 amps, an assumed efficiency of 83% with 36V in, and a maximum 45% duty factor, gives a maximum output power of 180 watts. Again, it is permissible to parallel FETs in an effort to lower the conduction losses and raise the useable output power of the converter.

Double-Ended Topologies

There are several commonly employed variants of double-ended converters. The terminology implies that the magnetic flux swing in the transformer primary is bi-directional. In other words, the transformer is being actively driven in two directions, as opposed to the forward and fly-back topologies where the transformer is driven in one direction and allowed to reset its core flux naturally. The double-ended approach has the advantage of utilizing the core volume more efficiently, and therefore allowing the use of a physically smaller transformer core. The price paid for this better utilization is more power switches and more complex transformer windings. There are two main topologies to discuss, push-pull and bridge.

Push-Pull Designs

Figure 8 shows a basic push-pull design. The main advantage of this design is grounded-source switches. This allows for a simple gate-drive design, requiring only two switches. The main disadvantage, like the single transistor forward and flyback designs, is the drain voltage of the two switches is inherently unconstrained. Therefore, there will typically be some form of snubbing and/or clamping, usually passive, on the FET drains. Operation is quite simple. Each FET gets turned on for some fraction of one half of an entire cycle. If each FET were to be operated for exactly 50% of a full period, the effective duty factor at the output of the secondary rectifiers would be 100%. This cannot be accomplished in practice, but a close approximation can be achieved. Also, the effective secondary side ripple frequency is doubled. This helps to minimize the size of the secondary inductor. Figure 9 shows idealized gate drive, FET drain, and transformer secondary waveforms. It should be noted that the theoretical minimum drain voltage seen by a primary FET in this configuration is 2-times the DC input voltage. As one FET is driven on, a voltage of Vin is developed across one half of the transformer primary. *An* equal voltage will be induced in the other half of the winding. This voltage is added to the input voltage, and impressed on the drain of the off FET. Since there is also unclamped leakage inductance associated with the transformer primary, there will be spikes substantially higher than twice the input. Consequently, only the 200V FDS2670 is suitable for applications where inputs as high as 72V could occur. About twice the power level of a single transistor forward converter can be obtained.

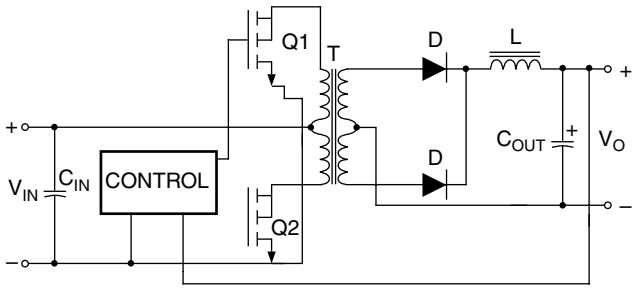

Figure 8. A basic push-pull design.

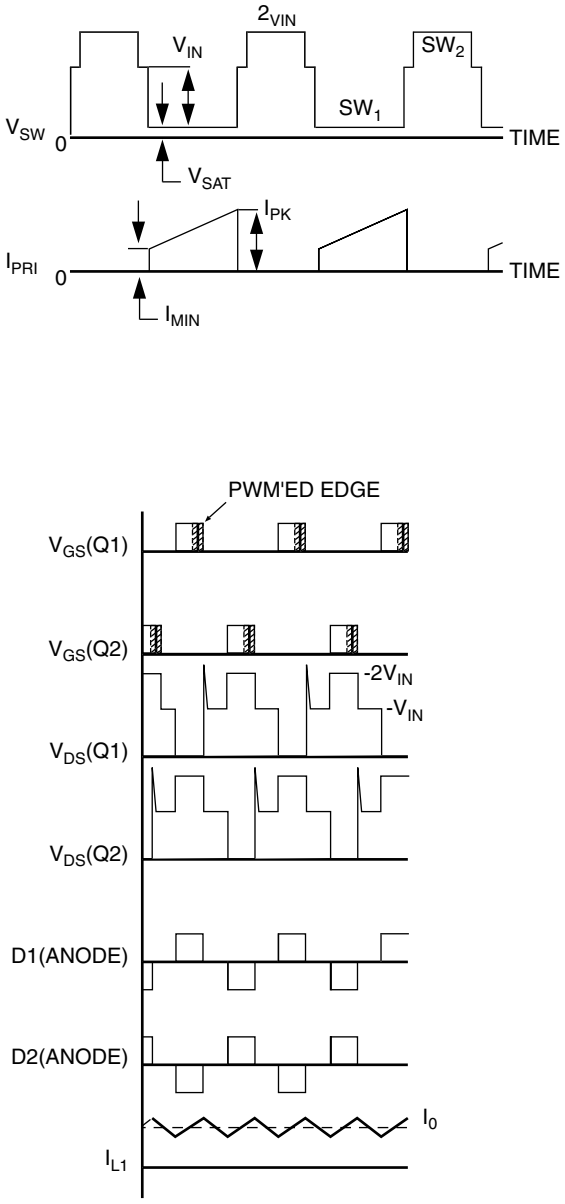

Figure 9. Voltage and current waveforms for the basic push-pull design.

Full-Bridge Designs

Full-bridge designs, sometimes called four transistor bridges, are generally used at very high power levels, mainly due to the cost of these designs. Two of the four switches have floating sources, so they each require an isolated gate drive, usually transformer coupled. The power transformers primary winding design is a simple single winding. The secondary, is generally center-tapped, at least for very low output voltage designs. The main advantage of the bridge topology is that the drain voltages of all four switches are constrained to Vin. Energy in the transformer's leakage inductance gets returned to the input and can help force commutate the switches. The switches get turned on across a diagonal of the bridge. Figure 10 shows the basic circuit design, and Figure 11 shows the idealized waveforms. Since the drain voltage is well clamped to Vin without snubbers, there is no concern for passive energy losses. This also allows the use of the 80V, FDS3570 in all four locations. With these devices, output power

levels approaching 390 watts are theoretically possible. Paralleling FETs allows this number to be increased. The output waveforms of the bridge design look the same as the push pull. The FET drain voltages are depicted in Figure 11.

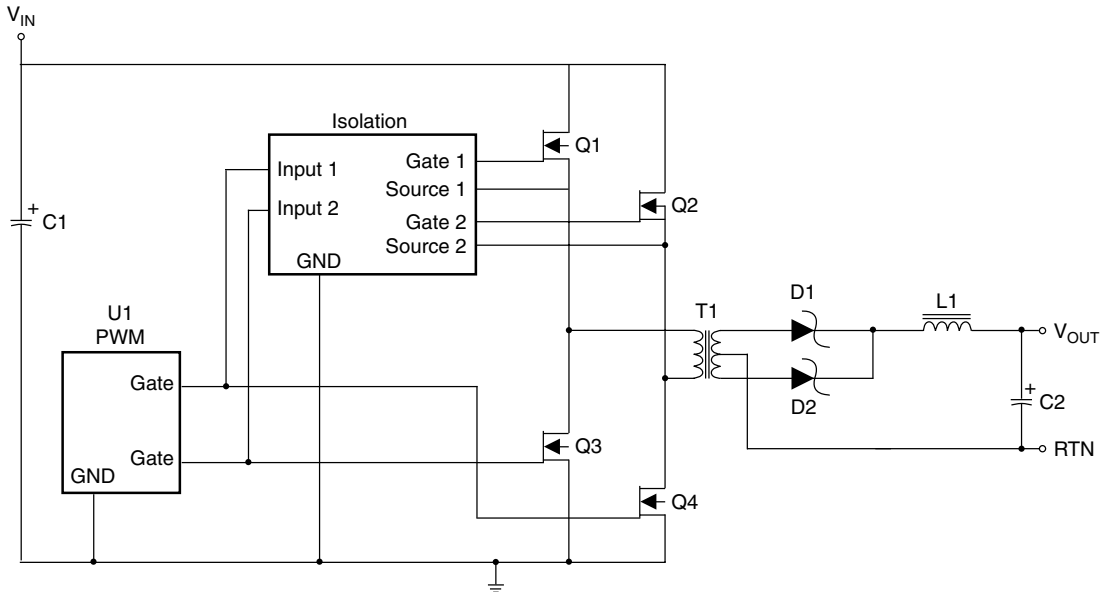

Figure 10. The basic circuit design for a full-bridge regulator topology.

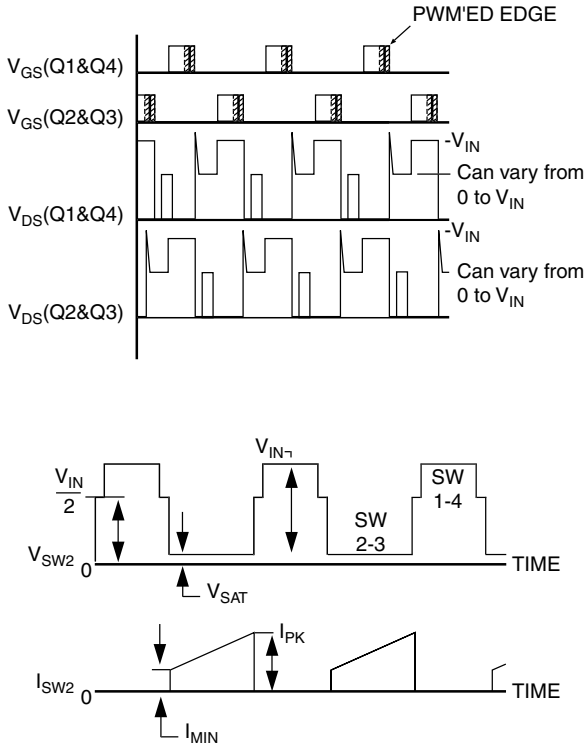

Figure 11. Voltage and current waveforms for the full-bridge regulator.

Table 1 shows the comparison of the topologies that have been discussed. Note that the relative cost increases significantly based on whether there is input/output isolation. Efficiency can range from *70* to *85%*. A summary of the first-pass selection of key MOSFET parameters is shown in Table 2. Parameters of the MOSFETS used in Application Note are shown in Table 3.

Topology	Max. Power (Watts)	Typical Efficiency (%)
Flyback	30	75
1 Transistor Forward	150	80
2 Transistor Forward	200	83
Push Pull	350	80
Full Bridge	500	85

Table 1: Comparison of various switching regulator topologies.

Topology	Maximum Drain Voltage	Average Drain Current
Flyback	1.5Vin(max)	751.5Pout/ Vin(max)
1 Transistor Forward	2.5 to 3.0 Vin(max)	1.3Pout/ Vin(max)0
2 Transistor Forward	Vin(max)	1.2Pout/ Vin(max)
Push Pull	352.5 to 3.0 Vin(max)0	0.65Pout/ Vin(max)
Full Bridge	Vin(max)	0.60Pout/ Vin(max)

Table 2: Power MOSFET voltage and current ratings versus power supply topology.

	Voltage(DS)	Current (ID max)	ON-Resistance (@VGS=10V)
FDS3570	80V	9 A	20 mΩ
FDS3670	100V	6.3A	32 mΩ
FDS2570	150V	4 A	80 mΩ
FDS2670	200V	3 A	130 mΩ

Table 3: PowerTrench® MOSFETs in SO-8 package for 48V Applications.

Synchronous rectification.

Synchronous rectification may be employed with all the previously mentioned topologies. This technique consists of replacing the output rectifiers with MOSFETs, striving to lower conduction losses. The concept is, however, not without its share of problems. The complexity of the drive and control circuitry increases dramatically. Timing of the gate-drive to the synchronous FETs is critical to avoid cross conduction. The parasitic capacitances and body diode reverse recovery characteristics of the output FETs contribute to substantial switching losses in these devices. The technique is most applicable for 12V and lower output voltages. The lower the output voltage, the greater the advantage of synchronous rectification. Much above the 12V level, the large parasitic losses make the approach much less advantageous.

Thermal Considerations

One of the main limiting factors in any power supply design is the ability to keep the junction temperatures of the power devices within *specified* limits. When using surface-mount power devices the primary heat sink is the PC board. The main constituents of PCBs are fiberglass

and copper. For example, we pack fiberglass in our walls to insulate our homes. Hardly the kind of material we would choose to conduct large amounts of heat away from our power devices. Copper is the primary means of conducting heat away from the source and into the air stream. Probably the biggest mistakes made in laying out PCBs for power devices are the removal of copper in the vicinity of the power devices, and the reliance on inner layers for interconnecting the power devices. When possible, leave as much copper around the power devices, and interconnect devices using topside copper. This allows the generated heat to spread laterally and to be removed into the air stream passing over the board. Thicker copper is better, and with most of the manufacturing technology currently in use, thermal reliefs are not required, nor should they be used.

Whenever possible, leave the plane areas under and around the power devices, and the inner layers and backside of the board intact. This helps with the heat spread and power dissipation. For optimal thermal control, add an area of large diameter vias around the power device that connect into the inner and back layers of the board. If possible, allow these vias to fill with solder to form a thermal pipe between all the layers. Avoid vias for power path interconnects, especially the commonly used micro-vias. If vias must be used to run power between layers, use a minimum of one via per amp of average current – two vias per amp are preferred.

Another consideration is the use of thermal pads for conduction of heat to the chassis. Manufacturers such as Bergquist, Avid, and Thermalloy, produce thick, compliant silicone pads that are loaded with thermally conductive materials. If the power devices can be mounted on the back side of a PCB, and a thermally conductive pad sandwiched between the PCB and a steel chassis, a great deal of heat will be very effectively removed. Surface mount heatsinks are also available from some of the previously mentioned manufacturers which drastically improve the PCB's ability to transfer heat to the airstream.

In all cases, airflow across the PCB is very important. Even a small amount of air movement will make a big difference in the device temperatures. Try to avoid putting the power devices in the airflow shadow of tall components such as a microprocessor or the power supply's own input or output capacitors.

Reference:

Marty Brown, "What Everyone Should Know About Switching Power Supplies"

Rudolf Severns, Gordon Bloom, "Modern DC-DC Switchmode Power Converter Circuits"

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