SINGLE-ENDED ANALOG-INPUT 20-BIT STEREO ANALOG-TO-DIGITAL CONVERTER

FEATURES

- Dual 20-Bit Monolithic ΔΣ ADC
- Single-Ended Voltage Input
- 64× Oversampling Decimation Filter:
  - Pass-Band Ripple: ±0.05 dB
  - Stop-Band Attenuation: –65 dB
- High Performance:
  - THD+N: –88 dB (typical)
  - SNR: 95 dB (typical)
  - Dynamic Range: 95 dB (typical)
  - Internal High-Pass Filter
- PCM Audio Interface:
  - Master/Slave Modes
  - Four Data Formats
- Sampling Rate: 4 kHz to 48 kHz
- System Clock: 256 f_S, 384 f_S, or 512 f_S
- Single 5-V Power Supply
- Small 24-Pin SSOP Package

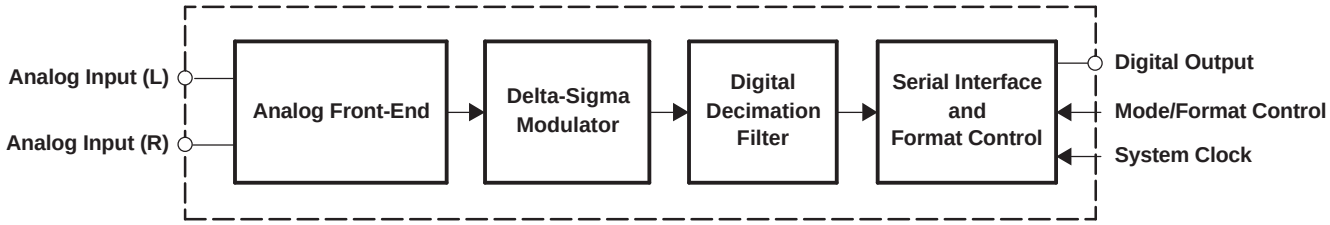
APPLICATIONS

- DVD Recorders
- DVD Receivers
- AV Amplifier Receivers
- Electric Musical Instruments

DESCRIPTION

The PCM1800 is a low-cost, single-chip stereo analog-to-digital converter (ADC) with single-ended analog voltage inputs. The PCM1800 uses a delta-sigma modulator with 64 times oversampling, including a digital decimation filter and a serial interface which supports both master and slave modes and four data formats. The PCM1800 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required.

The PCM1800 is fabricated using a highly advanced CMOS process and is available in a small 24-pin SSOP package.



B0003-01

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, slave mode, f_S = 44.1 kHz, 20-bit input data, and SYSCLK = 384 f_S, unless otherwise noted

PARAMETER		TEST CONDITIONS	PCM1800E			UNITS
			MIN	TYP	MAX	
RESOLUTION			20			Bits
DIGITAL INPUT/OUTPUT						
V_{IH} (1)	Input logic level		2			VDC
V_{IL} (1)					0.8	
I_{IN} (2)	Input logic current				±1	µA
I_{IN} (3)					100	
V_{OH} (4)	Output logic level	I_{OH} = –1.6 mA	4.5			VDC
V_{OL} (4)		I_{OL} = 3.2 mA			0.5	
f_S	Sampling frequency		4	44.1	48	kHz
	System clock frequency	256 f_S	1.024	11.2896	12.288	MHz
		384 f_S	1.536	16.9344	18.432	
		512 f_S	2.048	22.5792	24.576	
DC ACCURACY						
	Gain mismatch, channel-to-channel			±1	±2.5	% of FSR
	Gain error			±2	±5	% of FSR
	Gain drift			±20		ppm of FSR/°C
	Bipolar zero error	High-pass filter bypassed		±2		% of FSR
	Bipolar zero drift	High-pass filter bypassed		±20		ppm of FSR/°C
DYNAMIC PERFORMANCE (5)						
	THD+N at FS (–0.5 dB)			–88	–80	dB
	THD+N at –60 dB			–92		dB
	Dynamic range	A-weighted	90	95		dB
	Signal-to-noise ratio	A-weighted	90	95		dB
	Channel separation		88	93		dB
DYNAMIC PERFORMANCE (5)						
	Dynamic range	16-bit, A-weighted		94		dB
	Signal-to-noise ratio	16-bit, A-weighted		94		dB
	Channel separation	16-bit		92		dB
ANALOG INPUT						
	Input range	FS (V_{IN} = 0 dB)		2.828		Vp-p
	Center voltage			2.1		VDC
	Input impedance			30		kΩ
	Antialiasing filter frequency response	C_{EXT} = 470 pF, –3 dB		170		kHz
DIGITAL FILTER PERFORMANCE						

(1) Pins 6, 7, 8, 9, 10, 11, 16 and 12, 13, 14: RSTB, BYPAS, FMT0, FMT1, MODE0, MODE1, SYSCLK, and FSYNC, LRCK, BCK in slave mode
(2) Pins 16 and 12, 13, 14: SYSCLK and FSYNC, LRCK, BCK in slave mode (Schmitt-trigger input)
(3) Pins 6, 7, 8, 9, 10, 11: RSTB, BYPAS, FMT0, FMT1, MODE0, MODE1 (Schmitt-trigger input, with 100-kΩ typical pulldown resistor)
(4) Pins 15 and 12, 13, 14: DOUT and FSYNC, LRCK, BCK in master mode
(5) f_{IN} = 1 kHz, using the System Two™ audio measurement system by Audio Precision™, rms mode with 20-kHz LPF and 400-Hz HPF in the performance calculation.

ELECTRICAL CHARACTERISTICS (continued)

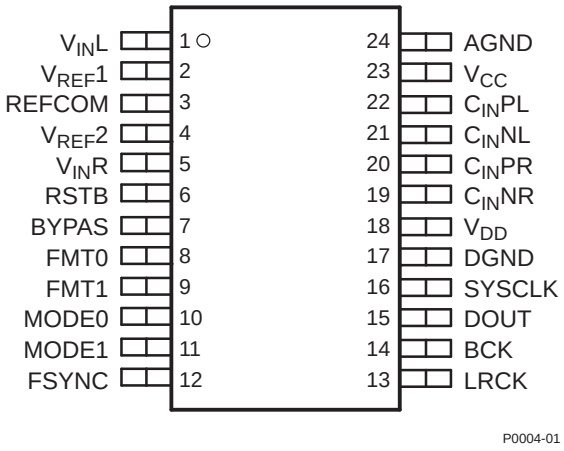
All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, slave mode, f_S = 44.1 kHz, 20-bit input data, and SYSCLK = 384 f_S, unless otherwise noted

PARAMETER		TEST CONDITIONS	PCM1800E			UNITS
			MIN	TYP	MAX	
	Pass band				0.454 f_S	Hz
	Stop band		0.583 f_S			Hz
	Pass-band ripple				±0.05	dB
	Stop-band attenuation		–65			dB
	Delay time (latency)			17.4/f_S		s
	High-pass frequency response	–3 dB		0.019 f_S		mHz
POWER SUPPLY REQUIREMENTS						
V_{CC}	Voltage range		4.5	5	5.5	VDC
V_{DD}			4.5	5	5.5	
	Supply current(6)	V_{CC} = V_{DD} = 5 V		18	25	mA
	Power dissipation	V_{CC} = V_{DD} = 5 V		90	125	mW
TEMPERATURE RANGE						
T_A	Operation		–25		85	°C
T_{stg}	Storage		–55		125	°C
θ_{JA}	Thermal resistance			100		°C/W

(6) No load on DOUT (pin 15) in the slave mode

PIN CONFIGURATION

PCM1800
(TOP VIEW)



P0004-01

PIN ASSIGNMENTS

NAME	PIN	I/O	DESCRIPTION
AGND	24	–	Analog ground
BCK	14	I/O	Bit clock input/output
BYPAS	7	I	High-pass filter bypass control(1)
$C_{IN}NL$	21	–	Antialias filter capacitor (–), Lch
$C_{IN}NR$	19	–	Antialias filter capacitor (–), Rch
$C_{IN}PL$	22	–	Antialias filter capacitor (+), Lch
$C_{IN}PR$	20	–	Antialias filter capacitor (+), Rch
DGND	17	–	Digital ground
DOUT	15	O	Audio data output
FMT0	8	I	Audio data format 0(1)
FMT1	9	I	Audio data format 1(1)
FSYNC	12	I/O	Frame synchronization, input/output
LRCK	13	I/O	Sampling clock input/output (f_S)
MODE0	10	I	Master/slave mode selection 0(1)
MODE1	11	I	Master/slave mode selection 1(1)
REFCOM	3	–	Reference decoupling common
SYSCLK	16	I	System clock input, 256 f_S, 384 f_S, or 512 f_S
RSTB	6	I	Reset input, active LOW(1)
V_{CC}	23	–	Analog power supply
V_{DD}	18	–	Digital power supply
$V_{IN}L$	1	I	Analog input, Lch
$V_{IN}R$	5	I	Analog input, Rch
$V_{REF}1$	2	–	Reference 1 decoupling capacitor
$V_{REF}2$	4	–	Reference 2 decoupling capacitor

(1) With 100-kΩ typical pulldown resistor

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE TYPE	PACKAGE CODE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA	QUANTITY
PCM1800E	24-pin SSOP	DB	PCM1800E	PCM1800E	Rails	58
				PCM1800E/2K	Tape and reel	2000

ABSOLUTE MAXIMUM RATINGS

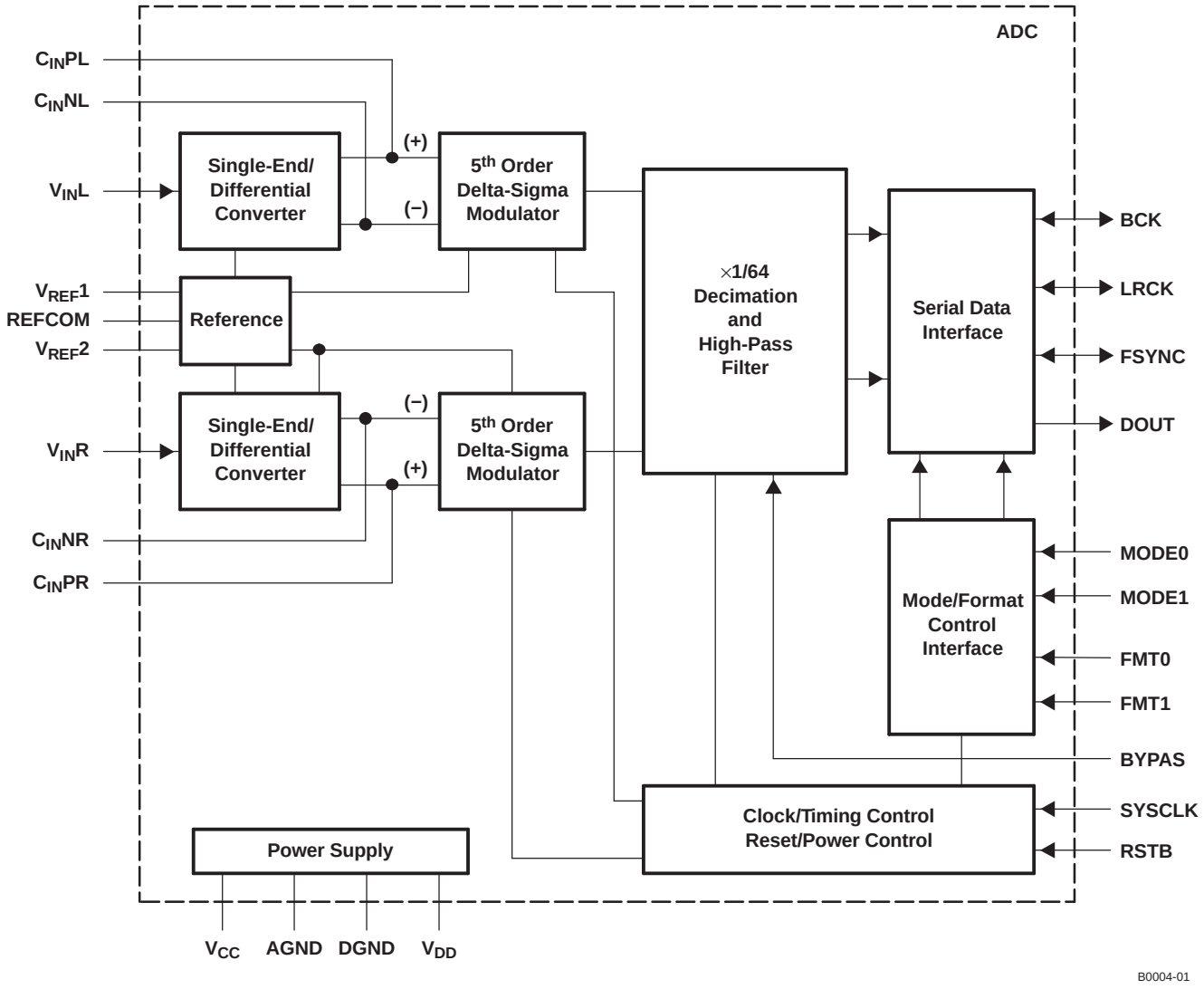
Supply voltage: V_{DD}, V_{CC}	–0.3 V to 6.5 V
Supply voltage differences	±0.1 V
GND voltage differences	±0.1 V
Digital input voltage	–0.3 V to (V_{DD} + 0.3 V), < 6.5 V
Analog input voltage	–0.3 V to (V_{CC} + 0.3 V), < 6.5 V
Input current (any pin except supplies)	±10 mA
Power dissipation	300 mW
Operating temperature range	–25°C to 85°C
Storage temperature	–55°C to 125°C
Lead temperature, soldering	260°C, 5 s
Package temperature (IR reflow, peak)	235°C

RECOMMENDED OPERATING CONDITIONS

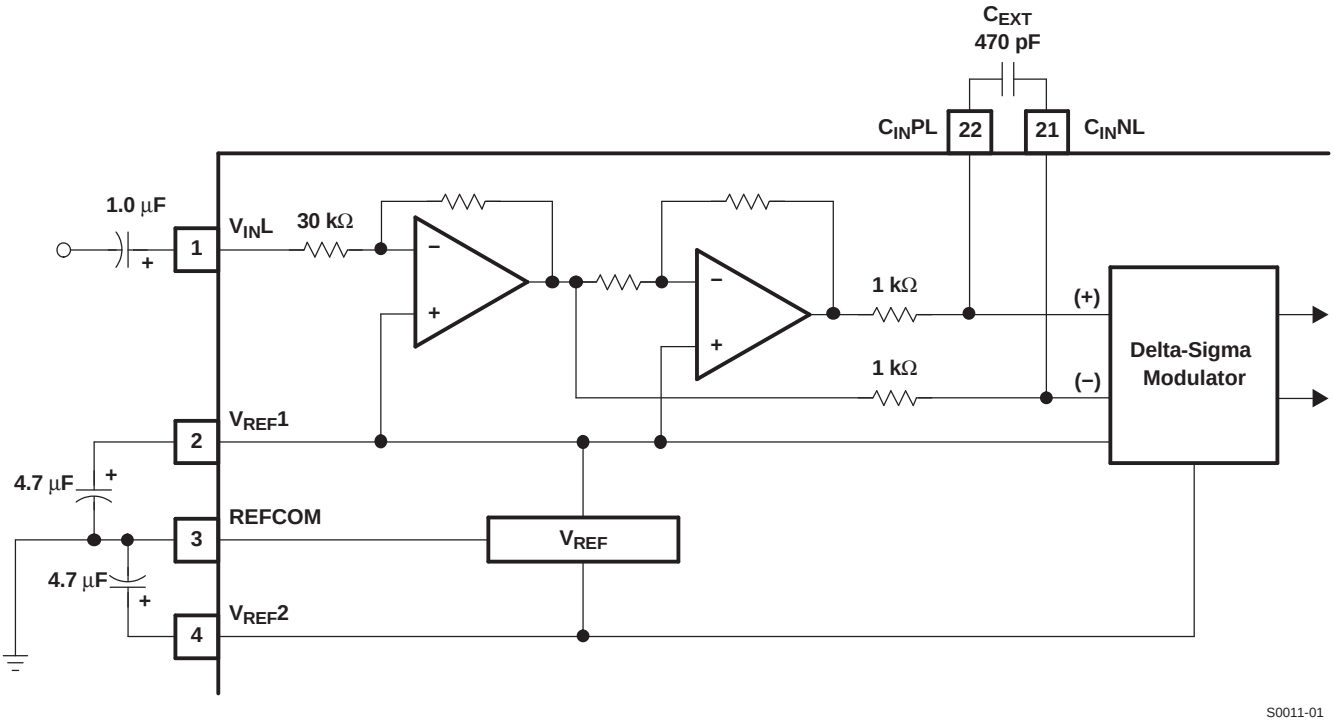
over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Analog supply voltage, V_{CC}		4.5	5	5.5	V
Digital supply voltage, V_{DD}		4.5	5	5.5	V
Analog input voltage, full-scale (–0 dB)			2.828		Vp-p
Digital input logic family			TTL		
Digital input clock frequency	System clock	8.192		24.576	MHz
	Sampling clock	32		48	kHz
Digital output load capacitance			10		pF
Operating free-air temperature, T_A		–25		85	°C

BLOCK DIAGRAM



ANALOG FRONT-END (Single Channel)



TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, slave mode, f_S = 44.1 kHz, 20-bit input data, and SYSCLK = 384 f_S, unless otherwise noted

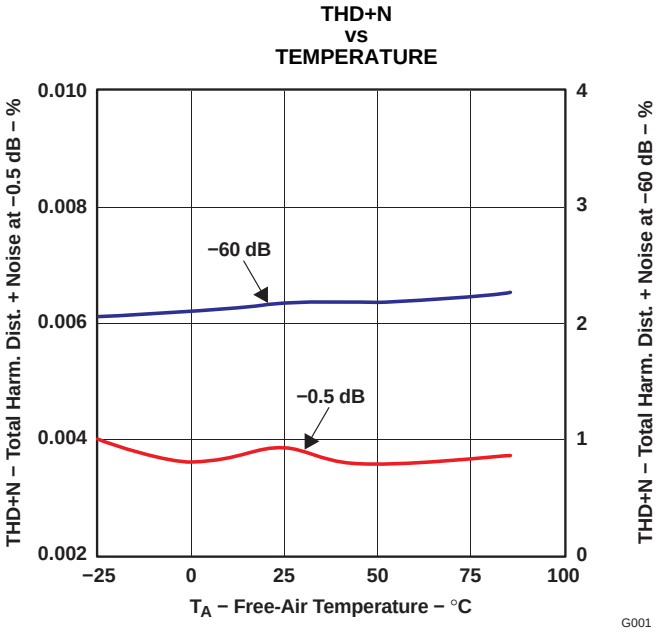


Figure 1.

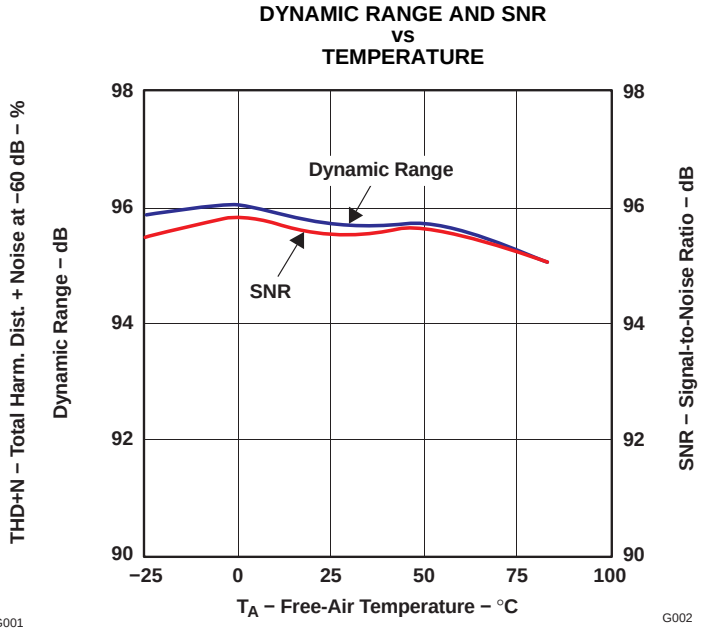


Figure 2.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, slave mode, f_S = 44.1 kHz, 20-bit input data, and SYSCLK = 384 f_S, unless otherwise noted

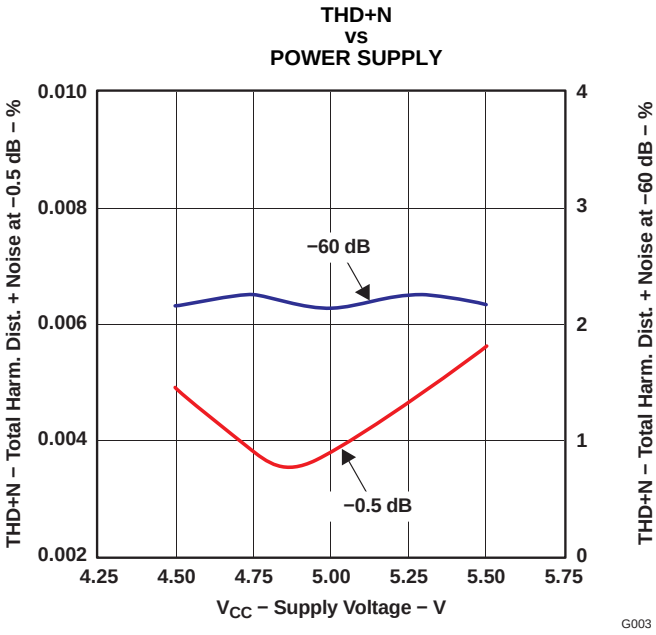


Figure 3.

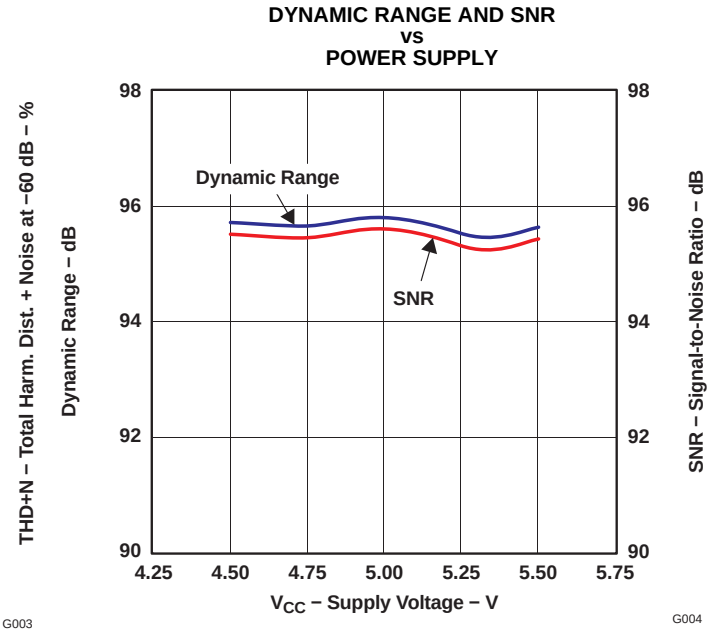


Figure 4.

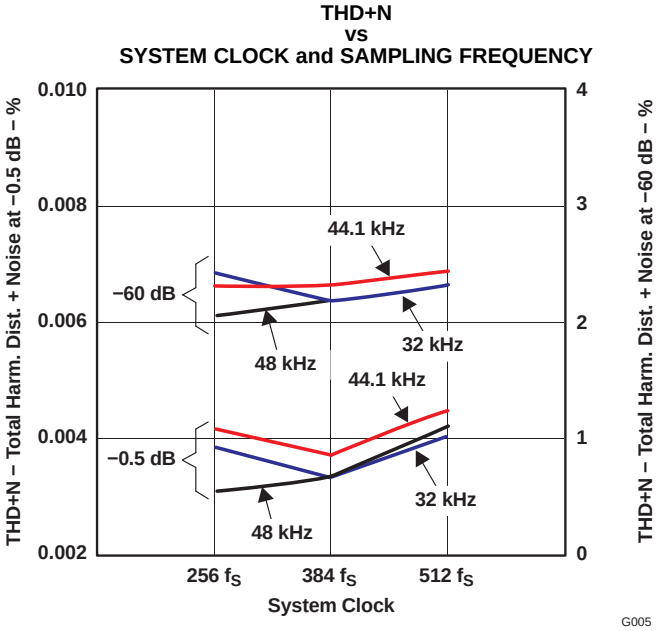


Figure 5.

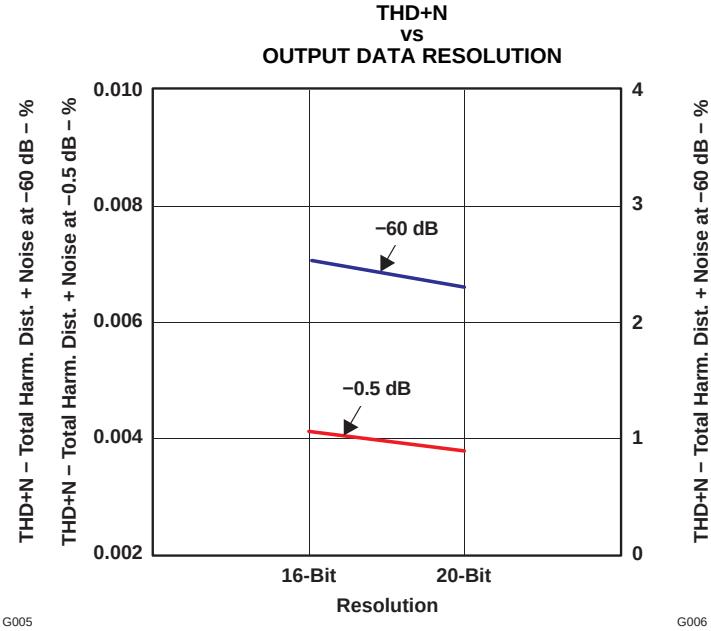


Figure 6.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, slave mode, f_S = 44.1 kHz, 20-bit input data, and SYSCLK = 384 f_S, unless otherwise noted

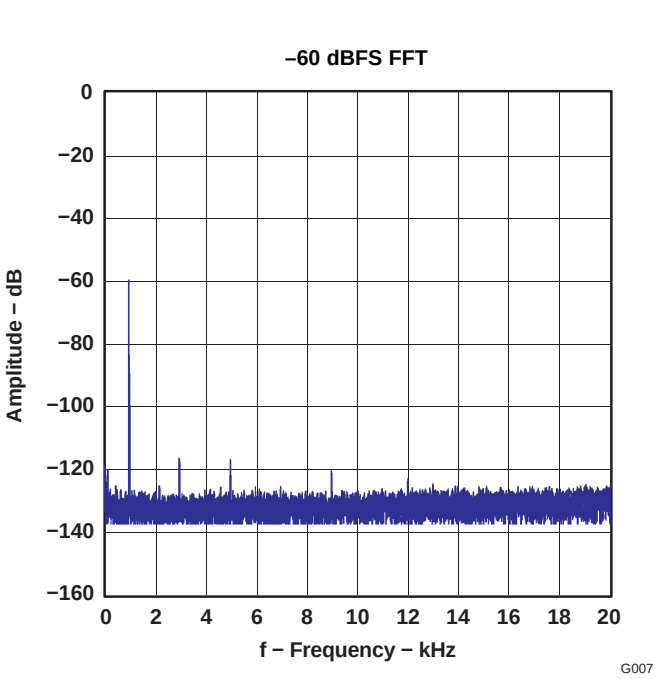


Figure 7.

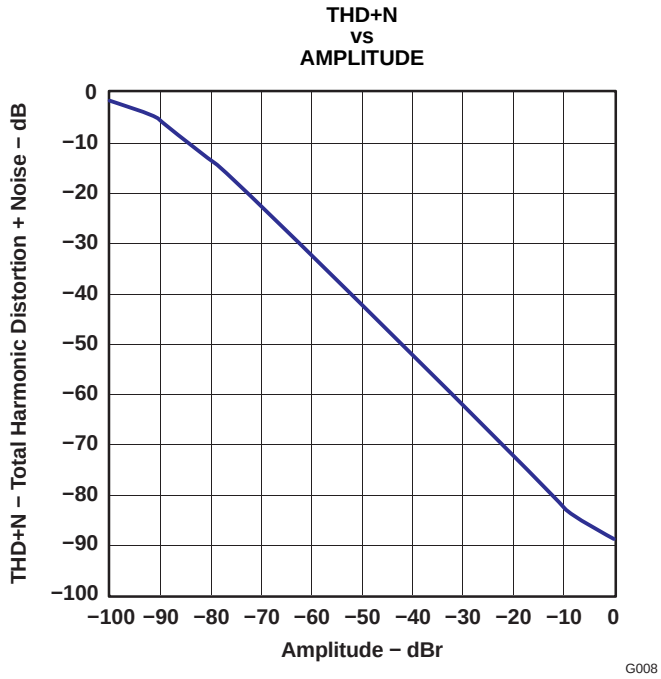


Figure 8.

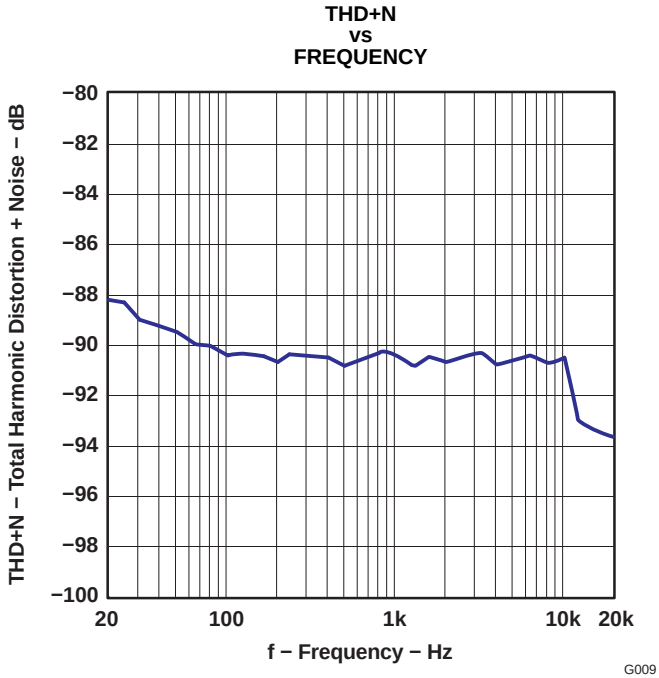


Figure 9.

TYPICAL PERFORMANCE CURVES FOR INTERNAL FILTERS

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, slave mode, f_S = 44.1 kHz, 20-bit input data, and SYSCLK = 384 f_S, unless otherwise noted

DECIMATION FILTER

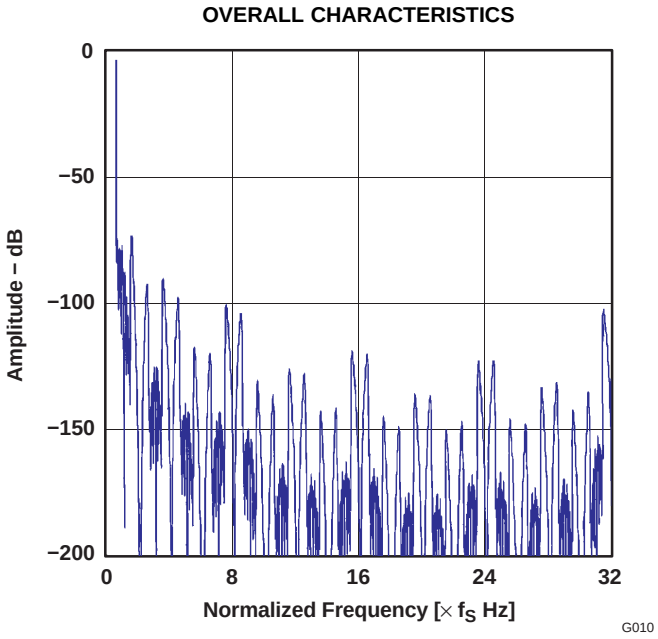


Figure 10.

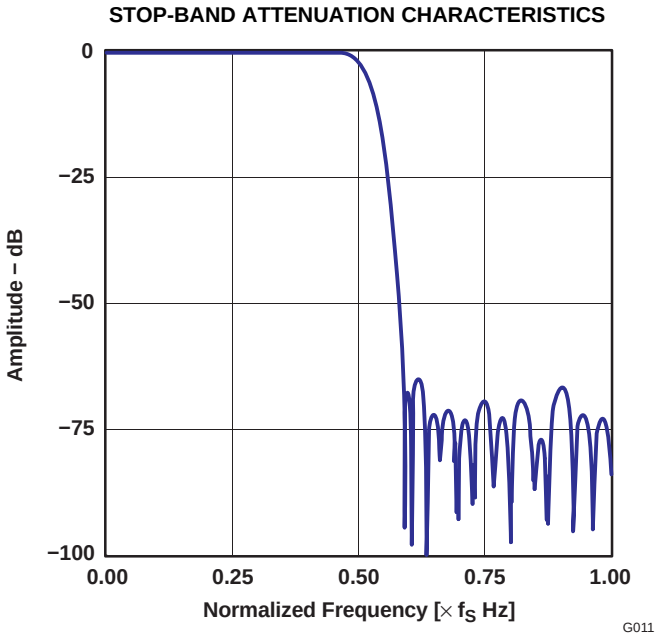


Figure 11.

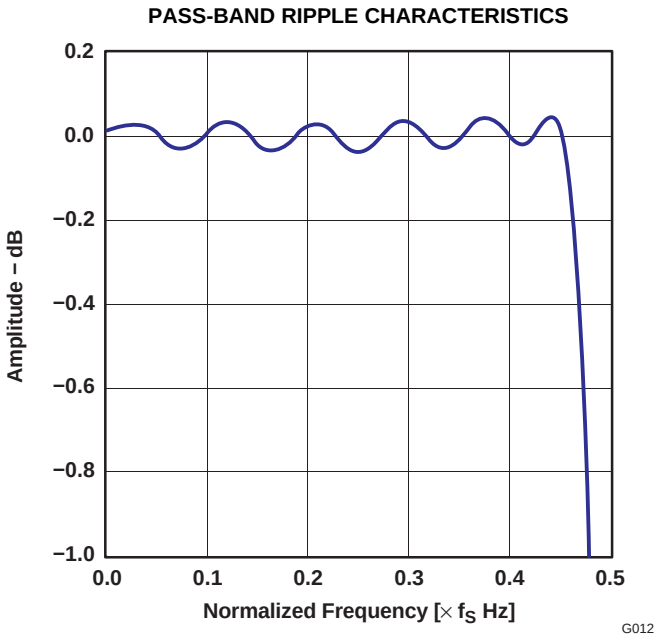


Figure 12.

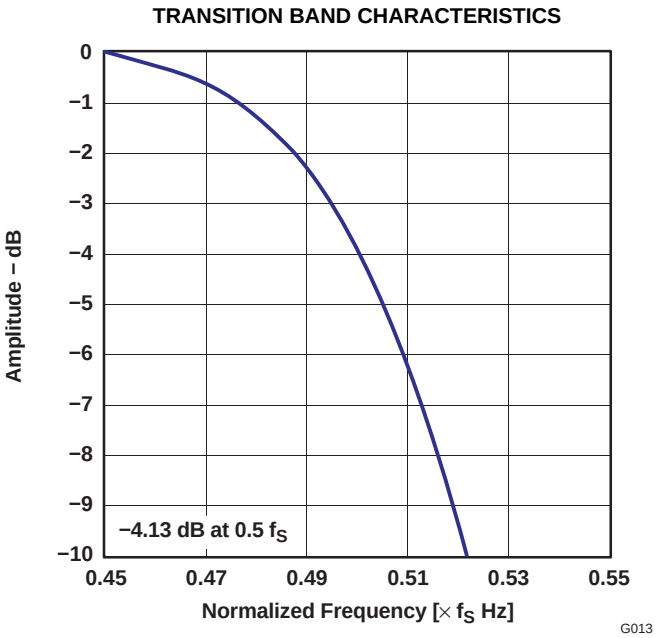


Figure 13.

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, slave mode, f_S = 44.1 kHz, 20-bit input data, and SYSCLK = 384 f_S, unless

TYPICAL PERFORMANCE CURVES FOR INTERNAL FILTERS (continued)

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 5 V, slave mode, f_S = 44.1 kHz, 20-bit input data, and SYSCLK = 384 f_S, unless otherwise noted

otherwise noted

HIGH-PASS FILTER

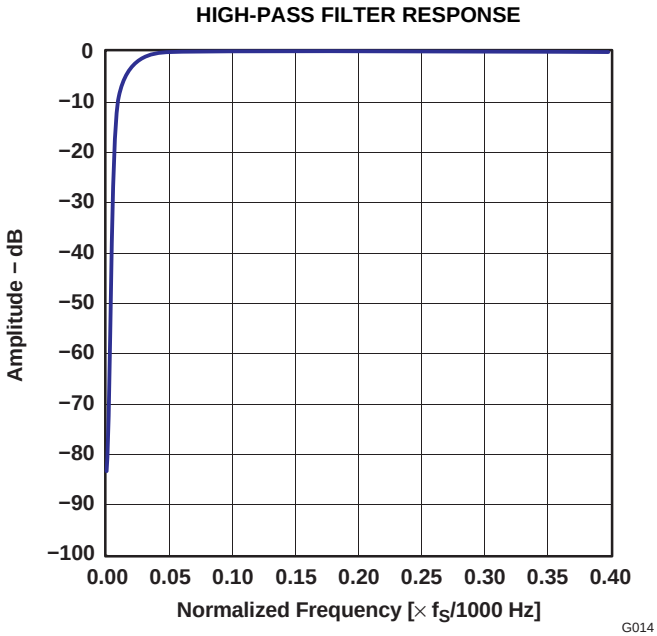


Figure 14.

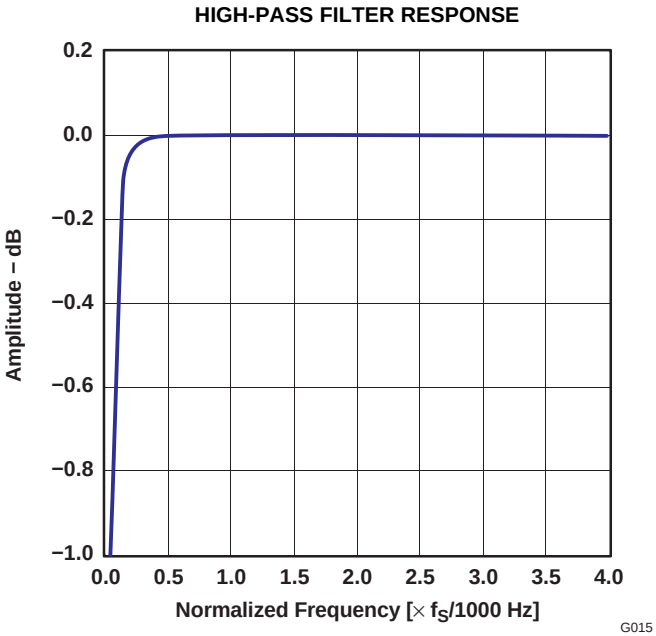


Figure 15.

ANTIALIASING FILTER

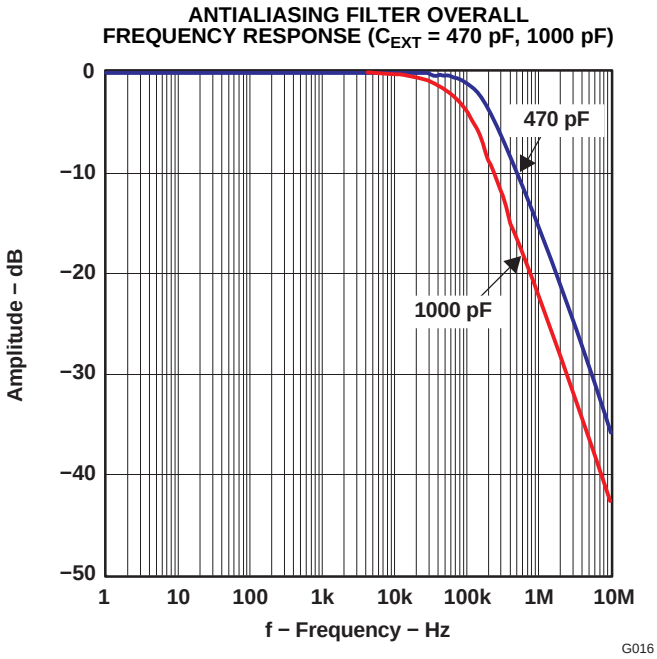


Figure 16.

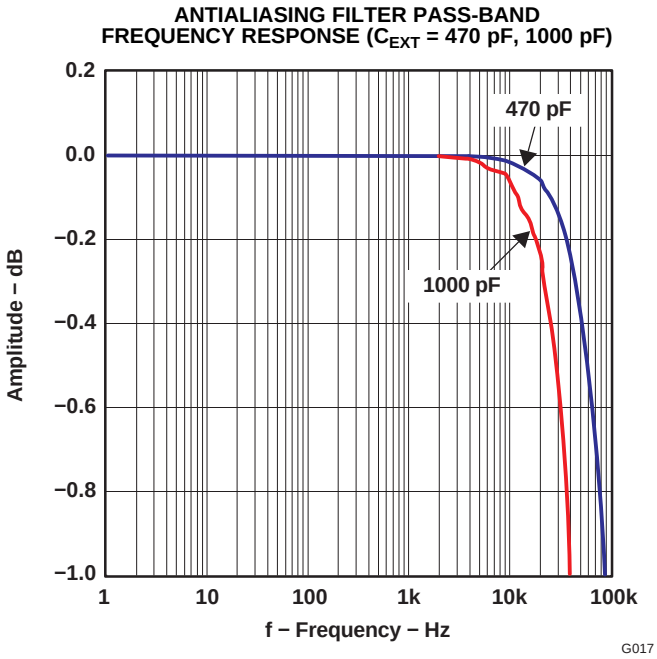


Figure 17.

THEORY OF OPERATION

The PCM1800 consists of a band-gap reference, two channels of a single-to-differential converter, a fully differential 5th-order delta-sigma modulator, a decimation filter (including digital high pass), and a serial interface circuit. The block diagram illustrates the total architecture of the PCM1800 and the analog front-end diagram illustrates the architecture of the single-to-differential converter and the antialiasing filter. Figure 18 illustrates the architecture of the 5th-order delta-sigma modulator and transfer functions.

An internal high-precision reference with two external capacitors provides all the reference voltages that are required by the converter, and defines the full-scale voltage range of both channels. The internal single-to-differential voltage converter saves the design, space, and extra parts needed for external circuitry required by many delta-sigma converters. The internal full-differential architecture provides a wide dynamic range and excellent power-supply rejection performance.

The input signal is sampled at a 64× oversampling rate, eliminating the need for a sample-and-hold circuit, and simplifying antialias filtering requirements. The 5th-order delta-sigma noise shaper consists of five integrators which use a switched-capacitor topology, a comparator, and a feedback loop consisting of a 1-bit DAC. The delta-sigma modulator shapes the quantization noise, shifting it out of the audio band in the frequency domain. The high order of the modulator enables it to randomize the modulator outputs, reducing idle tone levels.

The 64-f_S, 1-bit stream from the modulator is converted to 1-f_S, 20-bit digital data by the decimation filter, which also acts as a low-pass filter to remove the shaped quantization noise. The dc components are removed by a high-pass filter, and the filtered output is converted to time-multiplexed serial signals through a serial interface which provides flexible serial formats and master/slave modes.

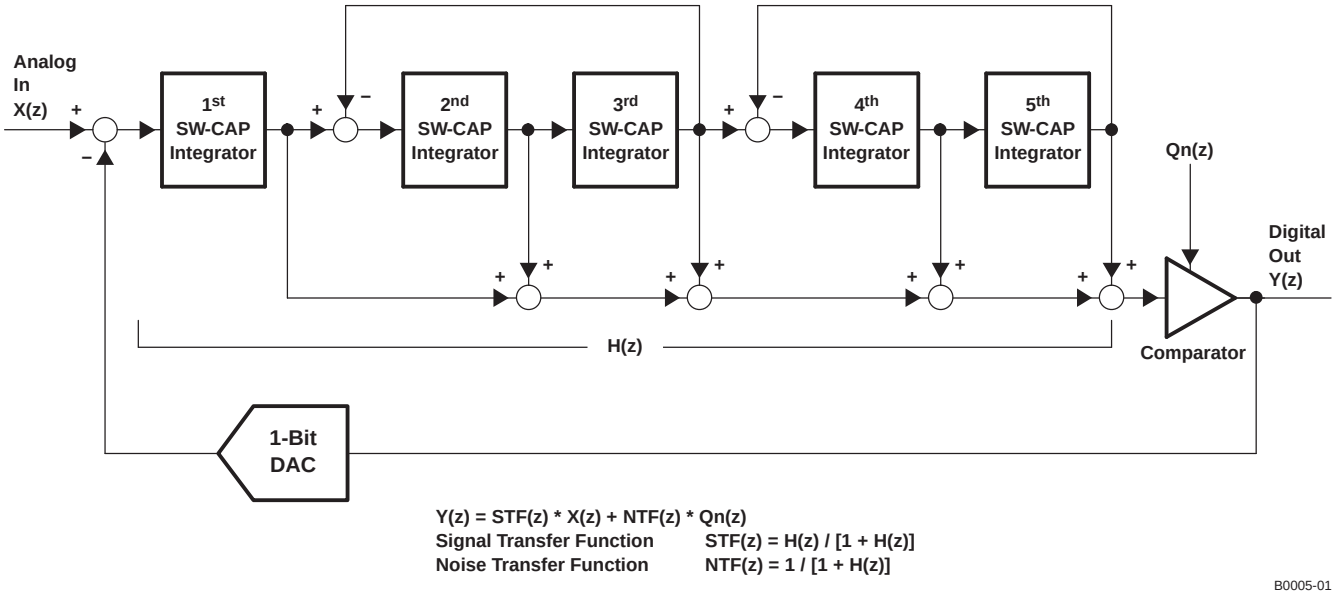


Figure 18. Simplified Diagram of the PCM1800 5th-Order Delta-Sigma Modulator

SYSTEM CLOCK

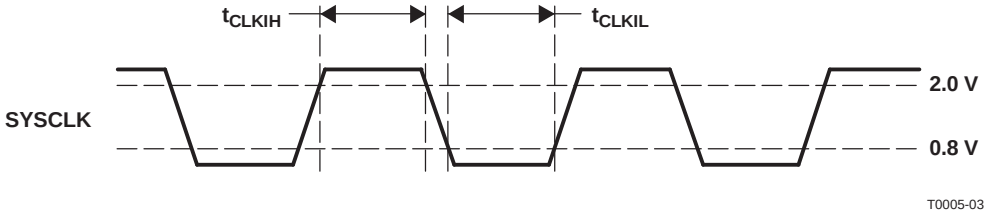
The system clock for the PCM1800 must be either 256 f_S, 384 f_S, or 512 f_S, where f_S is the audio sampling frequency. The system clock must be supplied on SYSCLK (pin 16).

The PCM1800 also has a system-clock detection circuit which automatically senses if the system clock is operating at 256 f_S, 384 f_S, or 512 f_S.

When the 384-f_S or 512-f_S system clock is in slave mode, the system clock is divided into 256 f_S automatically. The 256-f_S clock is used to operate the digital filter and the modulator. Table 1 lists the relationship of typical sampling frequencies and system clock frequencies. Figure 19 illustrates the system clock timing.

Table 1. System Clock Frequencies

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)		
	256 f_S	384 f_S	512 f_S
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760



System clock pulse duration, HIGH	$t_{(CLKIH)}$	12 ns (min)
System clock pulse duration, LOW	$t_{(CLKIL)}$	12 ns (min)

Figure 19. System Clock Timing

RESET AND POWER DOWN

The PCM1800 has both an internal power-on reset circuit and an external forced reset (RSTB, pin 6). The internal power-on reset initializes (resets) when the supply voltage (V_{CC}/V_{DD}) exceeds 4 V (typical). To initiate the reset sequence externally, apply a logic-level LOW to the RSTB pin.

The RSTB pin is terminated by an internal pulldown resistor. If the RSTB pin is unconnected, the ADC remains in the reset state. Because the system clock is used as the clock signal for the reset circuit, the system clock must be supplied as soon as power is applied; more specifically, the device must receive at least three system clock cycles before V_{DD} > 4 V and RSTB = HIGH. If this system clock requirement cannot be assured in an application, RSTB must be held LOW until the system clock is supplied. While V_{CC}/V_{DD} < 4 V (typical), RSTB = LOW, and for 1024 system clock periods after V_{CC}/V_{DD} > 4.0 V and RSTB = HIGH, the PCM1800 stays in the reset state and the digital output is forced to zero. The digital output is valid 18,436 f_S periods after release from the reset state. During reset, the logic circuits and the digital filter stop operating and enter the power-down mode. Figure 20 and Figure 21 illustrate the internal power-on reset and external reset timing.

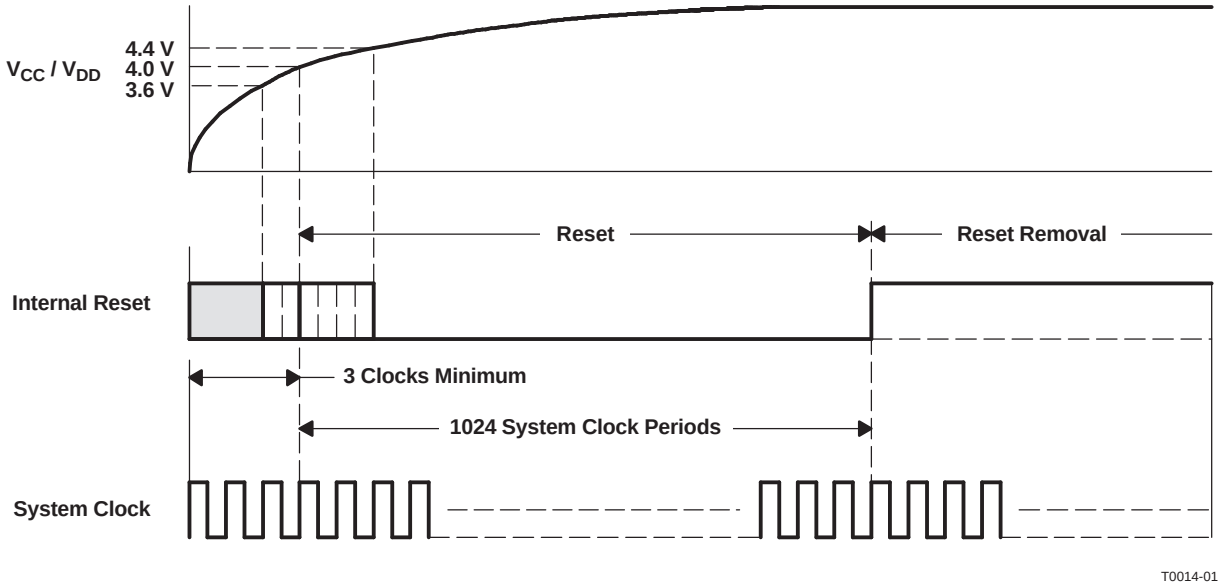


Figure 20. Internal Power-On Reset Timing

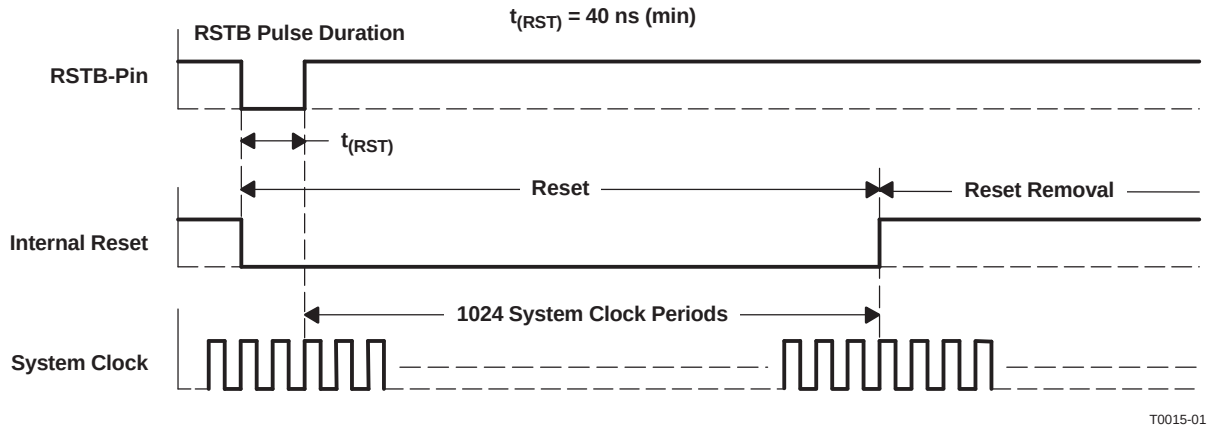


Figure 21. RSTB-Pin Reset Timing

SERIAL AUDIO DATA INTERFACE

The PCM1800 interfaces with the audio system through BCK (pin 14), LRCK (pin 13), FSYNC (pin 12), and DOUT (pin 15).

INTERFACE MODE

The PCM1800 supports master and slave modes as interface modes, which are selected by MODE1 (pin 11) and MODE0 (pin 10), as shown in Table 2. When in master mode, the PCM1800 provides the timing for serial audio data communications between the PCM1800 and the digital audio processor or external circuit. When in slave mode, the PCM1800 receives the timing for data transfer from an external controller.

Table 2. Interface Mode

MODE1	MODE0	INTERFACE MODE
0	0	Slave mode (256/384/512 f_S)
0	1	Master mode (512 f_S)
1	0	Master mode (384 f_S)
1	1	Master mode (256 f_S)

MASTER MODE

In master mode, BCK, LRCK, and FSYNC are output pins and are controlled by timing generated in the clock circuitry of the PCM1800.

FSYNC is used to designate the valid data from the PCM1800. The rising edge of FSYNC indicates the starting point of the converted audio data, and the following edge of this signal indicates the ending point of data. The frequency of this signal is fixed at 2× LRCK, and the duty-cycle ratio depends on the data bit length. The frequency of BCK is fixed at 64× LRCK.

SLAVE MODE

In slave mode, BCK, LRCK, and FSYNC are input pins. The PCM1800 accepts 64-BCK/LRCK, 48-BCK/LRCK (only for a 384-f_S system clock) or 32-BCK/LRCK format (only for 16-bit, right-justified format). FSYNC is used to enable the BCK signal, and the PCM1800 can shift out the converted data when FSYNC is HIGH.

DATA FORMAT

The PCM1800 supports four audio data formats in both master and slave modes. These data formats are selected by FMT1 (pin 9) and FMT0 (pin 8), as shown in Table 3. Figure 22 and Figure 23 illustrate the data formats in slave mode and master mode, respectively.

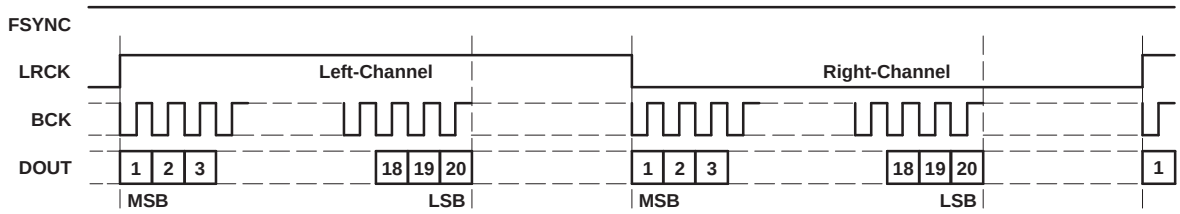
Table 3. Data Format

FORMAT NO.	FMT1 (1)	FMT0 (1)	DATA FORMAT
0	0	0	20-bit, left-justified
1	0	1	20-bit, I^2S
2	1	0	16-bit, right-justified
3	1	1	20-bit, right-justified

(1) FMT1 and FMT0 must be stable when RSTB changes from LOW to HIGH.

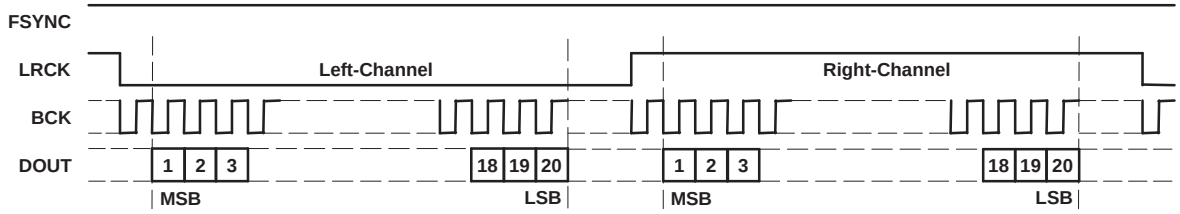
FORMAT 0: FMT[1:0] = 00

20-Bit, MSB-First, Left-Justified



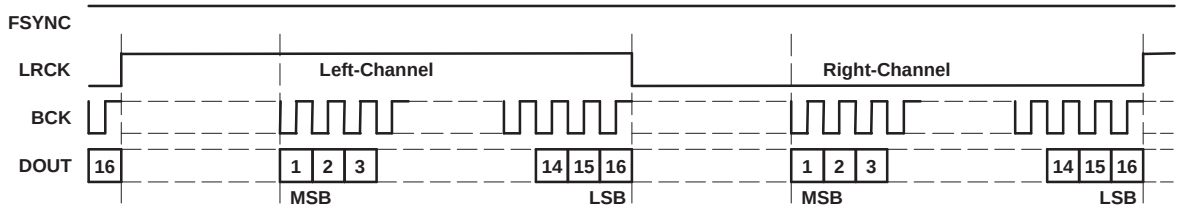
FORMAT 1: FMT[1:0] = 01

20-Bit, MSB-First, I^2S



FORMAT 2: FMT[1:0] = 10

16-Bit, MSB-First, Right-Justified



FORMAT 3: FMT[1:0] = 11

20-Bit, MSB-First, Right-Justified

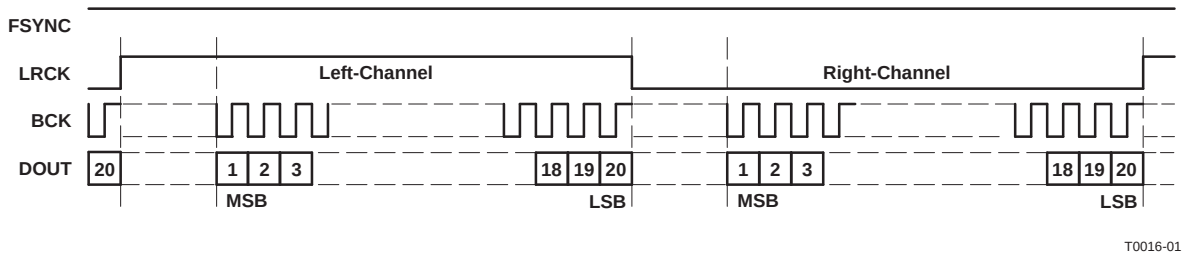
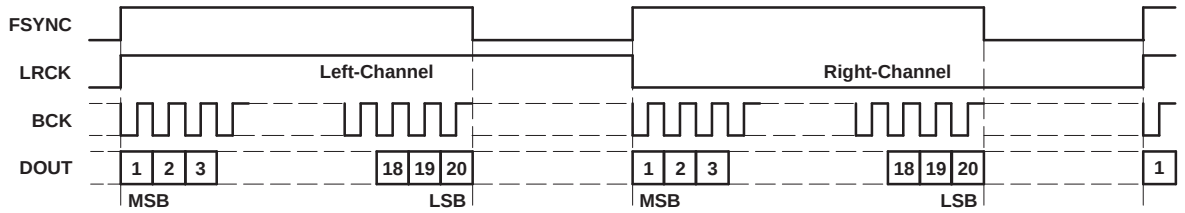


Figure 22. Audio Data Format (Slave Mode: FSYNC, LRCK, and BCK Are Inputs)

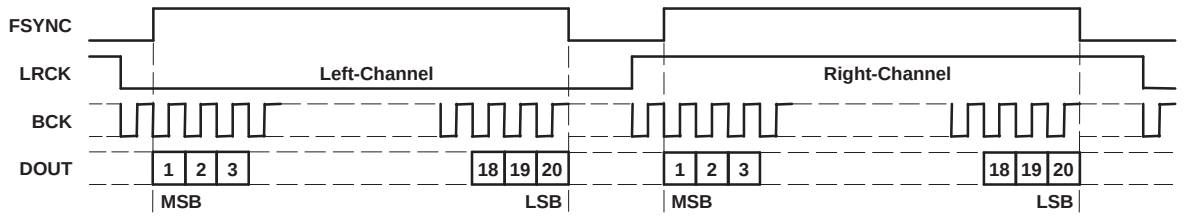
FORMAT 0: FMT[1:0] = 00

20-Bit, MSB-First, Left-Justified



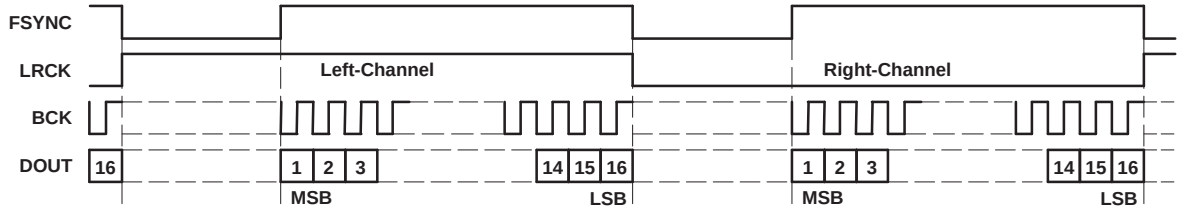
FORMAT 1: FMT[1:0] = 01

20-Bit, MSB-First, I^2S



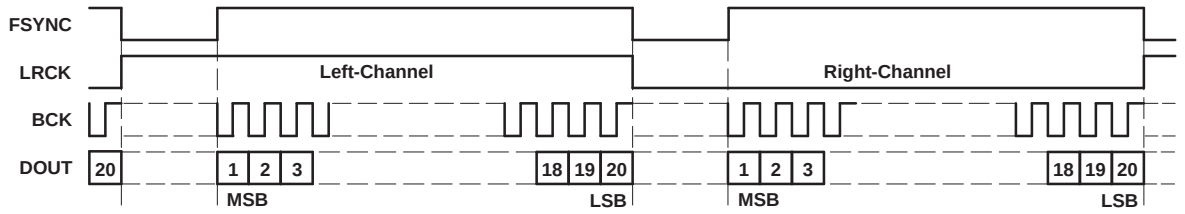
FORMAT 2: FMT[1:0] = 10

16-Bit, MSB-First, Right-Justified



FORMAT 3: FMT[1:0] = 11

20-Bit, MSB-First, Right-Justified

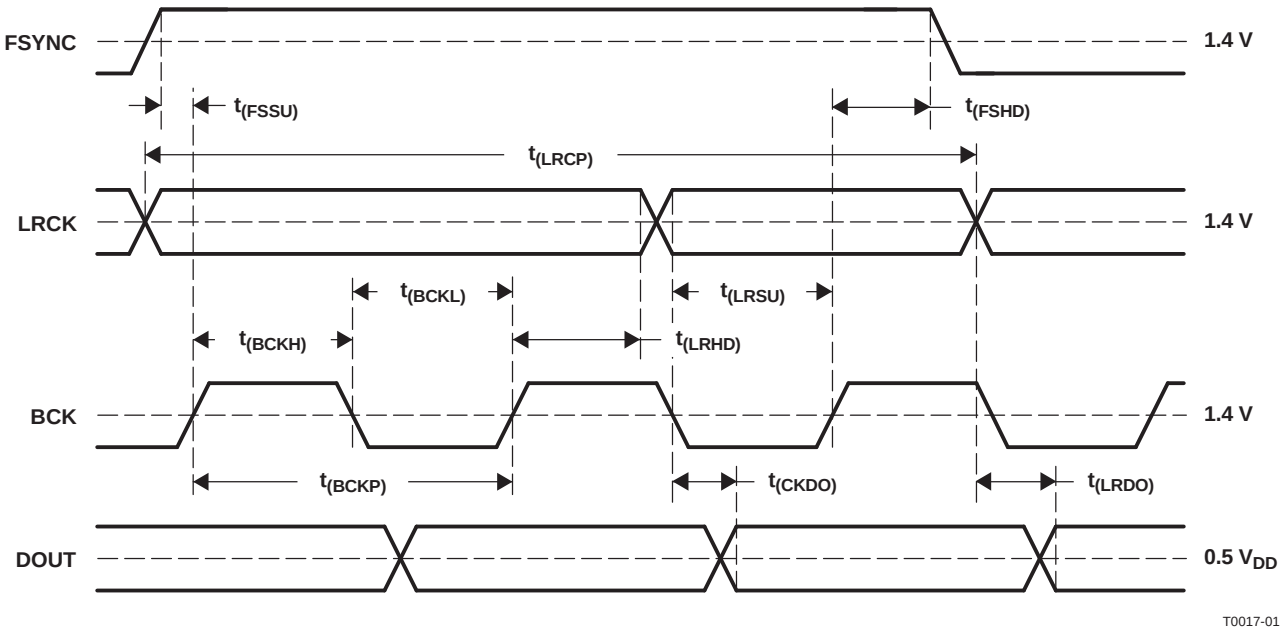


T0016-02

Figure 23. Audio Data Format (Master Mode: FSYNC, LRCK, and BCK Are Outputs)

INTERFACE TIMING

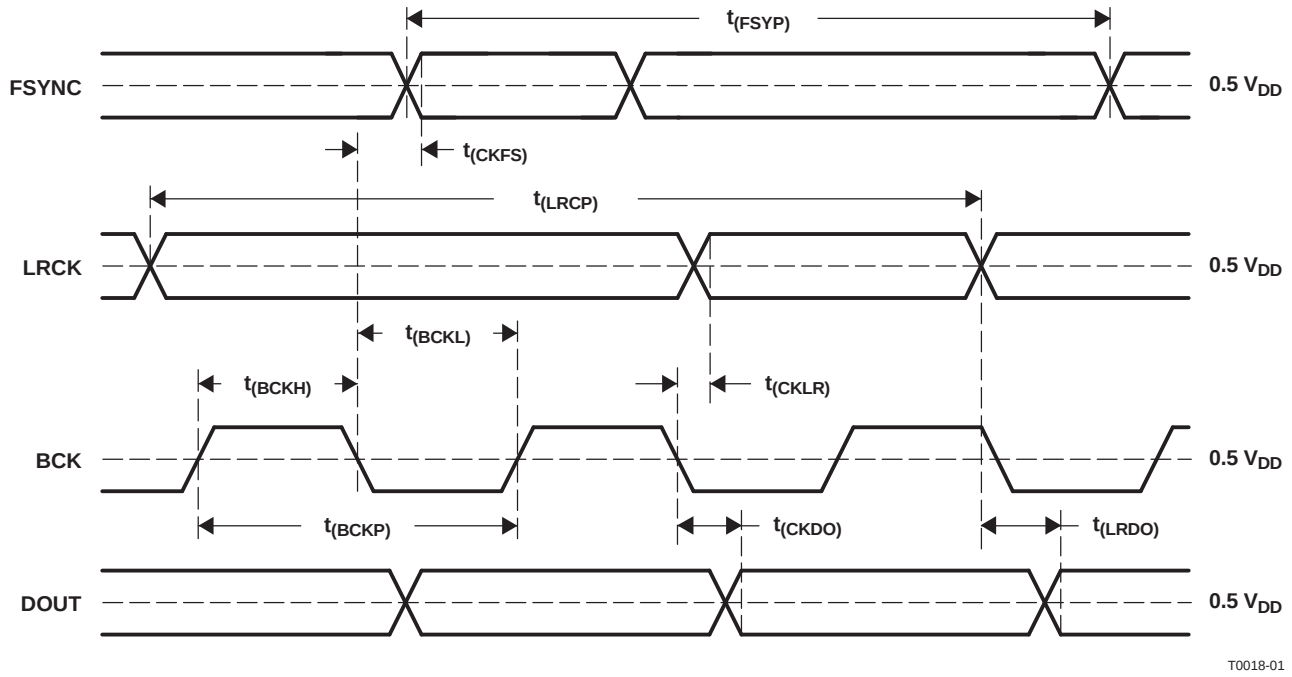
Figure 24 and Figure 25 illustrate the interface timing in slave mode and master mode, respectively.



DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNITS
BCK period	$t_{(BCKP)}$	300			ns
BCK pulse duration, HIGH	$t_{(BCKH)}$	120			ns
BCK pulse duration, LOW	$t_{(BCKL)}$	120			ns
LRCK setup time to BCK rising edge	$t_{(LRSU)}$	80			ns
LRCK hold time to BCK rising edge	$t_{(LRHD)}$	40			ns
LRCK period	$t_{(LRCP)}$	20			µs
FSYNC setup time to BCK rising edge	$t_{(FSSU)}$	40			ns
FSYNC hold time to BCK rising edge	$t_{(FSHD)}$	40			ns
Delay time, BCK falling edge to DOUT valid	$t_{(CKDO)}$	–20		40	ns
Delay time, LRCK edge to DOUT valid	$t_{(LRDO)}$	–20		40	ns
Rising time of all signals	$t_{(RISE)}$			20	ns
Falling time of all signals	$t_{(FALL)}$			20	ns

NOTE: Timing measurement reference level is $(V_{IH} + V_{IL})/2$. Rising and falling time is measured from 10% to 90% of the I/O signal swing. Load capacitance of the DOUT signal is 20 pF.

Figure 24. Audio Data Interface Timing (Slave Mode: FSYNC, LRCK, and BCK Are Inputs)



DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNITS
BCK period	$t_{(BCKP)}$	300	1/64 f_S	4800	ns
BCK pulse duration, HIGH	$t_{(BCKH)}$	150		2400	ns
BCK pulse duration, LOW	$t_{(BCKL)}$	150		2400	ns
Delay time, BCK falling edge to LRCK valid	$t_{(CKLR)}$	–20		40	ns
LRCK period	$t_{(LRCP)}$	20	$1/f_S$	320	µs
Delay time, BCK falling edge to FSYNC valid	$t_{(CKFS)}$	–20		40	ns
FSYNC period	$t_{(FSYP)}$	10	1/2 f_S	160	µs
Delay time, BCK falling edge to DOUT valid	$t_{(CKDO)}$	–20		40	ns
Delay time, LRCK edge to DOUT valid	$t_{(LRDO)}$	–20		40	ns
Rising time of all signals	$t_{(RISE)}$			20	ns
Falling time of all signals	$t_{(FALL)}$			20	ns

NOTE: Timing measurement reference level is $(V_{IH} + V_{IL})/2$. Rising and falling time is measured from 10% to 90% of the I/O signal swing. Load capacitance of the DOUT signal is 20 pF.

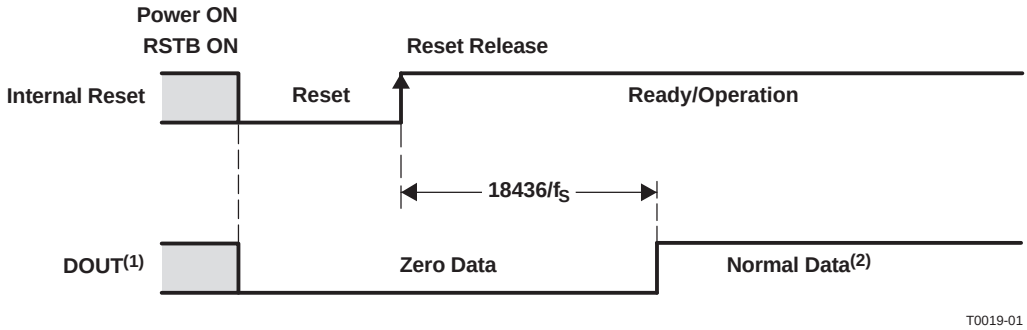
Figure 25. Audio Data Interface Timing (Master Mode: FSYNC, LRCK, and BCK Are Outputs)

SYNCHRONIZATION WITH DIGITAL AUDIO SYSTEM

In slave mode, the PCM1800 operates with LRCK synchronized to the system clock (SYSCLK). The PCM1800 does not require a specific phase relationship between LRCK and SYSCLK, but does require the synchronization of LRCK and SYSCLK. If the relationship between LRCK and SYSCLK changes more than 6 bit clocks (BCK) during one sample period due to LRCK or SYSCLK jitter, internal operation of the ADC halts within $1/f_S$ and the digital output is forced into the BPZ mode until resynchronization between LRCK and SYSCLK is completed. In case of changes less than 5 bit clocks (BCK), resynchronization does not occur, and the previously described digital output control and discontinuity does not occur.

ADC DATA OUTPUT AT RESET

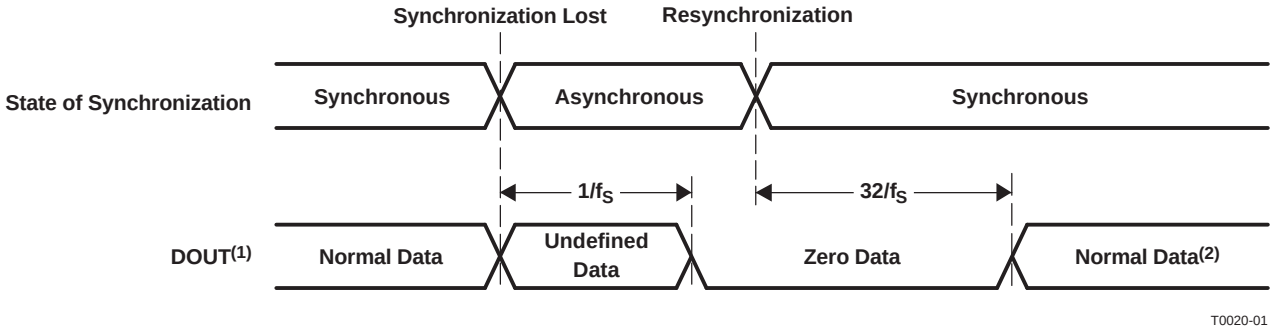
Figure 26 and Figure 27 illustrate the ADC digital output when the reset operation is done and when synchronization is lost, respectively. During undefined data, some noise may be generated in the audio signal. Also, the transition of normal to undefined data and undefined or zero data to normal makes a discontinuity in the data on the digital output, and may generate some noise in the audio signal.



(1) In the master mode, FSYNC, BCK, and LRCK are outputs similar to DOUT.

(2) The HPF transient response (exponentially attenuated signal from ±0.2% dc of FSR with 200-ms time constant) appears initially.

Figure 26. ADC Digital Output for Power-On Reset and RSTB Control



(1) Applies only for slave mode—the loss of synchronization never occurs in master mode.

(2) The HPF transient response (exponentially attenuated signal from ±0.2% dc of FSR with 200-ms time constant) appears initially.

Figure 27. ADC Digital Output During Loss of Synchronization Resynchronization

HPF BYPASS CONTROL

The built-in function for dc component rejection can be bypassed by BYPAS (pin 7) control (see Table 4). In bypass mode, the dc component of the input analog signal, the internal dc offset, etc., are also converted and output in the digital output data.

Table 4. HPF Bypass Control

BYPAS	HIGH-PASS FILTER (HPF) MODE
Low	Normal (dc cut) mode
High	Bypass (through) mode

APPLICATION INFORMATION

BOARD DESIGN AND LAYOUT CONSIDERATIONS

V_{CC}, V_{DD} PINS

The digital and analog power supply lines to the PCM1800 should be bypassed to the corresponding ground pins with both 0.1-µF ceramic and 10-µF tantalum capacitors as close to the pins as possible to maximize the dynamic performance of the ADC. Although the PCM1800 has two power lines to maximize the potential of dynamic performance, using one common power supply is recommended to avoid unexpected power supply problems, such as latch-up or power supply sequence.

AGND, DGND PINS

To maximize the dynamic performance of the PCM1800, the analog and digital grounds are not internally connected. These points should have low impedance to avoid digital noise feedback into the analog ground. They should be connected directly to each other under the part to reduce potential noise problems.

V_{IN} PINS

A 1-µF tantalum capacitor is recommended as an ac-coupling capacitor, which establishes a 5.3-Hz cutoff frequency. If a higher full-scale input voltage is required, the input voltage range can be increased by adding a series resistor to the V_{IN} pins.

V_{REF} INPUTS

A 4.7-µF tantalum capacitor is recommended between $V_{REF}1$, $V_{REF}2$, and REFCOM to ensure low source impedance for the ADC references. These capacitors should be located as close as possible to the $V_{REF}1$ and $V_{REF}2$ pins to reduce dynamic errors on the ADC references. The REFCOM pin also should be connected directly to AGND under the part.

C_{IN}P and C_{IN}N INPUTS

A 470-pF to 1000-pF film capacitor is recommended between C_{IN}PL and C_{IN}NL, C_{IN}PR and C_{IN}NR to create an antialiasing filter which has a 170-kHz to 80-kHz cutoff frequency. These capacitors should be located as close as possible to the C_{IN}P and C_{IN}N pins to avoid introducing unexpected noise or dynamic errors into the delta-sigma modulator. Four 10-pF–47-pF capacitors between C_{IN}XX and AGND may improve dynamic performance under disadvantageous actual conditions.

DOUT, BCK, LRCK, FSYNC PINS

In master mode, the DOUT, BCK, LRCK and FSYNC pins have a large load-drive capability, but locating the buffer near the PCM1800 and minimizing the load capacitance is recommended in order to minimize the digital-analog crosstalk and to maximize dynamic performance potential.

SYSTEM CLOCK

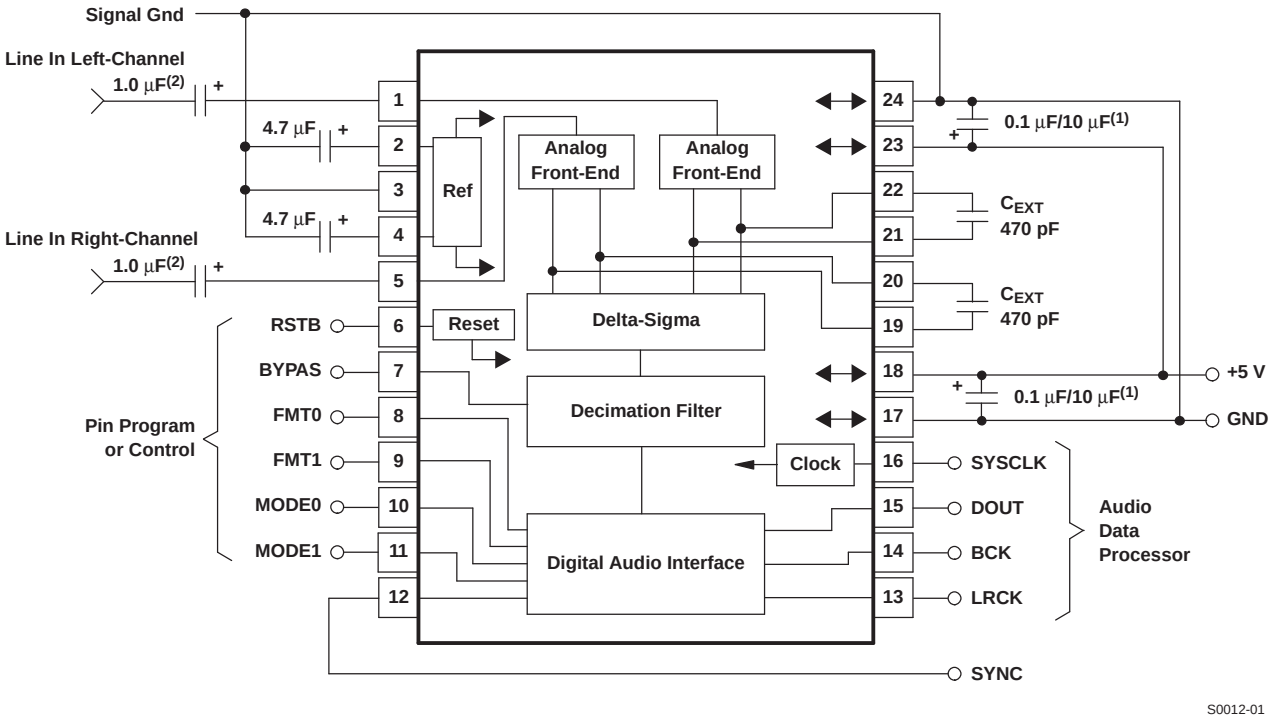
The quality of the system clock can influence dynamic performance in the PCM1800. The duty cycle, jitter, and threshold voltage at the system clock input pin must be carefully managed. When power is supplied to the part, the system clock, bit clock (BCK), and word clock (LRCK) should also be supplied simultaneously. Failure to supply the audio clocks results in a power dissipation increase of up to three times normal dissipation and can degrade long-term reliability if the maximum power dissipation limit is exceeded.

RSTB CONTROL

If the capacitance between $V_{REF}1$ and $V_{REF}2$ exceeds 4.7 µF, an external reset control with a delay-time circuit must be used.

TYPICAL CIRCUIT CONNECTION DIAGRAM

Figure 28 is a typical circuit connection diagram for which the cutoff frequency of the input HPF is about 5 Hz.



(1) Bypass capacitor = 0.1-µF ceramic and 10-µF tantalum, depending on layout and power supply.

(2) A 1-µF capacitor gives a 5.3-Hz cutoff frequency for the input HPF in normal operation and requires a power-on settling period with a 30-ms time constant during power-on initialization.

Figure 28. Typical Circuit Connection

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1800E	ACTIVE	SSOP	DB	24	58	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCM1800E	Samples
PCM1800E/2K	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		PCM1800E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

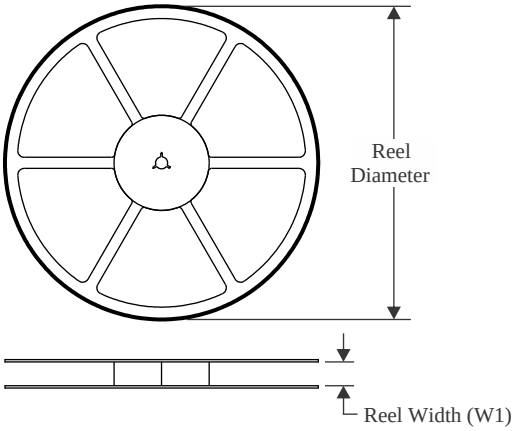
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

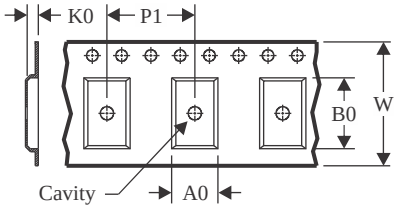
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

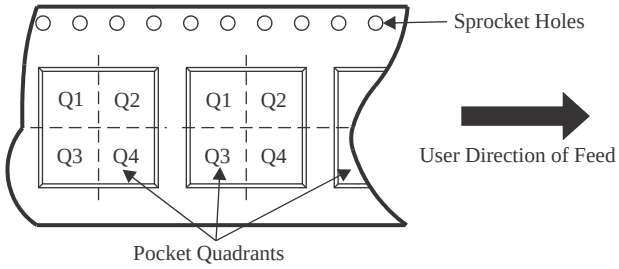


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

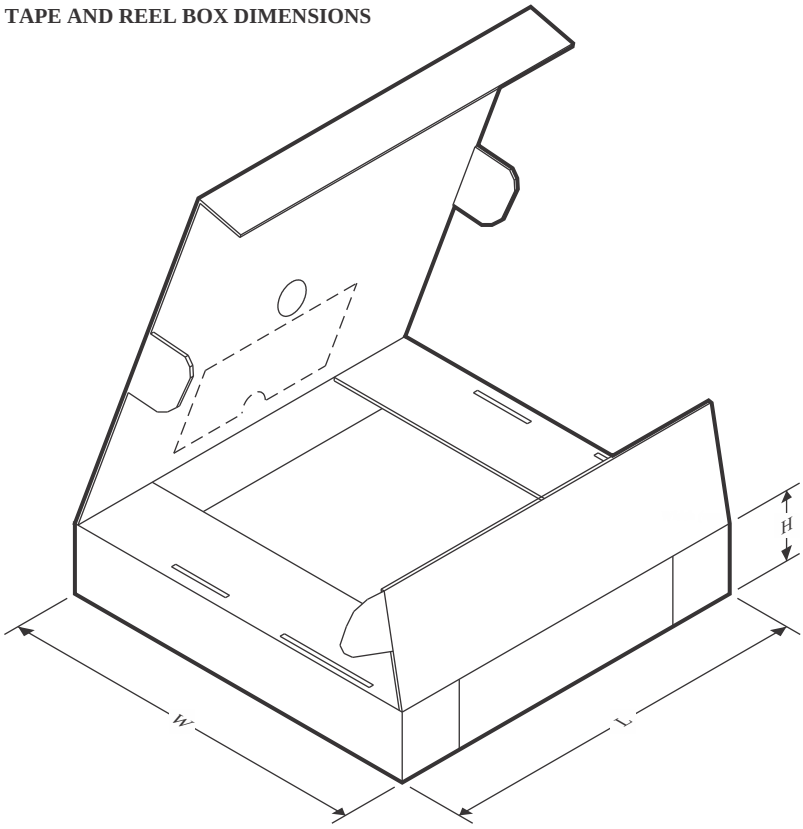
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1800E/2K	SSOP	DB	24	2000	330.0	17.4	8.5	8.6	2.4	12.0	16.0	Q1

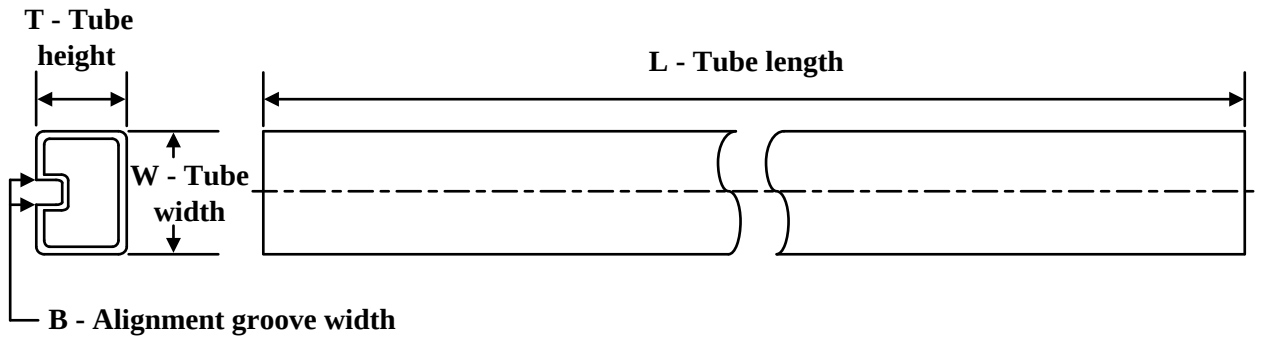
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1800E/2K	SSOP	DB	24	2000	336.6	336.6	28.6

TUBE



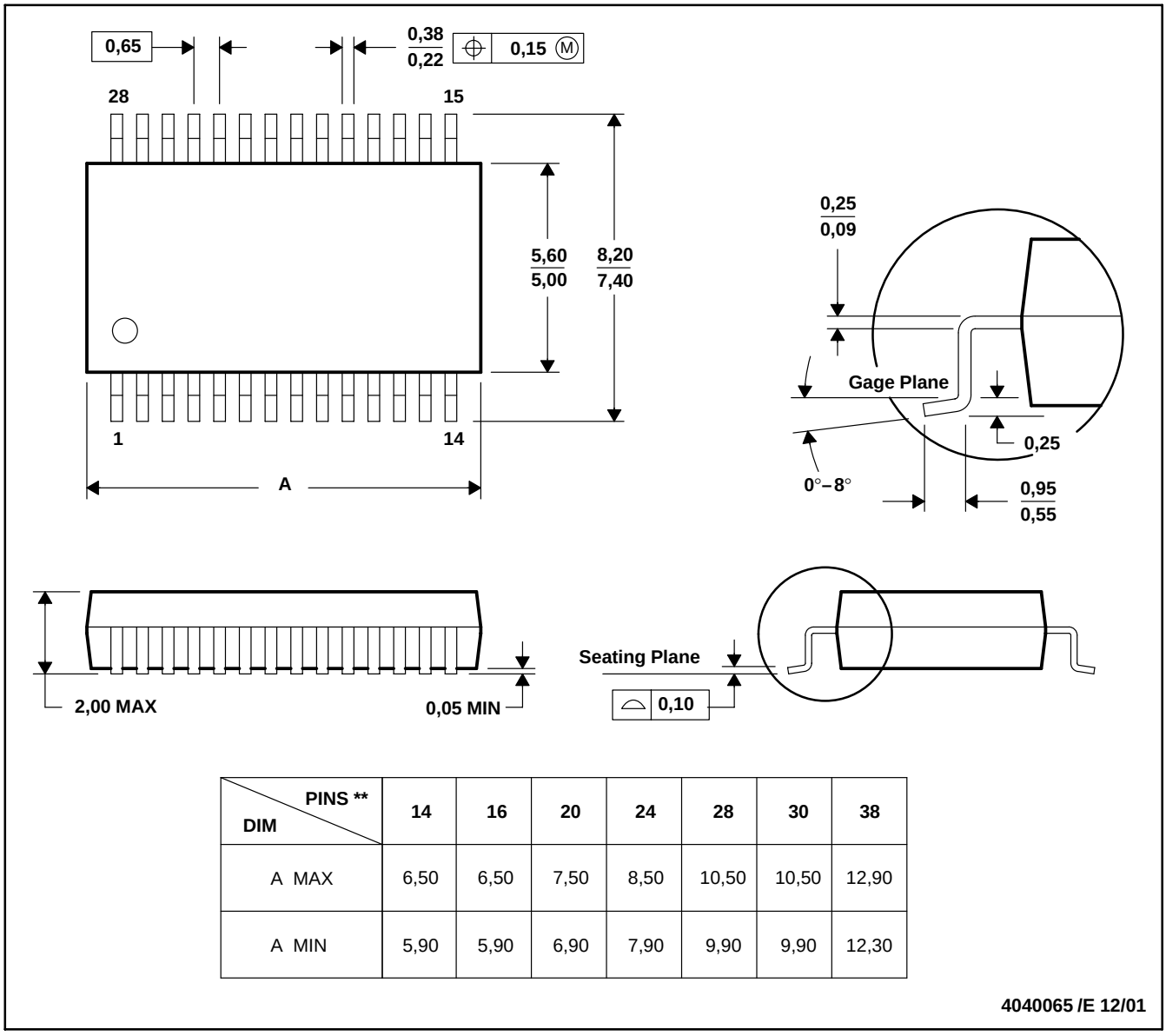
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCM1800E	DB	SSOP	24	58	500	10.6	500	9.6

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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