- **Low Supply Voltage Range, 2.7 V to 3.6 V**
- **Ultralow Power Consumption:**
  - **Active Mode: 400 μA at 1 MHz, 3.0 V**
  - **Standby Mode: 1.6 μA**
  - **Off Mode (RAM Retention): 0.1 μA**
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in Less Than 6 μs**
- **Frequency-Locked Loop, FLL+**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **Embedded Signal Processing for Single-Phase Energy Metering With Integrated Analog Front-End and Temperature Sensor (ESP430CE1)**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **Integrated LCD Driver for 128 Segments**
- **Serial Communication Interface (USART), Asynchronous UART or Synchronous SPI Selectable by Software**
- **Brownout Detector**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse**
- **Bootstrap Loader in Flash Devices**
- **Family Members Include:**
  - **MSP430FE423:**
    **8KB + 256B Flash Memory, 256B RAM**
  - **MSP430FE425:**
    **16KB + 256B Flash Memory, 512B RAM**
  - **MSP430FE427:**
    **32KB + 256B Flash Memory, 1KB RAM**
- **Available in 64-Pin Quad Flat Pack (QFP)**
- **For Complete Module Descriptions, Refer to the *MSP430x4xx Family User's Guide*, Literature Number SLAU056**

## description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6μs.

The MSP430FE42x series are microcontroller configurations with three independent 16-bit sigma-delta analog-to-digital (A/D) converters and an embedded signal processor core used to measure and calculate single-phase energy in both 2-wire and 3-wire configurations. Also included are a built-in 16-bit timer, 128 LCD segment drive capability, and 14 I/O pins.

Typical applications include 2-wire and 3-wire single-phase metering including tamper-resistant meter implementations.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.**

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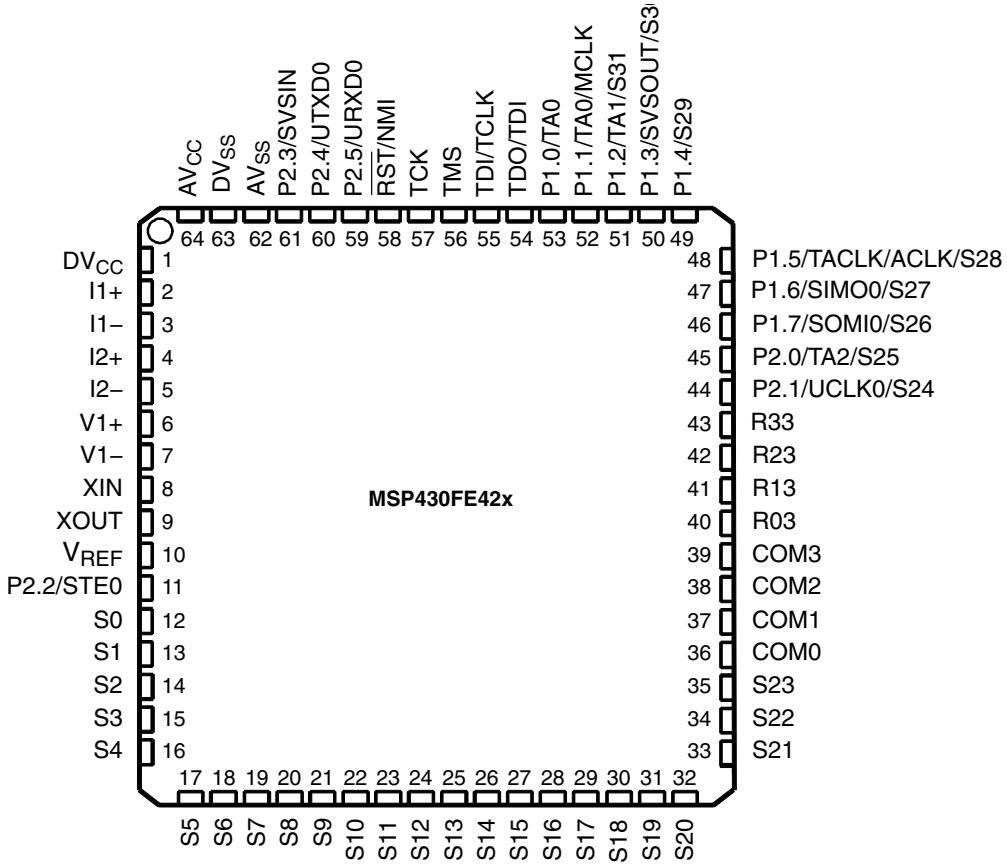
**AVAILABLE OPTIONS**

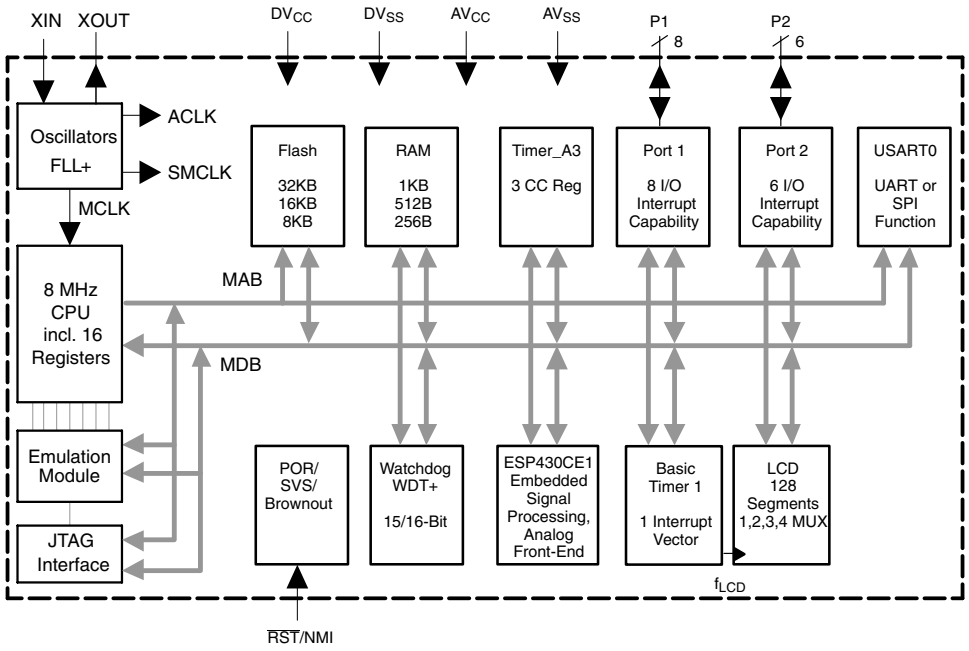
| $T_A$ | PACKAGED DEVICES |
|---|---|
| | PLASTIC 64-PIN QFP (PM) |
| –40°C to 85°C | MSP430FE423IPM<br>MSP430FE425IPM<br>MSP430FE427IPM |

## pin designation†




† Open connection recommended for all unused analog inputs.

## functional block diagram



## Terminal Functions

| TERMINAL PN NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| $DV_{CC}$ | 1 | | Digital supply voltage, positive terminal. |
| $I_1$+ | 2 | I | Current 1 positive analog input. – Internal connection to SD16 Channel 0 A0+. (see Note 1) |
| $I_1$– | 3 | I | Current 1 negative analog input. – Internal connection to SD16 Channel 0 A0–. (see Note 1) |
| $I_2$+ | 4 | I | Current 2 positive analog input. – Internal connection to SD16 Channel 1 A0+. (see Note 1) |
| $I_2$– | 5 | I | Current 2 negative analog input. – Internal connection to SD16 Channel 1 A0–. (see Note 1) |
| $V_1$+ | 6 | I | Voltage 1 positive analog input. – Internal connection to SD16 Channel 2 A0+. (see Note 1) |
| $V_{1-}$ | 7 | I | Voltage 1 negative analog input. – Internal connection to SD16 Channel 2 A0–. (see Note 1) |
| XIN | 8 | I | Input port for crystal oscillator XT1. Standard or watch crystals can be connected. |
| XOUT | 9 | O | Output terminal of crystal oscillator XT1 |
| $V_{REF}$ | 10 | I/O | Input for an external reference voltage / internal reference voltage output (can be used as mid-voltage) |
| P2.2/STE0 | 11 | I/O | General-purpose digital I/O / slave transmit enable—USART0/SPI mode |
| S0 | 12 | O | LCD segment output 0 |
| S1 | 13 | O | LCD segment output 1 |
| S2 | 14 | O | LCD segment output 2 |
| S3 | 15 | O | LCD segment output 3 |
| S4 | 16 | O | LCD segment output 4 |
| S5 | 17 | O | LCD segment output 5 |
| S6 | 18 | O | LCD segment output 6 |
| S7 | 19 | O | LCD segment output 7 |
| S8 | 20 | O | LCD segment output 8 |
| S9 | 21 | O | LCD segment output 9 |
| S10 | 22 | O | LCD segment output 10 |
| S11 | 23 | O | LCD segment output 11 |
| S12 | 24 | O | LCD segment output 12 |
| S13 | 25 | O | LCD segment output 13 |
| S14 | 26 | O | LCD segment output 14 |
| S15 | 27 | O | LCD segment output 15 |
| S16 | 28 | O | LCD segment output 16 |
| S17 | 29 | O | LCD segment output 17 |
| S18 | 30 | O | LCD segment output 18 |
| S19 | 31 | O | LCD segment output 19 |
| S20 | 32 | O | LCD segment output 20 |
| S21 | 33 | O | LCD segment output 21 |
| S22 | 34 | O | LCD segment output 22 |
| S23 | 35 | O | LCD segment output 23 |
| COM0 | 36 | O | Common output, COM0–3 are used for LCD backplanes. |
| COM1 | 37 | O | Common output, COM0–3 are used for LCD backplanes. |
| COM2 | 38 | O | Common output, COM0–3 are used for LCD backplanes. |
| COM3 | 39 | O | Common output, COM0–3 are used for LCD backplanes. |
| R03 | 40 | I | Input port of fourth positive (lowest) analog LCD level (V5) |

NOTE 1: Open connection recommended for all unused analog inputs.

## Terminal Functions (Continued)

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| PN NAME | NO. | | |
| R13 | 41 | I | Input port of third most positive analog LCD level (V4 or V3) |
| R23 | 42 | I | Input port of second most positive analog LCD level (V2) |
| R33 | 43 | O | Output port of most positive analog LCD level (V1) |
| P2.1/UCLK0/S24 | 44 | I/O | General-purpose digital I/O / external clock input-USART0/UART or SPI mode, clock output—USART0/SPI mode / LCD segment output 24 (See Note 1) |
| P2.0/TA2/S25 | 45 | I/O | General-purpose digital I/O / Timer_A Capture: CCI2A input, Compare: Out2 output / LCD segment output 25 (See Note 1) |
| P1.7/SOMI0/S26 | 46 | I/O | General-purpose digital I/O / slave out/master in of USART0/SPI mode / LCD segment output 26 (See Note 1) |
| P1.6/SIMO0/S27 | 47 | I/O | General-purpose digital I/O / slave in/master out of USART0/SPI mode / LCD segment output 27 (See Note 1) |
| P1.5/TACLK/ ACLK/S28 | 48 | I/O | General-purpose digital I/O / Timer_A and SD16 clock signal TACLK input / ACLK output (divided by 1, 2, 4, or 8) / LCD segment output 28 (See Note 1) |
| P1.4/S29 | 49 | I/O | General-purpose digital I/O / LCD segment output 29 (See Note 1) |
| P1.3/SVSOUT/ S30 | 50 | I/O | General-purpose digital I/O / SVS: output of SVS comparator / LCD segment output 30 (See Note 1) |
| P1.2/TA1/S31 | 51 | I/O | General-purpose digital I/O / Timer_A, Capture: CCI1A, CCI1B input, Compare: Out1 output / LCD segment output 31 (See Note 1) |
| P1.1/TA0/MCLK | 52 | I/O | General-purpose digital I/O / Timer_A, Capture: CCI0B input / MCLK output.<br>Note: TA0 is only an input on this pin / BSL receive |
| P1.0/TA0 | 53 | I/O | General-purpose digital I/O / Timer_A, Capture: CCI0A input, Compare: Out0 output / BSL transmit |
| TDO/TDI | 54 | I/O | Test data output port. TDO/TDI data output or programming data input terminal. |
| TDI/TCLK | 55 | I | Test data input or test clock input. The device protection fuse is connected to TDI. |
| TMS | 56 | I | Test mode select. TMS is used as an input port for device programming and test. |
| TCK | 57 | I | Test clock. TCK is the clock input port for device programming and test. |
| $\overline{\text{RST}}$/NMI | 58 | I | Reset input or nonmaskable interrupt input port |
| P2.5/URXD0 | 59 | I/O | General-purpose digital I/O / receive data in—USART0/UART mode |
| P2.4/UTXD0 | 60 | I/O | General-purpose digital I/O / transmit data out—USART0/UART mode |
| P2.3/SVSIN | 61 | I/O | General-purpose digital I/O / Analog input to brownout, supply voltage supervisor |
| $AV_{SS}$ | 62 | | Analog supply voltage, negative terminal. Supplies SD16, SVS, brownout, oscillator, and LCD resistive divider circuitry. |
| $DV_{SS}$ | 63 | | Digital supply voltage, negative terminal. |
| $AV_{CC}$ | 64 | | Analog supply voltage, positive terminal. Supplies SD16, SVS, brownout, oscillator, and LCD resistive divider circuitry; must not power up prior to $DV_{CC}$. |

NOTE 1: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

## short-form description

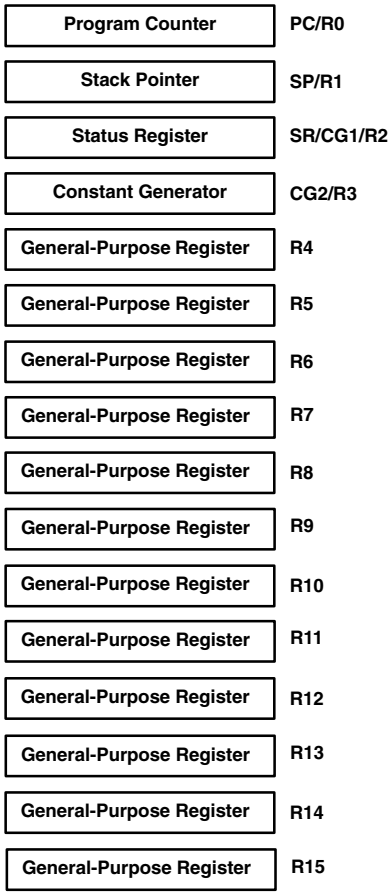
### CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.




### instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

**Table 1. Instruction Word Formats**

| | | |
|---|---|---|
| Dual operands, source-destination | e.g. ADD R4,R5 | R4 + R5 –––> R5 |
| Single operands, destination only | e.g. CALL R8 | PC –––>(TOS), R8–––> PC |
| Relative jump, un/conditional | e.g. JNE | Jump-on-equal bit = 0 |

**Table 2. Address Mode Descriptions**

| ADDRESS MODE | S | D | SYNTAX | EXAMPLE | OPERATION |
|---|---|---|---|---|---|
| Register | ● | ● | MOV Rs,Rd | MOV R10,R11 | R10 –––> R11 |
| Indexed | ● | ● | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5)–––> M(6+R6) |
| Symbolic (PC relative) | ● | ● | MOV EDE,TONI | | M(EDE) –––> M(TONI) |
| Absolute | ● | ● | MOV &MEM,&TCDAT | | M(MEM) –––> M(TCDAT) |
| Indirect | ● | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) –––> M(Tab+R6) |
| Indirect autoincrement | ● | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) –––> R11<br>R10 + 2–––> R10 |
| Immediate | ● | | MOV #X,TONI | MOV #45,TONI | #45 –––> M(TONI) |

NOTE: S = source D = destination

### operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
    ACLK and SMCLK remain active, MCLK is available to modules
    FLL+ loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
    ACLK and SMCLK remain active, MCLK is available to modules
    FLL+ loop control is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
    ACLK is disabled
    MCLK, FLL+ loop control, and DCOCLK are disabled
    DCO's dc-generator is disabled
    Crystal oscillator is stopped

### interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| Power-up<br>External Reset<br>Watchdog<br>Flash memory<br>PC Out-of-Range (see Note 4) | WDTIFG<br>KEYV<br>(see Note 1) | Reset | 0FFFEh | 15, highest |
| NMI<br>Oscillator Fault<br>Flash memory access violation | NMIIFG (see Notes 1 and 3)<br>OFIFG (see Notes 1 and 3)<br>ACCVIFG (see Notes 1 and 3) | (Non)maskable<br>(Non)maskable<br>(Non)maskable | 0FFFCh | 14 |
| ESP430 | MBCTL_OUTxIFG,<br>MBCTL_INxIFG<br>(see Notes 1 and 2) | Maskable | 0FFFAh | 13 |
| SD16 | SD16CCTLx SD16OVIFG,<br>SD16CCTLx SD16IFG<br>(see Notes 1 and 2) | Maskable | 0FFF8h | 12 |
| | | | 0FFF6h | 11 |
| Watchdog Timer | WDTIFG | Maskable | 0FFF4h | 10 |
| USART0 Receive | URXIFG0 | Maskable | 0FFF2h | 9 |
| USART0 Transmit | UTXIFG0 | Maskable | 0FFF0h | 8 |
| | | | 0FFEEh | 7 |
| Timer_A3 | TACCR0 CCIFG (see Note 2) | Maskable | 0FFECh | 6 |
| Timer_A3 | TACCR1 and TACCR2<br>CCIFGs, and TACTL TAIFG<br>(see Notes 1 and 2) | Maskable | 0FFEAh | 5 |
| I/O port P1 (eight flags) | P1IFG.0 to P1IFG.7<br>(see Notes 1 and 2) | Maskable | 0FFE8h | 4 |
| | | | 0FFE6h | 3 |
| | | | 0FFE4h | 2 |
| I/O port P2 (eight flags) | P2IFG.0 to P2IFG.7<br>(see Notes 1 and 2) | Maskable | 0FFE2h | 1 |
| Basic Timer1 | BTIFG | Maskable | 0FFE0h | 0, lowest |

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt-enable cannot.
4. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h–01FFh) or from within unused address ranges (from 0600h to 0BFFh).

## special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

## interrupt enable 1 and 2

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0h | UTXIE0 | URXIE0 | ACCVIE | NMIIE | | | OFIE | WDTIE |
| | rw–0 | rw–0 | rw–0 | rw–0 | | | rw–0 | rw–0 |

WDTIE: Watchdog-timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.

OFIE: Oscillator-fault interrupt enable

NMIIE: Nonmaskable interrupt enable

ACCVIE: Flash access violation interrupt enable

URXIE0: USART0: UART and SPI receive interrupt enable

UTXIE0: USART0: UART and SPI transmit interrupt enable

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1h | BTIE | | | | | | | |
| | rw-0 | | | | | | | |

BTIE: Basic Timer1 interrupt enable

## interrupt flag register 1 and 2

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 02h | UTXIFG0 | URXIFG0 | | NMIIFG | | | OFIFG | WDTIFG |
| | rw–1 | rw–0 | | rw–0 | | | rw–1 | rw–(0) |

WDTIFG: Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on $V_{CC}$ power up or a reset condition at the $\overline{RST}$/NMI pin in reset mode.

OFIFG: Flag set on oscillator fault

NMIIFG: Set via $\overline{RST}$/NMI pin

URXIFG0: USART0: UART and SPI receive flag

UTXIFG0: USART0: UART and SPI transmit flag

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 3h | BTIFG | | | | | | | |
| | rw-0 | | | | | | | |

BTIFG: Basic Timer1 interrupt flag

### module enable registers 1 and 2

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 04h | UTXE0 | URXE0<br>USPIE0 | | | | | | |
| | rw–0 | rw–0 | | | | | | |

URXE0: USART0: UART mode receive enable

UTXE0: USART0: UART mode transmit enable

USPIE0: USART0: SPI mode transmit and receive enable

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 05h | | | | | | | | |

**Legend:** **rw–0,1:** **Bit Can Be Read and Written. It Is Reset or Set by PUC.**
**rw–(0,1):** **Bit Can Be Read and Written. It Is Reset or Set by POR.**
**SFR Bit Not Present in Device.**

### memory organization

| | | MSP430FE423 | MSP430FE425 | MSP430FE427 |
|---|---|---|---|---|
| Memory | Size | 8KB | 16KB | 32KB |
| Interrupt vector | Flash | 0FFFFh – 0FFE0h | 0FFFFh – 0FFE0h | 0FFFFh – 0FFE0h |
| Code memory | Flash | 0FFFFh – 0E000h | 0FFFFh – 0C000h | 0FFFFh – 08000h |
| Information memory | Size | 256 Byte<br>010FFh – 01000h | 256 Byte<br>010FFh – 01000h | 256 Byte<br>010FFh – 01000h |
| Boot memory | Size | 1kB<br>0FFFh – 0C00h | 1kB<br>0FFFh – 0C00h | 1kB<br>0FFFh – 0C00h |
| RAM | Size | 256 Byte<br>02FFh – 0200h | 512 Byte<br>03FFh – 0200h | 1KB<br>05FFh – 0200h |
| Peripherals | 16-bit | 01FFh – 0100h | 01FFh – 0100h | 01FFh – 0100h |
| | 8-bit | 0FFh – 010h | 0FFh – 010h | 0FFh – 010h |
| | 8-bit SFR | 0Fh – 00h | 0Fh – 00h | 0Fh – 00h |

### bootstrap loader (BSL)

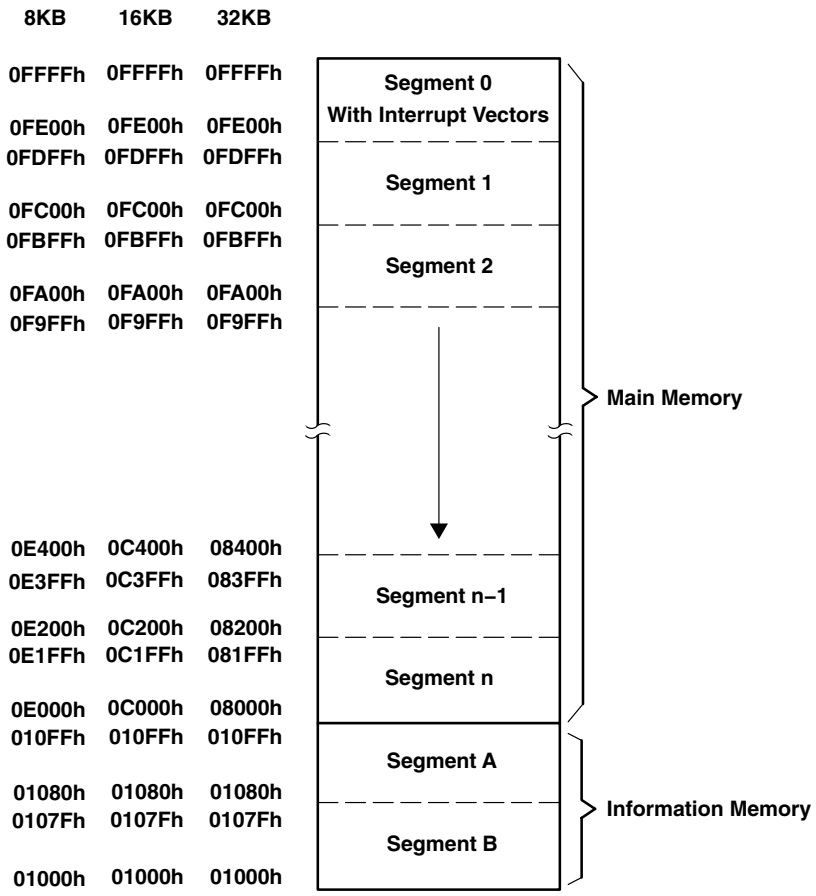
The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

| BSL Function | PM Package Pins |
|---|---|
| Data Transmit | 53 - P1.0 |
| Data Receive | 52 - P1.1 |

## flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0 to n. Segments A and B are also called *information memory.*
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.



### peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x4xx Family User's Guide*, literature number SLAU056.

### oscillator and system clock

The clock system in the MSP430FE42x family of devices is supported by the FLL+ module that includes support for a 32768 Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low-power consumption. The FLL+ features a digital frequency locked loop (FLL) hardware which in conjunction with a digital modulator stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768 Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8.

### brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, $V_{CC}$ may not have ramped to $V_{CC(min)}$ at that time. The user must ensure the default FLL+ settings are not changed until $V_{CC}$ reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when $V_{CC}$ reaches $V_{CC(min)}$.

### digital I/O

There are two 8-bit I/O ports implemented—ports P1 and P2 (only six P2 I/O signals are available on external pins):

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and six bits of P2.
- Read/write access to port-control registers is supported by all instructions.

**NOTE:**
Six bits of port P2 (P2.0 to P2.5) are available on external pins, but all control and data bits for port P2 are implemented.

### Basic Timer1

The Basic Timer1 has two independent 8-bit timers which can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 can be used to generate periodic interrupts and clock for the LCD module.

### LCD drive

The LCD driver generates the segment and common signals required to drive an LCD display. The LCD controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral.

### WDT+ watchdog timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

### timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

| TIMER_A3 SIGNAL CONNECTIONS | | | | | |
|---|---|---|---|---|---|
| **INPUT PIN NUMBER** | **DEVICE INPUT SIGNAL** | **MODULE INPUT NAME** | **MODULE BLOCK** | **MODULE OUTPUT SIGNAL** | **OUTPUT PIN NUMBER** |
| 48 - P1.5 | TACLK | TACLK | Timer | NA | |
| | ACLK | ACLK | | | |
| | SMCLK | SMCLK | | | |
| 48 - P1.5 | $\overline{\text{TACLK}}$ | INCLK | | | |
| 53 - P1.0 | TA0 | CCI0A | CCR0 | TA0 | 53 - P1.0 |
| 52 - P1.1 | TA0 | CCI0B | | | |
| | $DV_{SS}$ | GND | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | |
| 51 - P1.2 | TA1 | CCI1A | CCR1 | TA1 | 51 - P1.2 |
| 51 - P1.2 | TA1 | CCI1B | | | |
| | $DV_{SS}$ | GND | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | |
| 45 - P2.0 | TA2 | CCI2A | CCR2 | TA2 | 45 - P2.0 |
| | ACLK (internal) | CCI2B | | | |
| | $DV_{SS}$ | GND | | | |
| | $DV_{CC}$ | $V_{CC}$ | | | |

### USART0

The MSP430FE42x devices have one hardware universal synchronous/asynchronous receive transmit (USART0) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

### ESP430CE1

The ESP430CE1 module integrates a hardware multiplier, three independent 16-bit Sigma-Delta A/D converters (SD16) and an embedded signal processor (ESP430). The ESP430CE1 module measures 2 or 3-wire, single-phase energy and automatically calculates parameters which are made available to the MSP430 CPU. The module can be calibrated and initialized to accurately calculate energy, power factor, etc., for a wide range of metering sensor configurations.

## peripheral file map

| PERIPHERALS WITH WORD ACCESS | | | |
|---|---|---|---|
| **Watchdog** | Watchdog Timer control | WDTCTL | 0120h |
| **Timer_A3** | Timer_A interrupt vector | TAIV | 012Eh |
| | Timer_A control | TACTL | 0160h |
| | Capture/compare control 0 | TACCTL0 | 0162h |
| | Capture/compare control 1 | TACCTL1 | 0164h |
| | Capture/compare control 2 | TACCTL2 | 0166h |
| | Reserved | | 0168h |
| | Reserved | | 016Ah |
| | Reserved | | 016Ch |
| | Reserved | | 016Eh |
| | Timer_A register | TAR | 0170h |
| | Capture/compare register 0 | TACCR0 | 0172h |
| | Capture/compare register 1 | TACCR1 | 0174h |
| | Capture/compare register 2 | TACCR2 | 0176h |
| | Reserved | | 0178h |
| | Reserved | | 017Ah |
| | Reserved | | 017Ch |
| | Reserved | | 017Eh |
| **Hardware Multiplier (see Note 1)** | Sum extend | SUMEXT | 013Eh |
| | Result high word | RESHI | 013Ch |
| | Result low word | RESLO | 013Ah |
| | Second operand | OP2 | 0138h |
| | Multiply signed + accumulate/operand1 | MACS | 0136h |
| | Multiply + accumulate/operand1 | MAC | 0134h |
| | Multiply signed/operand1 | MPYS | 0132h |
| | Multiply unsigned/operand1 | MPY | 0130h |
| **Flash** | Flash control 3 | FCTL3 | 012Ch |
| | Flash control 2 | FCTL2 | 012Ah |
| | Flash control 1 | FCTL1 | 0128h |
| **SD16 (see Note 1) (see also: Peripherals with Byte Access)** | General Control | SD16CTL | 0100h |
| | Channel 0 Control | SD16CCTL0 | 0102h |
| | Channel 1 Control | SD16CCTL1 | 0104h |
| | Channel 2 Control | SD16CCTL2 | 0106h |
| | Reserved | | 0108h |
| | Reserved | | 010Ah |
| | Reserved | | 010Ch |
| | Reserved | | 010Eh |
| | Interrupt vector word register | SD16IV | 0110h |
| | Channel 0 conversion memory | SD16MEM0 | 0112h |

NOTE 1: Module is contained within ESP430CE1. Registers not accessible when ESP430 is active. ESP430 must be disabled or suspended to allow CPU access to these modules.

| PERIPHERALS WITH WORD ACCESS | | | |
|---|---|---|---|
| **SD16 (continued, see Note 1)** | Channel 1 conversion memory | SD16MEM1 | 0114h |
| | Channel 2 conversion memory | SD16MEM2 | 0116h |
| | Reserved | | 0118h |
| | Reserved | | 011Ah |
| | Reserved | | 011Ch |
| | Reserved | | 011Eh |
| **ESP430 (ESP430CE1)** | ESP430 Control | ESPCTL | 0150h |
| | Mailbox Control | MBCTL | 0152h |
| | Mailbox In 0 | MBIN0 | 0154h |
| | Mailbox In 1 | MBIN1 | 0156h |
| | Mailbox Out 0 | MBOUT0 | 0158h |
| | Mailbox Out 1 | MBOUT1 | 015Ah |
| | ESP430 Return Value 0 | RET0 | 01C0h |
| | : | : | : |
| | ESP430 Return Value 31 | RET31 | 01FEh |
| **PERIPHERALS WITH BYTE ACCESS** | | | |
| **SD16 (see Note 1) (see also: Peripherals with Word Access)** | Channel 0 Input Control | SD16INCTL0 | 0B0h |
| | Channel 1 Input Control | SD16INCTL1 | 0B1h |
| | Channel 2 Input Control | SD16INCTL2 | 0B2h |
| | Reserved | | 0B3h |
| | Reserved | | 0B4h |
| | Reserved | | 0B5h |
| | Reserved | | 0B6h |
| | Reserved | | 0B7h |
| | Channel 0 preload | SD16PRE0 | 0B8h |
| | Channel 1 preload | SD16PRE1 | 0B9h |
| | Channel 2 preload | SD16PRE2 | 0BAh |
| | Reserved | | 0BBh |
| | Reserved | | 0BCh |
| | Reserved | | 0BDh |
| | Reserved | | 0BEh |
| | Reserved | | 0BFh |
| **LCD** | LCD memory 20 | LCDM20 | 0A4h |
| | : | : | : |
| | LCD memory 16 | LCDM16 | 0A0h |
| | LCD memory 15 | LCDM15 | 09Fh |
| | : | : | : |
| | LCD memory 1 | LCDM1 | 091h |
| | LCD control and mode | LCDCTL | 090h |

NOTE 1: Module is contained within ESP430CE1. Registers not accessible when ESP430 is active. ESP430 must be disabled or suspended to allow CPU access to these modules.

## peripheral file map (continued)

| PERIPHERALS WITH BYTE ACCESS (CONTINUED) | | | |
|---|---|---|---|
| **USART0** | Transmit buffer | U0TXBUF | 077h |
| | Receive buffer | U0RXBUF | 076h |
| | Baud rate | U0BR1 | 075h |
| | Baud rate | U0BR0 | 074h |
| | Modulation control | U0MCTL | 073h |
| | Receive control | U0RCTL | 072h |
| | Transmit control | U0TCTL | 071h |
| | USART control | U0CTL | 070h |
| **Brownout, SVS** | SVS control register | SVSCTL | 056h |
| **FLL+ Clock** | FLL+ Control1 | FLL_CTL1 | 054h |
| | FLL+ Control0 | FLL_CTL0 | 053h |
| | System clock frequency control | SCFQCTL | 052h |
| | System clock frequency integrator | SCFI1 | 051h |
| | System clock frequency integrator | SCFI0 | 050h |
| **Basic Timer1** | BT counter2 | BTCNT2 | 047h |
| | BT counter1 | BTCNT1 | 046h |
| | BT control | BTCTL | 040h |
| **Port P2** | Port P2 selection | P2SEL | 02Eh |
| | Port P2 interrupt enable | P2IE | 02Dh |
| | Port P2 interrupt-edge select | P2IES | 02Ch |
| | Port P2 interrupt flag | P2IFG | 02Bh |
| | Port P2 direction | P2DIR | 02Ah |
| | Port P2 output | P2OUT | 029h |
| | Port P2 input | P2IN | 028h |
| **Port P1** | Port P1 selection | P1SEL | 026h |
| | Port P1 interrupt enable | P1IE | 025h |
| | Port P1 interrupt-edge select | P1IES | 024h |
| | Port P1 interrupt flag | P1IFG | 023h |
| | Port P1 direction | P1DIR | 022h |
| | Port P1 output | P1OUT | 021h |
| | Port P1 input | P1IN | 020h |
| **Special Functions** | SFR module enable 2 | ME2 | 005h |
| | SFR module enable 1 | ME1 | 004h |
| | SFR interrupt flag 2 | IFG2 | 003h |
| | SFR interrupt flag 1 | IFG1 | 002h |
| | SFR interrupt enable2 | IE2 | 001h |
| | SFR interrupt enable1 | IE1 | 000h |

## absolute maximum ratings†

Voltage applied at $V_{CC}$ to $V_{SS}$ . . . . . –0.3 V to + 4.1 V
Voltage applied to any pin (see Note 1) . . . . . –0.3 V to $V_{CC}$ + 0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature (unprogrammed device) . . . . . –55°C to 150°C
Storage temperature (programmed device) . . . . . –40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages referenced to $V_{SS}$. The JTAG fuse-blow voltage, $V_{FB}$, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

## recommended operating conditions (see Note 1)

| PARAMETER | | | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply voltage during program execution; ESP430 and SD16 disabled, $V_{CC}$ ($AV_{CC}$ = $DV_{CC}$ = $V_{CC}$) (see Note 1) | | MSP430FE42x | 1.8 | | 3.6 | V |
| Supply voltage during program execution; SVS enabled, PORON = 1, ESP430 and SD16 disabled, $V_{CC}$ ($AV_{CC}$ = $DV_{CC}$ = $V_{CC}$) (see Note 1 and Note 2) | | MSP430FE42x | 2.0 | | 3.6 | V |
| Supply voltage during program execution; ESP430 or SD16 enabled or during programming of flash memory, $V_{CC}$ ($AV_{CC}$ = $DV_{CC}$ = $V_{CC}$) (see Note 1) | | MSP430FE42x | 2.7 | | 3.6 | V |
| Supply voltage (see Note 1), $V_{SS}$ ($AV_{SS}$ = $DV_{SS}$ = $V_{SS}$) | | | 0 | | 0 | V |
| Operating free-air temperature range, $T_A$ | | MSP430FE42x | –40 | | 85 | °C |
| LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 3) | LF selected, XTS_FLL=0 | Watch crystal | | 32768 | | Hz |
| | XT1 selected, XTS_FLL=1 | Ceramic resonator | 450 | | 8000 | kHz |
| | XT1 selected, XTS_FLL=1 | Crystal | 1000 | | 8000 | kHz |
| Processor frequency (signal MCLK), $f_{(System)}$ (see Note 4) | | $V_{CC}$ = 2.7 V | DC | | 8.4 | MHz |
| | | $V_{CC}$ = 3.6 V | DC | | 8.4 | |

NOTES: 1. It is recommended to power $AV_{CC}$ and $DV_{CC}$ from the same source. A maximum difference of 0.3 V between $AV_{CC}$ and $DV_{CC}$ can be tolerated during power up and operation.
2. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing supply voltage. POR is going inactive when the supply voltage is raised above minimum supply voltage plus the hysteresis of the SVS circuitry.
3. The LFXT1 oscillator in LF-mode requires a watch crystal.
4. For frequencies above 8 MHz, MCLK is sourced by the built-in oscillator (DCO and FLL+).

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

### supply current into $AV_{CC}$ + $DV_{CC}$ excluding external current (see Note 1)

| PARAMETER | | TEST CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{(AM)}$ | Active mode, $f_{(MCLK)} = f_{(SMCLK)} = f_{(DCO)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz, XTS_FLL = 0 (program executes in flash) | $T_A$ = –40°C to 85°C | $V_{CC}$ = 3 V | | 400 | 500 | µA |
| $I_{(LPM0)}$ | Low-power mode, (LPM0/LPM1) $f_{(MCLK)} = f_{(SMCLK)} = f_{(DCO)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz, XTS_FLL = 0 FN_8=FN_4=FN_3=FN_2=0 (see Note 2) | $T_A$ = –40°C to 85°C | $V_{CC}$ = 3 V | | 130 | 150 | µA |
| $I_{(LPM2)}$ | Low-power mode, (LPM2) (see Note 2) | $T_A$ = –40°C to 85°C | $V_{CC}$ = 3 V | | 10 | 22 | µA |
| $I_{(LPM3)}$ | Low-power mode, (LPM3) (see Note 2) | $T_A$ = –40°C | $V_{CC}$ = 3 V | | 1.5 | 2.0 | µA |
| | | $T_A$ = 25°C | | | 1.6 | 2.1 | |
| | | $T_A$ = 60°C | | | 1.7 | 2.2 | |
| | | $T_A$ = 85°C | | | 2.0 | 2.6 | |
| $I_{(LPM4)}$ | Low-power mode, (LPM4) (see Note 2) | $T_A$ = –40°C | $V_{CC}$ = 3 V | | 0.1 | 0.5 | µA |
| | | $T_A$ = 25°C | | | 0.1 | 0.5 | |
| | | $T_A$ = 85°C | | | 0.8 | 2.5 | |

NOTES: 1. All inputs are tied to 0 V or $V_{CC}$. Outputs do not source or sink any current.
The current consumption in LPM2, LPM3, and LPM4 are measured with active Basic Timer1 and LCD (ACLK selected).
The current consumption of the ESP430CE1 and the SVS module are specified in their respective sections.
LPMx currents measured with WDT+ disabled.
The currents are characterized with a KDS Daishinku DT–38 (6 pF) crystal.
2. Current for brownout included.

### current consumption of active mode versus system frequency

$$I_{(AM)} = I_{(AM)\ [1\ MHz]} \times f_{(System)\ [MHz]}$$

### current consumption of active mode versus supply voltage

$$I_{(AM)} = I_{(AM)\ [3\ V]} + 170\ \mu A/V \times (V_{CC} - 3\ V)$$

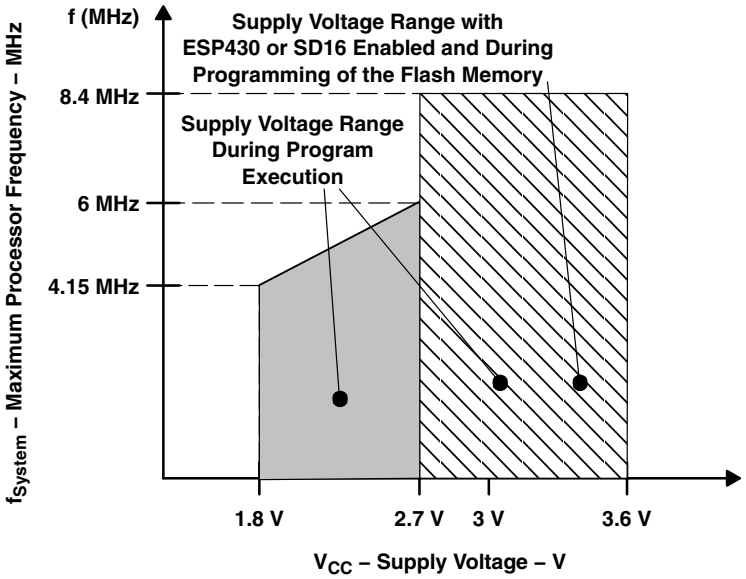



**Figure 1. Frequency vs Supply Voltage**

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### Schmitt-trigger inputs – Ports P1 and P2; $\overline{\text{RST}}$/NMI; JTAG: TCK, TMS, TDI/TCLK, TDO/TDI

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | $V_{CC}$ = 3 V | 1.5 | | 1.98 | V |
| $V_{IT-}$ | Negative-going input threshold voltage | $V_{CC}$ = 3 V | 0.9 | | 1.3 | V |
| $V_{hys}$ | Input voltage hysteresis ($V_{IT+} - V_{IT-}$) | $V_{CC}$ = 3 V | 0.45 | | 1 | V |

### inputs Px.x, TAx

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{(int)}$ | External interrupt timing | Port P1, P2: P1.x to P2.x, External trigger signal for the interrupt flag, (see Note 1) | 3 V | 1.5 | | | cycle |
| | | | 3 V | 50 | | | ns |
| $t_{(cap)}$ | Timer_A, capture timing | TAx | 3 V | 50 | | | ns |
| $f_{(TAext)}$ | Timer_A clock frequency externally applied to pin | TACLK, INCLK $t_{(H)} = t_{(L)}$ | 3 V | | | 10 | MHz |
| $f_{(TAint)}$ | Timer_A clock frequency | SMCLK or ACLK signal selected | 3 V | | | 10 | MHz |

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ cycle and time parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$. Both the cycle and timing specifications must be met to ensure the flag is set. $t_{(int)}$ is measured in MCLK cycles.

### leakage current (see Note 1)

| PARAMETER | | | TEST CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{lkg(P1.x)}$ | Leakage current | Port P1 | Port 1: $V_{(P1.x)}$ (see Note 2) | $V_{CC}$ = 3 V | | | ±50 | nA |
| $I_{lkg(P2.x)}$ | | Port P2 | Port 2: $V_{(P2.x)}$ (see Note 2) | | | | ±50 | |

NOTES: 1. The leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as an input.

### outputs – Ports P1 and P2

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH(max)}$ = –1.5 mA, | $V_{CC}$ = 3 V, | See Note 1 | $V_{CC}$–0.25 | | $V_{CC}$ | V |
| | | $I_{OH(max)}$ = –6 mA, | $V_{CC}$ = 3 V, | See Note 2 | $V_{CC}$–0.6 | | $V_{CC}$ | |
| $V_{OL}$ | Low-level output voltage | $I_{OL(max)}$ = 1.5 mA, | $V_{CC}$ = 3 V, | See Note 1 | $V_{SS}$ | | $V_{SS}$+0.25 | V |
| | | $I_{OL(max)}$ = 6 mA, | $V_{CC}$ = 3 V, | See Note 2 | $V_{SS}$ | | $V_{SS}$+0.6 | |

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

### output frequency

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{Px.y}$ | (1 ≤ x ≤ 2, 0 ≤ y ≤ 7) | $C_L$ = 20 pF, $I_L$ = ± 1.5mA | $V_{CC}$ = 3 V | DC | | 12 | MHz |
| $f_{ACLK}$, $f_{MCLK}$, $f_{SMCLK}$ | P1.1/TA0/MCLK P1.5/TACLK/ACLK/S28 | $C_L$ = 20 pF | $V_{CC}$ = 3 V | | | 12 | MHz |
| $t_{Xdc}$ | Duty cycle of output frequency | P1.5/TACLK/ACLK/ S28, $C_L$ = 20 pF $V_{CC}$ = 3 V | $f_{ACLK} = f_{LFXT1} = f_{XT1}$ | 40% | | 60% | |
| | | | $f_{ACLK} = f_{LFXT1} = f_{LF}$ | 30% | | 70% | |
| | | | $f_{ACLK} = f_{LFXT1}$ | | 50% | | |
| | | P1.1/TA0/MCLK, $C_L$ = 20 pF, $V_{CC}$ = 3 V | $f_{MCLK} = f_{DCOCLK}$ | 50%– 15 ns | 50% | 50%+ 15 ns | |

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**outputs – Ports P1 and P2 (continued)**

**TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE**

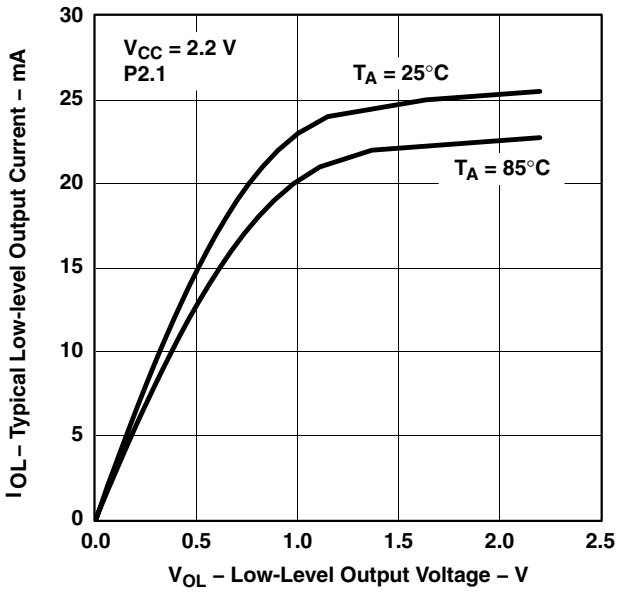



**Figure 2**

**TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE**

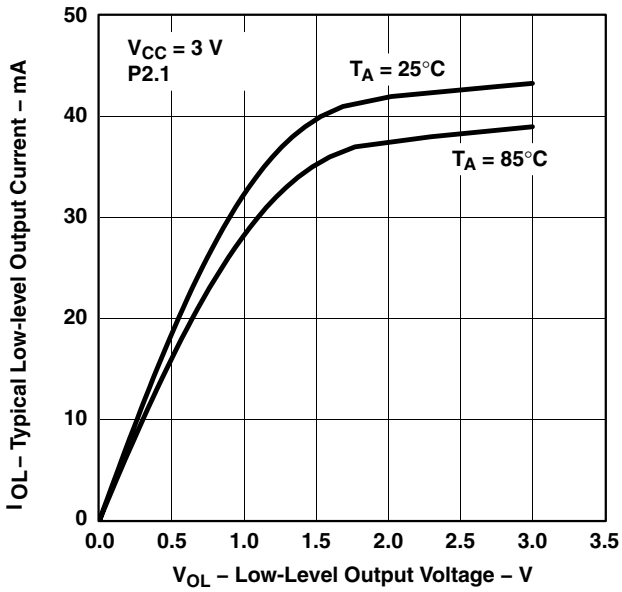



**Figure 3**

**TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE**

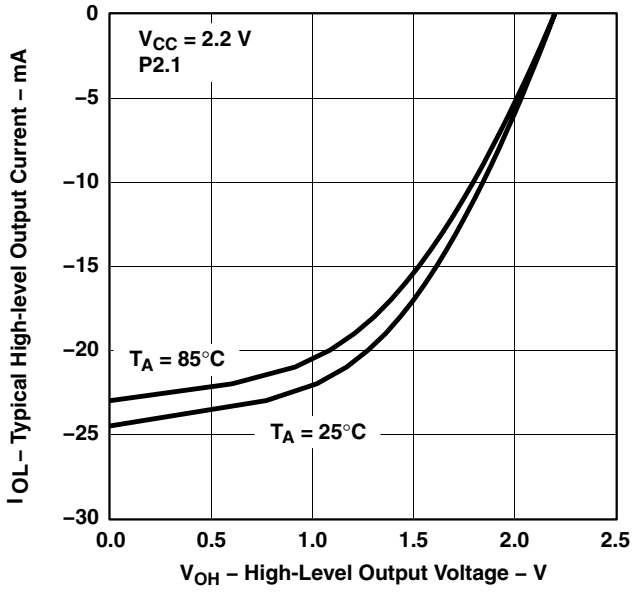



**Figure 4**

**TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE**

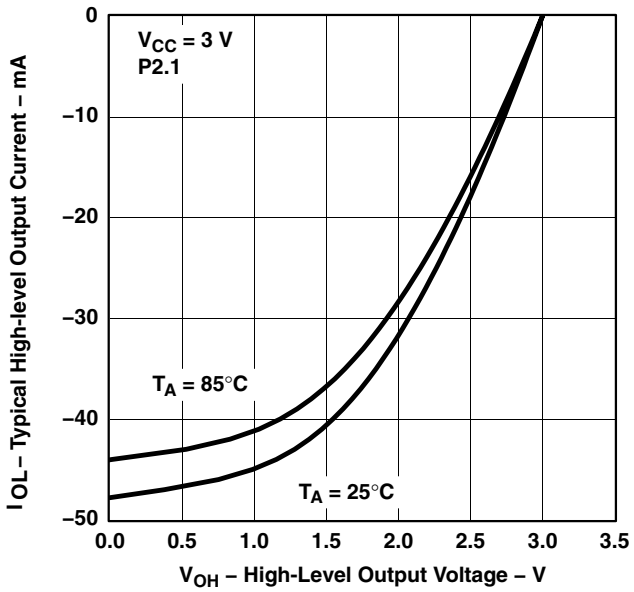



**Figure 5**

NOTE: One output loaded at a time

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### wake-up LPM3

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{d(LPM3)}$ | Delay time | f = 1 MHz | $V_{CC}$ = 3 V | | | 6 | µs |
| | | f = 2 MHz | | | | 6 | |
| | | f = 3 MHz | | | | 6 | |

### RAM (see Note 1)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| VRAMh | CPU halted (see Note 1) | 1.6 | | | V |

NOTE 1: This parameter defines the minimum supply voltage when the data in the program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

### LCD

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{(33)}$ | Analog voltage | Voltage at R33 | $V_{CC}$ = 3 V | 2.5 | | $V_{CC}$ +0.2 | V |
| $V_{(23)}$ | | Voltage at R23 | | | $(V_{33}–V_{03}) \times 2/3 + V_{03}$ | | |
| $V_{(13)}$ | | Voltage at R13 | | | $(V_{(33)}–V_{(03)}) \times 1/3 + V_{(03)}$ | | |
| $V_{(33)} – V_{(03)}$ | | Voltage at R33/R03 | | 2.5 | | $V_{CC}$ +0.2 | |
| $I_{(R03)}$ | Input leakage | R03 = $V_{SS}$ | No load at all segment and common lines, $V_{CC}$ = 3 V | | | ±20 | nA |
| $I_{(R13)}$ | | R13 = $V_{CC}/3$ | | | | ±20 | |
| $I_{(R23)}$ | | R23 = $2 \times V_{CC}/3$ | | | | ±20 | |
| $V_{(Sxx0)}$ | Segment line voltage | $I_{(Sxx)}$ = –3 µA, | $V_{CC}$ = 3 V | $V_{(03)}$ | | $V_{(03)}$ – 0.1 | V |
| $V_{(Sxx1)}$ | | | | $V_{(13)}$ | | $V_{(13)}$ – 0.1 | |
| $V_{(Sxx2)}$ | | | | $V_{(23)}$ | | $V_{(23)}$ – 0.1 | |
| $V_{(Sxx3)}$ | | | | $V_{(33)}$ | | $V_{(33)}$ + 0.1 | |

### USART0 (see Note 1)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(\tau)}$ | USART0: deglitch time | $V_{CC}$ = 3 V, SYNC = 0, UART mode | 150 | 280 | 500 | ns |

NOTE 1: The signal applied to the USART0 receive signal/terminal (URXD0) should meet the timing requirements of $t_{(\tau)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of $t_{(\tau)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0 line.

### POR brownout, reset (see Notes 1 and 2)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{d(BOR)}$ | Brownout | | | | 2000 | µs |
| $V_{CC(start)}$ | | $dV_{CC}/dt \le 3$ V/s (see Figure 6) | | $0.7 \times V_{(B_IT–)}$ | | V |
| $V_{(B_IT–)}$ | | $dV_{CC}/dt \le 3$ V/s (see Figure 6, Figure 7, Figure 8) | | | 1.71 | V |
| $V_{hys(B_IT–)}$ | | $dV_{CC}/dt \le 3$ V/s (see Figure 6) | 70 | 130 | 180 | mV |
| $t_{(reset)}$ | | Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally, $V_{CC}$ = 3 V | 2 | | | µs |

NOTES: 1. The current consumption of the brownout module is already included in the $I_{CC}$ current consumption data. The voltage level $V_{(B_IT–)} + V_{hys(B_IT–)}$ is ≤ 1.8 V.

2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B_IT–)} + V_{hys(B_IT–)}$. The default FLL+ settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* (SLAU056) for more information on the brownout/SVS circuit.

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

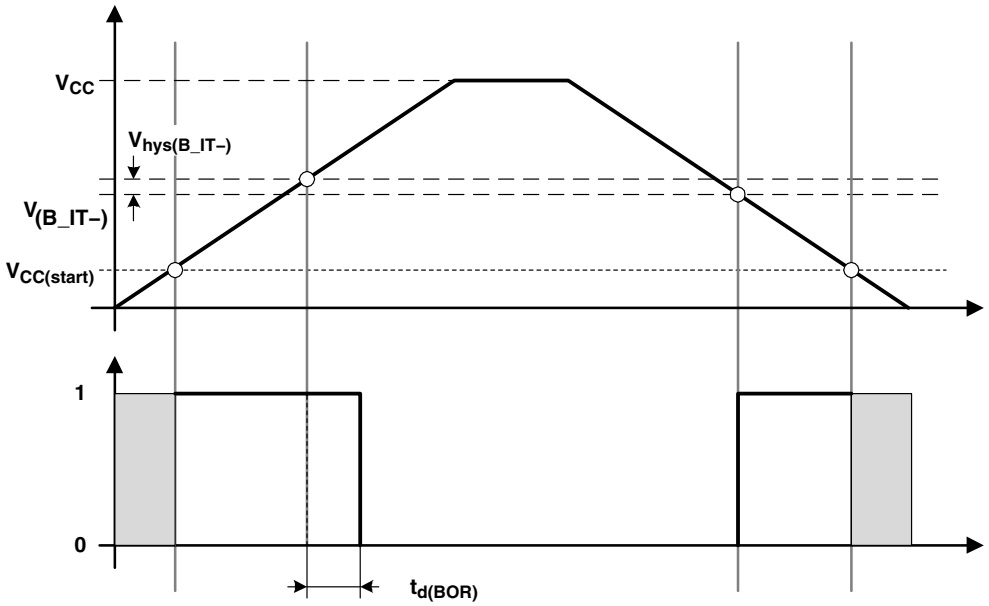



**Figure 6. POR/Brownout Reset (BOR) vs Supply Voltage**

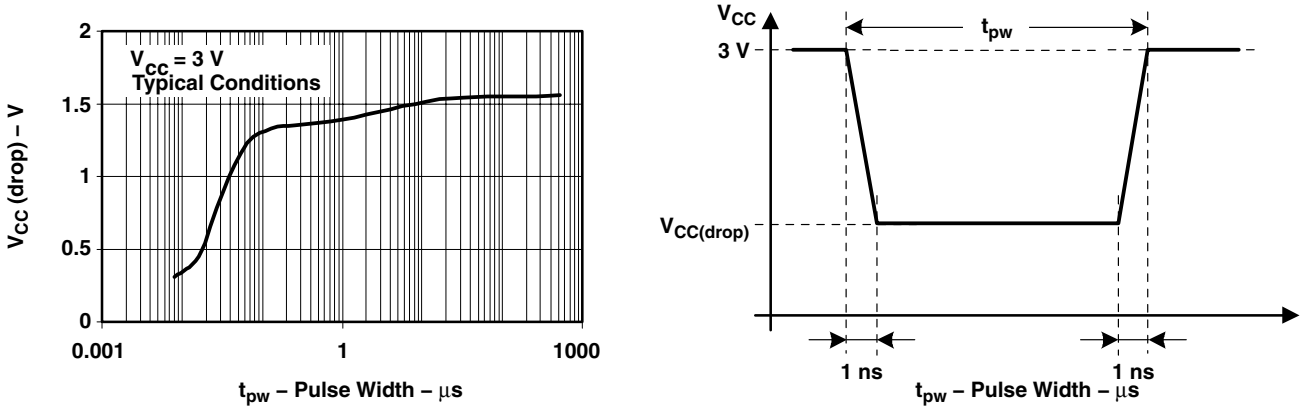



**Figure 7. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal**

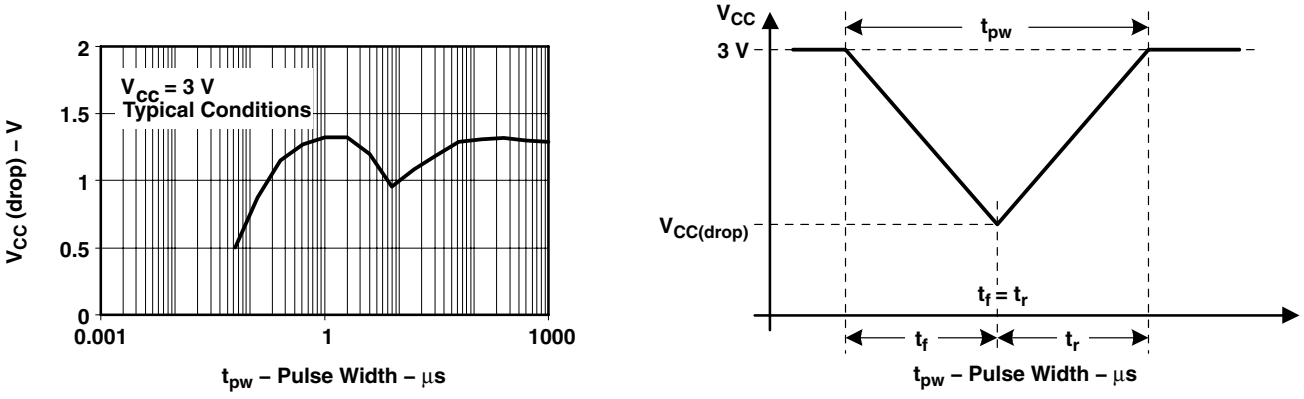



**Figure 8. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal**

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### SVS (supply voltage supervisor/monitor) (see Note 1)

| PARAMETER | TEST CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(SVSR)4}$ | $dV_{CC}/dt > 30$ V/ms (see Figure 9) | | 5 | | 150 | µs |
| | $dV_{CC}/dt \le 30$ V/ms | | | | 2000 | |
| $t_{d(SVSon)}$ | SVSon, switch from VLD=0 to VLD ≠ 0, $V_{CC}$ = 3 V | | 20 | | 150 | µs |
| $t_{settle}$ | VLD ≠ 0‡ | | | | 12 | µs |
| $V_{(SVSstart)}$ | VLD ≠ 0, $V_{CC}/dt \le 3$ V/s (see Figure 9) | | | 1.55 | 1.7 | V |
| $V_{hys(SVS_IT-)}$ | $V_{CC}/dt \le 3$ V/s (see Figure 9) | VLD = 1 | 70 | 120 | 155 | mV |
| | | VLD = 2 .. 14 | $V_{(SVS_IT-)}$ x 0.004 | | $V_{(SVS_IT-)}$ x 0.008 | |
| | $V_{CC}/dt \le 3$ V/s (see Figure 9), external voltage applied on P2.3 | VLD = 15 | 4.4 | | 10.4 | mV |
| $V_{(SVS_IT-)}$ | $V_{CC}/dt \le 3$ V/s (see Figure 9) | VLD = 1 | 1.8 | 1.9 | 2.05 | V |
| | | VLD = 2 | 1.94 | 2.1 | 2.25 | |
| | | VLD = 3 | 2.05 | 2.2 | 2.37 | |
| | | VLD = 4 | 2.14 | 2.3 | 2.48 | |
| | | VLD = 5 | 2.24 | 2.4 | 2.6 | |
| | | VLD = 6 | 2.33 | 2.5 | 2.71 | |
| | | VLD = 7 | 2.46 | 2.65 | 2.86 | |
| | | VLD = 8 | 2.58 | 2.8 | 3 | |
| | | VLD = 9 | 2.69 | 2.9 | 3.13 | |
| | | VLD = 10 | 2.83 | 3.05 | 3.29 | |
| | | VLD = 11 | 2.94 | 3.2 | 3.42 | |
| | | VLD = 12 | 3.11 | 3.35 | 3.61† | |
| | | VLD = 13 | 3.24 | 3.5 | 3.76† | |
| | | VLD = 14 | 3.43 | 3.7† | 3.99† | |
| | $V_{CC}/dt \le 3$ V/s (see Figure 9), external voltage applied on P2.3 | VLD = 15 | 1.1 | 1.2 | 1.3 | |
| $I_{CC(SVS)}$ (see Note 1) | VLD ≠ 0, $V_{CC}$ = 2.2 V/3 V | | | 10 | 15 | µA |

† The recommended operating voltage range is limited to 3.6 V.

‡ $t_{settle}$ is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.

NOTE 1: The current consumption of the SVS module is not included in the $I_{CC}$ current consumption data.

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

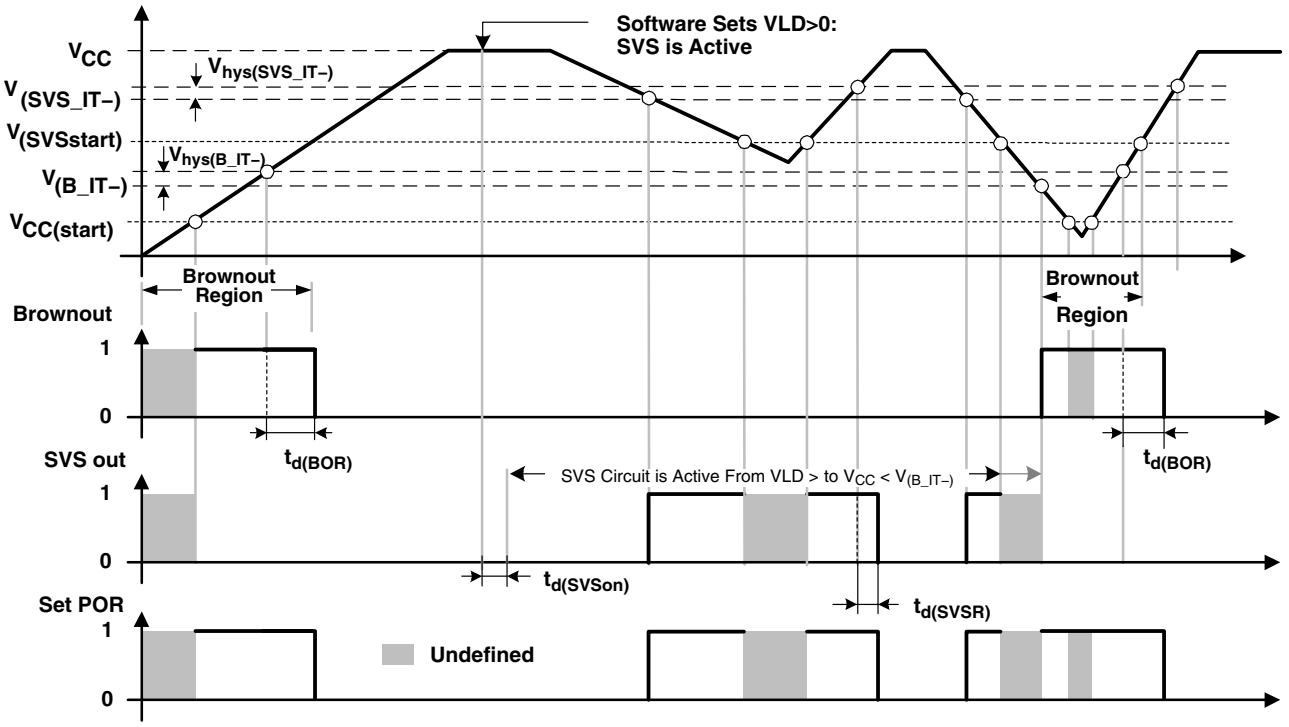



**Figure 9. SVS Reset (SVSR) vs Supply Voltage**

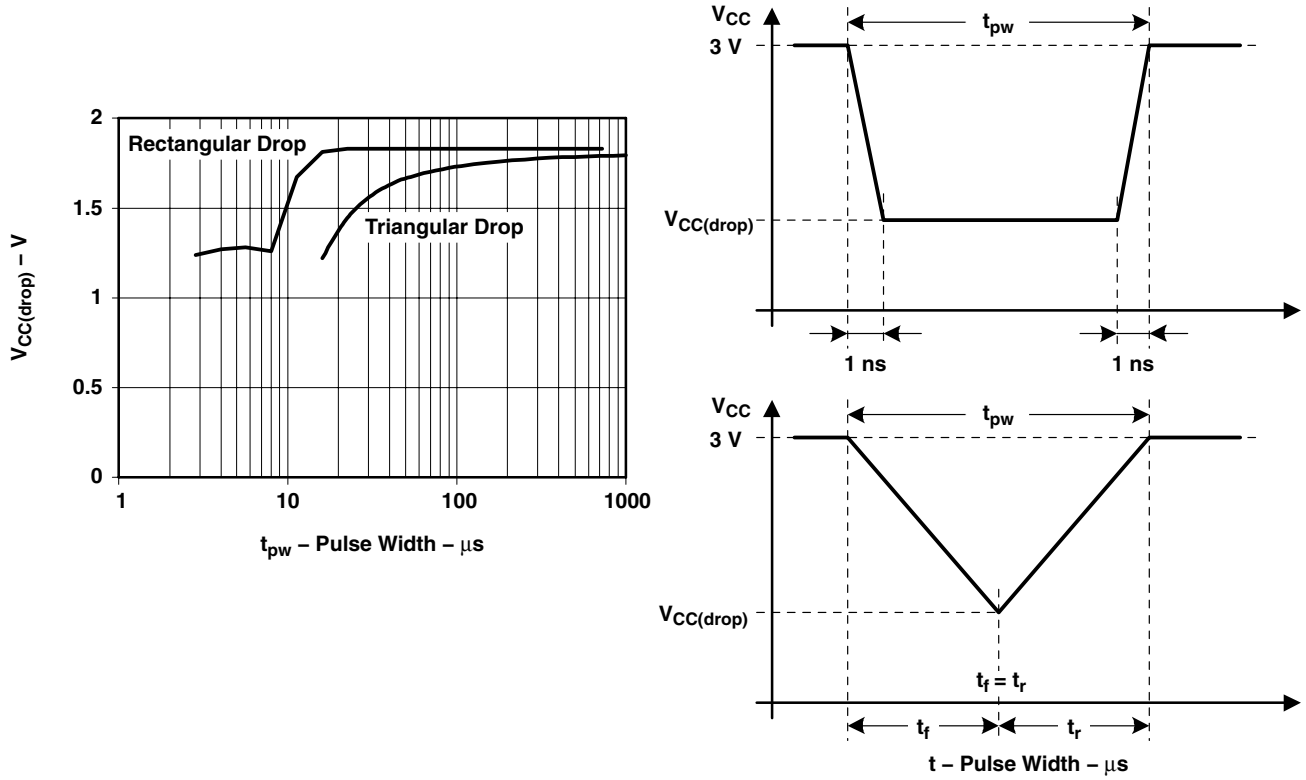



**Figure 10. $V_{CC(drop)}$ With a Square Voltage Drop and a Triangle Voltage Drop to Generate an SVS Signal**

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

**DCO**

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{(DCOCLK)}$ | $N_{(DCO)}$=01Eh, FN_8=FN_4=FN_3=FN_2=0, D = 2; DCOPLUS= 0, $f_{Crystal}$ = 32.768 kHz | 3 V | | 1 | | MHz |
| $f_{(DCO=2)}$ | FN_8=FN_4=FN_3=FN_2=0 ; DCOPLUS = 1 | 3 V | 0.3 | 0.7 | 1.3 | MHz |
| $f_{(DCO=27)}$ | FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1 | 3 V | 2.7 | 6.1 | 11.3 | MHz |
| $f_{(DCO=2)}$ | FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1 | 3 V | 0.8 | 1.5 | 2.5 | MHz |
| $f_{(DCO=27)}$ | FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1 | 3 V | 6.5 | 12.1 | 20 | MHz |
| $f_{(DCO=2)}$ | FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1 | 3 V | 1.3 | 2.2 | 3.5 | MHz |
| $f_{(DCO=27)}$ | FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1 | 3 V | 10.3 | 17.9 | 28.5 | MHz |
| $f_{(DCO=2)}$ | FN_8=0, FN_4= 1, FN_3= FN_2=x; DCOPLUS = 1 | 3 V | 2.1 | 3.4 | 5.2 | MHz |
| $f_{(DCO=27)}$ | FN_8=0, FN_4=1, FN_3= FN_2=x; DCOPLUS = 1 | 3 V | 16 | 26.6 | 41 | MHz |
| $f_{(DCO=2)}$ | FN_8=1, FN_4=FN_3=FN_2=x; DCOPLUS = 1 | 3 V | 4.2 | 6.3 | 9.2 | MHz |
| $f_{(DCO=27)}$ | FN_8=1,FN_4=FN_3=FN_2=x; DCOPLUS = 1 | 3 V | 30 | 46 | 70 | MHz |
| $S_n$ | Step size between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$, (see Figure 12 for taps 21 to 27) | 1 < TAP ≤ 20 | 1.06 | | 1.11 | |
| | | TAP = 27 | 1.07 | | 1.17 | |
| $D_t$ | Temperature drift, $N_{(DCO)}$ = 01Eh, FN_8=FN_4=FN_3=FN_2=0 D = 2; DCOPLUS = 0 | 3 V | –0.2 | –0.3 | –0.4 | %/°C |
| $D_V$ | Drift with $V_{CC}$ variation, $N_{(DCO)}$ = 01Eh, FN_8=FN_4=FN_3=FN_2=0 D = 2; DCOPLUS = 0 | | 0 | 5 | 15 | %/V |

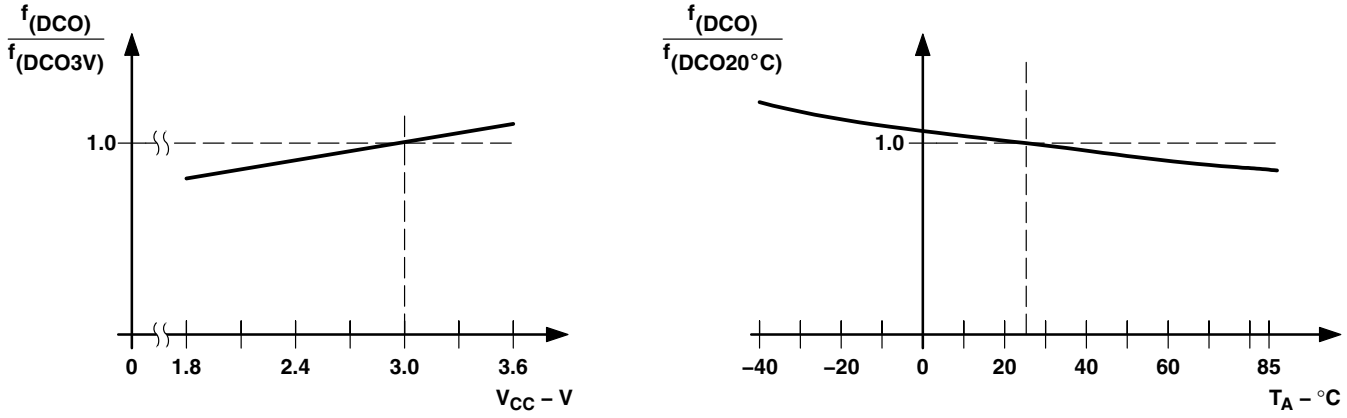



**Figure 11. DCO Frequency vs Supply Voltage $V_{CC}$ and vs Ambient Temperature**

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

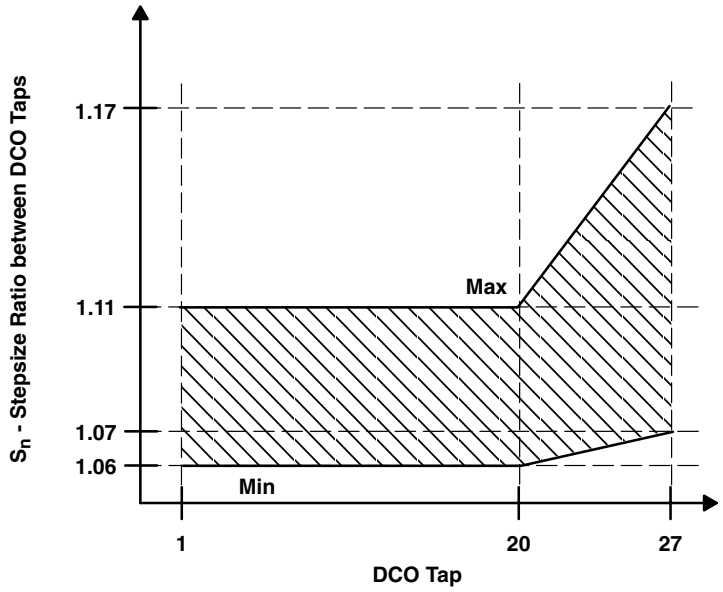



**Figure 12. DCO Tap Step Size**

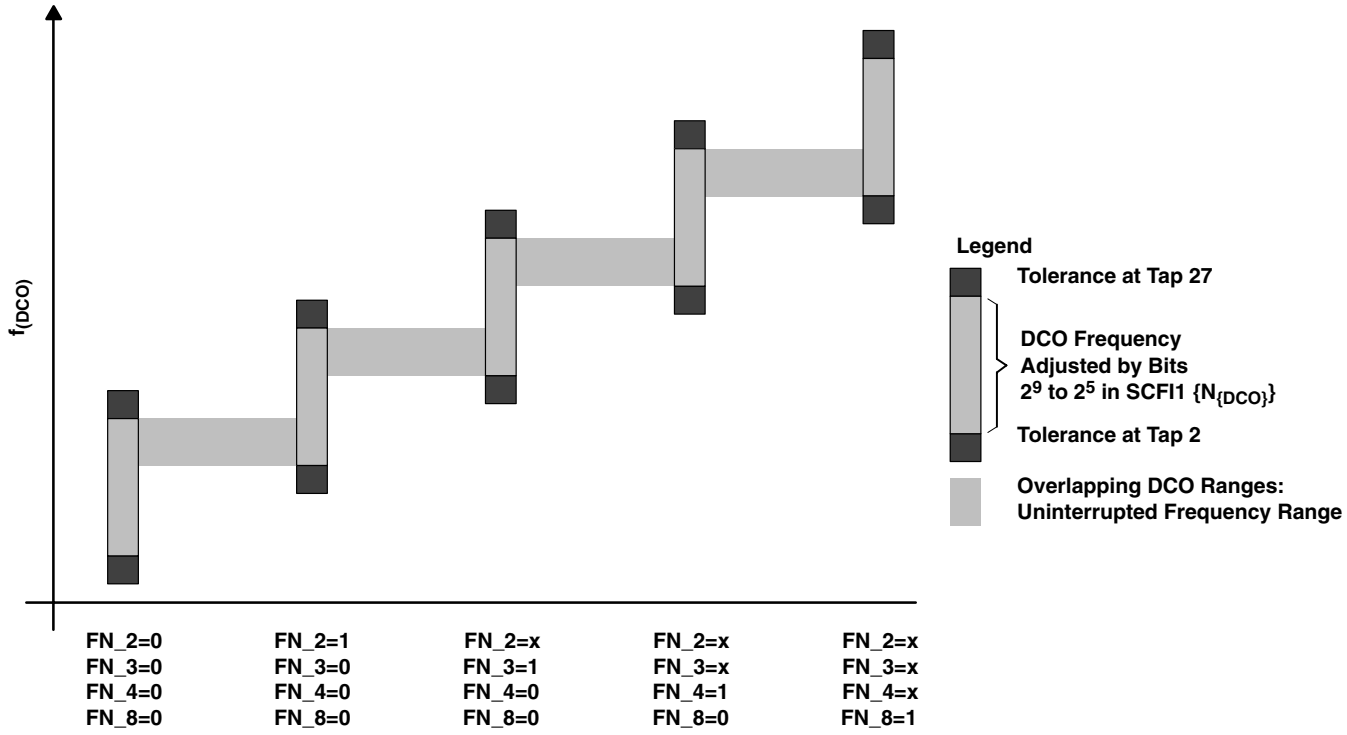



**Figure 13. Five Overlapping DCO Ranges Controlled by FN_x Bits**

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{XIN}$ | Integrated input capacitance (see Note 4) | OSCCAPx = 0h | 3 V | | 0 | | pF |
| | | OSCCAPx = 1h | 3 V | | 10 | | |
| | | OSCCAPx = 2h | 3 V | | 14 | | |
| | | OSCCAPx = 3h | 3 V | | 18 | | |
| $C_{XOUT}$ | Integrated output capacitance (see Note 4) | OSCCAPx = 0h | 3 V | | 0 | | pF |
| | | OSCCAPx = 1h | 3 V | | 10 | | |
| | | OSCCAPx = 2h | 3 V | | 14 | | |
| | | OSCCAPx = 3h | 3 V | | 18 | | |
| $V_{IL}$ | Input levels at XIN | see Note 3 | 2.2 V/3 V | $V_{SS}$ | | $0.2\times V_{CC}$ | V |
| $V_{IH}$ | | | | $0.8\times V_{CC}$ | | $V_{CC}$ | |

NOTES:
1. The parasitic capacitance from the package and board may be estimated to be 2pF. The effective load capacitor for the crystal is $(C_{XIN} \times C_{XOUT}) / (C_{XIN} + C_{XOUT})$. It is independent of XTS_FLL .
2. To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines must be observed:
   - Keep as short a trace as possible between the ’FE42x and the crystal.
   - Design a good ground plane around oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to XIN an XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
3. Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.
4. External capacitance is recommended for precision real-time clock applications; OSCCAPx = 0h.

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### ESP430CE1, SD16 and ESP430 power supply and recommended operating conditions

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | $AV_{CC} = DV_{CC}$<br>$AV_{SS} = DV_{SS} = 0V$ | | | 2.7 | | 3.6 | V |
| $I_{ESP430CE1}$ | Total Digital & Analog supply current when ESP430 and SD16 active ($I_{AVCC} + I_{DVCC}$) | SD16LP = 0, $f_{MCLK}$ = 4MHz, $f_{SD16} = f_{MCLK}/4$, SD16REFON = 1, SD16VMIDON = 0 | GAIN(V): 1, GAIN(I1): 1, I2: off | 3 V | | 2.0 | 2.6 | mA |
| | | | GAIN(V): 1, GAIN(I1): 32, I2: off | 3 V | | 2.4 | 3.3 | |
| | | | GAIN(V): 1, GAIN(I1): 1, GAIN(I2): 1 | 3 V | | 2.7 | 3.6 | |
| | | | GAIN(V): 1, GAIN(I1): 32, GAIN(I2): 32 | 3 V | | 3.4 | 4.9 | |
| | | SD16LP = 1, $f_{MCLK}$ = 2MHz, $f_{SD16} = f_{MCLK}/4$, SD16REFON = 1, SD16VMIDON = 0 | GAIN(V): 1, GAIN(I1): 1, I2: off | 3 V | | 1.5 | 2.1 | |
| | | | GAIN(V): 1, GAIN(I1): 32, I2: off | 3 V | | 1.6 | 2.1 | |
| | | | GAIN(V): 1, GAIN(I1): 1, GAIN(I2): 1 | 3 V | | 2.1 | 2.8 | |
| | | | GAIN(V): 1, GAIN(I1): 32, GAIN(I2): 32 | 3 V | | 2.2 | 3.0 | |
| $I_{SD16}$ | Analog supply current: 1 active SD16 channel including internal reference (ESP430 disabled) | SD16LP = 0, $f_{SD16}$ = 1 MHz, SD16OSR = 256 | GAIN: 1, 2 | 3 V | | 650 | 950 | µA |
| | | | GAIN: 4, 8, 16 | 3 V | | 730 | 1100 | |
| | | | GAIN: 32 | 3 V | | 1050 | 1550 | |
| | | SD16LP = 1, $f_{SD16}$ = 0.5 MHz, SD16OSR = 256 | GAIN: 1 | 3 V | | 620 | 930 | |
| | | | GAIN: 32 | 3 V | | 700 | 1060 | |
| $f_{MAINS}$ | Mains frequency range | | | | 33 | | 80 | Hz |
| $f_{SD16}$ | Analog front-end input clock frequency | SD16LP = 0 (Low power mode disabled) | | 3 V | | 1 | | MHz |
| | | SD16LP = 1 (Low power mode enabled) | | 3 V | | 0.5 | | |

### ESP430CE1, SD16 input range (see Note 1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{ID}$ | Differential input voltage range for specified performance (see Note 2) | SD16GAINx = 1, SD16REFON = 1 | | | ±500 | | mV |
| | | SD16GAINx = 2, SD16REFON = 1 | | | ±250 | | |
| | | SD16GAINx = 4, SD16REFON = 1 | | | ±125 | | |
| | | SD16GAINx = 8, SD16REFON = 1 | | | ±62 | | |
| | | SD16GAINx = 16, SD16REFON = 1 | | | ±31 | | |
| | | SD16GAINx = 32, SD16REFON = 1 | | | ±15 | | |
| $Z_I$ | Input impedance (one input pin to $AV_{SS}$) | $f_{SD16}$ = 1MHz, SD16GAINx = 1 | 3 V | | 200 | | kΩ |
| | | $f_{SD16}$ = 1MHz, SD16GAINx = 32 | 3 V | | 75 | | |
| $Z_{ID}$ | Differential Input impedance (IN+ to IN–) | $f_{SD16}$ = 1MHz, SD16GAINx = 1 | 3 V | 300 | 400 | | kΩ |
| | | $f_{SD16}$ = 1MHz, SD16GAINx = 32 | 3 V | 100 | 150 | | |
| $V_I$ | Absolute input voltage range | | | $AV_{SS}$- 1.0V | | $AV_{CC}$ | V |
| $V_{IC}$ | Common-mode input voltage range | | | $AV_{SS}$- 1.0V | | $AV_{CC}$ | V |

NOTES: 1. All parameters pertain to each SD16 channel.
2. The analog input range depends on the reference voltage applied to $V_{REF}$. If $V_{REF}$ is sourced externally, the full-scale range is defined by $V_{FSR+} = +(V_{REF}/2)/GAIN$ and $V_{FSR-} = -(V_{REF}/2)/GAIN$. The analog input range should not exceed 80% of $V_{FSR+}$ or $V_{FSR-}$.

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### ESP430CE1, SD16 performance ($f_{SD16}$ = 1MHz, SD16OSRx = 256, SD16REFON = 1)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| SINAD | Signal-to-noise + distortion ratio | SD16GAINx = 1,Signal Amplitude = 500mV | $f_{IN}$ = 50 Hz, 100 Hz | 3 V | 83.5 | 85 | | dB |
| | | SD16GAINx = 2,Signal Amplitude = 250mV | | 3 V | 81.5 | 84 | | |
| | | SD16GAINx = 4,Signal Amplitude = 125mV | | 3 V | 76 | 79.5 | | |
| | | SD16GAINx = 8,Signal Amplitude = 62mV | | 3 V | 73 | 76.5 | | |
| | | SD16GAINx = 16,Signal Amplitude = 31mV | | 3 V | 69 | 73 | | |
| | | SD16GAINx = 32,Signal Amplitude = 15mV | | 3 V | 62 | 69 | | |
| G | Nominal gain | SD16GAINx = 1 | | 3 V | 0.97 | 1.00 | 1.02 | |
| | | SD16GAINx = 2 | | 3 V | 1.90 | 1.96 | 2.02 | |
| | | SD16GAINx = 4 | | 3 V | 3.76 | 3.86 | 3.96 | |
| | | SD16GAINx = 8 | | 3 V | 7.36 | 7.62 | 7.84 | |
| | | SD16GAINx = 16 | | 3 V | 14.56 | 15.04 | 15.52 | |
| | | SD16GAINx = 32 | | 3 V | 27.20 | 28.35 | 29.76 | |
| $E_{OS}$ | Offset error | SD16GAINx = 1 | | 3 V | | | ±0.2 | %FSR |
| | | SD16GAINx = 32 | | 3 V | | | ±1.5 | |
| $dE_{OS}/dT$ | Offset error temperature coefficient | SD16GAINx = 1 | | 3 V | | ±4 | ±20 | ppm FSR/°C |
| | | SD16GAINx = 32 | | 3 V | | ±20 | ±100 | |
| CMRR | Common-mode rejection ratio | SD16GAINx = 1, Common-mode input signal: $V_{ID}$ = 500 mV, $f_{IN}$ = 50 Hz, 100 Hz | | 3 V | | >90 | | dB |
| | | SD16GAINx = 32, Common-mode input signal: $V_{ID}$ = 16 mV, $f_{IN}$ = 50 Hz, 100 Hz | | 3 V | | >75 | | |
| AC PSRR | AC power supply rejection ratio | SD16GAINx = 1, $V_{CC}$ = 3 V ± 100 mV, $f_{VCC}$ = 50 Hz | | 3 V | | >80 | | dB |
| $X_T$ | Crosstalk | | | 3 V | | <–100 | | dB |

### ESP430CE1, SD16 temperature sensor

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $TC_{Sensor}$ | Sensor temperature coefficient | | | 1.18 | 1.32 | 1.46 | mV/K |
| $V_{Offset,sensor}$ | Sensor offset voltage | | | –100 | | 100 | mV |
| $V_{Sensor}$ | Sensor output voltage (see Note 2) | Temperature sensor voltage at $T_A$ = 85°C | 3 V | 435 | 475 | 515 | mV |
| | | Temperature sensor voltage at $T_A$ = 25°C | 3 V | 355 | 395 | 435 | |
| | | Temperature sensor voltage at $T_A$ = 0°C | 3 V | 320 | 360 | 400 | |

NOTES: 1. The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ ( 273 + T [°C] ) + $V_{Offset,sensor}$ [mV]
2. Results based on characterization and/or production test, no $TC_{Sensor}$ or $V_{Offset,sensor}$.

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### ESP430CE1, SD16 built-in voltage reference

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF}$ | Internal reference voltage | SD16REFON = 1, SD16VMIDON = 0 | 3 V | 1.14 | 1.20 | 1.26 | V |
| $I_{REF}$ | Reference supply current | SD16REFON = 1, SD16VMIDON = 0 | 3 V | | 175 | 260 | μA |
| TC | Temperature coefficient | SD16REFON = 1, SD16VMIDON = 0 (see Note 1) | 3 V | | 20 | 50 | ppm/K |
| $C_{REF}$ | $V_{REF}$ load capacitance | SD16REFON = 1, SD16VMIDON = 0 (see Note 2) | | | 100 | | nF |
| $I_{LOAD}$ | $V_{REF(I)}$ maximum load current | SD16REFON = 0, SD16VMIDON = 0 | 3 V | | | ±200 | nA |
| $t_{ON}$ | Turn-on time | SD16REFON = 0 → 1, SD16VMIDON = 0, $C_{REF}$ = 100 nF | 3 V | | 5 | | ms |
| DC PSR | DC power supply rejection, $\Delta V_{REF}/\Delta V_{CC}$ | SD16REFON = 1, SD16VMIDON = 0, $V_{CC}$ = 2.5 V to 3.6 V | | | 200 | | μV/V |

NOTES: 1. Calculated using the box method: (MAX(–40...85°C) – MIN(–40...85°C)) / MIN(–40...85°C) / (85 – (–40°C))
2. There is no capacitance required on $V_{REF}$. However, a capacitance of at least 100nF is recommended to reduce any reference voltage noise.

### ESP430CE1, SD16 reference output buffer

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF,BUF}$ | Reference buffer output voltage | SD16REFON = 1, SD16VMIDON = 1 | 3 V | | 1.2 | | V |
| $I_{REF,BUF}$ | Reference supply + reference output buffer quiescent current | SD16REFON = 1, SD16VMIDON = 1 | 3 V | | 385 | 600 | μA |
| $C_{REF(O)}$ | Required load capacitance on $V_{REF}$ | SD16REFON = 1, SD16VMIDON = 1 | | 470 | | | nF |
| $I_{LOAD,Max}$ | Maximum load current on $V_{REF}$ | SD16REFON = 1, SD16VMIDON = 1 | 3 V | | | ±1 | mA |
| | Maximum voltage variation vs load current | $\|I_{LOAD}\|$ = 0 to 1mA | 3 V | –15 | | +15 | mV |
| $t_{ON}$ | Turn-on time | SD16REFON = 0 → 1, SD16VMIDON = 1, $C_{REF}$ = 470 nF | 3 V | | 100 | | μs |

### ESP430CE1, SD16 external reference input

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF(I)}$ | Input voltage range | SD16REFON = 0 | 3 V | 1.0 | 1.25 | 1.5 | V |
| $I_{REF(I)}$ | Input current | SD16REFON = 0 | 3 V | | | 50 | nA |

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### ESP430CE1, active energy measurement test conditions and accuracy, $T_A$ = 25°C (See Note 1)

- $f_{ACLK}$ = 32,768 Hz (watch crystal)
- $f_{MCLK}$ = 4.194MHz (FLL+)
- $f_{SD16} = f_{MCLK}/4$ = 1.049MHz
- Single point calibration at I = 10 A, PF = 0.5 lagging
- Measurements according to IEC1036
- Input conditions (unless otherwise noted):
  $I_B$ = 6 A, $I_{MAX} = n * I_B$ = 60 A, n = 10, $V_N$ = 230 V, $f_{MAINS}$ = 50 Hz

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Maximum error | I = 0.05*$I_B$, V = $V_N$, PF = 1.0 | V1 SD16GAINx = 1<br>I1 SD16GAINx = 1<br><br>See Figure 14:<br>R1 = 0Ω, RB = 12.4Ω | 3 V | | ±0.17 | | % |
| | I = 0.1*$I_B$ to $I_{MAX}$, V = $V_N$, PF = 1.0 | | 3 V | | ±0.18 | | |
| | I = 0.1*$I_B$, V = $V_N$, PF = 0.5 lagging | | 3 V | | ±0.19 | | |
| | I = 0.2*$I_B$ to $I_{MAX}$, V = $V_N$, PF = 0.5 lagging | | 3 V | | ±0.27 | | |
| | I = 0.1*$I_B$, V = $V_N$, PF = 0.8 leading | | 3 V | | ±0.15 | | |
| | I = 0.2*$I_B$ to $I_{MAX}$, V = $V_N$, PF = 0.8 leading | | 3 V | | ±0.24 | | |
| | I = 0.2*$I_B$ to $I_{MAX}$, V = $V_N$, PF = 0.25 lagging | | 3 V | | ±0.38 | | |

- Input conditions (unless otherwise noted):
  $I_B$ = 10 A, $I_{MAX} = n * I_B$ = 60 A, n = 6, $V_N$ = 230 V, $f_{MAINS}$ = 50 Hz

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Maximum error | I = 0.05*$I_B$, V = $V_N$, PF = 1.0 | V1 SD16GAINx = 1<br>I1 SD16GAINx = 32<br><br>See Figure 15:<br>$R_{shunt}$ = 0.2mΩ | 3 V | | ±0.11 | | % |
| | I = 0.1*$I_B$ to $I_{MAX}$, V = $V_N$, PF = 1.0 | | 3 V | | ±0.18 | | |
| | I = 0.1*$I_B$, V = $V_N$, PF = 0.5 lagging | | 3 V | | ±0.45 | | |
| | I = 0.2*$I_B$ to $I_{MAX}$, V = $V_N$, PF = 0.5 lagging | | 3 V | | ±0.33 | | |
| | I = 0.1*$I_B$, V = $V_N$, PF = 0.8 leading | | 3 V | | ±0.10 | | |
| | I = 0.2*$I_B$ to $I_{MAX}$, V = $V_N$, PF = 0.8 leading | | 3 V | | ±0.18 | | |
| | I = 0.2*$I_B$ to $I_{MAX}$, V = $V_N$, PF = 0.25 lagging | | 3 V | | ±0.51 | | |

NOTES: 1. Measurements performed using complete hardware solution. Error shown contain temperature dependencies of all components including the MSP430FE42x, crystal, and discrete components.
2. I1 SD16GAIN x = 1,4: CT part number = T60404–E4624–X101 ( Vacuumschmelze)
I1 SD16GAINx = 8: shunt part number = A–H2–R005–F1–K2–0.1 (Isabellenhütte Heusler GmbH KG)
I1 SD16GAINx = 32: shunt part number = BVO–M–R0002–5.0 (Isabellenhütte Heusler GmbH KG)

**electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)**

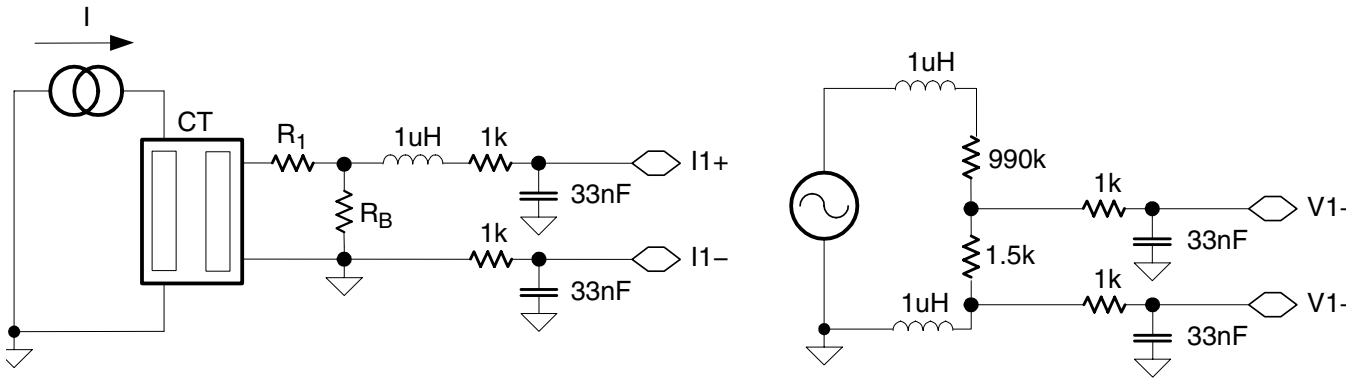



**Figure 14. Energy measurement test circuitry (SD16GAINx = 1, 4)**

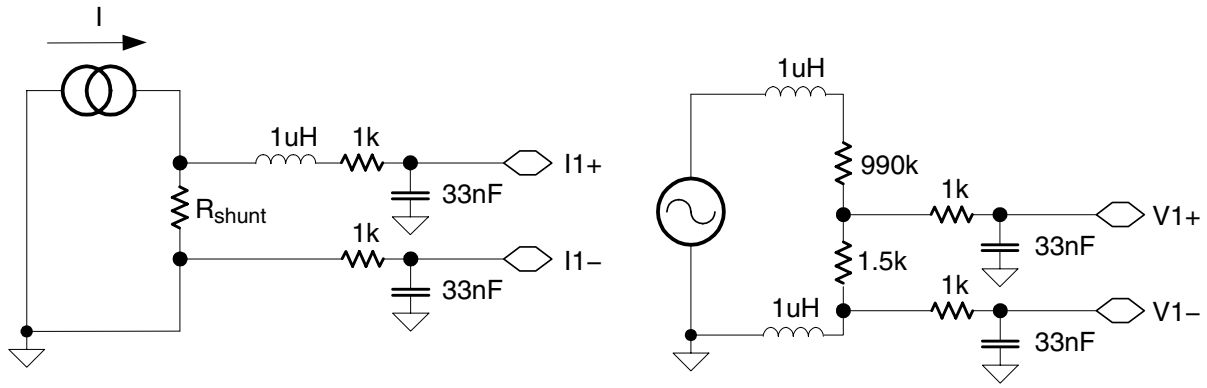



**Figure 15. Energy measurement test circuitry (SD16GAINx = 8, 32)**

**ESP430CE1, I1 SD16GAINx = 1 typical characteristics (see Note 1)**

**MEASUREMENT ERROR AS % OF READING**
**($T_A$ = 25°C)**

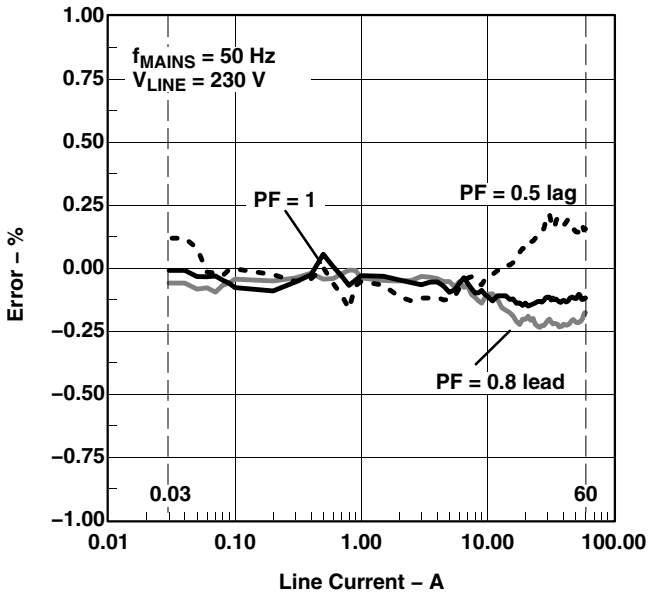



**Figure 16**

**MEASUREMENT ERROR AS % OF READING**
**($T_A$ = –40°C)**

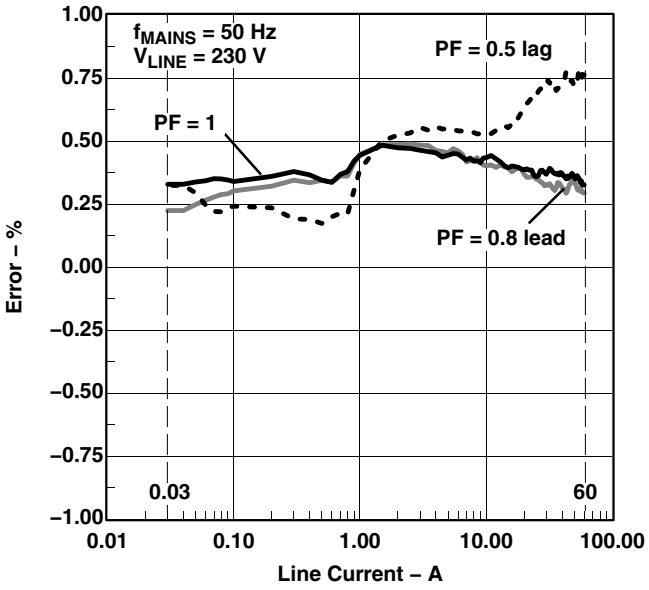



**Figure 17**

**MEASUREMENT ERROR AS % OF READING**
**($T_A$ = 85°C)**

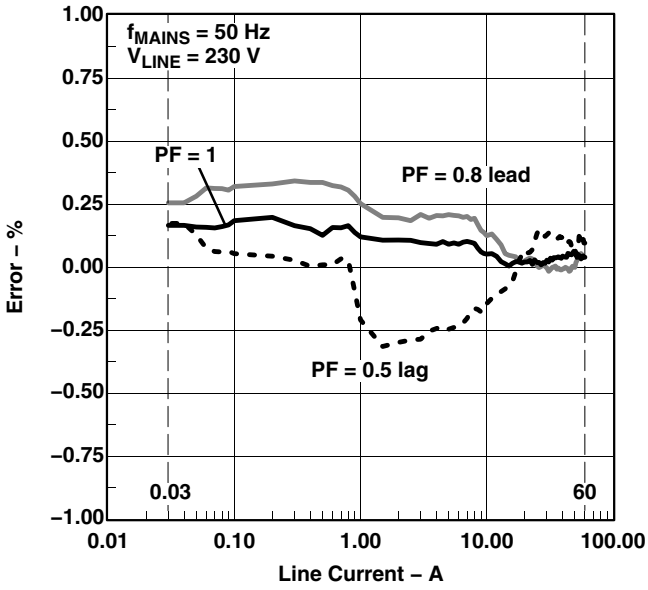



**Figure 18**

NOTES: 1. Results corrected for typical phase error of CT used. (–40°C to 25°C: –0.7°; 25°C to 85°C: +0.5°)
See Figure 14 for test circuitry: CT part number = T60404–E4624–X101 ( Vacuumschmelze), $R_1$ = 0Ω, $R_B$ = 12.4Ω

### ESP430CE1, I1 SD16GAINx = 4 typical characteristics (see Note 1)

**MEASUREMENT ERROR AS % OF READING**
**($T_A$ = 25°C)**

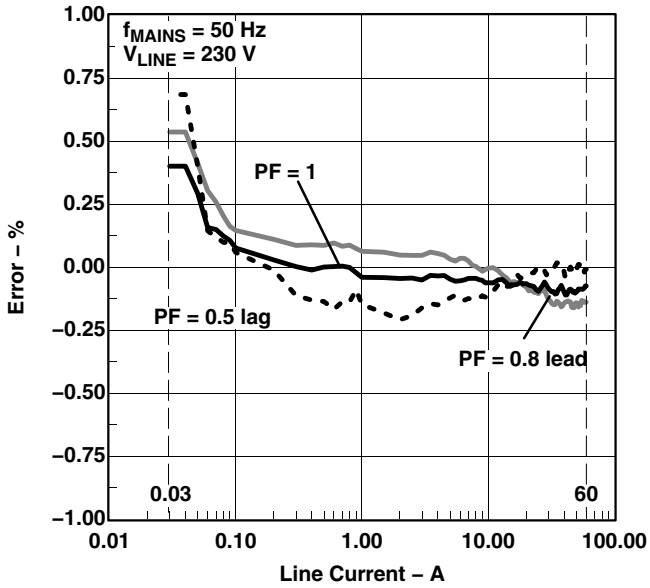



**Figure 19**

**MEASUREMENT ERROR AS % OF READING**
**($T_A$ = –40°C)**

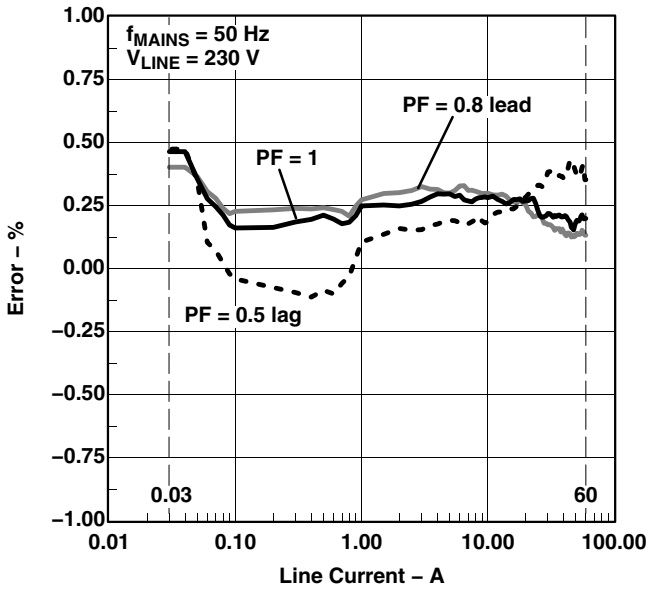



**Figure 20**

**MEASUREMENT ERROR AS % OF READING**
**($T_A$ = 85°C)**

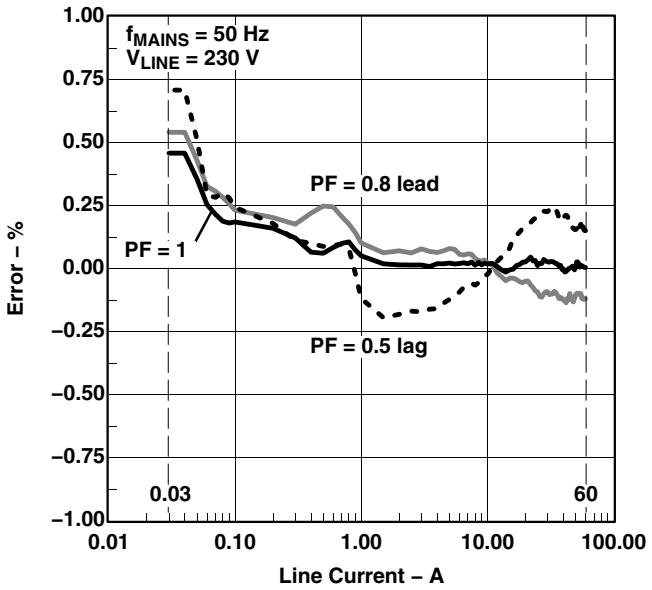



**Figure 21**

NOTES: 1. Results corrected for typical phase error of CT used. (–40°C to 25°C: –0.7°; 25°C to 85°C: +0.5°)
See Figure 14 for test circuitry: CT part number = T60404–E4624–X101 ( Vacuumschmelze), $R_1$ = 9.36Ω, $R_B$ = 3.16Ω

**ESP430CE1, I1 SD16GAINx = 8 typical characteristics (see Note 1)**

**MEASUREMENT ERROR AS % OF READING**
**($T_A$ = 25°C)**

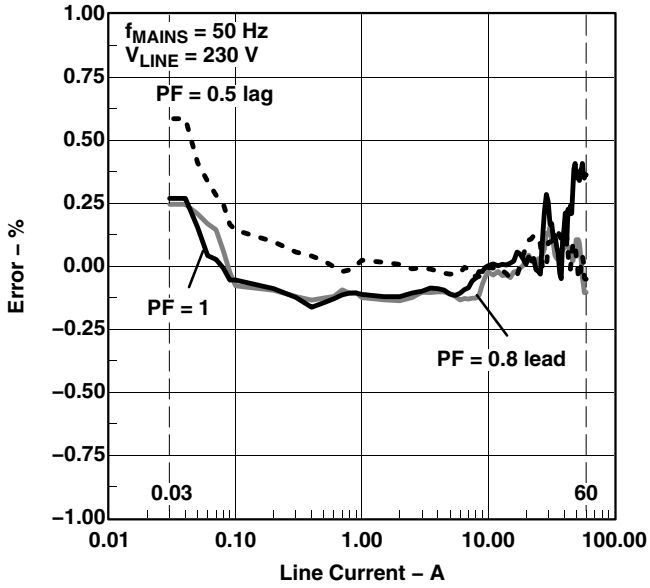



**Figure 22**

**MEASUREMENT ERROR AS % OF READING**
**($T_A$ = –40°C)**

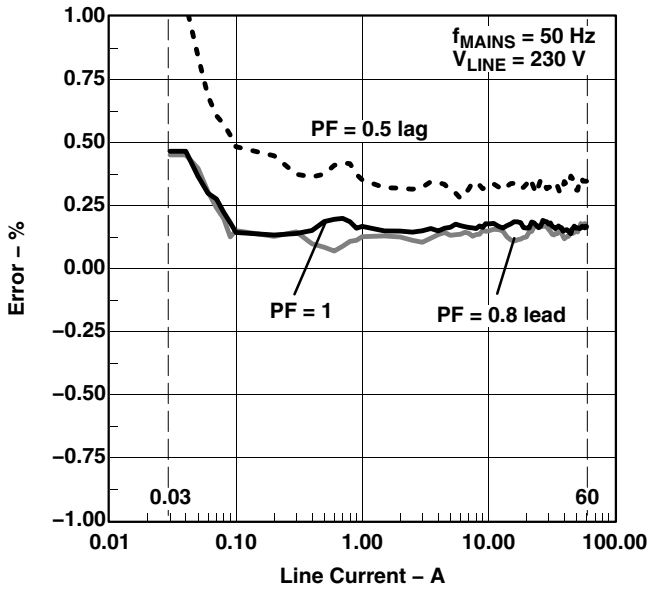



**Figure 23**

**MEASUREMENT ERROR AS % OF READING**
**($T_A$ = 85°C)**

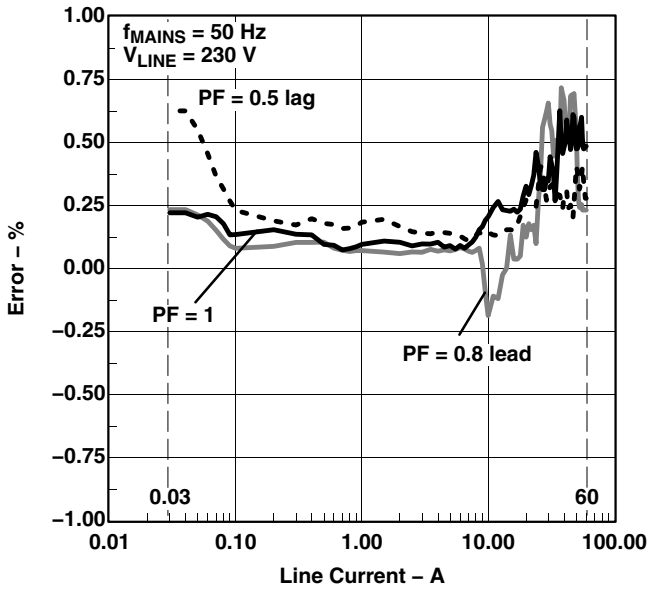



**Figure 24**

NOTES: 1. See Figure 15 for test circuitry: shunt part number = A–H2–R005–F1–K2–0.1 (Isabellenhütte Heusler GmbH KG)

**ESP430CE1, I1 SD16GAINx = 32 typical characteristics (see Note 1)**

**MEASUREMENT ERROR AS % OF READING**
**($T_A$ = 25°C)**

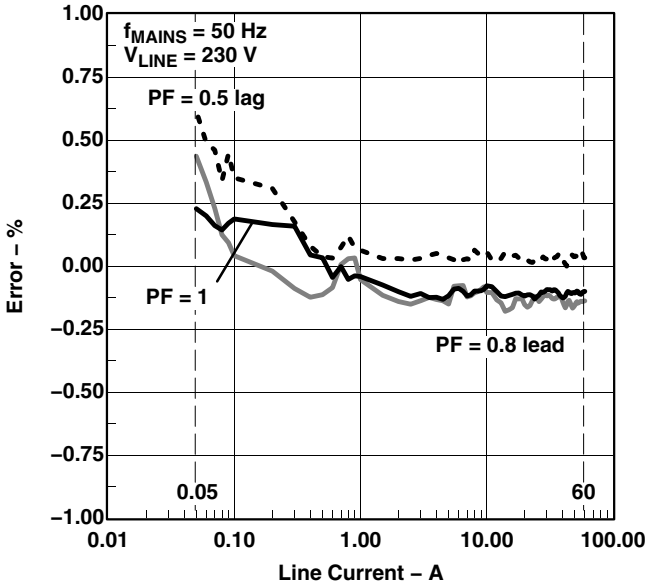



**Figure 25**

**MEASUREMENT ERROR AS % OF READING**
**($T_A$ = –40°C)**

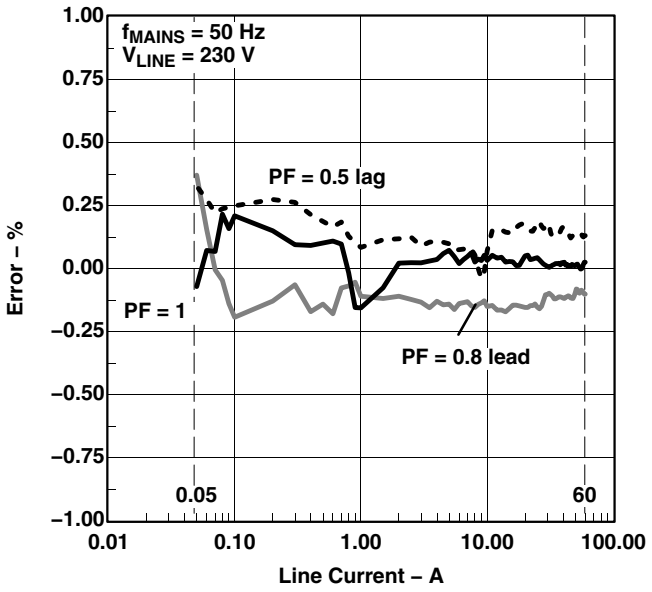



**Figure 26**

**MEASUREMENT ERROR AS % OF READING**
**($T_A$ = 85°C)**

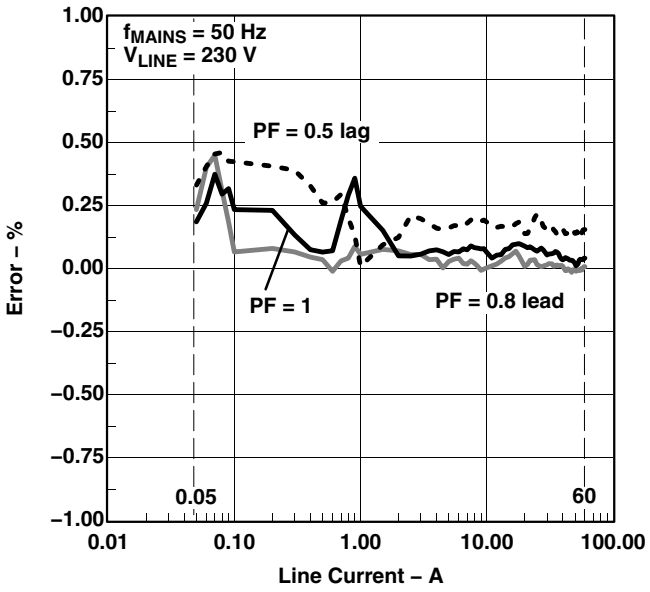



**Figure 27**

NOTES: 1. See Figure 15 for test circuitry: shunt part number = BVO–M–R0002–5.0 (Isabellenhütte Heusler GmbH KG)

## electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### Flash Memory

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC(PGM/ERASE)}$ | Program and Erase supply voltage | | | 2.7 | | 3.6 | V |
| $f_{FTG}$ | Flash Timing Generator frequency | | | 257 | | 476 | kHz |
| $I_{PGM}$ | Supply current from $DV_{CC}$ during program | | 2.7 V/ 3.6 V | | 3 | 5 | mA |
| $I_{ERASE}$ | Supply current from $DV_{CC}$ during erase | | 2.7 V/ 3.6 V | | 3 | 7 | mA |
| $t_{CPT}$ | Cumulative program time | see Note 1 | 2.7 V/ 3.6 V | | | 10 | ms |
| $t_{CMErase}$ | Cumulative mass erase time | see Note 2 | 2.7 V/ 3.6 V | 200 | | | ms |
| | Program/Erase endurance | | | $10^4$ | $10^5$ | | cycles |
| $t_{Retention}$ | Data retention duration | $T_J$ = 25°C | | 100 | | | years |
| $t_{Word}$ | Word or byte program time | see Note 3 | | | 35 | | $t_{FTG}$ |
| $t_{Block, 0}$ | Block program time for 1st byte or word | | | | 30 | | |
| $t_{Block, 1-63}$ | Block program time for each additional byte or word | | | | 21 | | |
| $t_{Block, End}$ | Block program end-sequence wait time | | | | 6 | | |
| $t_{Mass Erase}$ | Mass erase time | | | | 5297 | | |
| $t_{Seg Erase}$ | Segment erase time | | | | 4819 | | |

NOTES: 1. The cumulative programming time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms ( = 5297x1/$f_{FTG}$,max = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller's state machine ($t_{FTG}$ = 1/$f_{FTG}$).

### JTAG Interface

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{TCK}$ | TCK input frequency | see Note 1 | 2.2 V | 0 | | 5 | MHz |
| | | | 3 V | 0 | | 10 | MHz |
| $R_{Internal}$ | Internal pull-up resistance on TMS, TCK, TDI/TCLK | see Note 2 | 2.2 V/ 3 V | 25 | 60 | 90 | kΩ |

NOTES: 1. $f_{TCK}$ may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

### JTAG Fuse (see Note 1)

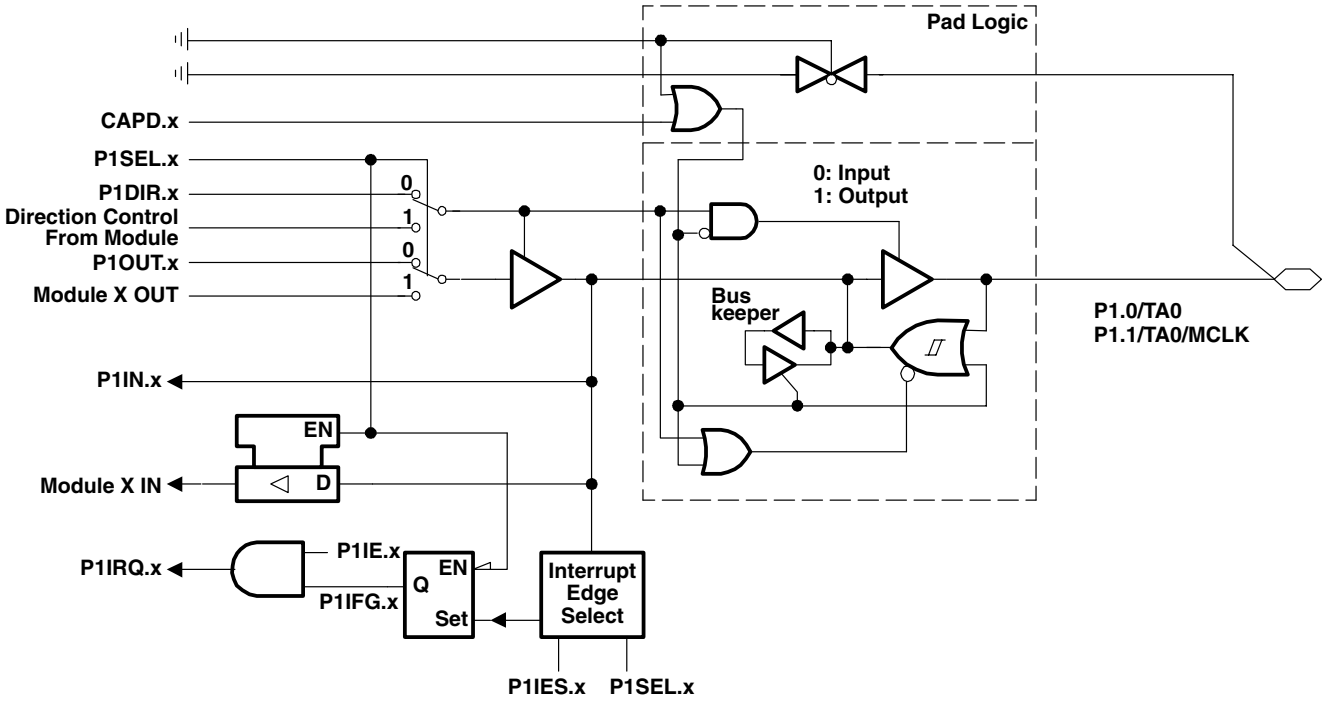
| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC(FB)}$ | Supply voltage during fuse-blow condition | $T_A$ = 25°C | | 2.5 | | | V |
| $V_{FB}$ | Voltage level on TDI/TCLK for fuse-blow | | | 6 | | 7 | V |
| $I_{FB}$ | Supply current into TDI/TCLK during fuse-blow | | | | | 100 | mA |
| $t_{FB}$ | Time to blow fuse | | | | | 1 | ms |

NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

## APPLICATION INFORMATION

### input/output schematic

#### Port P1, P1.0 to P1.1, input/output with Schmitt-trigger




NOTE: $0 \le x \le 1$.
Port Function is Active if CAPD.x = 0

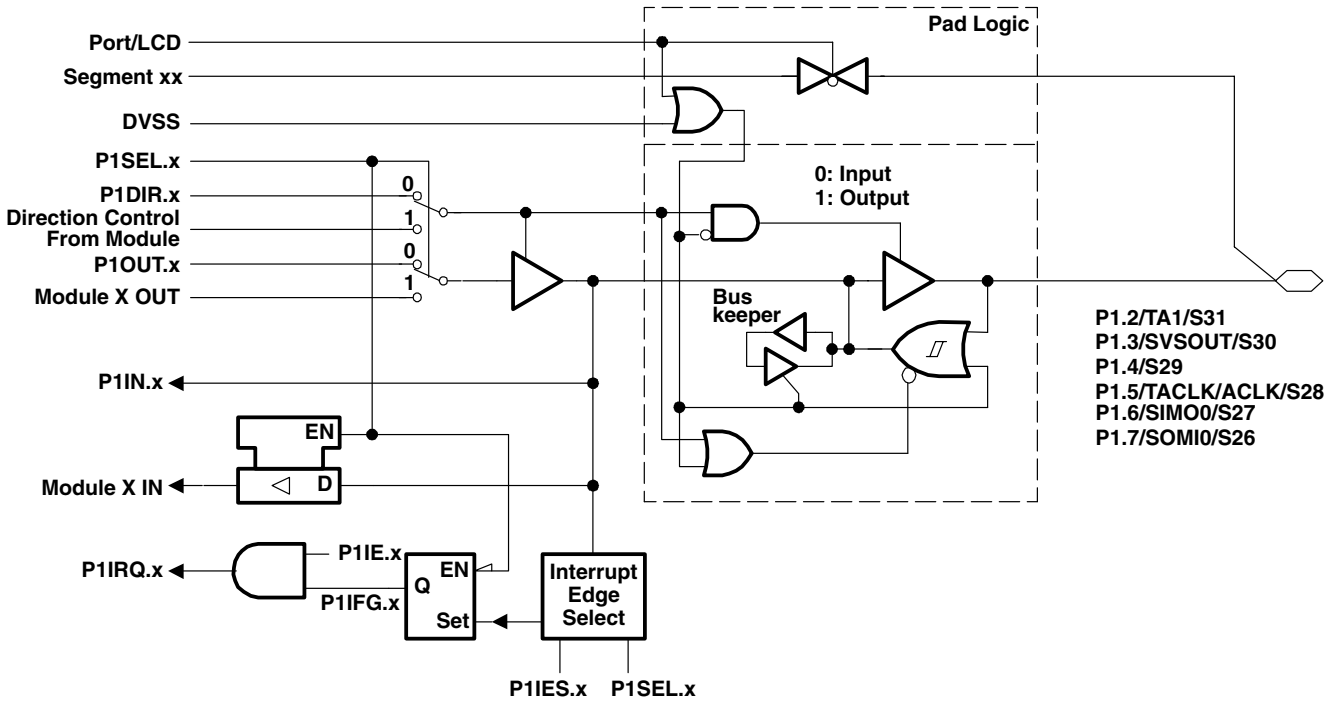
| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN | PnIE.x | PnIFG.x | PnIES.x | CAPD.x |
|---|---|---|---|---|---|---|---|---|---|---|
| P1SEL.0 | P1DIR.0 | P1DIR.0 | P1OUT.0 | Out0 Sig.† | P1IN.0 | CCI0A† | P1IE.0 | P1IFG.0 | P1IES.0 | DVSS |
| P1SEL.1 | P1DIR.1 | P1DIR.1 | P1OUT.1 | MCLK | P1IN.1 | CCI0B† | P1IE.1 | P1IFG.1 | P1IES.1 | DVSS |

† Timer_A3

## APPLICATION INFORMATION

### input/output schematic (continued)

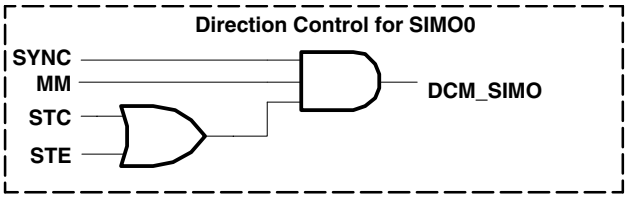
#### Port P1, P1.2 to P1.7, input/output with Schmitt-trigger

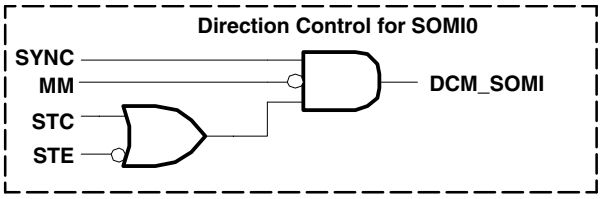



NOTE: $2 \le x \le 7$.
Port Function is Active if Port/LCD = 0

| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN | PnIE.x | PnIFG.x | PnIES.x | Port/LCD | Segment |
|---|---|---|---|---|---|---|---|---|---|---|---|
| P1SEL.2 | P1DIR.2 | P1DIR.2 | P1OUT.2 | Out1 Sig.† | P1IN.2 | CCI1A† | P1IE.2 | P1IFG.2 | P1IES.2 | 0: LCDM < 0E0h<br>1: LCDM ≥ 0E0h | S31 |
| P1SEL.3 | P1DIR.3 | P1DIR.3 | P1OUT.3 | SVSOUT | P1IN.3 | unused | P1IE.3 | P1IFG.3 | P1IES.3 | | S30 |
| P1SEL.4 | P1DIR.4 | P1DIR.4 | P1OUT.4 | DVSS | P1IN.4 | unused | P1IE.4 | P1IFG.4 | P1IES.4 | | S29 |
| P1SEL.5 | P1DIR.5 | P1DIR.5 | P1OUT.5 | ACLK | P1IN.5 | TACLK† | P1IE.5 | P1IFG.5 | P1IES.5 | | S28 |
| P1SEL.6 | P1DIR.6 | DCM_SIMO | P1OUT.6 | SIMO0(o)‡ | P1IN.6 | SIMO0(i)‡ | P1IE.6 | P1IFG.6 | P1IES.6 | 0: LCDM < 0C0h<br>1: LCDM ≥ 0C0h | S27 |
| P1SEL.7 | P1DIR.7 | DCM_SOMI | P1OUT.7 | SOMI0(o)‡ | P1IN.7 | SOMI0(i)‡ | P1IE.7 | P1IFG.7 | P1IES.7 | | S26 |

† Timer_A3
‡ USART0

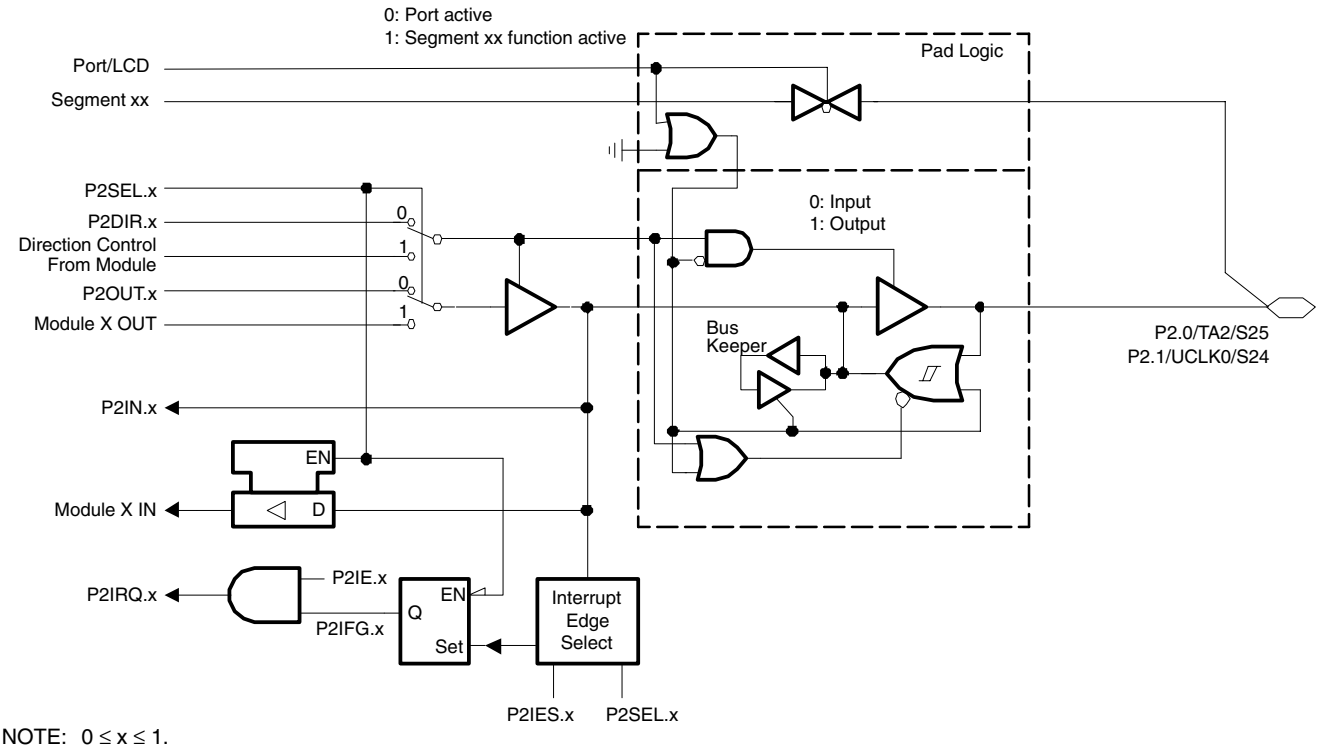


## APPLICATION INFORMATION

### input/output schematic (continued)

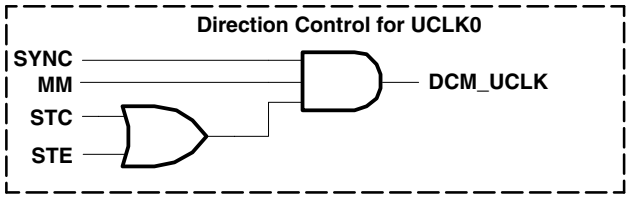
#### port P2, P2.0 to P2.1, input/output with Schmitt-trigger




NOTE: $0 \le x \le 1$.
Port Function is Active if Port/LCD = 0

| PnSel.x | PnDIR.x | Dir. Control from module | PnOUT.x | Module X OUT | PnIN.x | Module X IN | PnIE.x | PnIFG.x | PnIES.x | Port/LCD | Segment |
|---|---|---|---|---|---|---|---|---|---|---|---|
| P2Sel.0 | P2DIR.0 | P2DIR.0 | P2OUT.0 | Out2sig.† | P2IN.0 | CCI2A † | P2IE.0 | P2IFG.0 | P2IES.0 | 0: LCDM < 0E0h | S25 |
| P2Sel.1 | P2DIR.1 | DCM_UCLK | P2OUT.1 | UCLK0(o)‡ | P2IN.1 | UCLK0(i)‡ | P2IE.1 | P2IFG.1 | P2IES.1 | 1: LCDM ≥ 0E0h | S24 |

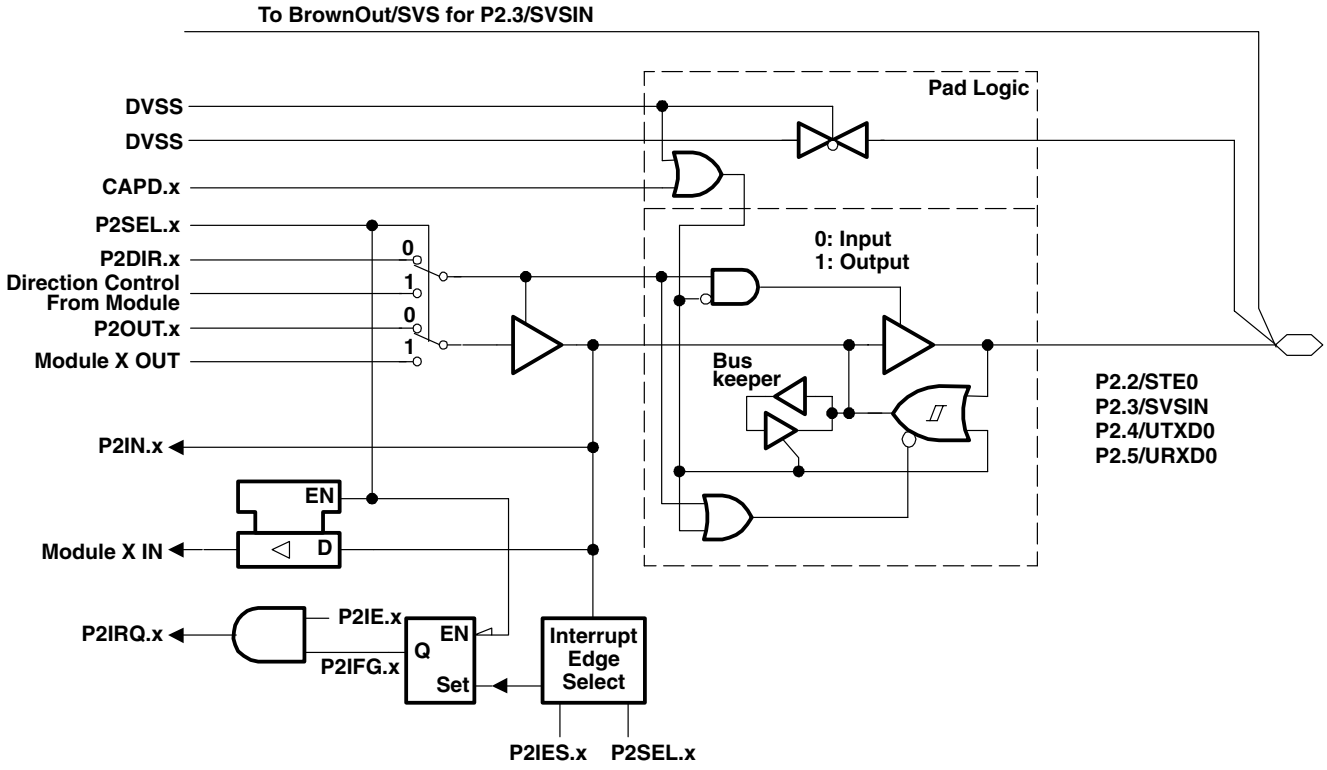
† Timer_A3
‡ USART0



## APPLICATION INFORMATION

### input/output schematic (continued)

#### port P2, P2.2 to P2.5, input/output with Schmitt-trigger




NOTE: $2 \le x \le 5$
Port function is active if CAPD.x = 0

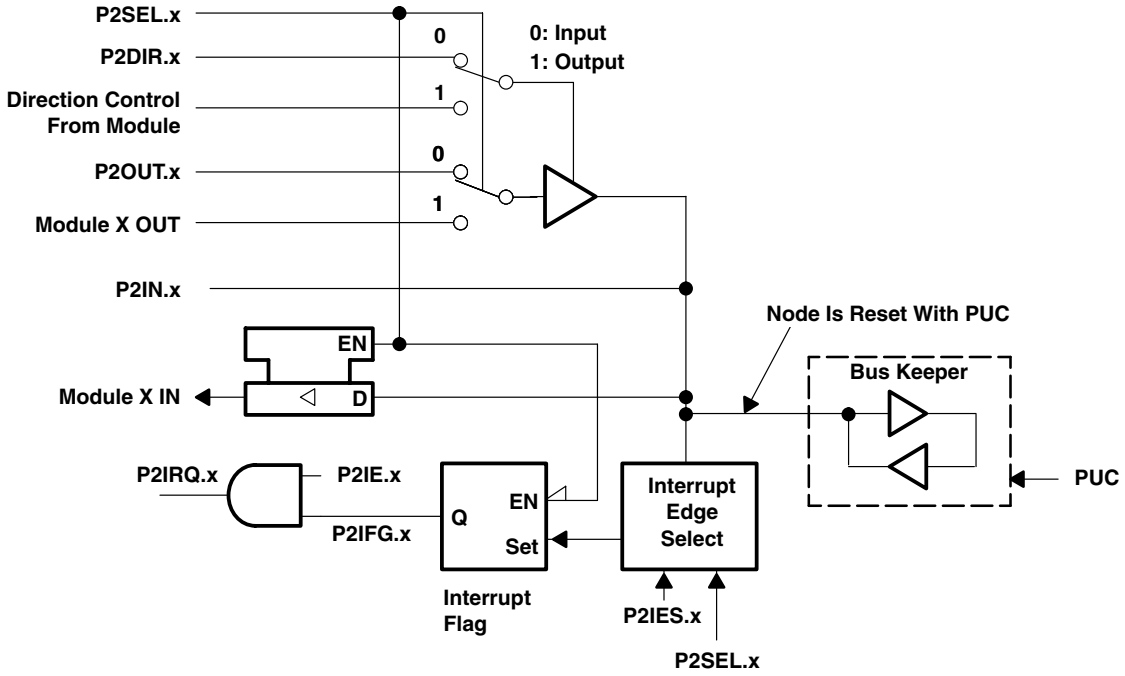
| PnSEL.x | PnDIR.x | Direction Control From Module | PnOUT.x | Module X OUT | PnIN.x | Module X IN | PnIE.x | PnIFG.x | PnIES.x | CAPD.x |
|---|---|---|---|---|---|---|---|---|---|---|
| P2SEL.2 | P2DIR.2 | DVSS | P2OUT.2 | DVSS | P2IN.2 | STE0† | P2IE.2 | P2IFG.2 | P2IES.2 | DVSS |
| P2SEL.3 | P2DIR.3 | P2DIR.3 | P2OUT.3 | DVSS | P2IN.3 | unused | P2IE.3 | P2IFG.3 | P2IES.3 | SVSCTL VLD = 1111b |
| P2SEL.4 | P2DIR.4 | DVCC | P2OUT.4 | UTXD0† | P2IN.4 | unused | P2IE.4 | P2IFG.4 | P2IES.4 | DVSS |
| P2SEL.5 | P2DIR.5 | DVSS | P2OUT.5 | DVSS | P2IN.5 | URXD0† | P2IE.5 | P2IFG.5 | P2IES.5 | DVSS |

† USART0

## APPLICATION INFORMATION

### input/output schematic (continued)

#### Port P2, unbonded GPIOs P2.6 and P2.7



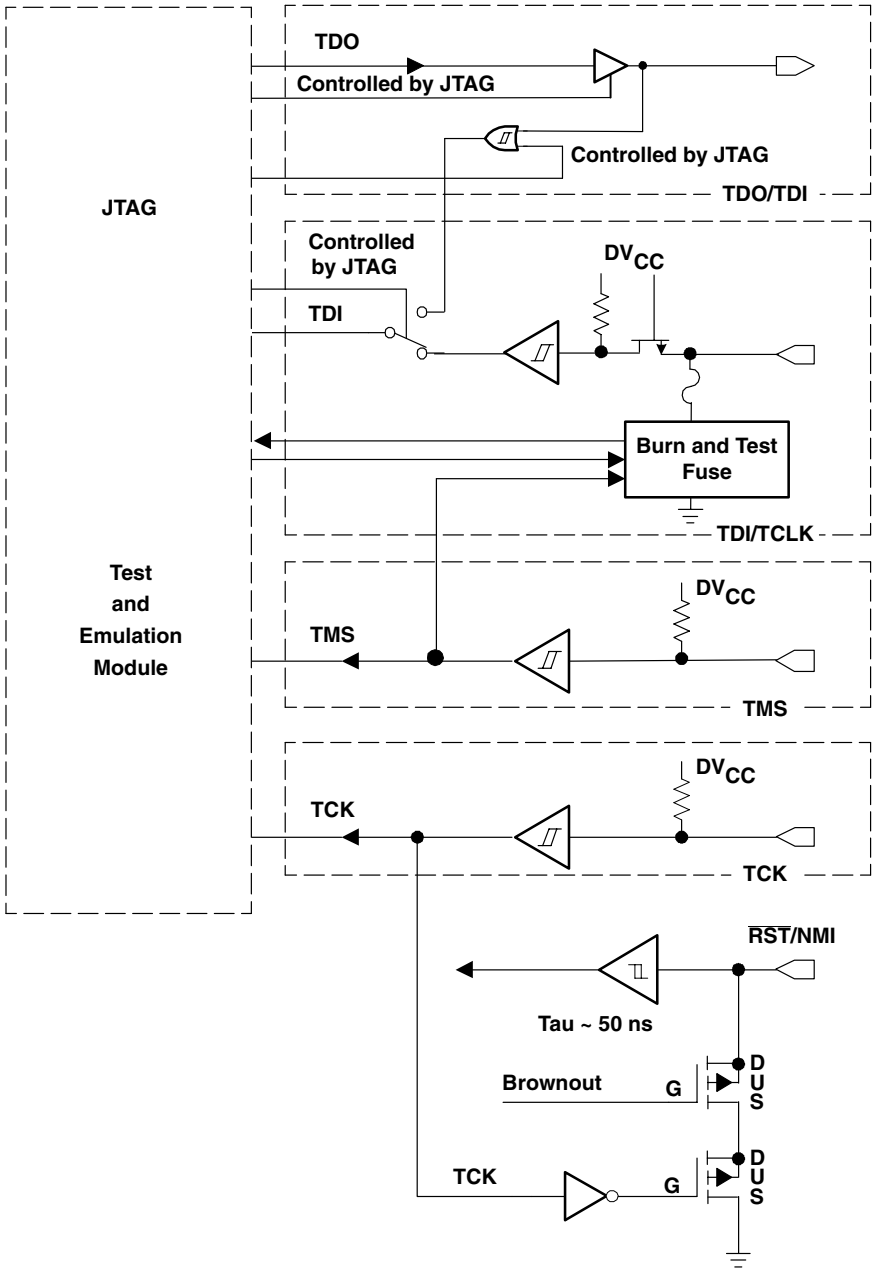

NOTE: x = Bit/identifier, 6 to 7 for port P2 without external pins

| P2Sel.x | P2DIR.x | DIRECTION CONTROL FROM MODULE | P2OUT.x | MODULE X OUT | P2IN.x | MODULE X IN | P2IE.x | P2IFG.x | P2IES.x |
|---|---|---|---|---|---|---|---|---|---|
| P2Sel.6 | P2DIR.6 | P2DIR.6 | P2OUT.6 | $DV_{SS}$ | P2IN.6 | unused | P2IE.6 | P2IFG.6 | P2IES.6 |
| P2Sel.7 | P2DIR.7 | P2DIR.7 | P2OUT.7 | $DV_{SS}$ | P2IN.7 | unused | P2IE.7 | P2IFG.7 | P2IES.7 |

NOTE: Unbonded GPIOs 6 and 7 of port P2 can be used as interrupt flags. Only software can affect the interrupt flags. They work as software interrupts.

## APPLICATION INFORMATION

### JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt-trigger or output



## APPLICATION INFORMATION

### JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, $I_{TF}$, of 1.8 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 28). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

The JTAG pins are terminated internally, and therefore do not require external termination.

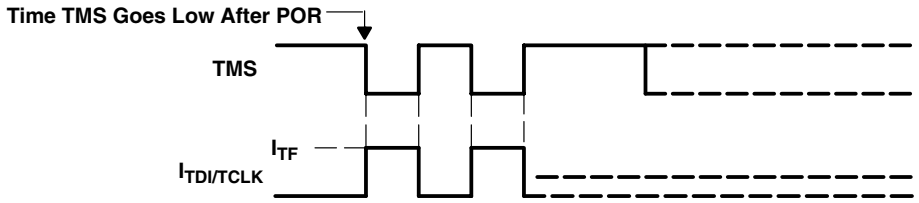



**Figure 28. Fuse Check Mode Current, MSP430FE42x**

## Data Sheet Revision History

| Literature Number | Summary |
|---|---|
| SLAS396 | Preliminary Product Preview data sheet release |
| SLAS396A | Production Data data sheet release |
| SLAS396B | Updated functional block diagram (page 3)<br>Clarified test conditions in recommended operating conditions table (page 17)<br>Changed “Supply voltage during program execution; SVS enabled, PORON = 1, ESP430 and SD16 disabled” MIN value from 2.2 V to 2.0 V (page 17)<br>Clarified test conditions for $I_{(LPM0)}$ in supply current into $AV_{CC}$ + $DV_{CC}$ table (page 18)<br>Clarified test conditions in USART0 table (page 21)<br>Changed PSRR to AC PSRR in EP430CP1, SD16 performance table (page 29)<br>Added DC PSR in EP430CP1, SD16 built-in voltage reference table (page 30)<br>Added $t_{ON}$ parameter to ESP430CE1, SD16 built-in voltage reference table (page 30)<br>Corrected PF = 0 to PF = 1 in Figure 16 through Figure 27 (page 33 through page 36)<br>Changed $t_{CPT}$ maximum value from 4 ms to 10 ms in Flash memory table (page 37) |
| SLAS396C | Modified labels on Figure 16 through Figure 27 (page 33 through page 36) |

NOTE: Page and figure numbers refer to the respective document revision and may differ in other revisions.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| MSP430FE423IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| MSP430FE423IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| MSP430FE425IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| MSP430FE425IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| MSP430FE427IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |
| MSP430FE427IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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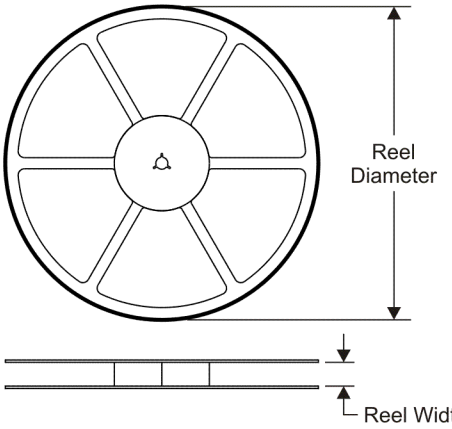
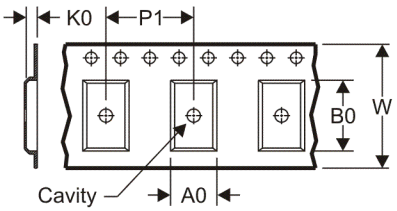
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

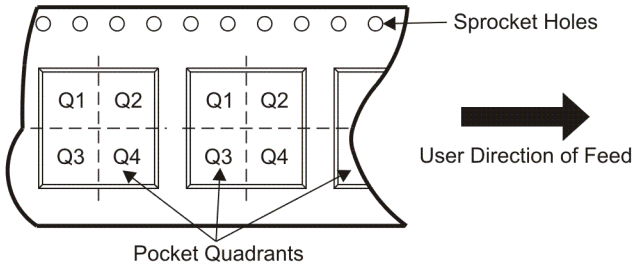



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

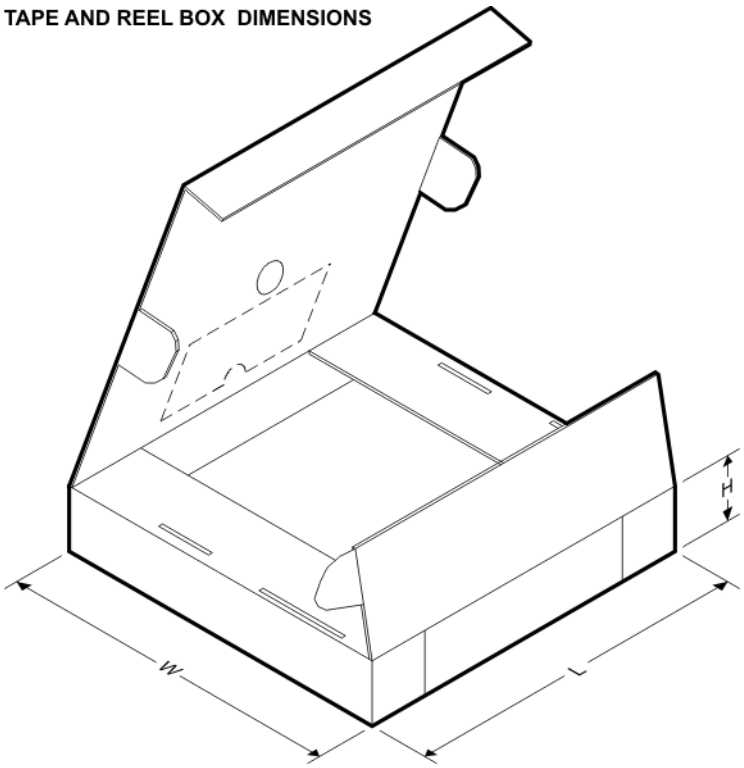
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430FE423IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 12.3 | 12.3 | 2.5 | 16.0 | 24.0 | Q2 |
| MSP430FE425IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 12.3 | 12.3 | 2.5 | 16.0 | 24.0 | Q2 |
| MSP430FE427IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 12.3 | 12.3 | 2.5 | 16.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

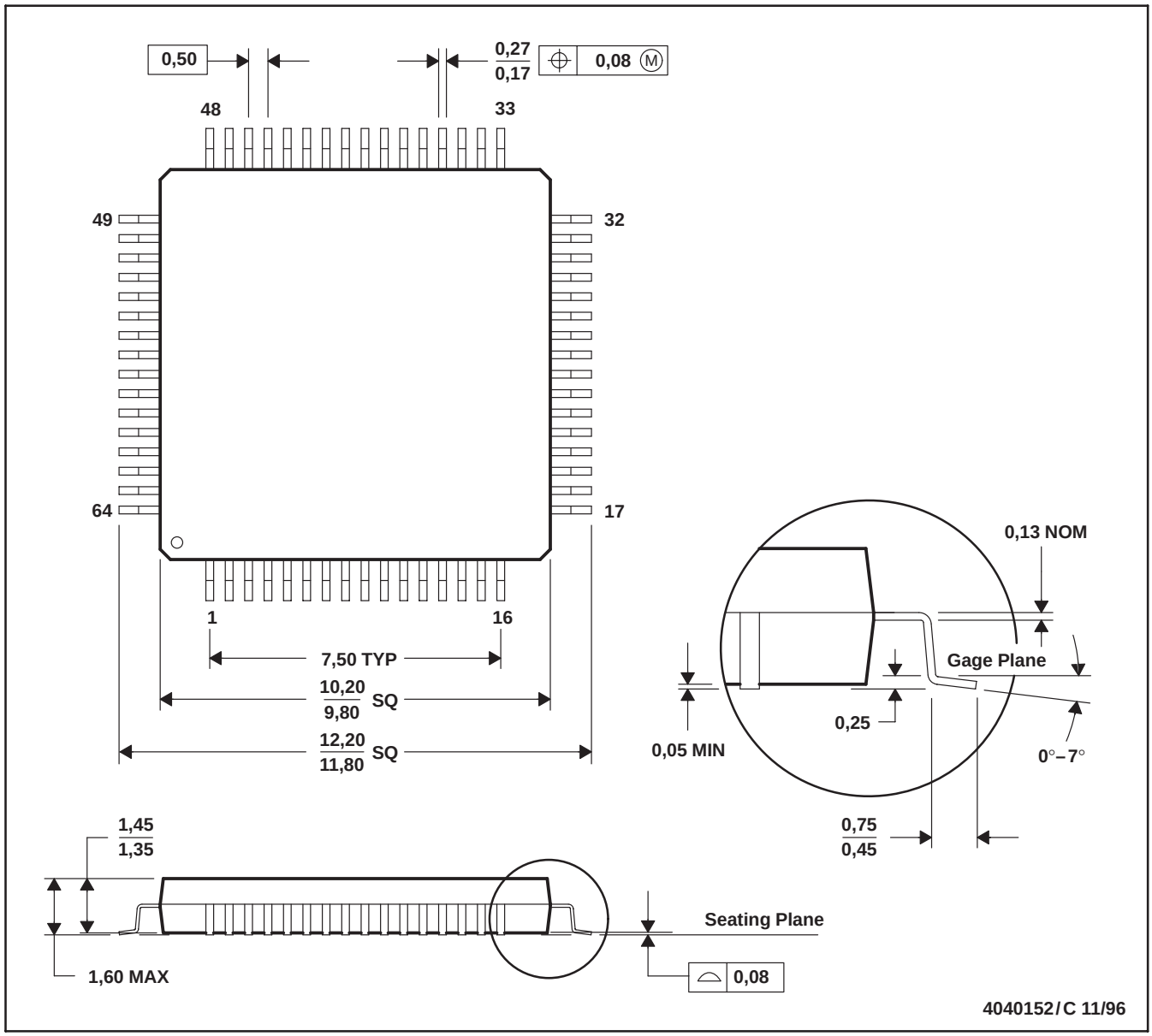



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| MSP430FE423IPMR | LQFP | PM | 64 | 1000 | 333.2 | 345.9 | 41.3 |
| MSP430FE425IPMR | LQFP | PM | 64 | 1000 | 333.2 | 345.9 | 41.3 |
| MSP430FE427IPMR | LQFP | PM | 64 | 1000 | 333.2 | 345.9 | 41.3 |

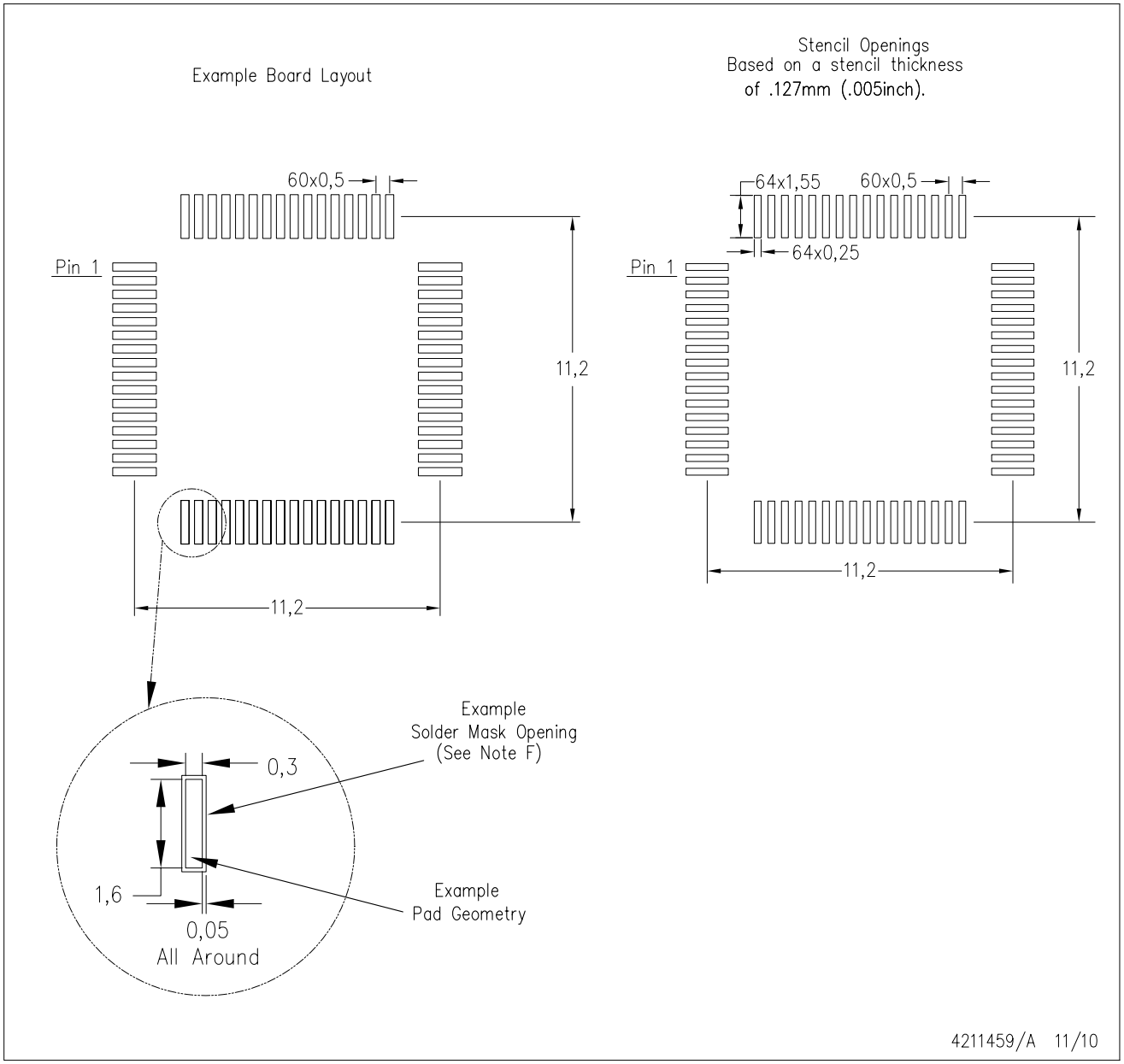
MTQF008A – JANUARY 1995 – REVISED DECEMBER 1996

**PM (S-PQFP-G64)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

PM (S–PQFP–G64) PLASTIC QUAD FLATPACK




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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