High Performance 1A LDO

ISL80101

The ISL80101 is a low voltage, high current, single output LDO specified at 1A output current. This LDO operates from input voltages of 2.2V to 6V. Fixed output voltage options are available in 1.8V, 2.5V, 3.3V and 5.0V versions. Other custom voltage options are available upon request. For the adjustable output version of the ISL80101, please refer to the ISL80101-ADJ datasheet.

A sub-micron BiCMOS process is utilized for this product family to deliver the best in class analog performance and overall value. This CMOS LDO consumes significantly lower quiescent current as a function of load compared to bipolar LDOs, which translates into higher efficiency and packages with smaller footprints. State of the art internal compensation achieves a very fast load transient response. An external capacitor on the soft-start pin provides an adjustable soft-starting ramp. The ENABLE feature allows the part to be placed into a low quiescent current shutdown mode. A Power-Good logic output signals a fault condition.

Table 1 shows the differences between the ISL80101 and others in its family:

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	PROGRAMMABLE I_{LIMIT}	I_{LIMIT} (DEFAULT)	ADJ or FIXED V_{OUT}
ISL80101-ADJ	No	1.75A	ADJ
ISL80101	No	1.75A	1.8V, 2.5V, 3.3V, 5.0V
ISL80101A	Yes	1.62A	ADJ
ISL80121-5	Yes	0.75A	5.0V

Features

- ±0.2% Initial V_{OUT} Accuracy
- ±1.8% V_{OUT} Accuracy Guaranteed Over Line, Load and T_J = -40°C to +125°C
- Very Low 130mV Dropout Voltage at V_{OUT} = 2.5V
- Very Fast Transient Response
- Programmable Soft-starting
- Power-Good Output
- Excellent 58dB PSRR at 1kHz
- Current Limit Protection
- Thermal Shutdown Function
- Available in a 10 Ld DFN Package
- Pb-Free (RoHS Compliant)

Applications

- DSP, FPGA and µP Core Power Supplies
- Noise-Sensitive Instrumentation Systems
- Post Regulation of Switched Mode Power Supplies
- Industrial Systems
- Medical Equipment
- Telecommunications and Networking Equipment
- Servers
- Hard Disk Drives (HD/HDD)

Related Literature

- See AN1592, "ISL80101 High Performance 1A LDO Evaluation Board User Guide"

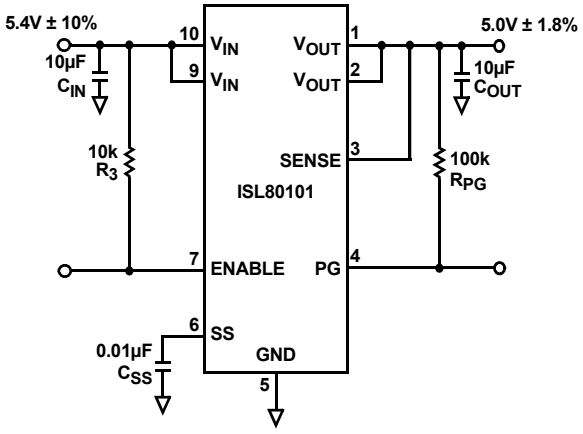


FIGURE 1. TYPICAL APPLICATION CIRCUIT

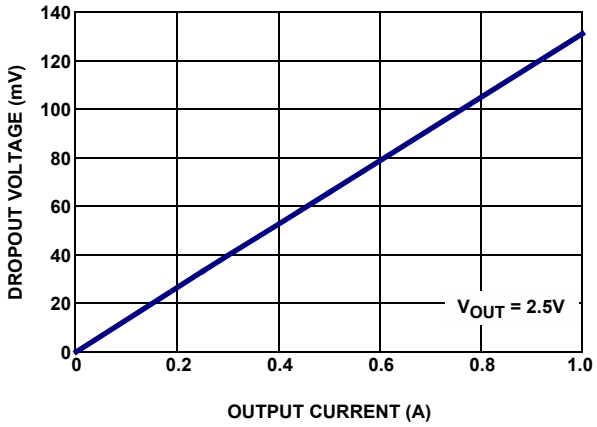
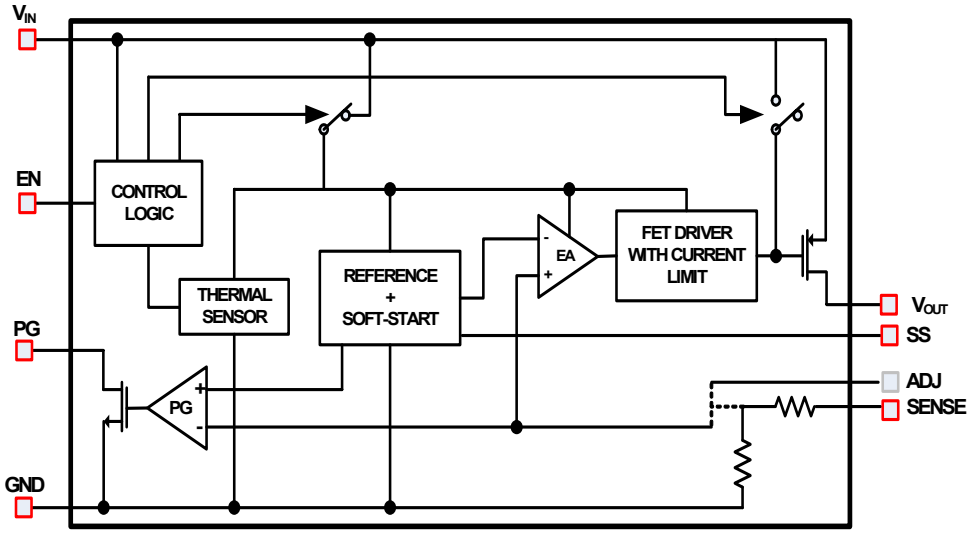


FIGURE 2. DROPOUT vs LOAD CURRENT

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-468-3774 | Copyright Intersil Americas Inc. 2009, 2011. All Rights Reserved
Intersil (and design) is a trademark owned by Intersil Corporation or one of its subsidiaries.
All other trademarks mentioned are the property of their respective owners.

Block Diagram



Ordering Information

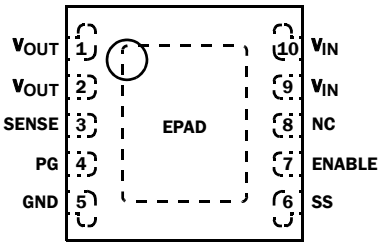
PART NUMBER (Notes 1, 3, 4)	PART MARKING	V_{OUT} VOLTAGE (Note 2)	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG DWG. #
ISL80101IR18Z	DZEB	1.8V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101IR25Z	DZFB	2.5V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101IR33Z	DZGB	3.3V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101IR50Z	DZHB	5.0V	-40 to +125	10 Ld 3x3 DFN	L10.3x3
ISL80101EVAL2Z	Evaluation Board				

NOTES:

1. Add "-T*" for Tape and Reel. Please refer to TB347 for details on reel specifications.
2. For other output voltages, contact Intersil Marketing.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL80101. For more information on MSL please see Technical Brief TB363.

Pin Configurations

ISL80101
(10 LD 3X3 DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 2	V_{OUT}	Regulated output voltage. A minimum 10µF X5R/X7R output capacitor is required for stability. See “External Capacitor Requirements” on page 8 for more details.
3	SENSE	The PGOOD circuit uses this input to monitor the output voltage status, providing a remote voltage sense.
4	PG	This is an open drain logic output used to indicate the status of the output voltage. Logic low indicates V_{OUT} is not in regulation. This pin must be grounded if not used.
5	GND	Ground.
6	SS	External capacitor on this pin adjusts startup ramp and controls inrush current.
7	ENABLE	V_{IN} independent chip enable. TTL and CMOS compatible.
8	NC	No connection. Leave floating.
9, 10	V_{IN}	Input supply. A minimum of 10µF X5R/X7R input capacitor is required for proper operation. See “External Capacitor Requirements” on page 8 for more details.
-	EPAD	EPAD at ground potential. It is recommended to solder the EPAD to the ground plane.

Absolute Maximum Ratings

V_{IN} Relative to GND (Note 5) . . . . . -0.3V to +6.5V
V_{OUT} Relative to GND (Note 5) . . . . . -0.3V to +6.5V
PG, ENABLE, SENSE, SS
Relative to GND (Note 5) . . . . . -0.3V to +6.5V
ESD Rating
Human Body Model (Tested per JESD22 A114F) 2.5kV
Machine Model (Tested per JESD22 A115C) 250V
Latch Up (Tested per JESD78C, Class 2, Level A) . . . . . ±100mA at +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld DFN Package (Notes 6, 7)	48	7

Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions (Notes 8, 9)

Junction Temperature Range (TJ) (Note 8) . . . . . -40°C to +125°C
V_{IN} Relative to GND . . . . . 2.2V to 6V
V_{OUT} Range . . . . . 800mV to 5V
PG, ENABLE, SENSE/ADJ, SS relative to GND . . . . . 0V to 6V
PG Sink Current . . . . . <10mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. Absolute maximum voltage rating is defined as the voltage applied for a lifetime average duty cycle above 6V of 1%.
6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
7. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
8. Extended operation at these conditions may compromise reliability. Exceeding these limits will result in damage. Recommended operating conditions define limits where specifications are guaranteed.
9. Electromigration specification defined as lifetime average junction temperature of +110°C where max rated DC current = lifetime average current.

Electrical Specifications

Unless otherwise noted, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 2.2\mu F$, $T_J = +25°C$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Applications Information" on page 8 and Tech Brief TB379. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNITS
DC CHARACTERISTICS						
DC Output Voltage Accuracy	V_{OUT}	$V_{OUT} + 0.4V < V_{IN} < 6V$, $0A < I_{LOAD} < 1A$	**-1.8**		**1.8**	%
DC Input Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	$V_{OUT} + 0.4V < V_{IN} < 6V$			1	%
DC Output Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	$0A < I_{LOAD} < 1A$, All voltage options	**-1**			%
Ground Pin Current	I_Q	$I_{LOAD} = 0A$, $2.2V < V_{IN} < 6V$		3	**5**	mA
		$I_{LOAD} = 1A$, $2.2V < V_{IN} < 6V$		5	**7**	mA
Ground Pin Current in Shutdown	I_{SHDN}	ENABLE Pin = 0.2V, $V_{IN} = 6V$		0.2	**12**	µA
Dropout Voltage (Note 11)	V_{DO}	$I_{LOAD} = 1A$, $V_{OUT} = 2.5V$		130	**212**	mV
Output Short Circuit Current	OCP	$V_{OUT} = 0V$, $2.2V < V_{IN} < 6V$		1.75		A
Thermal Shutdown Temperature	TSD	$2.2V < V_{IN} < 6V$		160		°C
Thermal Shutdown Hysteresis (Rising Threshold)	TSDn	$2.2V < V_{IN} < 6V$		30		°C
AC CHARACTERISTICS						
Input Supply Ripple Rejection	PSRR	f = 1kHz, $I_{LOAD} = 1A$; $V_{IN} = 2.2V$		58		dB
		f = 120Hz, $I_{LOAD} = 1A$; $V_{IN} = 2.2V$		72		dB
Output Noise Voltage		$I_{LOAD} = 1A$, BW = 10Hz < f < 100kHz		63		μV_{RMS}
ENABLE PIN CHARACTERISTICS						
Turn-on Threshold		$2.2V < V_{IN} < 6V$	**0.3**	0.8	**1**	V
Hysteresis (Rising Threshold)		$2.2V < V_{OUT} + 0.4V < 6V$	**10**	80	**200**	mV

Electrical Specifications Unless otherwise noted, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 2.2\mu F$, $T_J = +25°C$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Applications Information" on page 8 and Tech Brief TB379. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNITS
ENABLE Pin Turn-on Delay		$C_{OUT} = 10\mu F$, $I_{LOAD} = 1A$		100		µs
ENABLE Pin Leakage Current		$V_{IN} = 6V$, ENABLE = 3V			**1**	µA
SOFT-START CHARACTERISTICS						
SS Pin Currents (Note 11)	IPD	$V_{IN} = 3.5V$, ENABLE = 0V, SS = 1V	**0.5**	1	**1.3**	mA
	ICHG		**-3.3**	-2	**-0.8**	µA
PG PIN CHARACTERISTICS						
V_{OUT} PG Flag Threshold			**75**	85	**92**	$\%V_{OUT}$
V_{OUT} PG Flag Hysteresis				4		%
PG Flag Low Voltage		$V_{IN} = 2.5V$, $I_{SINK} = 500\mu A$			**100**	mV
PG Flag Leakage Current		$V_{IN} = 6V$, PG = 6V			**1**	µA

NOTES:

10. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

11. Dropout is defined as the difference in supply V_{IN} and V_{OUT} when the output is below its nominal regulation..

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A.

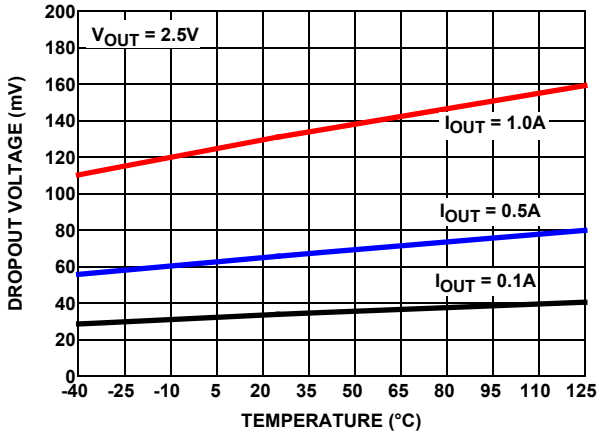


FIGURE 3. DROPOUT vs TEMPERATURE

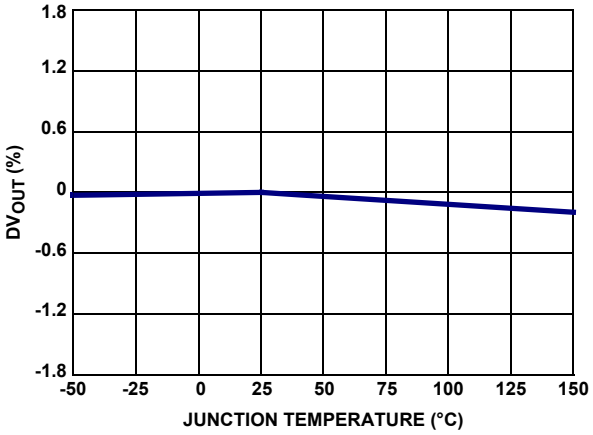


FIGURE 4. V_{OUT} vs TEMPERATURE

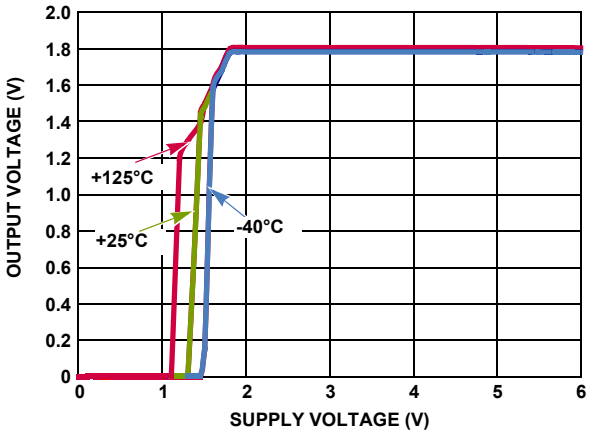


FIGURE 5. OUTPUT VOLTAGE vs SUPPLY VOLTAGE

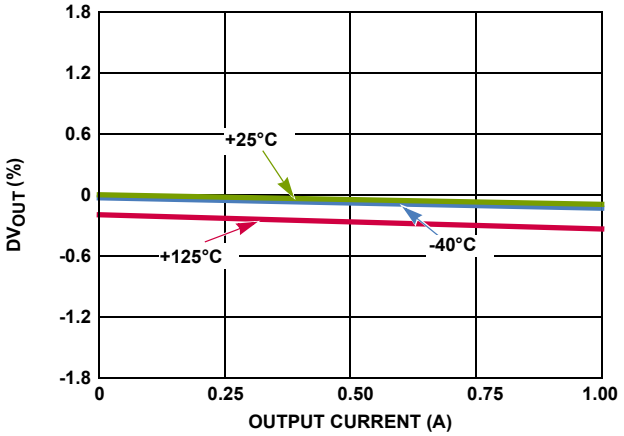


FIGURE 6. OUTPUT VOLTAGE vs OUTPUT CURRENT

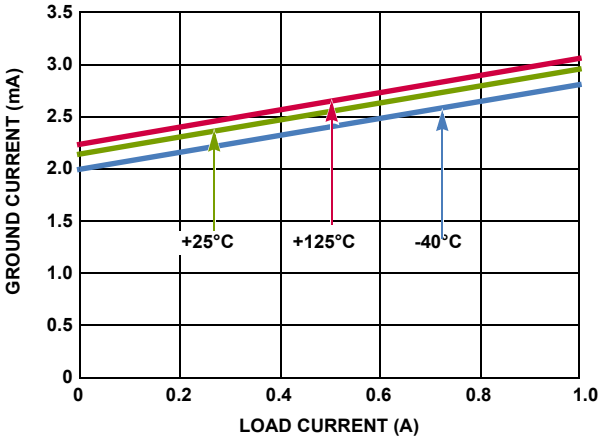


FIGURE 7. GROUND CURRENT vs LOAD CURRENT

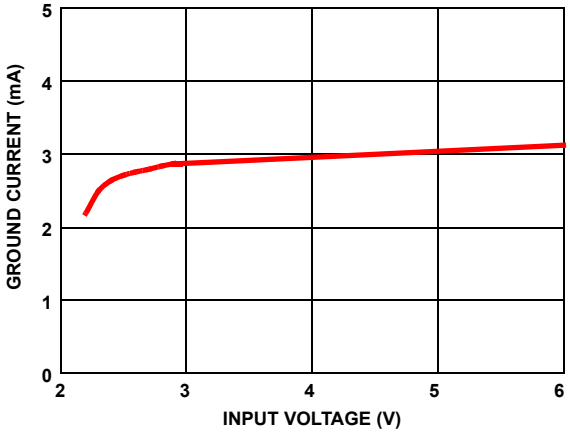


FIGURE 8. GROUND CURRENT vs SUPPLY VOLTAGE

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

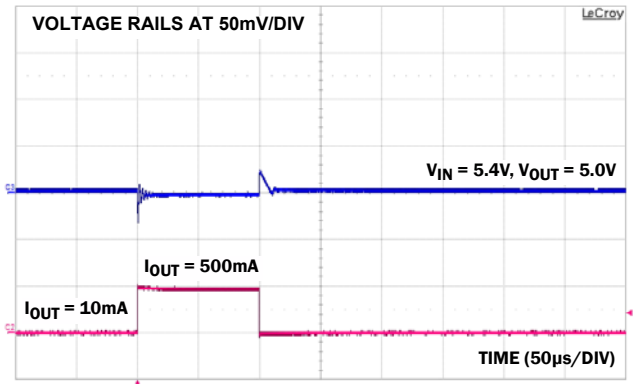


FIGURE 9A.

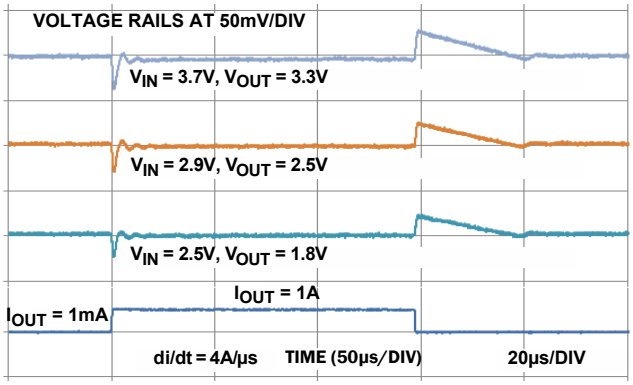


FIGURE 9B.

FIGURE 9. LOAD TRANSIENT RESPONSE

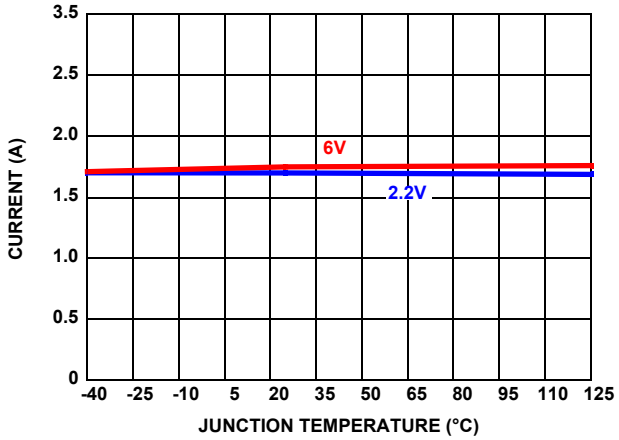


FIGURE 10. CURRENT LIMIT vs TEMPERATURE (V_{OUT} = 0V)

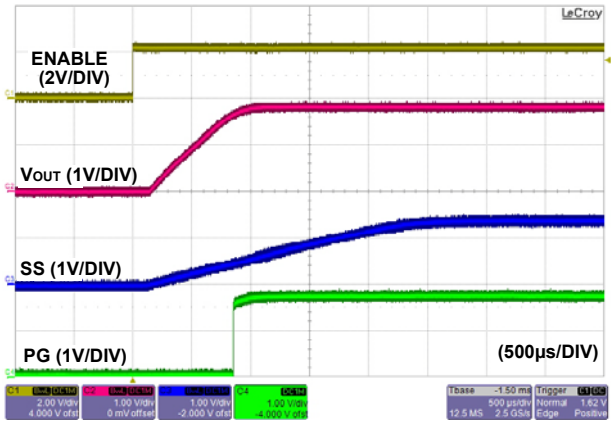


FIGURE 11. ENABLE START-UP (Css = 2.2nF)

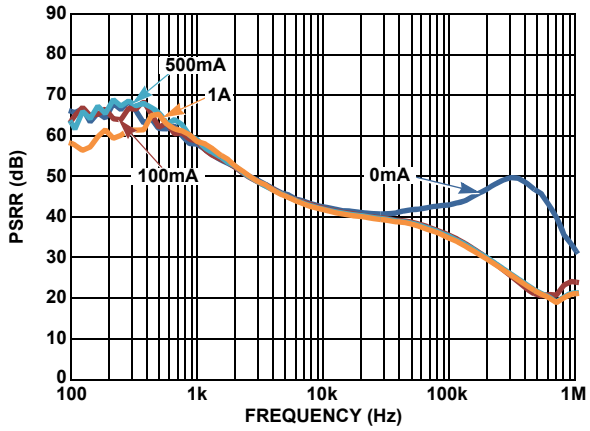


FIGURE 12. PSRR vs FREQUENCY AND LOAD CURRENT

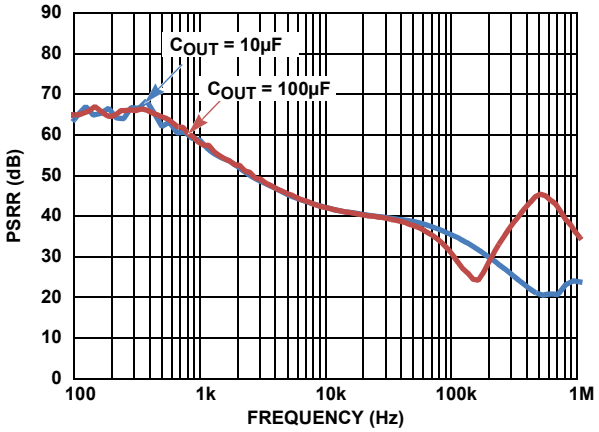


FIGURE 13. PSRR vs FREQUENCY AND OUTPUT CAPACITANCE (I_{OUT} = 100mA)

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

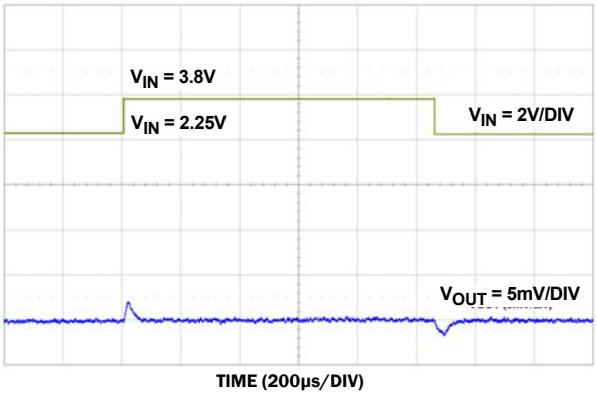


FIGURE 14. LINE TRANSIENT RESPONSE

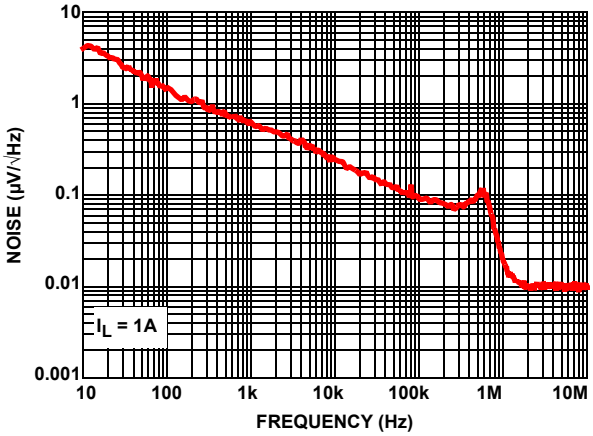


FIGURE 15. OUTPUT NOISE SPECTRAL DENSITY

Applications Information

Input Voltage Requirements

The ISL80101 is capable of delivering the following fixed output voltages: 1.8V, 2.5V, 3.3V, 5.0V. Due to the nature of an LDO, V_{IN} must be some margin higher than V_{OUT} plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from V_{IN} to V_{OUT}. The generous dropout specification of this family of LDOs allows applications to design a level of efficiency.

Enable Operation

The ENABLE turn-on threshold is typically 800mV with 80mV of hysteresis. An internal pull-up or pull-down resistor to change these values is available upon request. As a result, this pin must not be left floating, and should be tied to V_{IN} if not used. A 1kΩ to 10kΩ pull-up resistor is required for applications that use open collector or open drain outputs to control the ENABLE pin. The ENABLE pin may be connected directly to V_{IN} for applications with outputs that are always on.

Power-Good Operation

PG is a logic output that indicates the status of V_{OUT} and V_{IN}. The PG flag is an open-drain NMOS that can sink up to 10mA during a fault condition. The PG pin requires an external pull-up resistor typically connected to the V_{OUT} pin. The PG pin should not be pulled up to a voltage source greater than V_{IN}. PG goes low when the output voltage drops below 84% of the nominal output voltage or if the part is disabled. PG functions during current limit and thermal shutdown. For applications not using this feature, connect this pin to ground.

Soft-Start Operation

The soft-start circuit controls the rate at which the output voltage rises up to regulation at power-up or LDO enable. This start-up ramp time can be set by adding an external capacitor from the SS pin to ground. An internal 2µA current source charges up this C_{SS} and the feedback reference voltage is clamped to the voltage across it. The start-up time is set by Equation 1.

$$t_{start} = \frac{C_{SS} \times 0.5}{2\mu A} \quad \text{(EQ. 1)}$$

Equation 2 determines the C_{SS} required for a specific start-up in-rush current, where V_{OUT} is the output voltage, C_{OUT} is the total capacitance on the output and I_{INRUSH} is the desired in-rush current.

$$C_{SS} = \frac{V_{OUT} \times C_{OUT} \times 2\mu A}{I_{INRUSH} \times 0.5V} \quad \text{(EQ. 2)}$$

The external capacitor is always discharged to ground at the beginning of start-up or enabling.

External Capacitor Requirements

External capacitors are required for proper operation. Careful attention must be paid to the layout guidelines and selection of capacitor type and value to ensure optimal performance.

OUTPUT CAPACITOR

The ISL80101 applies state-of-the-art internal compensation to keep the selection of the output capacitor simple for the customer. Stable operation over full temperature, V_{IN} range, V_{OUT} range and load extremes are guaranteed for all capacitor types and values assuming a minimum of 10µF X5R/X7R is used for local bypass on V_{OUT}. This output capacitor must be connected to the V_{OUT} and GND pins of the LDO with PCB traces no longer than 0.5cm.

There is a growing trend to use very-low ESR multilayer ceramic capacitors (MLCC) because they can support fast load transients and also bypass very high frequency noise from other sources. However, the effective capacitance of MLCCs drops with applied voltage, age, and temperature. X7R and X5R dieletric ceramic capacitors are strongly recommended as they typically maintain a capacitance range within ±20% of nominal voltage over full operating ratings of temperature and voltage.

Additional capacitors of any value in ceramic, POSCAP, alum/tantalum electrolytic types may be placed in parallel to improve PSRR at higher frequencies and/or load transient AC output voltage tolerances.

INPUT CAPACITOR

For proper operation, a minimum capacitance of 10µF X5R/X7R is required at the input. This ceramic input capacitor must be connected to the V_{IN} and GND pins of the LDO with PCB traces no longer than 0.5cm.

Power Dissipation and Thermals

The junction temperature must not exceed the range specified in the "Recommended Operating Conditions (Notes 8, 9)" on page 4. The power dissipation can be calculated by using Equation 3:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad \text{(EQ. 3)}$$

The maximum allowable junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, $T_{A(MAX)}$ determine the maximum allowable power dissipation, as shown in Equation 4:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad \text{(EQ. 4)}$$

θ_{JA} is the junction-to-ambient thermal resistance.

For safe operation, enure that the power dissipation P_D, calculated from Equation 3, is less than the maximum allowable power dissipation $P_{D(MAX)}$.

The DFN package uses the copper area on the PCB as a heat-sink. The EPAD of this package must be soldered to the copper plane (GND plane) for effective heat dissipation. Figure 16 shows a curve for the θ_{JA} of the DFN package for different copper area sizes.

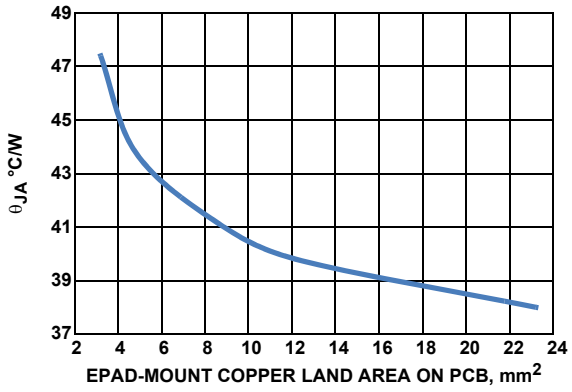


FIGURE 16. 3mmx3mm-10 PIN DFN ON 4-LAYER PCB WITH THERMAL VIAS θ_{JA} vs EPAD-MOUNT COPPER LAND AREA ON PCB

Thermal Fault Protection

The power level and the thermal impedance of the package (+45°C/W for DFN) determine when the junction temperature exceeds the thermal shutdown temperature. In the event that the die temperature exceeds around +160°C, the output of the LDO will shut down until the die temperature cools down to about +130°C.

Current Limit Protection

The ISL80101 LDO incorporates protection against overcurrent due to any short or overload condition applied to the output pin. The LDO performs as a constant current source when the output current exceeds the current limit threshold noted in the "Electrical Specifications" table on page 4. If the short or overload condition is removed from V_{OUT}, then the output returns to normal voltage regulation mode. In the event of an overload condition, the LDO may begin to cycle on and off due to the die temperature exceeding thermal fault condition and subsequently cooling down after the power device is turned off.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
7/27/11	FN6931.1	Added Related Literature
7/20/11		Main change - Deleted Adjustable Output Voltage Option Version from datasheet, now only refers to fixed output voltage option includes removal of all graphics referring to Adjustable voltage option. Modified page 1 by adding Table of key differences, graphics and changes to text page 2 - Updated Ordering Information by: Removing ADJ Device ISL80101IRAJZ plus Eval boards. Updated Tape and Reel Note by changing "Add "-T" or "TK"..." to "Add "T*"..." Updated Abs Max Rating and Thermal Information by adding ESD ratings and Latchup Changed 10 Ld DFN Tja and Tjc from “45, 4” to “48, 7” Updated DC Output Voltage Accuracy by combining Vout options Removed Feedback Pin (Adj Option Only), Feedback Input Current Specs Removed "(1A Version)" from Output Short circuit Current Spec Removed Adjustable In-Rush Current Limit Characteristics and replaced with Soft-Start Characteristics page 5 - Electrical Spec Note changed from "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design." To "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." Complete Rewrite of Applications Information POD L10.3x3 Changed Note 4 from "Dimension b applies..." to "Lead width applies..." Changed Note callout in Detail X from 4 to 5 Changed height in side view from 0.90 MAX to 1.00 MAX Added Note 4 callout next to lead width in Bottom View In Land Pattern, corrected lead shape for 4 corner pins to "L" shape (was rectangular and did not match bottom view)
12/21/2009	FN6931.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL80101

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/search.php

For additional products, see www.intersil.com/product_tree

Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems as noted in the quality certifications found at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

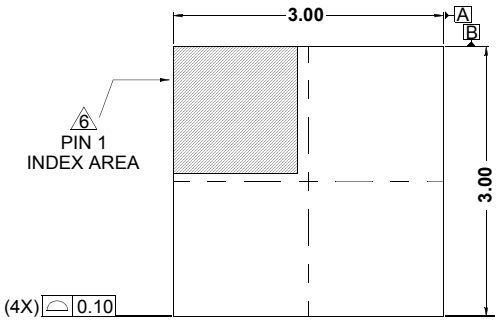
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

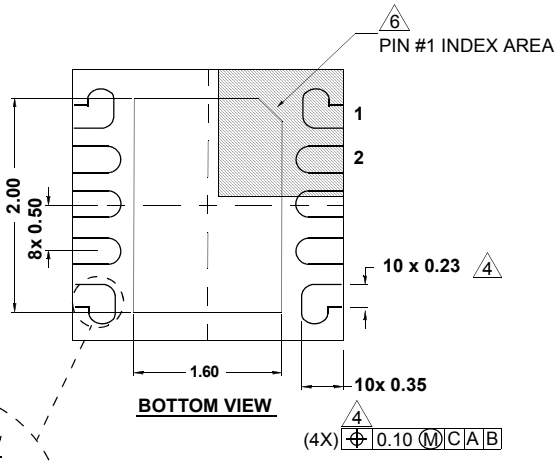
L10.3x3

10 LEAD DUAL FLAT PACKAGE (DFN)

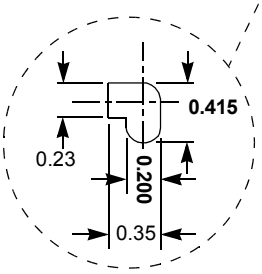
Rev 6, 09/09

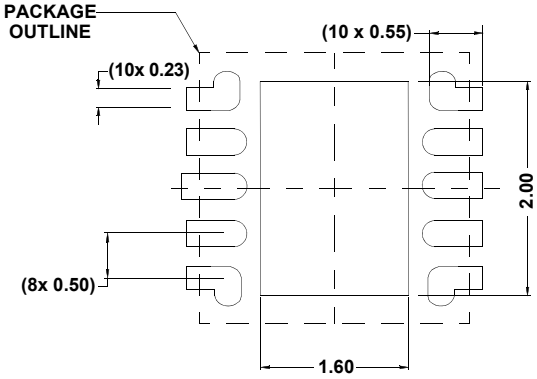


TOP VIEW

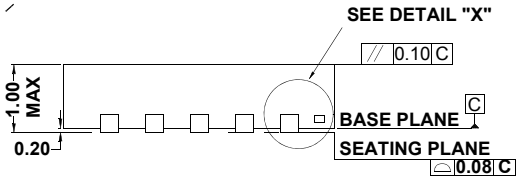


BOTTOM VIEW

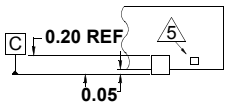




TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.