Data Sheet | February 1999 | File Number 3288.6

Digital Down Converter

The Digital Down Converter (DDC) is a single chip synthesizer, quadrature mixer and lowpass filter. Its input data is a sampled data stream of up to 16 bits in width and up to a 75 MSPS data rate. The DDC performs down conversion, narrowband low pass filtering and decimation to produce a baseband signal.

The internal synthesizer can produce a variety of signal formats. They are: CW, frequency hopped, linear FM up chirp, and linear FM down chirp. The complex result of the modulation process is lowpass filtered and decimated with identical real filters in the in-phase (I) and quadrature (Q) processing chains.

Lowpass filtering is accomplished via a High Decimation Filter (HDF) followed by a fixed Finite Impulse Response (FIR) filter. The combined response of the two stage filter results in a -3dB to -102dB shape factor of better than 1.5. The stopband attenuation is greater than 106dB. The composite passband ripple is less than 0.04dB. The synthesizer and mixer can be bypassed so that the chip operates as a single narrow band low pass filter.

The chip receives forty bit serial commands as a control input. This interface is compatible with the serial I/O port available on most microprocessors.

The output data can be configured in fixed point or single precision floating point. The fixed point formats are 16, 24, 32, or 38-bit, two's complement, signed magnitude, or offset binary.

The circuit provides an IEEE 1149.1 Test Access Port.

Features

- 75 MSPS Input Data Rate
- 16-Bit Data Input; Offset Binary or 2's Complement Format
- Spurious Free Dynamic Range Through Modulator >102dB
- Frequency Selectivity: <0.006Hz
- Identical Lowpass Filters for I and Q
- Passband Ripple: <0.04dB
- Stopband Attenuation: >104dB
- Filter -3dB to -102dB Shape Factor: <1.5
- Decimation Factors from 32 to 131,072
- IEEE 1149.1 Test Access Port
- HSP50016-EV Evaluation Board Available

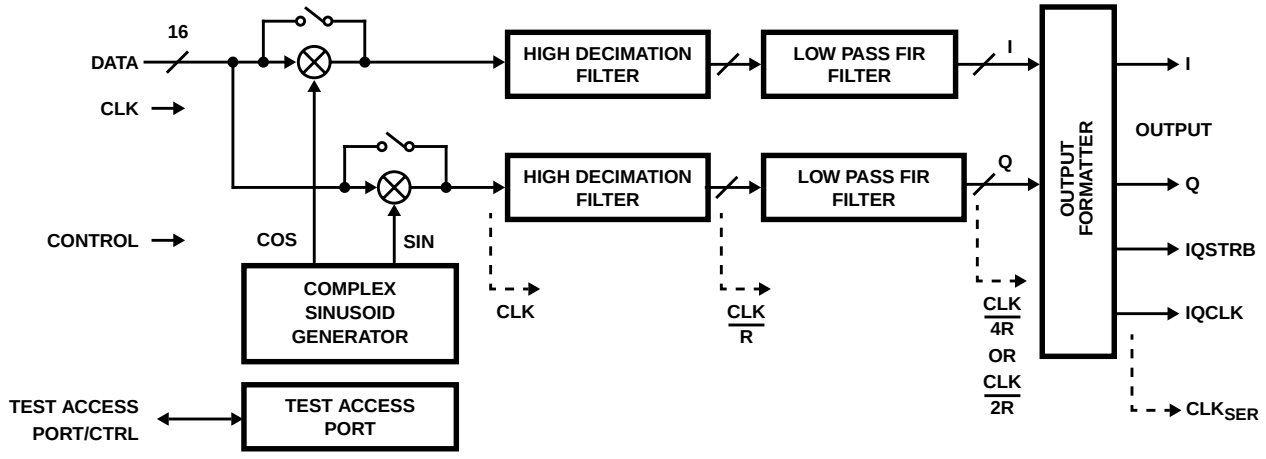
Applications

- Cellular Base Stations
- Smart Antennas
- Channelized Receivers
- Spectrum Analysis
- Related Products: HI5703, HI5746, HI5766 A/Ds

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP50016JC-52	0 to 70	44 Ld PLCC	N44.65
HSP50016JC-75	0 to 70	44 Ld PLCC	N44.65
HSP50016GC-52	0 to 70	48 Ld CPGA	G48.A

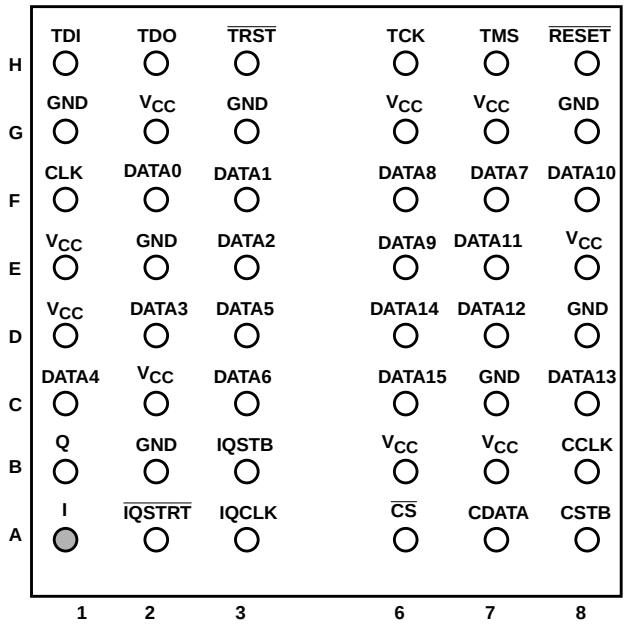
Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Pinouts

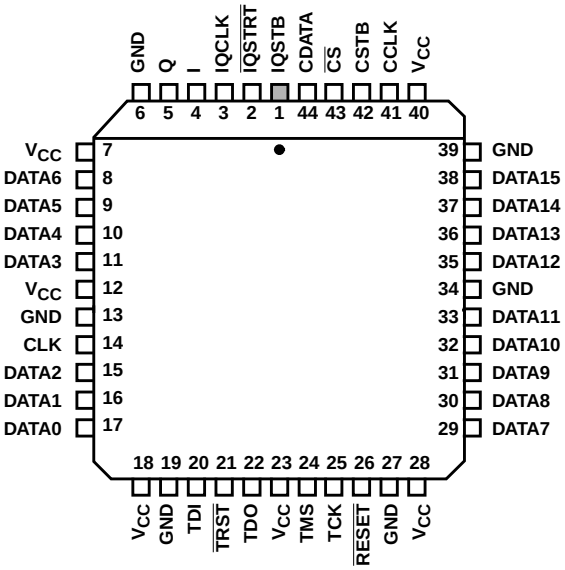
48 PIN CPGA
BOTTOM VIEW



48 PIN CPGA
TOP VIEW

	1	2	3		6	7	8
A	I	$\overline{IQSTRT}$	IQCLK		$\overline{CS}$	CDATA	CSTB
B	Q	GND	IQSTB		V_{CC}	V_{CC}	CCLK
C	DATA4	V_{CC}	DATA6		DATA15	GND	DATA13
D	V_{CC}	DATA3	DATA5		DATA14	DATA12	GND
E	V_{CC}	GND	DATA2		DATA9	DATA11	V_{CC}
F	CLK	DATA0	DATA1		DATA8	DATA7	DATA10
G	GND	V_{CC}	GND		V_{CC}	V_{CC}	GND
H	TDI	TDO	$\overline{TRST}$		TCK	TMS	$\overline{RESET}$

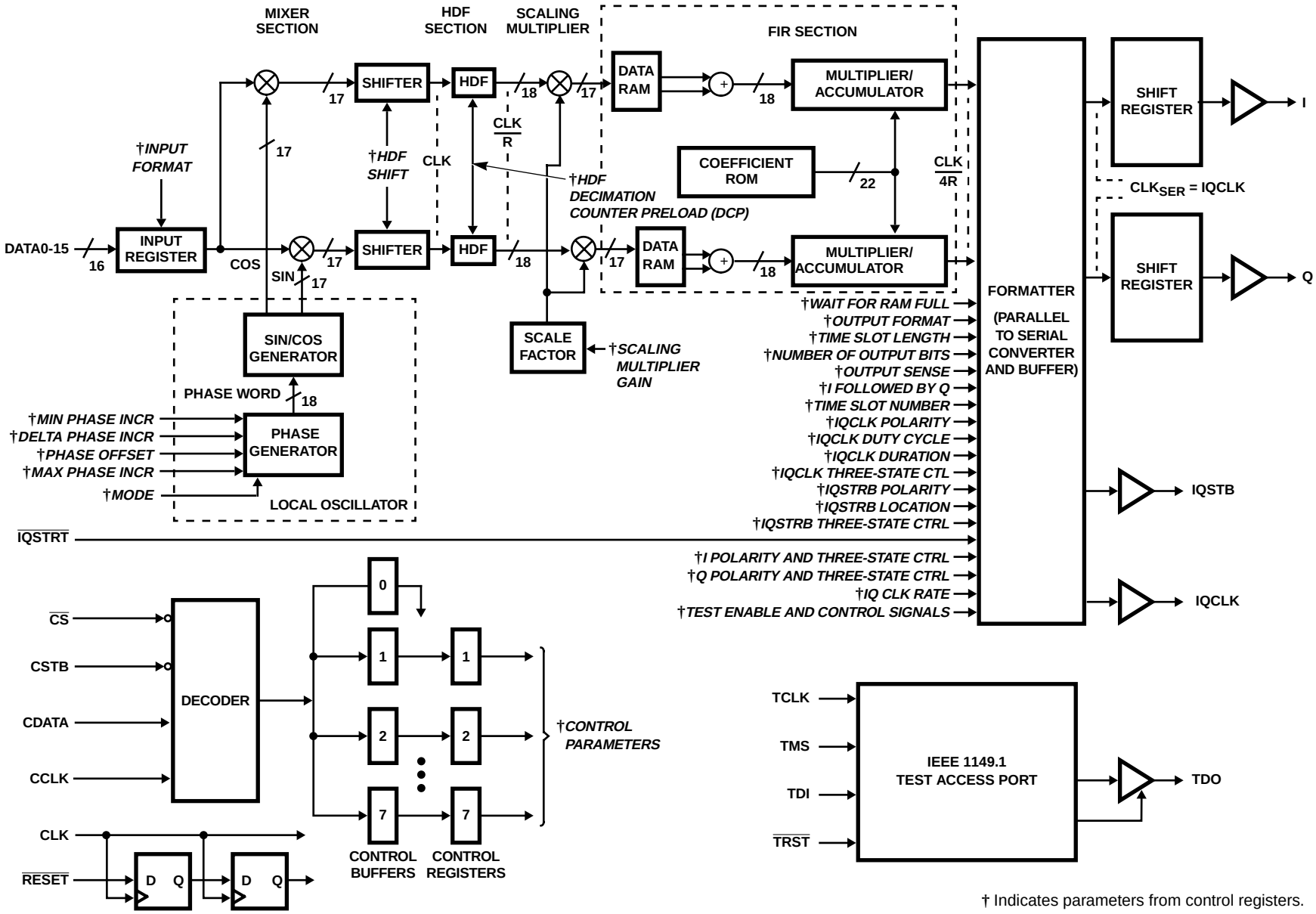
44 LEAD PLCC
TOP VIEW



Pin Description

NAME	TYPE	DESCRIPTION
V_{CC}	-	+5V Power.
GND	-	Ground.
DATA0-15	I	Input Data Bus. Selectable between two's complement and offset binary. DATA0 is the LSB.
CLK	I	Clock for input data bus. f_S is the frequency of CLK, which is also the input sample rate.
$\overline{\text{RESET}}$	I	$\overline{\text{RESET}}$ initializes the internal state of the DDC. During $\overline{\text{RESET}}$, all internal processing stops. $\overline{\text{RESET}}$ facilitates the synchronization of multiple chips for Auto Three-State operation. If the Force bits in Control Word 7 are inactive and the IEEE Test Access Port is in an Idle state, $\overline{\text{RESET}}$ causes the IQCLK, IQSTB, I and Q outputs to go to a high impedance state. All Control Registers are updated from their respective Control Buffer Registers on the third rising edge of CLK after the deassertion of $\overline{\text{RESET}}$. If $\overline{\text{RESET}}$ is deasserted t_{RS} nanoseconds prior to the rising edge of CLK, the internal reset will deassert synchronously. If t_{RS} is violated, then the circuit contains a synchronizer which will cause reset to be deasserted internally one or more clocks later. An initial reset is required to guarantee proper operation of the DDC. Active low.
I	O	The I output has three modes: I data; I data followed by Q data; real data.
Q	O	The Q output has two modes: Q data and the carry out of the Phase Adder.
IQCLK	O	IQ Clock: Bit or word clock for the I and Q outputs.
IQSTB	O	IQ Strobe: Beginning or end of word indicator for I and Q.
$\overline{\text{IQSTRT}}$	I	IQ Start: Initiates output data sequence. Active low.
CDATA	I	Control Data: Port for control data input.
CCLK	I	Control Data Clock: Control data input bit clock.
CSTB	I	Control Data Strobe: Beginning of word indicator for control data.
$\overline{\text{CS}}$	I	Chip Select: Enables control data loading of DDC. Active low.
TCK	I	Test Clock: Bit Clock for IEEE 1149.1 Data. This signal should be either tied low or pulled high when the TAP is not used.
TMS	I	Test Port Mode Select: This signal should be either left unconnected or pulled high when the TAP is not used.
TDI	I	Test Data Input for IEEE Test Port: This signal should be either left unconnected or pulled high when the TAP is not used.
TDO	O	Test Data Output for IEEE Test Port: This output will be in the high impedance state when the TAP is not used.
$\overline{\text{TRST}}$	I	Test Port Reset. Active Low. This signal should be tied low when the TAP is not used.

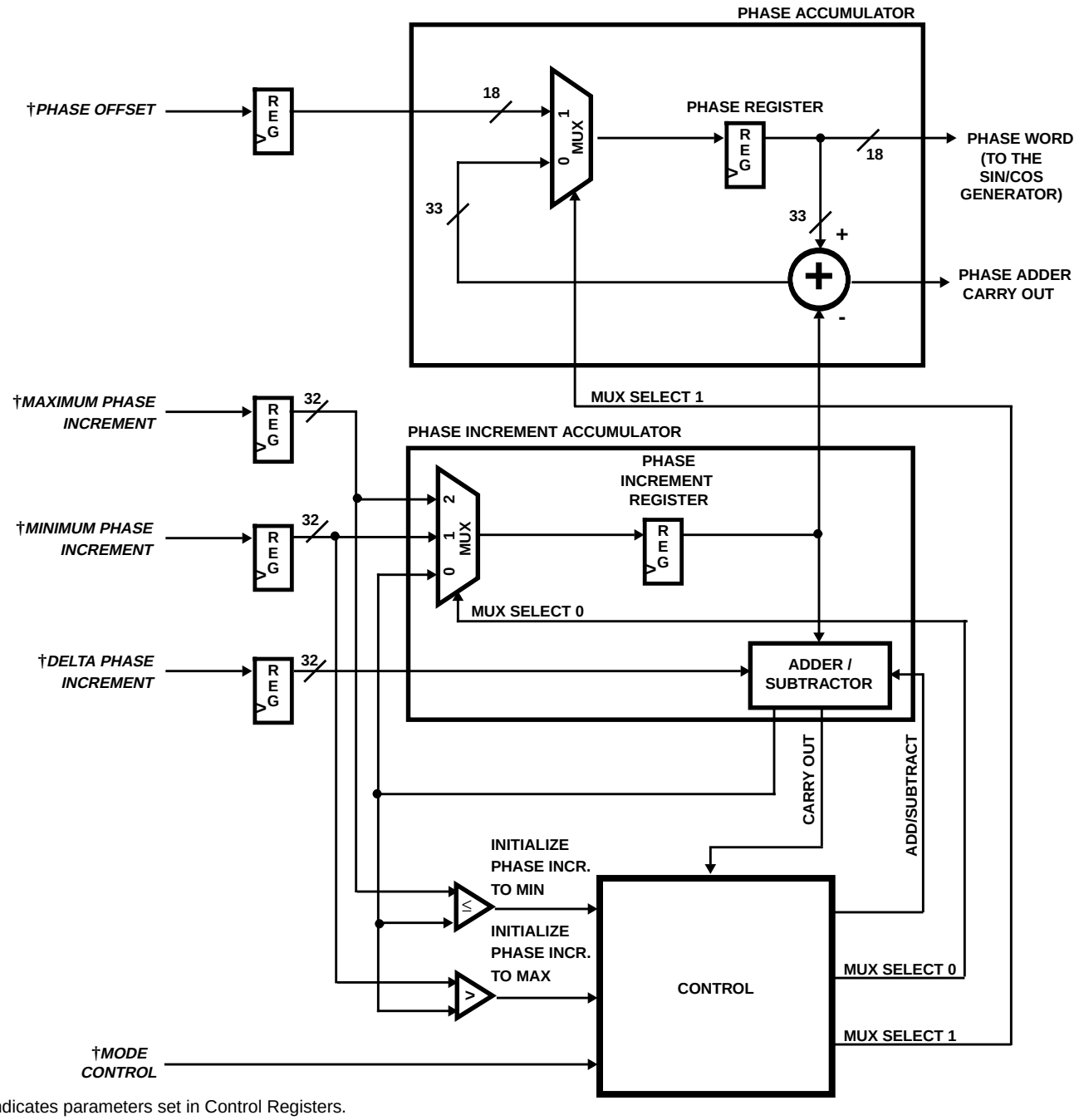
DDC Functional Block Diagram



† Indicates parameters from control registers.

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

Phase Generator Block Diagram



† Indicates parameters set in Control Registers.

FIGURE 2. PHASE GENERATOR BLOCK DIAGRAM

Functional Description

The primary function of the DDC is to extract a narrow frequency band of interest from a wideband input, convert that band to baseband and output it in either a quadrature or real form. This narrow band extraction is accomplished by down converting and centering the band of interest at DC. The conversion is done by multiplying the input data with a quadrature sinusoid. A quadrature lowpass filter is applied to the multiplier outputs. Identical real lowpass filters are provided in the in-phase (I) and quadrature phase (Q) processing branches. Each filtering chain consists of a cascaded HDF and FIR filter, which extracts the band of interest. During filtering, the signal is decimated by a rate which is proportional to the output bandwidth. The bandwidth of the resulting signal is the double sided passband width of the lowpass filters. An Output Formatter manipulates the filter output to provide the data in a variety of serial data formats.

Local Oscillator

Signal data clocked into the DATA0-15 input of the DDC is multiplied by a quadrature sinusoid in the Mixer Section (see Figure 1). The data input to the DDC is a 16-bit real data stream which is sampled on the rising edges of CLK. It can be in two's complement or offset binary format.

The input data is passed to a mixer, which is composed of two real multipliers. One of these multiplies the input data samples by the in-phase (cosine) component of the quadrature sinusoid, and the other multiplies the input data samples by the quadrature (sine) component. The in-phase and quadrature data paths are designated I and Q respectively. The sine and cosine are generated in the local oscillator as shown in Figure 1.

The local oscillator is programmed to produce a quadrature sinusoid with programmable frequency and phase. The frequency can be constant (Continuous Wave - CW), linearly increasing (up chirp), linearly decreasing (down chirp), or linear up/down chirp. The initial phase of the waveform is set by the phase offset.

The phase, frequency and chirp limits of the quadrature sinusoid are controlled by the Phase Generator (Figure 2). The output of the Phase Generator is an 18-bit phase word that represents the current phase angle of the complex sinusoid. The Phase Generator automatically increments the phase angle by a preprogrammed amount on every rising edge of CLK. Stepping the output phase from 0 through full scale (2^{18} - 1) steps the phase angle of the quadrature sinusoid from 0 to $(-2+2^{-17})\pi$ radians. ***NOTE: The phase is stepped in a clockwise (decreasing) direction to support down conversion.*** The frequency of the complex sinusoid is determined by the number of clocks needed for the phase to step though its full range of 2π radians. The required phase increment for a given local oscillator frequency is calculated by:

$$\text{Phase Increment} = \text{INT}\left[(f_C/f_S)\,2^{33}\right]\text{H}$$
$$f_C = (\text{Phase Incr})\,f_S\,2^{-33};\ 0 < f_C < f_S/2 \qquad \text{(EQ. 1)}$$

where:

f_C is the desired local oscillator frequency

f_S is the input sampling frequency

Phase Increment is the Control Word Value (in Hex)

There are five parameters which control the Phase Generator: Phase offset, minimum phase increment, maximum phase increment, delta phase increment and Mode Control. These values are programmed via Control Words 2, 3, and 4. Mode Control is used to select the function of the other parameters.

The phase offset is the initial setting of the phase word going to the SIN/COS Generator. Subsequent phases of the sinusoid are calculated relative to this offset. The minimum phase increment has two mode dependent functions: when the SIN/COS Generator is forming a CW waveform, the minimum phase increment is the phase step taken on every clock. When the SIN/COS Generator is producing a chirped sinusoid, the minimum phase increment is the smallest phase step taken. Maximum phase increment is only used during Chirped Modes; it is the largest allowable phase increment. During Chirp Modes, the delta phase increment is the difference between successive phase increments.

The four phase parameters are stored in their respective registers in the Phase Generator. The Phase Register stores the current phase angle. On the first clock following the deassertion of $\overline{\text{RESET}}$, the 18 MSBs of the Phase Register are loaded from the Phase Offset Register. On every rising edge of CLK thereafter, the output of the Phase Increment Register is subtracted from the 32 LSBs of the current phase. The 33-bit difference is stored back in the Phase Register on the next CLK. The 18 most significant bits of the Phase Register form the phase word, which is the input to the SIN/COS Generator.

Figure 3 gives a graphic representation of the phase parameters for the CW case. To understand their interrelationships, the phase should be visualized as the angle of a rotating vector. When the local oscillator in the DDC is programmed to generate a CW waveform, the multiplexers are configured so that the Minimum Phase Increment is stored in the Phase Increment Register; this value is subtracted from the output of the Phase Register on every CLK and the difference becomes the new Phase Register value. The Delta Phase Increment and Maximum Phase Increment are ignored when generating a CW.

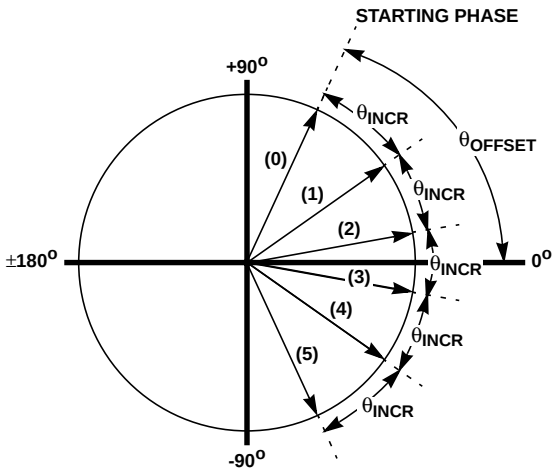


FIGURE 3. PHASE WORD PARAMETERS FOR CW CASE

In Up Chirp Mode the local oscillator generates a signal with a linearly increasing frequency (Figure 4A). The Phase Increment Register is initially loaded with the minimum Phase Increment value; on every clock, the contents of the Phase Increment Register is subtracted from the current output of the Phase Register. Simultaneously, the Delta

Phase Increment Register is added to the 24 LSBs of the output of the Phase Increment Register. On the next CLK, that sum is stored back in the Phase Increment Register, the new phase is stored in the Phase Register and the process is repeated. The phase increment is allowed to grow until the next phase increment would equal or exceed the maximum phase increment value. When this happens, the Phase Increment Register is reset to the minimum phase increment and the cycle starts over again.

NOTE: The phase increment is never equal to the maximum phase increment, since the Phase Increment Register is reloaded if the next phase increment value would be greater than the maximum phase increment.

From the time the Phase Generator starts at the minimum phase increment until it reaches the maximum phase increment, the phase word on clock n is given by:

$$\text{Phase Word} = \text{Phase Offset} - [\text{Minimum Phase Increment} + n\ (\text{Delta Phase Increment})] \quad \text{(EQ. 2)}$$

An example of the outputs of the Phase Increment Register, Phase Register, and the I output of the SIN/COS Generator are shown in Figure 4B.

In Down Chirp Mode the local oscillator generates a signal with a linearly decreasing frequency (Figure 5A). The maximum phase increment is loaded into the Phase Increment Register and the phase offset value goes into the Phase Register. The delta phase increment is subtracted from the 24 LSBs of the phase increment to form a new phase increment at each clock. The phase increment is allowed to diminish until it reaches the minimum phase increment value, then it is reset to the maximum phase increment value and the cycle is repeated. Note that the value of the phase increment can be equal to, but never less than the minimum phase increment, since the Phase Increment Register is reloaded if the next phase increment value would be less than the minimum phase increment. This feature protects the DDC from exceeding the Nyquist frequency. In this case, from the time the Phase Generator starts at the maximum phase increment until it reaches the minimum phase increment, the phase word on clock n is given by:

$$\text{Phase Word} = \text{Phase Offset} - [\text{Minimum Phase Increment} - n\ (\text{Delta Phase Increment})] \quad \text{(EQ. 3)}$$

See Figure 5B for a graphical representation of this process.

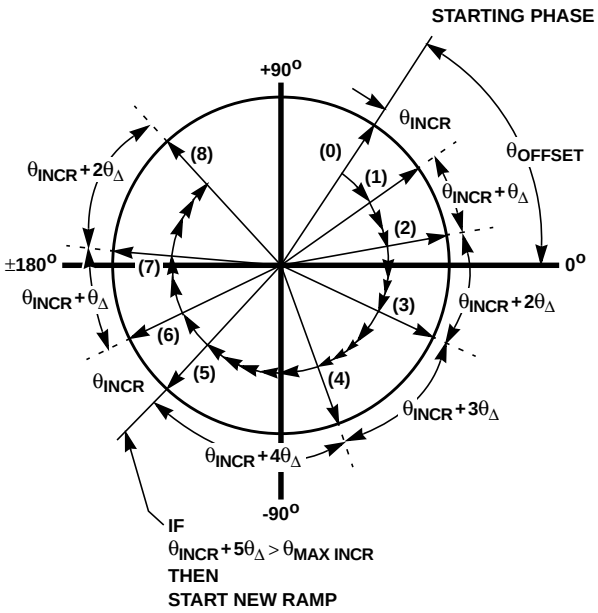


FIGURE 4A. PHASE WORD DURING UP CHIRP

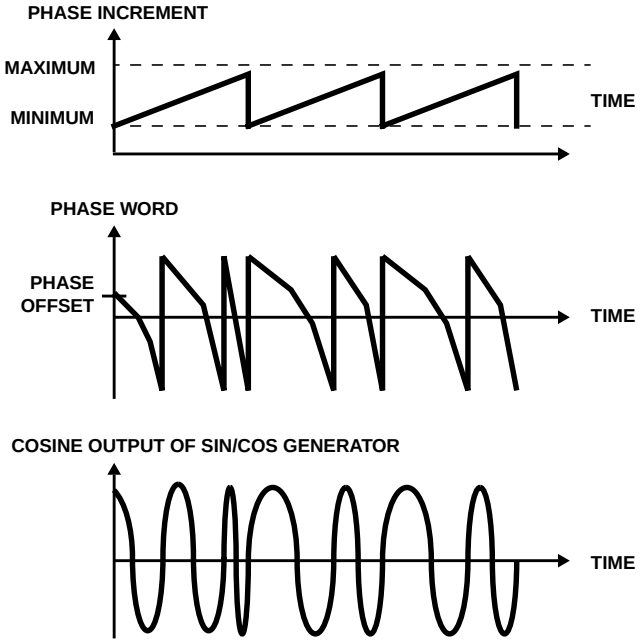


FIGURE 4B. UP CHIRP

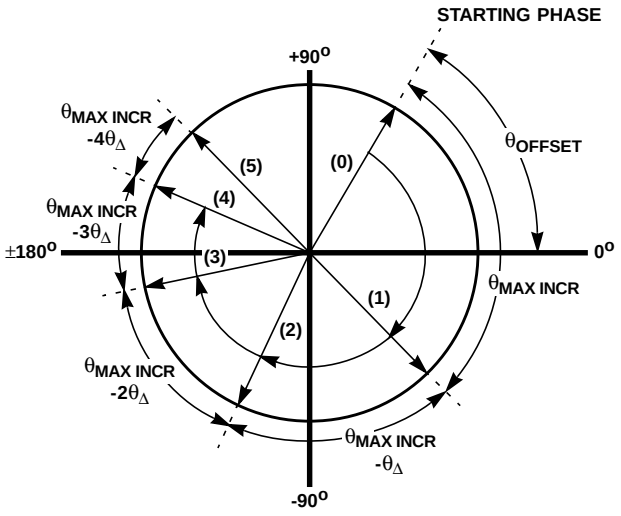


FIGURE 5A. PHASE WORD DURING DOWN CHIRP

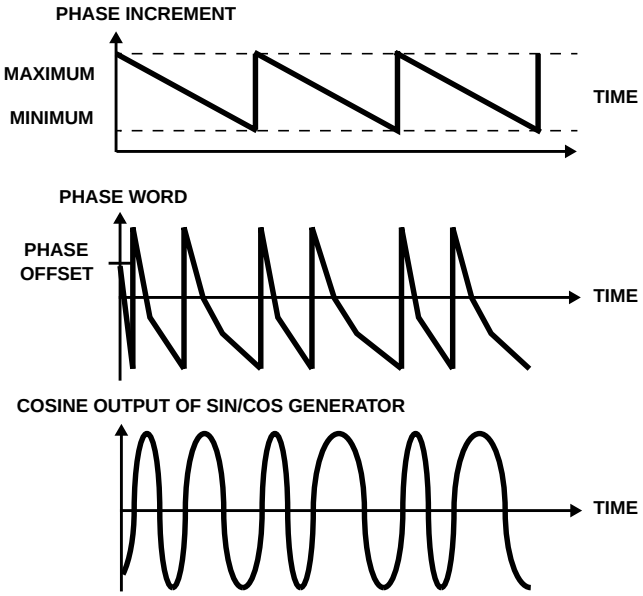


FIGURE 5B. DOWN CHIRP

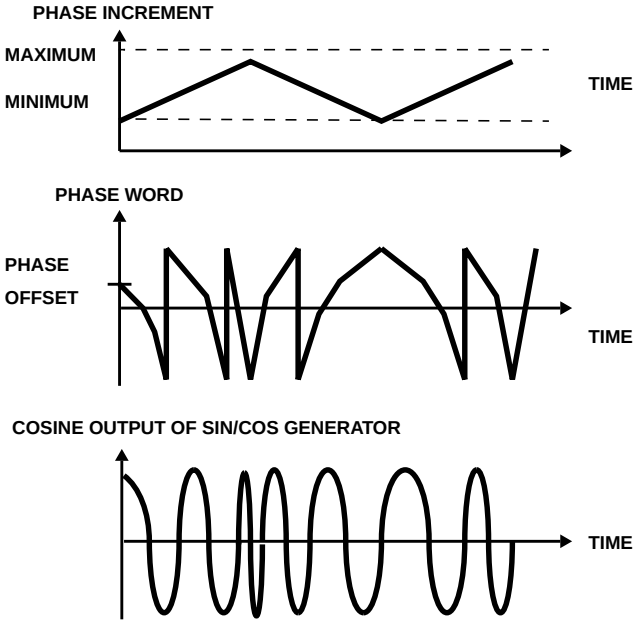


FIGURE 6. UP/DOWN CHIRP

In Up/down Chirp Mode, the phase accumulator is set to the phase offset value and the minimum phase increment is loaded into the Phase Increment Register. The delta phase increment is added to the 24 LSBs of the Phase Increment Register to form a new phase increment at each clock. The phase increment is allowed to grow until it nears the maximum phase increment value (as defined in the up chirp description). The delta phase increment value is then subtracted from the least significant bits of the Phase Increment Register to form a new phase increment at each clock. The phase increment is allowed to diminish until it reaches the minimum phase increment value (as defined in the down chirp description). The Phase Increment Register is then reloaded with the minimum phase increment, and the up/down cycle begins again. See Figure 6 for a graphical representation of this process.

The minimum and maximum phase increments have allowable values from 0 to 2^{32}-1. This corresponds to the phase increment:

$$0 < \text{Phase Increment} < \pi(1 - 2^{-32}) \text{ radians} \quad \text{(EQ. 4)}$$

The Delta Phase Increment parameter can take on values from 0 to 2^{24} - 1 which corresponds to the Delta Phase Increment:

$$0 < \text{Delta Phase Increment} < \pi(2^{-8} - 2^{-32}) \text{ radians} \quad \text{(EQ. 5)}$$

The output of the phase accumulator forms the input to the SIN/COS Generator which in turn produces a quadrature vector which rotates clockwise: the outputs are cos(ωn) and -sin(ωn). The outputs of the SIN/COS Generator are two's complement values which are scaled to prevent overflow in subsequent operations in the DDC under normal operation. The scale factor has a negligible effect on the end to end DDC gain.

The frequency resolution of the DDC = (frequency of CLK)/(Number of Phase Register bits). At the maximum clock rate, this results in a frequency selectivity of 75MHz/2^{33} = 0.009Hz. The 18-bit phase word yields a phase noise figure of greater than 102dB.

Mixer

The Mixer performs quadrature modulation by multiplying the output of the SIN/COS Generator by the input data. The outputs of the I and Q multipliers are symmetrically rounded to 17 bits to preserve the 102dB spurious free dynamic range (SFDR). The result of the quadrature modulation process is passed to the High Decimating Filter (HDF) Section.

High Decimation Filter

The High Decimation Filter (HDF) Section is comprised of two real HDF filters, one processing the I data branch and one processing the Q data branch. Each branch has the lowpass response shown in Figure 7. The normalized HDF frequency impulse response is given by the equation:

$$H(f) = \left[\frac{\text{Sin}(\pi F_S)}{\text{Sin}(\pi F_S/R)}\right]^5 \left[\frac{1}{R}\right]^5 \quad \text{(EQ. 6)}$$

where F_S is the input sampling rate; R is the decimation (rate change) factor.

Figure 7A shows this equation plotted from DC to the first null, while Figure 7B shows the equation plotted from DC response to f_S.

NOTE: The HDF is a true FIR filter; i.e., the phase is linear.

The data path through the HDF was designed to ensure a true 16-bit noise floor (approximately 98dB) at the output of the DDC. The structure of the HDF filter used in the DDC is a five stage decimation filter. The width of each successive stage decreases such that the LSBs are lost due to truncation [1]. As a result, the data must be processed in the MSBs of the filter so that the noise due to truncation is below the required noise floor. Thus, the input data of the HDF must be shifted so that its output data fills the HDF output word. The shift is a function of the desired HDF decimation rate R and the number of HDF filter stages (which is fixed at 5). The shift is performed by the Data Shifter, which positions the input data to the HDF for the maximum dynamic range while avoiding overflow errors. The shift factor is programmed into the Shift field of Control Word 4. The value in this field is calculated by the equation:

$$\text{Shift} = 75 - \text{Ceiling}(5 \log_2(R)) \quad \text{(EQ. 7)}$$

where R is the HDF decimation factor and Ceiling(X) denotes the ceiling function of X; i.e., the result is X if X is an integer, otherwise the result is the next higher integer.

During $\overline{\text{RESET}}$, the HDF is initialized and will not output any information until it is filled with new data.

NOTE: The output rate of the HDF is CLK divided by the HDF decimation factor (CLK/R). The HDF decimation counter preload (DCP) is programmed in Control Word 5, bits 21-35 and has the value: DCP = R -I, where R is the HDF decimation factor.

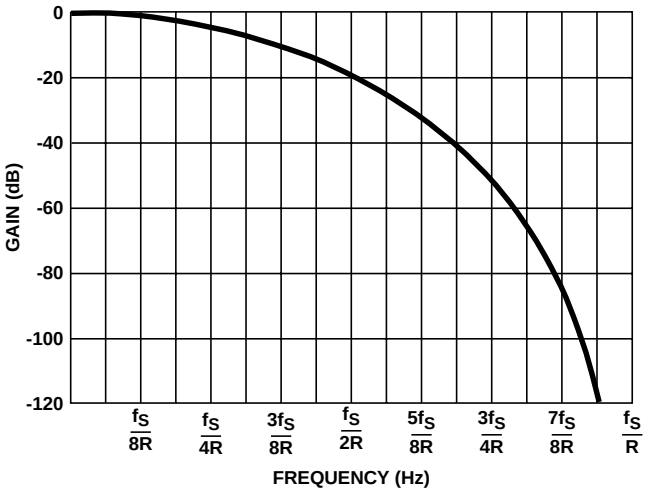


FIGURE 7A. FREQUENCY RESPONSE OF HIGH DECIMATION FILTER FROM DC TO FIRST NULL (FOR R = 16) Gain (dB) = 20log [H(f)]

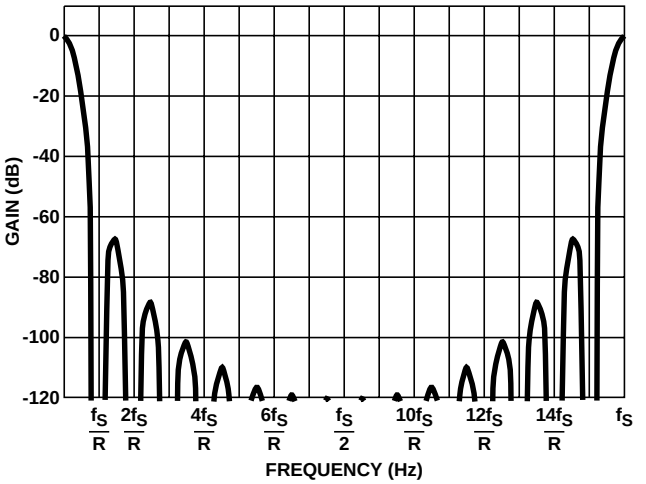


FIGURE 7B. DDC HC FREQUENCY RESPONSE (FOR R = 16) Gain (dB) = 20log[H(f)]

Scaling Multipliers

The output of each HDF is passed to a Scaling Multiplier. The Scaling Multipliers are used to compensate for the HDF gain, which is between 1 (inclusive) and 0.5 (non-inclusive), or (0.5, 1.0). The gain through the HDF is dependent on the decimation factor: when the decimation is an even power of two, the HDF gain is equal to 1; otherwise, the gain must be compensated for in the Scaling Multiplier. The HDF gain is given by the equation:

$$\text{HDF Gain} = R^5/2^{\text{CEILING}(5\log_2(R))} \quad \text{(EQ. 8)}$$

where R is the HDF decimation factor. The compensating Scale Factor, which is input to both Scaling Multipliers, is given by the equation:

$$\text{Scale Factor} = 2^{\text{CEILING}(5\log_2(R))}/R^5 \quad \text{(EQ. 9)}$$

where R is the HDF decimation factor.

NOTE: The Scale Factor falls in the interval [1, 2). The output of the scaling multiplier is symmetrically rounded to 17 bits.

The binary formats of the inputs and outputs of the scaling multiplier are as follows:

Input from HDF:	$a_0(-2^0).\ a_1(2^{-1})\ a_2(2^{-2})...\ a_{17}(2^{-17})$
Scale factor:	$a_0(2^0).\ a_1(2^{-1})\ a_2(2^{-2})...\ a_{15}(2^{-15})$
Output:	$a_0(-2^0).\ a_1(2^{-1})\ a_2(2^{-2})...\ a_{16}(2^{-16})$

FIR Filter

The Scaling Multiplier output is passed to the FIR Filter, which performs aliasing attenuation, passband roll off compensation and transition band shaping. The FIR Filter Section is functionally two identical 121 tap lowpass FIR filters, one each for the I and Q channel. The two filters are each implemented as sum of products, each with a single multiplier, with the coefficients stored in ROM. The filters' passbands are precompensated to be the inverse of the response of the HDF. The frequency responses of the HDF, FIR, and Composite HDF/FIR filters are shown in Figure 8. The composite passband of the HDF and FIR filter frequency response is shown in Figure 9. The FIR coefficients are scaled so that the maximum gain of the composite filter is less than or equal to 0dB. The composite passband ripple is less than 0.04dB.

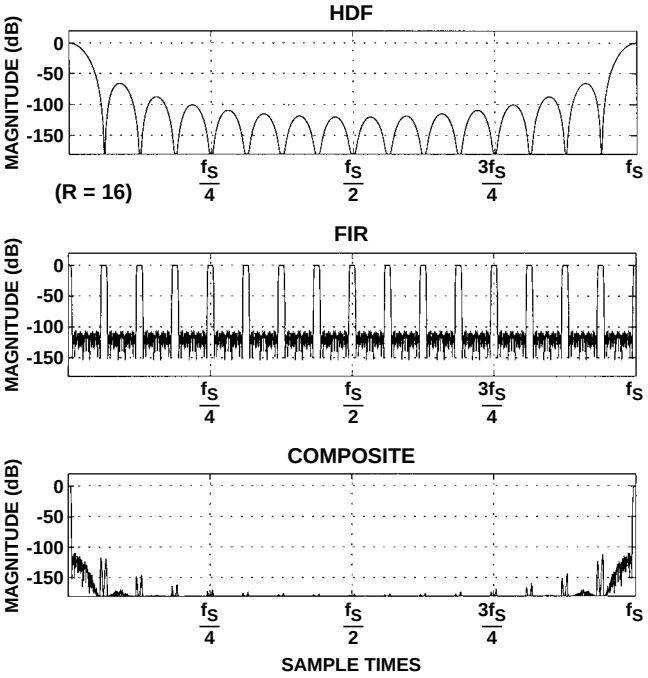


FIGURE 8A. DDC HDF, FIR, AND COMPOSITE FILTER RESPONSE (FOR R = 16)

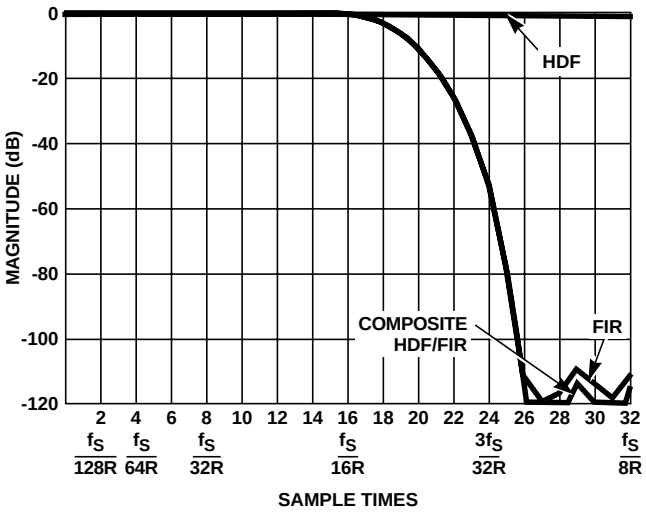


FIGURE 8B. DDC FILTER RESPONSES (FOR R = 16)

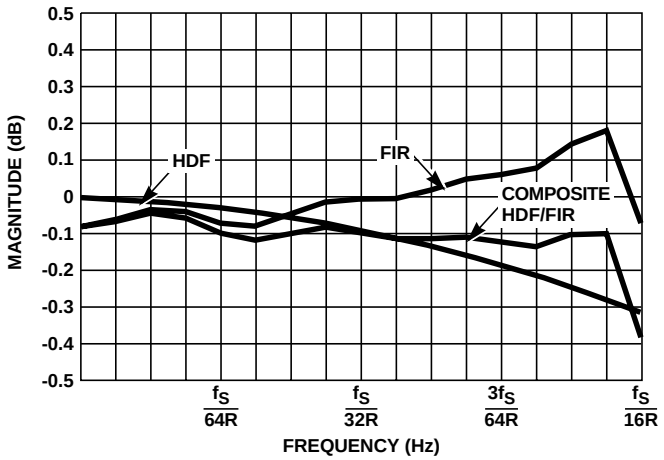


FIGURE 9. FIR COMPENSATION FOR HDF ROLL OFF (FOR R = 16)

The coefficients of the filter are quantized to 22 bits to preserve greater than 106dB of stopband attenuation. The sum of products of each filter output calculation is a 38-bit number with 37 fractional bits.

When a quadrature output is selected, the outputs of the FIR filters are decimated by a factor of four. When real output is selected, only the I output is active. The output is decimated by two in this case. When Filter Only Mode is selected, only the I filter path is active and its output is decimated by four.

The composite filter bandwidths are a function of the HDF decimation rate and the FIR Filter shape. The double sided bandwidths are specified by Equations 10 and 11.

$$-3dB\ BW_{DS} = 0.1375F_S/R \quad 16 < R < 16384 \qquad \text{(EQ. 10)}$$

$$-102dB\ BW_{DS} = 0.2002F_S/R \quad 16 < R < 16384 \qquad \text{(EQ. 11)}$$

where F_S = CLK; R = HDF Decimation Factor.

The single sided bandwidths are specified in Equations 12 and 13.

$$-3dB\ BW_{SS} = 0.06875F_S/R \qquad \text{(EQ. 12)}$$

$$-102dB\ BW_{SS} = 0.100097F_S/R \qquad \text{(EQ. 13)}$$

where F_S = CLK; R = HDF Decimation Factor.

NOTE: The output data rate of the FIR is the HDF output rate divided by either 2 or 4, depending on mode. Recall the HDF output rate is CLK/R. (See Table 1.)

TABLE 1. FIR OUTPUT RATE AND DECIMATION

OUTPUT MODE	FIR OUTPUT RATE	FIR DECIMATION
Real	CLK/2R	2
Complex	CLK/4R	4
Filter Only	CLK/4R	4

R - HDF Decimation Factor

Output Formatter

The circuit has two serial data outputs, I and Q. The timing of the output bits is referenced to IQCLK and IQSTB. There are several modes of operation for the data and control line interface, all of which were designed to be compatible with common microprocessors. These interface modes are selected by loading the appropriate control words (see Tables 3 through 10, with Table 9 containing most interface parameters).

Quadrature data output can occur in one of two ways: simultaneously or sequentially. The simultaneous method clocks out the I and Q data on their respective serial output pins. The I followed by Q method clocks I and Q out sequentially on the I output pin: the entire I word is serially clocked out first, then the entire Q word. In real data Output Mode, the Formatter converts the quadrature data to real and clocks it out serially on the I output pin. In all modes, the I and Q outputs return to the zero state after the last bit is transmitted.

When the “I followed by Q” signal (CW6, bit 35) is low, I data will appear on the I output and Q data will appear on the Q output.

When the “I followed by Q” signal (CW6, bit 35) is asserted, the Q output is inactive and I data, followed by Q data appear on the I output. When in this state, and both the “Test Enable” signal (CW1, Bit 3), and “Q Strobe on Rollover” signal (CW7, Bit 10) signal are asserted, the Phase

Generator Carry Out will appear on the output. Control Word 5 contains fields to set the number of output bits transmitted to the arithmetic representation and interface control of the serial output data. Control Word 4, Bits 31-32, allow selection of baseband centered quadrature on baseband offset quadrature complex outputs. Control Word 4, Bit 0, allows selection of spectral inversion. In addition, the output drivers for I, Q, IQCLK and IQSTB can be individually enabled or placed in a high impedance state using Control Word 6, Bits 20-28. These options are explained below.

When the “Output Spectrum” signal (CW4, bits 31-32) is set to “01”, then the real output data appears on the I output and the Q output in the I/Q separate mode. When in I Mode followed by Q Mode, the Q slot is also real data since the real mode outputs at twice the rate of the complex mode (CW4, bits 31-32 = 00).

When set for fixed point output, the output data can be in two's complement, offset binary or signed magnitude form. Data is converted to offset binary by complementing the most significant bit of a two's complement number. The length of the output data word can be 16, 24, 32 or 38-bits. The first three options are symmetrically rounded to the LSB of the output data; the fourth option represents the full 38-bit width of the accumulator and so represents exact arithmetic.

The output has a saturation option to prevent possible overflow due to a step input at power up. When Overflow Protection is enabled, the output is forced to be either the most positive or most negative number. Saturation is available in all four fixed point output options, and is set via Control Word 7, Bit 0.

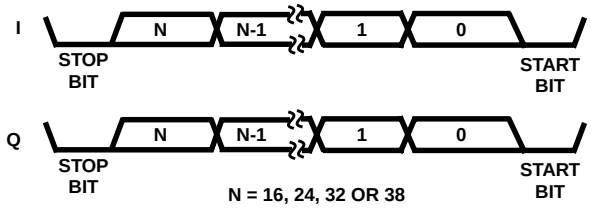
Data can also be output in single precision floating point format (see Table 2). For all output data formats, the internal calculations are performed in exact two’s complement integer arithmetic and the resulting data is converted in the Output Formatter.

TABLE 2. FLOATING POINT FORMAT

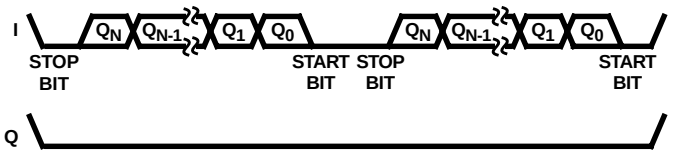
SIGN	EXPONENT	MANTISSA	
-2^0	2^7 to 2^0	Implied 1	0.2^{-1} to 2^{-23}

The I and Q pins can be programmed for either simultaneous or I followed by Q output. In simultaneous mode, the I and Q data appear on the I and Q pins, respectively. Each data sample is preceded by a leading zero bit, followed by the output data, followed by a trailing zero bit. In I followed by Q Mode, the output data appears on the I pin, and consists of a leading zero bit, then the I data, a trailing zero, a leading zero, the Q data, and finally a trailing zero bit. In Figures 10 through 12, the leading and trailing zero bits occur before bit 0 and after bit N, respectively.

$$\text{IQCLK Rate} = \frac{\text{CLK}}{\text{IQCLK Frequency}} - 1 \qquad \text{(EQ. 14)}$$



A. SIMULTANEOUS OUTPUT MODE



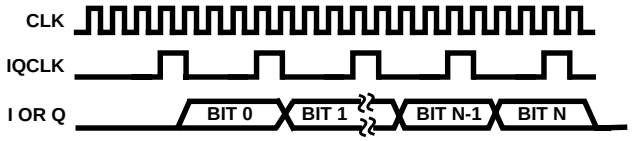
B. I FOLLOWED BY Q OUTPUT MODE

FIGURE 10. DATA OUTPUT MODES

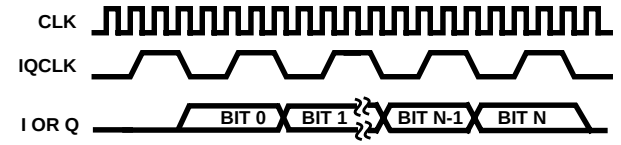
IQCLK is used to delineate the bit or word timing of the I and Q outputs. There are several options on the configuration of IQCLK, which are controlled with Control Word 6 (see Table 8). The frequency of IQCLK is programmed to be a fraction of the CLK frequency, from (CLK rate)/2 to (CLK rate)/8192 (see Equation 14). If IQCLK Rate = 0, then IQCLK remains in its inactive state and the output bits change on the rising edges of CLK.

IQCLK can be programmed to be active continuously, or only during I or Q data output via the IQCLK duration bit. Using the IQCLK Duty Cycle bit, IQCLK is selectable as either 50% duty cycle or to be high for one period of CLK. In addition, the Formatter can be set so that the data bits are clocked on either the positive or negative edges of IQCLK with the IQCLK Polarity bit. Figure 11 shows the various modes of operation with IQCLK Polarity programmed for active high operation.

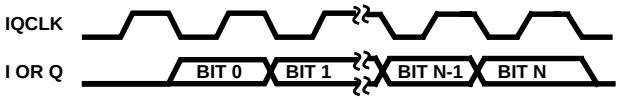
Control Word 6 also configures IQSTB, as shown in Figure 12. When programmed for Active Prior to Data Word, IQSTB is high for one period of IQCLK and terminates simultaneously with the beginning of the first data bit; otherwise it goes active with the beginning of the first bit and inactive with the end of the last bit. IQSTB can be programmed to be either active high or low.



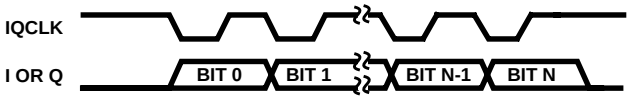
A. IQCLK DUTY CYCLE: ACTIVE TIME = CLK PERIOD (IQCLK POLARITY = 0)



B. IQCLK DUTY CYCLE: 50%

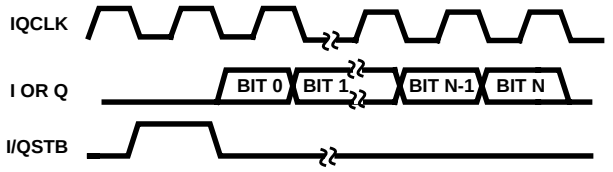


C. IQCLK DURATION: CONTINUOUS

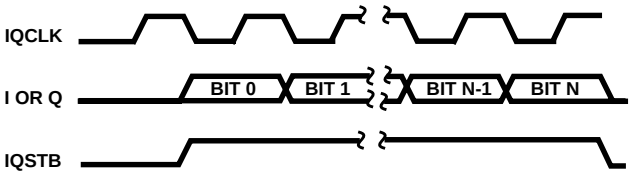


D. IQCLK DURATION: ACTIVE DURING I OR Q ONLY

FIGURE 11. TIMING FOR CLK, IQCLK, IQSTB, I AND Q



A. IQSTB ACTIVE PRIOR TO DATA WORD



B. IQSTB ACTIVE DURING DATA WORD

FIGURE 12. IQSTB TIMING

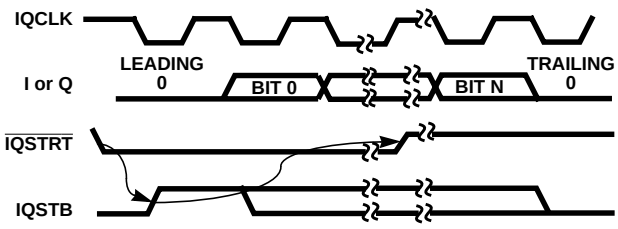


FIGURE 13. REQUESTED DATA OUTPUT TIMING

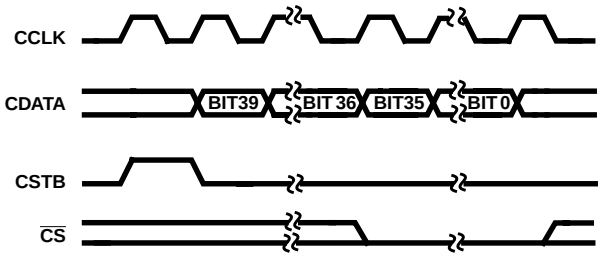


FIGURE 14. CONTROL WORD TIMING DIAGRAM

Data can be read out of the DDC on request through the use of the $\overline{\text{IQSTRT}}$ pin. After passing through the Output Formatter, the I and Q data are stored in output buffers, which are updated at the end of the FIR Filter processing cycle. The $\overline{\text{IQSTRT}}$ and IQSTB lines form a two line handshake as shown in Figure 13. $\overline{\text{IQSTRT}}$ initiates the request. If the buffer has data in it, the DDC will begin an output data sequence on the next edge of IQCLK. The DDC will then put out one bit per IQCLK until the output cycle is complete. In I followed by Q Mode, one $\overline{\text{IQSTRT}}$ will initiate an I output word followed by a Q output word. In real data Output Mode, one IQSTRT will initiate two samples of real data on the I pin.

To avoid the generation of multiple read cycles, IQSTRT must go inactive within 10 cycles of IQCLK after the initiation of IQSTB. The DDC will not update the output buffer again until the current output cycle has completed. When IQSTRT is used in this handshake mode, it must consist of pulses that satisfy the set up and hold requirements listed in the AC Timing Specifications and the pulses must occur at a rate of at least CLK/(HDF Decimation Factor x 4 -1). This mode of operation requires the Time Slot Number in Control Word 6 to be 0.

NOTE: When handshake mode is not used, $\overline{\text{IQSTRT}}$ should be at a logic low.

Auto Three-State Mode for IQCLK, IQSTB, I and Q allows multiple chips to operate using common data and output control lines. Each chip is assigned a Time Slot Number on the bus to use for outputting its data. All outputs programmed for Auto Three-State Mode are active during their time slot and are in a high impedance state at all other times. A time slot starts one CLK period prior to the beginning of the first bit of I or Q and ends (Time Slot Length) CLK periods afterwards. Assignment of a time slot is with reference to the deassertion of $\overline{\text{RESET}}$. The minimum possible Time Slot Length for a given application is:

$$\text{Length}_{MIN} = [(\text{Number of Output Bits} + 2) \times \text{Mode}] + 1; \text{ or} \quad \text{(EQ. 15)}$$

where Mode = 2 if the DDC is in either Real Output or I followed By Q Mode; else Mode = 1.

Note that Equation 15 is useful in all modes for calculating the number of IQCLKs necessary to complete one output data cycle. For a given decimation rate and output word length, the maximum value in the IQCLK Rate field is:

$$IQCLKRate_{MAX} = Floor\left[\frac{(R)\times 4}{Length_{MIN}}\right] - 1; \quad \text{(EQ. 16)}$$

where Floor(X) represents the integer part of X, R is the HDF decimation factor, 4 is the FIR decimation factor.

Example Clock Calculations

Clarification of the use of Equations 14-16, the calculation of the HDF and FIR clocks and the calculation of the IQCLK is best done by example:

The sample clock, CLK, is 10MHz . . . . . CLK = 10MHz
The HDF Decimation Factor, R, is 100 (which makes the decimation counter preload = 99). . . . . R = 100
The Output Mode is I followed by Q . . . . . Mode = 2
Complex output . . . . . FIR Decimation = 4
The desired number of output bits is 32.

1. We begin by identifying the HDF Input Rate:
   HDF Input Rate = CLK = 10MHz . . . . . CLK = 10MHz
2. Next we calculate the HDF Output Rate:
   HDF Output Rate = CLK/R = 10MHz/(100) = 100kHz
   . . . . . .HDF Output Rate = 100kHz
3. Next we calculate the FIR output Rate:
   FIR Output Rate = CLK/4R = 25kHz.
   . . . . . FIR Output Rate = 25kHz
4. Next we calculate the minimum time slot length:
   Equation 15:
   $Length_{MIN}$ = [(Number of Output Bits + 2) x Mode] +1
   where the number of output bits = 32 and the Mode is 2 because of the I followed by Q output selection.
   $Length_{MIN}$ = [(32 + 2) x 2] +1 = 69 IQCLKs
   . . . . . $Length_{MIN}$ = 69 IQCLKs
5. Next we calculate the IQCLK frequency:
   IQCLK frequency = [(F_S)($Length_{MIN}$)/(R)(4)] - 1
   IQCLK frequency = [(10MHz)(69)/(100)(4)] - 1 = 1.725MHz
   The IQCLK frequency can be no slower than 1.725MHz if all of the bits are to be output of the DDC in a time slot.
   . . . . . .Slowest Serial Output Rate = 1.725MHz
6. The Programmed value for the maximum IQCLK Rate, from Equation 16, is:
   $IQCLKRATE_{MAX}$ = Floor[(R) x 4/ $Length_{MIN}$] -1
   $IQCLKRATE_{MAX}$ = Floor[(100 x 4)/69] - 1 = 4
   The IQCLKRATE can be not greater than 4 if all of the bits are to be output of the DDC in a time slot.
   . . . . . Control Word Value for IQCLK Ratemax =

   $[00004]H; 0\ 0000\ 0000\ 0100_{LSB}$
7. Let's sanity check with Equation 14.
   IQCLK Rate = [(CLK/IQCLKfreq)-1] = [10E6/1.725E6] -1 = 4.
   This checks!

Control Word Input

The DDC has eight 40-bit control words which are loaded through the four pin control interface. The format and timing of this interface is compatible with the serial interface timing of most common DSP microprocessors (see Figure 14). The words are shifted MSB first, where bit 39 of the control word is the MSB. Bits 39 through 37 are the control word address, i.e., the target control buffer. $\overline{CS}$ must go low before bit 35 is clocked in. All 40 bits of the control word must be loaded. The formats of the control words are shown in Tables 3 through 10.

The control words are double buffered: each control word is initially loaded into one of eight control buffers for subsequent down loading into the corresponding Control Register. The internal circuitry of the DDC uses the Control Registers to regulate its operation. Control buffers can be downloaded in one of two ways. Loading a Buffer Register with bit 36 = 1 causes all Control Registers to be updated from their respective control buffers when the current word is finished loading. If bit 36 = 0, then only that control buffer is updated and the operation of the DDC is not affected. All Control Registers are updated from their respective buffers on the third rising edge of CLK following the deassertion of RESET. ***NOTE: Control Word 0 is unique in that it is only used to update the seven Control Registers, and it is recognized by the DDC regardless of the state of CS.*** In systems with multiple DDCs, this allows the user to update the configuration of all chips simultaneously without using RESET.

To ensure that the control information is properly loaded, the frequency of CLK must be greater than the frequency of CCLK. In addition, $\overline{RESET}$ must remain inactive during the loading of a control word.

TABLE 3. DESTINATION ADDRESS = 0

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	000 = Control Word 0
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-32	Reserved	All Zeroes

TABLE 4. PHASE GENERATOR/TEST ENABLE/OUTPUT REGISTER

DESTINATION ADDRESS = 1		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	001 = Control Word 1
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-4	Minimum Phase Increment	Bits 35-4 = $2^{31}...2^{0}$. Range: 0 < Minimum Phase Increment < π $(1-2^{-32})$ radians. In the CW mode this is the phase increment of the NCO which is added to the NCO intitial phase offset state. The desired Sin/Cos generator (local oscillator) frequency is set by the equation: **f_C = (phase increment)$f_S 2^{-33}$**; where f_C is the desired local oscillator frequency, f_S is the input sampling frequency, and phase increment is the control word value in hexidecimal. To calculate the value to be programmed into this field, use this equation: **phase increment = INT[f_C / f_S)2^{33}]hex** Some examples of phase increments and local oscillator frequencies: 00000000h: f_C = zero frequency 00000001h: $f_C = f_S / 2^{33}$ - lowest frequency (75MHz x 2^{-33} = 8.73mHz) 10000000h: $f_C = f_S /32$ 20000000h: $f_C = f_S /16$ 40000000h: $f_C = f_S /8$ 80000000h: $f_C = f_S /4$ ffffffffh: $f_C = (0.49999) f_S$ - highest frequency (75MHz x 2^{-33} = 37.49MHz) In the CHIRP modes, this is the smallest allowable phase increment. In the Filter Only mode, this parameter should be set to 0.
3	Test Enable	0 = Test Features Disabled 1 = Test Features Enabled
2-0	Phase Generator Mode	000 = Filter Only 001 = Normal Mode (CW) 010 = Reserved 011 = Up Chirp 100 = Reserved 101 = Down Chirp 110 = Reserved 111 = Up/Down Chirp ***Note that the lsb sets the gain through the DDC as follows:*** ***0 = Gain is1*** ***1 = Gain is 2***

TABLE 5. PHASE GENERATOR REGISTER

DESTINATION ADDRESS = 2		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	010 = Control Word 2
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-32	Reserved	All Zeroes
31-0	Maximum Phase Increment	Bits 31-0 = 2^{31}... 2^{0}. Range: is 0 < Maximum Phase Increment < $\pi(1-2^{-32})$ radians. This parameter is only used in the CHIRP modes, and this is the largest allowable phase increment. Set to 0 in the Filter Only and CW modes.

TABLE 6. PHASE GENERATOR/OUTPUT TIME SLOT REGISTER

DESTINATION ADDRESS = 3		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	011 = Control Word 3
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-32	Reserved	All Zeroes
31-18	Time Slot Length	Time Slot Length in IQCLK Periods; Bits 31-18 = 2^{13}... 2^{0}. Range is (19,25, 33, 37, 39, 49, 65 and 77) The equation for calculating the value for this field is: **TSL = [[(Number of Output Bits + 2)Mode] + 1]Hex**; where mode is 2 if the DDC is in either the real or I followed by Q mode. Mode is 1 for all other DDC operational modes. Allowable Minimum Time Slot Lengths: (18)1 + 1 = 19 (13 hexidecimal) (18)2 + 1 = 37 (25 hexidecimal); Real Output or I followed by Q (24)1 + 1 = 25 (19 hexidecimal) (24)2 + 1 = 49 (31 hexidecimal); Real Output or I followed by Q (32)1 + 1 = 33 (21 hexidecimal) (32)2 + 1 = 65 (41 hexidecimal); Real Output or I followed by Q (38)1 + 1 = 39 (27 hexidecimal) (38)2 + 1 = 77 (4d hexidecimal); Real Output or I followed by Q
17-0	Phase Offset	Starting Phase Angle of Phase Accumulator; Range = 0 to 2π. Bits 17-0 = 2^{32}... 2^{15}. Some example phase offset hexidecimal values : `0000` - 0 `1000` - π/2 `2000` - π `3000` - 3π/2 `3fff` - 2π

TABLE 7. PHASE GENERATION/HDF.OUTPUT REGISTER

DESTINATION ADDRESS = 4		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	100 = Control Word 4
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-33	Reserved	All Zeroes
32-31	Output Spectrum	00 = No Up Conversion,Complex Output 01 = Up Convert by f”/4, Real Output 10 = Up Convert by f”/2,Complex Output 11 = Reserved Mode
30-7	Delta Phase Increment	24-Bit Delta Phase Increment. Bits 30-7 = 2^{23}... 2^{0}. Range: 0 < Delta Phase Increment < π (2^{-8}-2^{-32})
6-1	HDF Data Shift (Shift Factor)	16-Bit HDF Gain Compensation Number - the shift portion. HDF Input Data Shift (Towards LSB). Bits 6-1 = 2^{5}...2^{0}. Range: 0 ≤ Shift Factor ≤ 55 decimal; Range: [0 ≤ Shift Factor ≤ 37]hex Calculate the value for this field using this equation: **HDF Data Shift = [75 - Ceiing(5 $\log_2$(R))]hex** Note: $\log_2(x) = (3.32)\log(x)$
0	Spectral Reverse	0 = Normal Output 1 = Spectrally Reversed Output

TABLE 8. HDF/OUTPUT REGISTER

DESTINATION ADDRESS = 5		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	101 = Control Word 5
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-21	HDF Decimation Counter Preload (HDF DCP)	HDF Decimation Counter Preload. Range: 15 < HDF Decimation Counter Preload < 32,767 Calculate the value for this feild using this equation: **HDF DCP = R - 1;** where R is the HDF decimation (rate change) factor. Common HDF decimation (rate change) factors and associated hexidecimal HDF DCP values: `000f`: R = 16 `00ff`: R = 128 `01ff`: R = 512 `03ff`: R = 1,024 `07ff`: R = 2,048 `0fff`: R = 4,096 `1fff`: R = 8,192 `3fff`: R = 16,384 `7fff`: R = 32,768

TABLE 8. HDF/OUTPUT REGISTER (Continued)

<table>
<tr><th colspan="3">DESTINATION ADDRESS = 5</th></tr>
<tr><th>BIT POSITION</th><th>FUNCTION</th><th>DESCRIPTION</th></tr>
<tr><td>20-5</td><td>Scaling Multiplier Gain (Scale Factor)</td><td>16-Bit HDF Gain Compensation Number - the multiplier portion.
Range: 1 ≤ Scale Factor < 2,
Field Format = $2^{0}.2^{-1}...2^{-15}$.
Calculate the value for this field using this equation:
Scale Factor = $2^{CEILING(5log_2(R))}/(R)^5$; where R is the HDF decimation (rate change) factor and CEILING(x) is equal to x for integer values, otherwise is equal to the next higher integer.
Common HDF decimation factors (R), decimation counter preload (DCP) and Scale Factors (SF) values:
<table><tr><th>R</th><th>DCP(dec)</th><th>DCP(hex)</th><th>SF(dec)</th><th>SF(hex)</th></tr><tr><td>16</td><td>15</td><td>000f</td><td>1.000</td><td>8000</td></tr><tr><td>128</td><td>127</td><td>007f</td><td>1.000</td><td>8000</td></tr><tr><td>512</td><td>511</td><td>01ff</td><td>1.00</td><td>8000</td></tr><tr><td>1,024</td><td>1,023</td><td>03ff</td><td>1.000</td><td>8000</td></tr><tr><td>2,048</td><td>2,047</td><td>07ff</td><td>1.000</td><td>8000</td></tr><tr><td>4,096</td><td>4,095</td><td>0fff</td><td>1.000</td><td>8000</td></tr><tr><td>8,192</td><td>8,191</td><td>1fff</td><td>1.00</td><td>8000</td></tr><tr><td>16,384</td><td>16,382</td><td>3fff</td><td>1.00</td><td>8000</td></tr><tr><td>32,768</td><td>32,768</td><td>7fff</td><td>1.000</td><td>8000</td></tr></table>
Note that the Scale Factor is 1 (8000hex) for power of 2 decimation factors.
The compensation for the HDF gain is performed with a shifter and a multiplier. Thus to program the HDF Gain compensation, there is an associated Shift Factor and the Scale Factor. As the Decimation Factor increases, the multiplier moves away from the value 1 and approaches the value 2. When the calculated value for the multiplier equals or exceeds 2, the shifter is incremented and the multiplier returns to 1 and increases towards 2 again as the Decimation Factor increases.
As an example, the table below details the values of Scale Factor for values of R from 16 to 32:
<table><tr><th>R</th><th>DCP(dec)</th><th>DCP(hex)</th><th>SF(dec)</th><th>SF(hex)</th></tr><tr><td>16</td><td>15</td><td>000f</td><td>1.000000000</td><td>8000</td></tr><tr><td>17</td><td>16</td><td>0010</td><td>1.477013647</td><td>BD0E</td></tr><tr><td>18</td><td>17</td><td>0011</td><td>1.109857915</td><td>8E0F</td></tr><tr><td>19</td><td>18</td><td>0012</td><td>1.693916116</td><td>D8D2</td></tr><tr><td>20</td><td>19</td><td>0013</td><td>1.310720000</td><td>A7C5</td></tr><tr><td>21</td><td>20</td><td>0014</td><td>1.026983417</td><td>8374</td></tr><tr><td>22</td><td>21</td><td>0015</td><td>1.627707993</td><td>D058</td></tr><tr><td>23</td><td>22</td><td>0016</td><td>1.303318981</td><td>A6D3</td></tr><tr><td>24</td><td>23</td><td>0017</td><td>1.053497942</td><td>86D9</td></tr><tr><td>25</td><td>24</td><td>0018</td><td>1.717986918</td><td>DBE6</td></tr><tr><td>26</td><td>25</td><td>0019</td><td>1.412060017</td><td>B4BE</td></tr><tr><td>27</td><td>26</td><td>001a</td><td>1.169233029</td><td>95A9</td></tr><tr><td>28</td><td>27</td><td>001b</td><td>1.949663831</td><td>F98E</td></tr><tr><td>29</td><td>28</td><td>001c</td><td>1.635911864</td><td>D165</td></tr><tr><td>30</td><td>29</td><td>001d</td><td>1.380840823</td><td>B0BF</td></tr><tr><td>31</td><td>30</td><td>001e</td><td>1.172037271</td><td>9605</td></tr><tr><td>32</td><td>31</td><td>001f</td><td>1.000000000</td><td>8000</td></tr></table></td></tr>
<tr><td>4-3</td><td>Output Format</td><td>00 = Two’s Complement
01 = Offset Binary
10 = Sign Magnitude
11 = Single Precision Floating Point Format</td></tr>
</table>

TABLE 8. HDF/OUTPUT REGISTER (Continued)

DESTINATION ADDRESS = 5		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
2-1	Number Of Output Bits	00 = 16 Bits 01 = 24 Bits 10 = 32 Bits 11 = 38 Bits
0	Output Sense	0 = LSB First 1 = MSB First

TABLE 9. INPUT AND OUTPUT FORMAT REGISTER

DESTINATION ADDRESS = 6		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	110 = Control Word 6
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35	I followed by Q	0 = I and Q Output Separately 1 = I and Q Data Output on I Pin
34-29	Time Slot Number	Bits 34-29 = $2^5...2^0$. Range: 0 < Time Slot Number < 63. This implies that 64 different channels may be mutliplexed, assigning one time slot per channel.
28	IQCLK Polarity	0 = Output Data Stable On Rising Edge Of IQCLK; IQCLK High between I or Q Bit Periods when IQCLK Duration = 0. 1 = Output Data Stable on Falling Edge of IQCLK; IQCLK Low between I or Q Bit Periods when IQCLK Duration = 0.
27	IQCLK Duty Cycle	0 = IQCLK Active Time = CLK Period. 1 = 50% Duty Cycle
26	IQCLK Duration	0 = Active During I or Q Output Periods Only 1 = Active Continuously
25-24	IQCLK Three-State Control	00 = Three-State IQCLK 01 = Enable IQCLK 1x = Auto-Three-State Enable IQCLK (during time slot)
23	IQSTB Polarity	0 = Active High 1 = Active Low
22	IQSTB Location	0 = IQSTB Prior to the Beginning of the Data Word. 1 = IQSTB During the Data Word.
21-20	IQSTB Three-State Control	00 = Three-State IQSTB 01 = Enable IQSTB 1x = Auto Three-State Enable IQSTB (during time slot)
19	I Polarity	0 = True Data 1 = Inverted Data
18-17	I Three-State Control	00 = Three-State I 01 = Enable I 1x = Auto Three-State Enable I (during time slot)
16	Q Polarity	0 = True Data 1 = Inverted Data

TABLE 9. INPUT AND OUTPUT FORMAT REGISTER (Continued)

DESTINATION ADDRESS = 6		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
15-14	Q Three-State Control	00 = Three-State Q 01 = Enable Q 1x = Auto Three-State Enable Q (during time slot)
13	Input Format	0 = Offset Binary 1 = Two's Complement
12-0	IQCLK Rate Counter Preload	I/QCLK Rate Counter Preload, Bits 12-0 = $2^{12} \cdots 2^{0}$. Range: 2 ≤ IQCLK Rate Counter Preload ≤ 1701. To calculate the value in this field use this equation: **IQCLK Rate Counter Preload = [FLOOR[(HDF Decimation Factor x 4)/TSL] - 1]hex**; where FLOOR(x) represents the integer part of x, and TSL is the decimal value of Control Word 3, bit 31-18.

TABLE 10. PHASE OFFSET REGISTER

DESTINATION ADDRESS = 7		
BIT POSITION	**FUNCTION**	**DESCRIPTION**
39-37	Address	111 = Control Word 7
36	Update	0 = Update Only This Control Register 1 = Update All Control Registers
35-14	Reserved	All Zeroes
13	Data	0 = Normal Data Input 1 = Force Input Data to 8000 Hex.
12-11	FIR Accumulator Control	00 = Normal Accumulation - The accumulator is reset on every FIR cycle. 01 = No Accumulation -The accumulator is disabled. 10 = Continuous Accumulation -The accumulator is not reset on every FIR cycle. This test mode was created to allow the user to perform the equivilent of a check sum test. A very long term test could be run and an accumulated output would yeild a specific numeric value. If the answer differed, the part is not functioning properly. 11 = Reserved
10	Q Strobe on Roll Over	0 = Q carries Normal Data 1 = Q Strobes When Phase Generator Rolls Over
9	Force Outputs	0 = Normal Output Response 1 = Force Outputs
8	IQCLK Forced Data	If Bit 9 = 1, Force IQCLK = Bit 8; Else Normal
7	IQSTB Forced Data	If Bit 9 = 1, Force IQSTB = Bit 7; Else Normal.
6	I Forced Data	If Bit 9 = 1, Force I = Bit 6; Else Normal.
5	Q Forced Data	If Bit 9 = 1, Force Q = Bit 5; Else Normal.
4	Sin/Cos Generator Bypass	0 = Sin Cos Generator Normal, 1 = Bypass Sin Cos Generator; Sin = Cos = 0.fffff (approximately 1)
3	Scaling Multiplier Bypass	0 = Scaling Multiplier Normal, 1 = Scale Factor = 1.
2	Reserved	Must be Zero for Proper Operation while Test Features are Enabled.
1	Wait For RAM Full	If Bit = 0, DDC will Output Data Normally after a Reset, which will Include Unpredictable Data in Data RAMs. If Bit = 1, No Chip Output will Occur until Sufficient Data RAM Locations are Written.
0	Disable Overflow Protection	0 = Normal Operation 1 = Disable Overflow Protection

HSP50016 supports two types of testing. Control Word 7 can be used to verify the operation of the circuit through the divide and conquer method. Setting the Enable Test Bit (Control Word 1, Bit 3) equal to a 1 enables the test features controlled by Control Word 7. (This bit is in Control Word 1 so that Word 7 does not have to be loaded if the test features are not being used.) The functions allowed by Control Word 7 are shown in Table 10.

NOTE: Asserting bits 9 and 13 of Control Word 7 will put all outputs to a static mode. This may remove strobe enables or clocks used to read the data signals. This Test Mode was intended for interface evaluation at the board level.

The DDC also has a Test Access Port (TAP). This port is fully conformant to IEEE Std. 1149.1 - 1990 - IEEE Standard Test Access Port and Boundary-Scan [2]. The TAP supports the following instructions: BYPASS, SAMPLE/PRELOAD, INTEST, EXTEST, RUNBIST and IDCODE. In addition, there are seven instructions called RDCNTLWD1-7, which read the contents of the control words over the TAP. The address bits and bit 36 are only used to determine the destination of data during loading; they are not stored, so they are not read out with the RDCNTLWD1-7 instruction.

Summary

To use the DDC in a down conversion application three items must be considered and designed to compliance. Solutions must satisfy all three items.

1. The Nyquist Sampling Rate for the bandwidth of interest $F_S \geq 2BW$, where BW is the bandwidth of interest.
2. The composite FIR/HDF double sided bandwidth, $BW_{-3dB} = 0.1375F_S/R$.
3. The desired serial output clock rate (total decimation, plus parallel to serial conversion rate increase).

$$\text{IQCLK Frequency} = \left[\frac{f_S \ \text{Length}_{MIN}}{(R_{FIR})\ (R)}\right] - 1$$

NOTE: R_{FIR} = 2 for real mode, 4 for all other modes.

Applications

Down Conversion

The primary spectral operation in the DDC is down conversion of an input signal to base band, see Figure 15. This process is done in two steps: multiplication of the input waveform by an internally generated quadrature sinusoid, i.e., modulation and lowpass filtering to attenuate the unwanted spectral components. The unwanted spectral components have two sources, the input signal and an artifact of the modulation process.

The modulation process can be written as:

$$u(n) = x(n)e^{-j\omega}c = x(n)[\cos(\omega_c) - j\sin(\omega_c)] \quad \text{(EQ. 17)}$$

Where x(n) is the real input data sequence, $\omega = 2\pi f$, and ω_c is the frequency of the signal generated by the SIN/COS Generator.

For demonstration purposes let $x(n) = \cos(\omega_k n)$. The multiplication then becomes:

$$\begin{aligned} u(n) &= \cos(\omega_k n)[\cos(\omega_c n) - j\sin(\omega_c n)] \\ &= 1/2[\cos((\omega_k - \omega_c)n) + \cos((\omega_k + \omega_c)n) \\ &\quad - j(\sin((\omega_k + \omega_c)n) - \sin((\omega_k - \omega_c)n))] \end{aligned} \quad \text{(EQ. 18)}$$

The signal u(n) is passed through a low pass filter; assuming that the filter passes the low frequency terms with no degradation and attenuates the high frequency terms completely, the filtering operation produces the output:

$$\begin{aligned} v(n) &= 1/2(\cos((\omega_k - \omega_c)n) + j\sin((\omega_k - \omega_c)n)) \\ &= 1/2e^{j(\omega_k - \omega_c)n} \end{aligned} \quad \text{(EQ. 19)}$$

When the magnitude of the input signal x(n) is one, the magnitude of v(n) is 1/2. Both the I and Q channels are multiplied by a factor of two to yield:

$$\begin{aligned} w(n) &= \cos((\omega_k - \omega_c)n) + j\sin((\omega_k - \omega_c)n) \\ &= e^{j(\omega_k - \omega_c)n}. \end{aligned} \quad \text{(EQ. 20)}$$

Figure 16 shows an HSP50016 in a single channel down conversion circuit. Notice that the input data is only 12 bits, so it is justified to the MSB of the DDC's input data. If a smaller sample width is used, it is recommended that the MSB of the data is input into DATA15. The unused bits are connected to ground. This alignment makes it easier to locate the position of the MSB in the output data. Note that the input is configured for offset binary arithmetic and the output is set up for I followed by Q, which enables the use of only one serial connection to the output processor. The serial data clock of the processor and the Control Clock of the DDC are driven by a TTL compatible oscillator. (IQCLK cannot be used for this purpose since its frequency is indeterminate until the DDC has been configured). Note that many processors provide a bit clock which eliminates the need for the external oscillator.

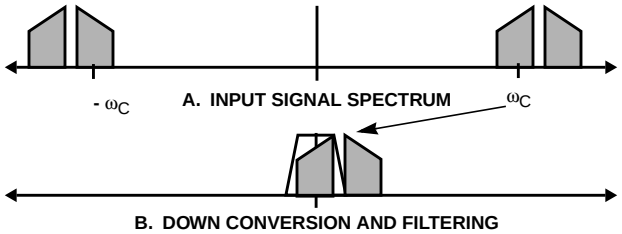


FIGURE 15. DOWN CONVERSION

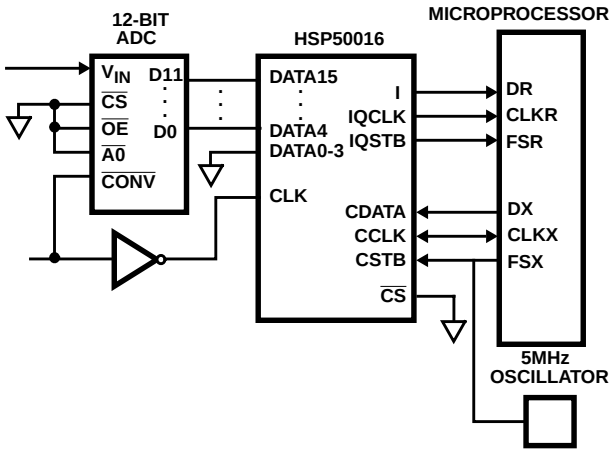


FIGURE 16. CIRCUIT FOR SINGLE CHANNEL OPERATION

An example of the control word contents for this mode of operation is given in Tables 11 through 17. In this setup, the DDC has been configured for a constant down conversion frequency, decimation by 64 and Test Features disabled. Bit fields of three bits or less are in binary notation; longer fields are in hexadecimal. Control Words Zero and Seven are not used.

TABLE 11. SAMPLE FORMAT FOR CONTROL WORD 1 - PHASE GENERATOR/TEST ENABLE

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	001 = Control Word 1.
36	Update	1 = Control Register Update.
35-4	Minimum Phase Increment	Minimum Phase Increment Computed according to $[f_C/f_S]\ 2^{33}$.
3	Test Enable	0 = Test Features Disabled.
2-0	Phase Generator Mode	001 = Normal Mode.

0011 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX 0001

TABLE 12. SAMPLE FORMAT FOR CONTROL WORD 2 - PHASE GENERATOR

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	010 = Control Word 2.
36	Update	1 = Control Register Update.
35-32	Reserved	All Zeroes.
31-0	Maximum Phase Increment	All Zeroes.

0101 0000 0000 0000 0000 0000 0000 0000 0000 0000

TABLE 13. SAMPLE FORMAT FOR CONTROL WORD 3 - PHASE GENERATOR/OUTPUT TIME SLOT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	011 = Control Word 3.
36	Update	1 = Control Register Update.
35-32	Reserved	All Zeroes.
31-18	Time Slot Length	All Zeroes.
17-0	Phase Offset	All Zeroes.

0111 0000 0000 0000 0000 0000 0000 0000 0000 0000

TABLE 14. SAMPLE FORMAT FOR CONTROL WORD 4 - PHASE GENERATOR/HDF/OUTPUT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	100 = Control Word 4.
36	Update	1 = Control Register Update.
35-33	Reserved	All Zeroes.
32	Up Convert	0 = Do Not Up convert.
31	Real Mode	0 = Complex Mode.
30-7	Delta Phase Increment	All Zeroes.
6-1	Shift	37 = Decimal 55, the Shift Corresponding to HDF Decimation by 16.
0	Spectral Reverse	0 = No Spectral Reversal

1001 0000 0000 0000 0000 0000 0000 0000 0110 1110

TABLE 15. SAMPLE FORMAT FOR CONTROL WORD 5 HDF/OUTPUT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	101 = Control Word 5.
36	Update	1 = Control Register Update.
35-21	HDF Decimation Counter Preload	F = Decimation by 16 in HDF.
20-5	Scaling Multiplier Gain	8000 = Scaling Multiplier Gain of 1.
4-3	Output Format	00 = Two's Complement.
2-1	Number of Output Bits	00 = 16-Bits.
0	Output Sense	1 = MSB First.

1011 0000 0000 0001 1111 0000 0000 0000 0000 0000

TABLE 16. SAMPLE FORMAT FOR CONTROL WORD 6 - OUTPUT

BIT POSITION	FUNCTION	DESCRIPTION
39-37	Address	110 = Control Word 6.
36	Update	1 = Control Register Update.
35	I followed by Q	1 = I and Q Data Output on I Pin.
34-29	Time Slot	Time Slot Number = 0.
28	IQCLK Polarity	0 = Data Stable on Rising Edge of IQCLK.
27	IQCLK Duty Cycle	1 = IQCLK Duty Cycle is 50%.
26	IQCLK Duration	1 = Active Continuously.
25-24	IQCLK Three-State Control	01 = Enable IQCLK.
23	IQSTB Polarity	0 = IQSTB Active High.
22	IQSTB Location	0 = IQSTB Active Prior to the Beginning of the Data Word.
21-20	IQSTB Three-State	01 = Enable IQSTB.
19	I Polarity	0 = I Output Active High.
18-17	I Three-State Control	01 = Enable I.
16	Q Polarity	0 = Q Output Active High.
15-14	Q Three-State Control	00 = Disable Q.
13	Input Format	1 = Two's complement.
12-0	IQCLK Rate	All Zeroes = CLK Used to Clock Output Bits.

1101 1000 0000 1101 0001 0010 001X XXXX XXXX XXXX

TABLE 17. SUMMARY OF CONTROL WORDS FOR THE EXAMPLE

CONTROL WORD	HEX VALUE
0	0 0 0 0 0 0 0 0 0 0
1	3 X X X X X X X X 1
2	5 0 0 0 0 0 0 0 0 0
3	7 0 0 0 0 0 0 0 0 0
4	9 0 0 0 0 0 0 0 6 E
5	B 0 0 1 F 0 0 0 0 0
6	D 8 0 D 1 2 X X X X
7	0 0 0 0 0 0 0 0 0 0

Quadrature To Real Conversion

After the input data has been processed by the DDC, the output can be converted into a real signal if desired. In that case, the baseband centered quadrature signal is upcobaseband. The real part of the upconverted signal is taken as the output. To satisfy the Nyquist criteria, the sample rate of the resulting signal must be at least twice the minimum sample rate of the I and Q components of the quadrature signal. This prevents one sideband from aliasing onto the other sideband when the real part of the output signal is taken.

The spectrum of a quadrature signal which has been over sampled by 2 is shown in Figure 17A. This represents the output of the filters. As described in the previous paragraph, the oversampling is a necessary feature of this process, since the final signal will occupy twice the bandwidth of the filter output. To prevent aliasing upon taking the real part of the signal, it is necessary to perform an up conversion by f"/4, where f" is the decimated sample frequency. (Note that f_S is defined as the input sampling frequency, f' is the input sampling frequency divided by the HDF decimation rate R, and f" is f' divided by the FIR decimation rate. f" is the FIR output sampling rate). The up conversion function is:

$$e^{j2\pi nf"/4f"} = e^{j\pi n/2} \quad \text{(EQ. 21)}$$

For n = 0, 1, 2, 3, 4,... the output values of the local oscillator in rectangular representation are: 1 + 0j, 0 + j, -1 + 0j, 0 - j, 1 + 0j,.... Since the real half of the complex multiplication of the local oscillator values by the filtered signal values (the desired output is the real part of the product) require only trivial operations, this up conversion is done in the Formatter. Figure 17B shows the signal spectrum after up conversion. Figure 17C shows the spectrum of the real output signal.

Continuing with the single tone example from the previous section, the quadrature signal output from the FIR filters is:

$$w(n) = \cos((\omega_k - \omega_c)n) + j\sin((\omega_k - \omega_c)n) = e^{j(\omega_k - \omega_c)n} \quad \text{(EQ. 22)}$$

Multiplying w(n) by the up convert function and summing the result is equivalent to the output sequence:

$$\begin{aligned} &y(n) = 1 \times \cos((\omega_k - \omega_c)n), \\ &y(n+1) = j \times j\sin((\omega_k - \omega_c)(n+1)), \\ &y(n+2) = -1 \times \cos((\omega_k - \omega_c)(n+2)), \\ &y(n+3) = -j \times j\sin((\omega_k - \omega_c)(n+3)), \\ &y(n+4) = 1 \times \cos((\omega_k - \omega_c)(n+4)),... \end{aligned} \quad \text{(EQ. 23)}$$

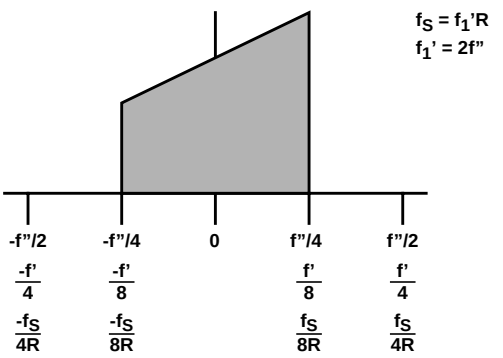
$$y = \cos((\omega_k - \omega_c)n), -\sin((\omega_k - \omega_c)(n+1)), -\cos((\omega_k - \omega_c)(n+2)), \sin((\omega_k - \omega_c)(n+3)), \cos((\omega_k - \omega_c)(n+4)),...$$

Or:

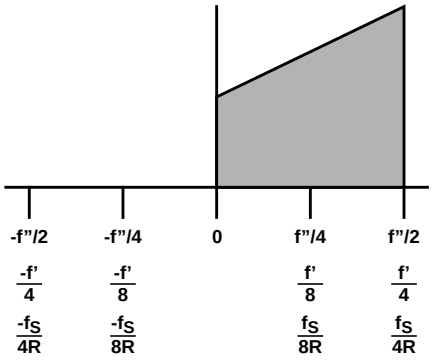
$$y = RE(w(n)), - IM(w(n+1)), - RE(w(n+2)), IM(w(n+3)), RE(w(n+4)),...$$

Since $|e^{j\pi n/2}| = 1$ and $|w(n)| = 1$, no further magnitude corrections are required.

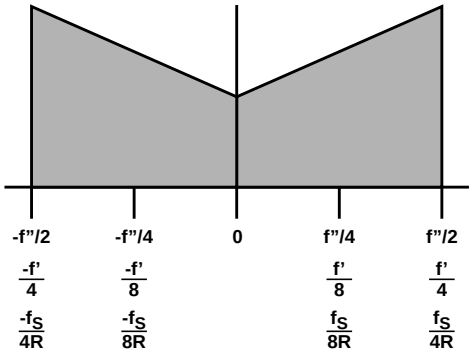
The setup for this application is similar to that of the down conversion circuit given above, except the Output Formatter is set for Real Mode (Bit 31 in Control Word 4). This bit configures the part for up conversion by f"/4 and summing of the real and imaginary parts of the filter output.



A. OUTPUT OF FIR FILTERS: SIGNAL OVERSAMPLED BY 2



B. FIRST OPERATION IN FORMATTER: UP CONVERT BY SAMPLE FREQUENCY / 4



C. SECOND OPERATION IN FORMATTER: I OUTPUT = I + Q

FIGURE 17. QUADRATURE TO REAL CONVERSION OF AN OUTPUT SIGNAL

Up Conversion by f"/2

This operation allows the user to exchange the positions of the upper and lower halves of a down converted signal while leaving each half unchanged. Quadrature up conversion by f"/2 is performed by multiplying the output signal by $e^{j2\pi nf"/2} = \cos(2pnf"/2) + j \sin(2pnf"/2)$. When sampled at a rate of f", cos(2pnf"/2) takes on the values 1, -1, 1, -1,... and sin(2pnf"/2) always = 0. Thus, the up convert LO sequence is:

$$e^{j\pi n} = 1 + j0, -1 + j0, 1 + j0, \ldots \quad \text{(EQ. 24)}$$

This sequence is multiplied by the output of the I and Q branches of the filter:

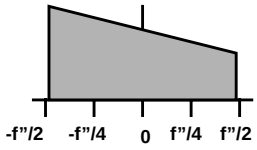
$$w(n) = \cos((\omega_k - \omega_c)n) + j\sin((\omega_k - \omega_c)n) = e^{j(\omega_k - \omega_c)n}, \quad \text{(EQ. 25)}$$

yielding an output sequence:

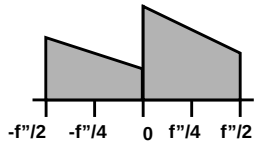
$$y = (RE(w(n)), IM(w(n))), \quad \text{(EQ. 26)}$$
$$-RE(w(n+1)), - IM(w(n+1))),$$
$$RE(w(n+2)), IM(w(n+2))), \ldots$$

The Formatter contains the circuitry to shift the quadrature output spectrum up by one half of the output sample frequency f". This operation is independent of the function of the Phase Generator and Mixer. The spectra of the outputs of the Filter and Formatter are shown in Figure 18.

The setup is identical to the down conversion configuration, except that the Up Convert Bit is set in Control Word 4.



A. OUTPUT OF FIR FILTERS



B. FILTER OUTPUT UP CONVERTED BY OUTPUT SAMPLE FREQUENCY / 2

FIGURE 18. UP CONVERSION BY F" / 2

Quadrature Spectral Reversal

Spectral reversal is often used to negate a spectral reversal which has occurred due to a previous operation in the processing chain. Examples of this are spectral reversal in an analog down conversion or in a constructive aliasing operation. The DDC gives the user the ability to convert the signal to baseband in either forward or reverse fashion. Quadrature spectral reversal is achieved by translating the lower sideband of the input to baseband rather than the upper sideband. This is implemented in the DDC by mixing the input signal with $e^{j2\pi f_c n}$ - that is, up converting the input rather than down converting it. The resulting signal is:

$$u(n)= x(n)e^{j2\pi f_c n} = x(n)[\cos(\omega_c n) + j\sin(\omega_c n)] \quad \text{(EQ. 27)}$$

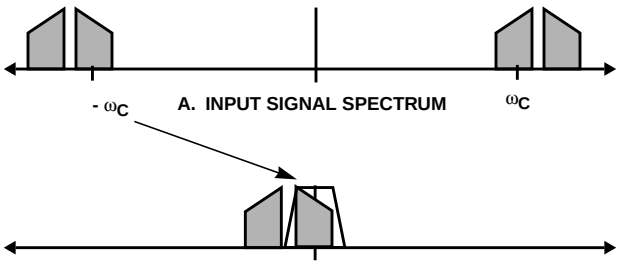
Assuming $x(n) = \cos(\omega_k n)$,

$$\begin{aligned} u(n) &= \cos(\omega_k n)[\cos(\omega_c n) + j\sin(\omega_c n)] \quad \text{(EQ. 28)} \\ &= [\cos((\omega_k - \omega_c)n) + \cos((\omega_k + \omega_c)n) \\ &\quad + j(\sin((\omega_k + \omega_c)n) - \sin((\omega_k - \omega_c)n))] \end{aligned}$$

After quadrature filtering and correcting for the gain of 1/2, we have:

$$\begin{aligned} w(n) &= \cos((\omega_k - \omega_c)n) - j\sin((\omega_k - \omega_c)n) \quad \text{(EQ. 29)} \\ &= \cos(-(\omega_k - \omega_c)n) + j\sin(-(\omega_k - \omega_c)n) \\ &= \cos((\omega_c - \omega_k)n) + j\sin((\omega_c - \omega_k)n) \\ &= e^{j(\omega_c - \omega_k)n} \end{aligned}$$

The appropriate spectral plots are shown in Figure 19. In up conversion, the sine output of the SIN/COS Generator is negated so that the vector output of the Local Oscillator rotates counter clockwise. This is implemented by setting the Spectral Reverse bit in Control Word 4 to a one. Otherwise, the setup for this mode is the same as the one for down conversion.

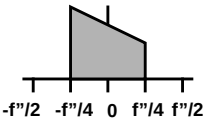


B. UP CONVERSION AND FILTERING

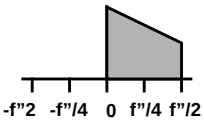
FIGURE 19. UP CONVERSION OF FILTER OUTPUT SIGNAL

Real Spectral Reversal

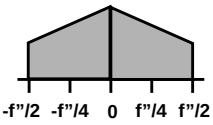
Real spectral reversal is simply quadrature spectral reversal with quadrature to real conversion in the Formatter. The up converted and filtered signal w(n) is upconverted again by f”/4 in the Formatter. Each sideband of the result is spectrally reversed from the sidebands that would have been produced by down conversion with quadrature to real conversion. The output spectrum is shown in Figure 20.



A. OUTPUT OF FILTERS: SIGNAL OVERSAMPLED BY 2



B. FIRST OPERATION IN FORMATTER: UP CONVERT BY SAMPLE FREQUENCY / 4



C. SECOND OPERATION IN FORMATTER: I OUTPUT = I + Q

FIGURE 20. QUADRATURE TO REAL CONVERSION OF AN OUTPUT SIGNAL

The setup for this application is similar to that of down conversion, except in Control Word 4, where the Spectral Reverse and Real Output bits are set to one.

High Decimation Filter Only

The DDC can be operated as a single high decimation filter. This is done by setting the Phase Generator to Filter Only and the Minimum Phase Increment and Phase Offset to 0. This multiplies the incoming data stream by a constant hexadecimal 3FFFF in the I channel and 0 in the Q channel. The HDF Section of the circuit requires a minimum decimation rate of 16 to allow sufficient time for the FIR to compute its response. This mode of operation implements a filter which has a decimation rate from 64 to 131,072. The frequency response is shown in Figures 7, 8 and 9. Only the I output has valid data in this mode; the Q output should be set to high impedance state to reduce circuit noise.

Multichannel Operation

Several DDCs can be placed in parallel with each one operating on a different frequency band. To minimize wiring, their outputs can be configured so that they are connected over a common serial bus. Each DDC is assigned a time slot number (Control Word 6) and a time slot length (Control Word 3). Each DDC in turn controls the bus for long enough to output its data, then relinquishes the bus. The time slot assignment and length are programmed at configuration time. Up to 64 chips can be multiplexed in this manner.

Figure 21 shows a Block Diagram of this configuration. The DDCs are configured by the microprocessor by first writing a logical 0 to its Chip Select line. The control words are written to that part in any order. When the part has been configured, $\overline{CS}$ is written high again, and the next part is configured in the same manner. Collisions are prevented by programming each DDC with a unique Time Slot number, which holds its output from 0 to 63 output word times before transmission. Each part also has a Time Slot Length, whose minimum value is given in Equation 8. Note that a value greater than the minimum can be used to give the processor time to operate on the data

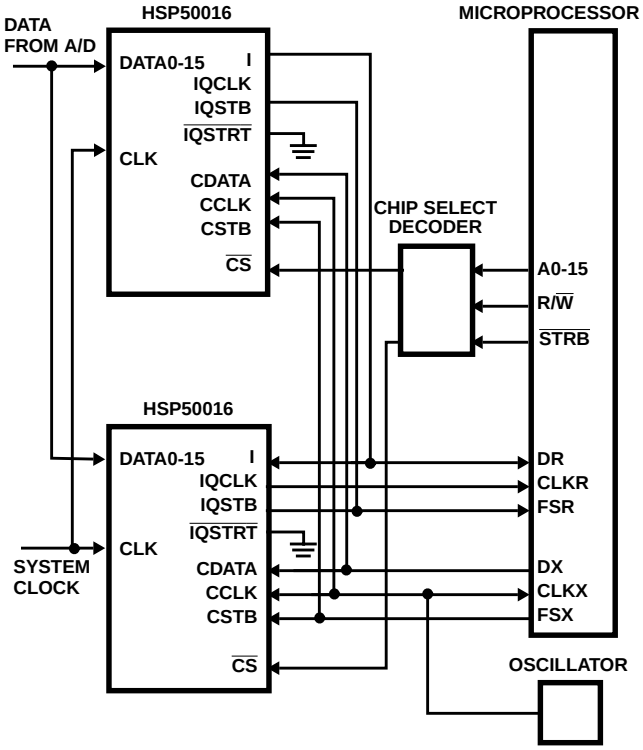


FIGURE 21. CIRCUIT FOR MULTIPLE CHANNEL OPERATION (AUTO THREE-STATE)

The corresponding Configuration Register setup is similar to that of single channel down conversion, except for the Auto Three-State fields. In this example, the first DDC in the chain is set to drive IQCLK; the others have this output set for high impedance. (It makes no difference which DDC is chosen to be the one to drive IQCLK, but it must be active continuously). The unused outputs are put in their high impedance condition on the other DDCs to minimize power consumption. Note also that this example shows all DDCs in I followed by Q Mode so that only one data line to the microprocessor is necessary. Figure 22 gives the timing of the output data.

When operating a set of HSP50016s in the Multiple Channel Operation Mode, the two control signals that ensure proper time slot operation are: $\overline{CS}$ and $\overline{RESET}$. The $\overline{CS}$ allows unique Control Word loading of each DDC. The $\overline{RESET}$ synchronizes all of the DDC's to the start of the first time slot.

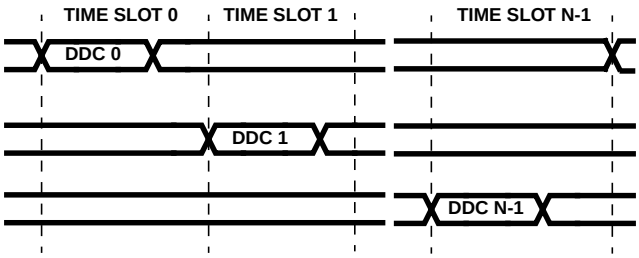


FIGURE 22. TIMING FOR MULTIPLE CHANNEL OPERATION (AUTO THREE-STATE)

NOTE: In this mode, it was anticipated that parallel DDC's would be programmed identically, except for the NCO (L.O.) frequency and Time Slot Number. This implies identical HDF Decimation factors, Time Slot Length's, Number of Output Bits, Output Mode are identical in all DDCs. This means that the output rate of all DDC HDFs, FIRs and Parallel to Serial Converters are identical.

The DDC keeps an internal count of the number of IQCLK periods that have transpired since the rising edge of $\overline{RESET}$. The internal counter of each DDC is set to enable the serial output at the time slot number assigned to that DDC. The count is based on the time slot length, number of output bits, HDF decimation, and Output Mode programmed to that part.

NOTE: In the Multiple Channel Operation Mode, all the time slot lengths should be set to the same value to avoid output signal contention. The time slot length should be equal to the largest "minimum time slot length" as calculated by Equation 15, for every DDC in the multichannel arrangement. Note that Equation 8 is in IQCLK periods, not CLK periods. Equations 7 and 9 will be helpful in making the translation to CLK periods.

This mode does not require that all of the time slots be used (assigned to a DDC). If only two parts were used and the maximum time signal isolation was desired, one could assign the first signal time slot 31 and the second signal time slot 63. This would ensure that the maximum separation in time occurred. It is the designers responsibility to ensure that the output rate, including the decimation is consistent with the time allotted to output each signal.

Let's return to the clock calculation example found in the Output Formatter, and add the requirement of 4 time slots. The calculations in the Example Clock Calculation Section remain true, but step 8 must be added:

8. Now lets consider the multichannel timing. Each channel must output the data at no less than 1.725MHz to get all the I/Q data out in the allocated time for the assigned time slot. Time margin is created when the output is clocked out at a higher rate. Because each channel is outputting data in only one of four channels, the effective output rate for each channel is 1.725MHz /4 = 431.25kHz, even though the part is outputting data 1.7MHz in every time slot. . . . . Effective Channel Output Rate = 431.25kHz

Alternatively, the processor can request data from each of the DDCs asynchronously. In this setup, Requested Output Mode is used. The Data Concentrator polls each channel individually and is responsible for ensuring that each channel is polled before the output data is lost. The Data Concentrator is a custom circuit designed by the user. A Block Diagram of such a system is shown in Figure 23. The interface between the controller and the DDCs has been omitted for the sake of clarity.

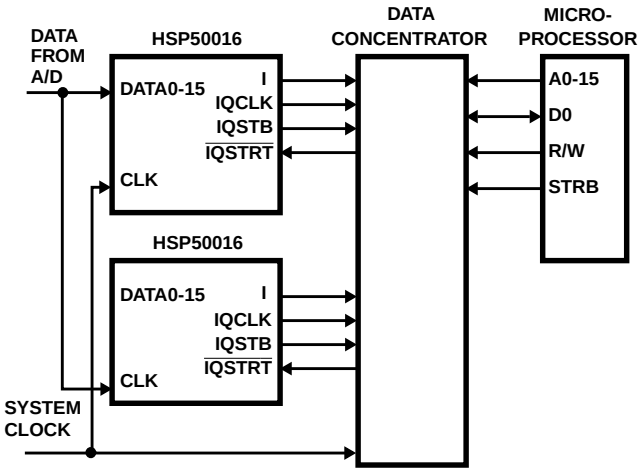


FIGURE 23. CIRCUIT FOR MULTIPLE CHANNEL OPERATION (REQUESTED OUTPUT)

References

[1] Hogenauer, Eugene V., An Economical Class of Digital Filters for Decimation and Interpolation, IEEE Transactions on Acoustics, Speech and Signal Processing, April 1981.

[2] IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1 - 1990.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.75V to +5.25V
Operating Temperature Range . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CPGA Package	45	7
PLCC Package	35	N/A

Maximum Junction Temperature
CPGA Package . . . . . 150^oC
PLCC Package . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Die Characteristics

Gate Count . . . . . 65,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 5.0V ±5%, T_A = 0^o to 70^oC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Power Supply Current	I_{CCOP}	V_{CC} = Max, CLK Frequency 52.6MHz Notes 2, 3	-	394	mA
		V_{CC} = Max, CLK Frequency 76.9MHz Notes 2, 3	-	577	mA
Standby Power Supply Current	I_{CCSB}	V_{CC} = Max, Outputs Not Loaded	-	500	µA
Input Leakage Current	I_I	V_{CC} = Max, Input = 0V or V_{CC} TMS, TDI, $\overline{TRST}$	-500	10	µA
		V_{CC} = Max, Input = 0V or V_{CC} All other inputs	-10	10	µA
Output Leakage Current	I_O	V_{CC} = Max, Input = 0V or V_{CC}	-10	10	µA
Logical One Input Voltage	V_{IH}	V_{CC} = Max	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = Min	-	0.8	V
Logical One Input Voltage: CLK, $\overline{TRST}$	V_{IHC}	V_{CC} = Max	3.0	-	V
Logical One Output Voltage	V_{OH}	I_{OH} = -5mA, V_{CC} = Min	2.6	-	V
Logical Zero Output Voltage	V_{OL}	I_{OL} = 5mA, V_{CC} = Min	-	0.4	V
Input Capacitance	C_{IN}	CLK Frequency 1MHz All measurements referenced to GND. T_A = 25^oC, Note 4	-	10	pF
Output Capacitance	C_{OUT}		-	10	pF

NOTES:

2. Power supply current is proportional to frequency. Typical rating is 7.5mA/MHz. Note that operation at maximum clock frequency will exceed maximum junction temperature of device. Use of a heat sink and/or air flow is required under these conditions: Recommended heat sink is EG&G Wakefield D10650-40.
3. Output load per test circuit and C_L = 40pF.
4. Not tested, but characterized at initial design and at major process/design changes.

AC Electrical Specifications

V_{CC} = 5.0V ±5%, T_A = 0^o to 70^oC, (Note 5)

PARAMETER	SYMBOL	NOTES	-52(52.6)MHz		-75(76.9)MHz		UNITS
			MIN	MAX	MIN	MAX	
CLK Period	t_{CP}		19	-	13	-	ns
CLK High	t_{CH}		7	-	5	-	ns
CLK Low	t_{CL}		7	-	5	-	ns
Setup Time DATA0-15 to CLK	t_{DS}		10	-	7	-	ns
Hold Time DATA0-15 from CLK	t_{DH}		1	-	1	-	ns
$\overline{RESET}$ Pulse Width	t_{RL}		t_{CP}+11	-	t_{CP}+8	-	ns

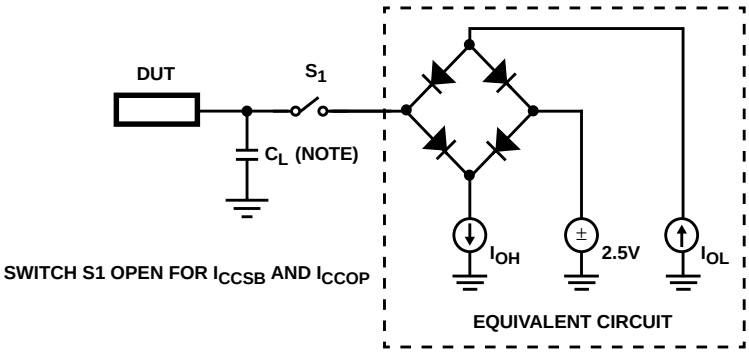
AC Electrical Specifications V_{CC} = 5.0V ±5%, T_A = 0^o to 70^oC, (Note 5) **(Continued)**

PARAMETER	SYMBOL	NOTES	-52(52.6)MHz		-75(76.9)MHz		UNITS
			MIN	MAX	MIN	MAX	
$\overline{RESET}$, $\overline{IQSTRT}$ Setup Time from CLK	t_{RS}	Note 6	10	-	7	-	ns
RESET, $\overline{IQSTRT}$ Hold Time to CLK	t_{RH}	Note 6	1	-	1	-	ns
CLK to I, Q, IQSTB, IQCLK Delay	t_{DO}		-	15	-	12	ns
CCLK Period	t_{CCP}		100	-	100	-	ns
CCLK High	t_{CCH}		40	-	40	-	ns
CCLK Low	t_{CCL}		40	-	40	-	ns
CDATA, CSTB, $\overline{CS}$ Setup to CCLK	t_{CDS}		30	-	30	-	ns
CDATA, CSTB, $\overline{CS}$ Hold from CCLK	t_{CDH}		30	-	30	-	ns
CCLK Low Setup to CLK	t_{CLS}	Notes 6, 7	30	-	30	-	ns
CCLK High Hold from CLK	t_{CHH}	Notes 6, 7, 10	30	-	30	-	ns
TCK Period	t_{TCP}	Note 8	100	-	100	-	ns
TCK High	t_{TH}		40	-	40	-	ns
TCK Low	t_{TL}		40	-	40	-	ns
$\overline{TRST}$ Pulse Width	t_{TRL}		100	-	100	-	ns
TCK to TDO, Data Delay	t_{TDO}		-	30	-	30	ns
Setup Time On All Inputs to TCK	t_{ATS}	Note 9	30	-	30	-	ns
Hold Time On All Inputs from TCK	t_{ATH}	Note 9	30	-	30	-	ns
TCK Setup Time to CLK	t_{TCS}	Note 8	30	-	30	-	ns
TCK Hold Time from CLK	t_{TCH}	Note 8	30	-	30	-	ns
Output Enable Time from CLK	t_{OE}	Note 10	-	18	-	12	ns
Output Disable Time from CLK	t_{OD}	Note 10	-	18	-	12	ns
Output Enable Time from TCK	t_{TOE}	Note 10	-	32	-	32	ns
Output Disable Time from TCK	t_{TOD}	Note 10	-	32	-	32	ns
Output Rise, Fall Time	t_{RF}	Note 10	-	5	-	5	ns

NOTES:

5. AC tests performed with C_L= 40pF, I_{OL} = 5mA, and I_{OH} = -5mA. Input reference level for CLK, $\overline{TRST}$ is 2.0V, all other inputs 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V; V_{OH} = V_{OL} = 2.5V.
6. These are asynchronous inputs; setup and hold times must only be maintained in order to predict which clock cycle they take effect internally.
7. Timing must only be maintained when Update bit is active in control word data being loaded.
8. Special Timing relationship between TCK and CLK is required for Test Instructions RUNBIST, EXTEST and INTEST.
9. All inputs except $\overline{TRST}$, and only when TCK is driving internal clock.
10. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.

AC Test Load Circuit



NOTE: Test head capacitance.

Waveforms

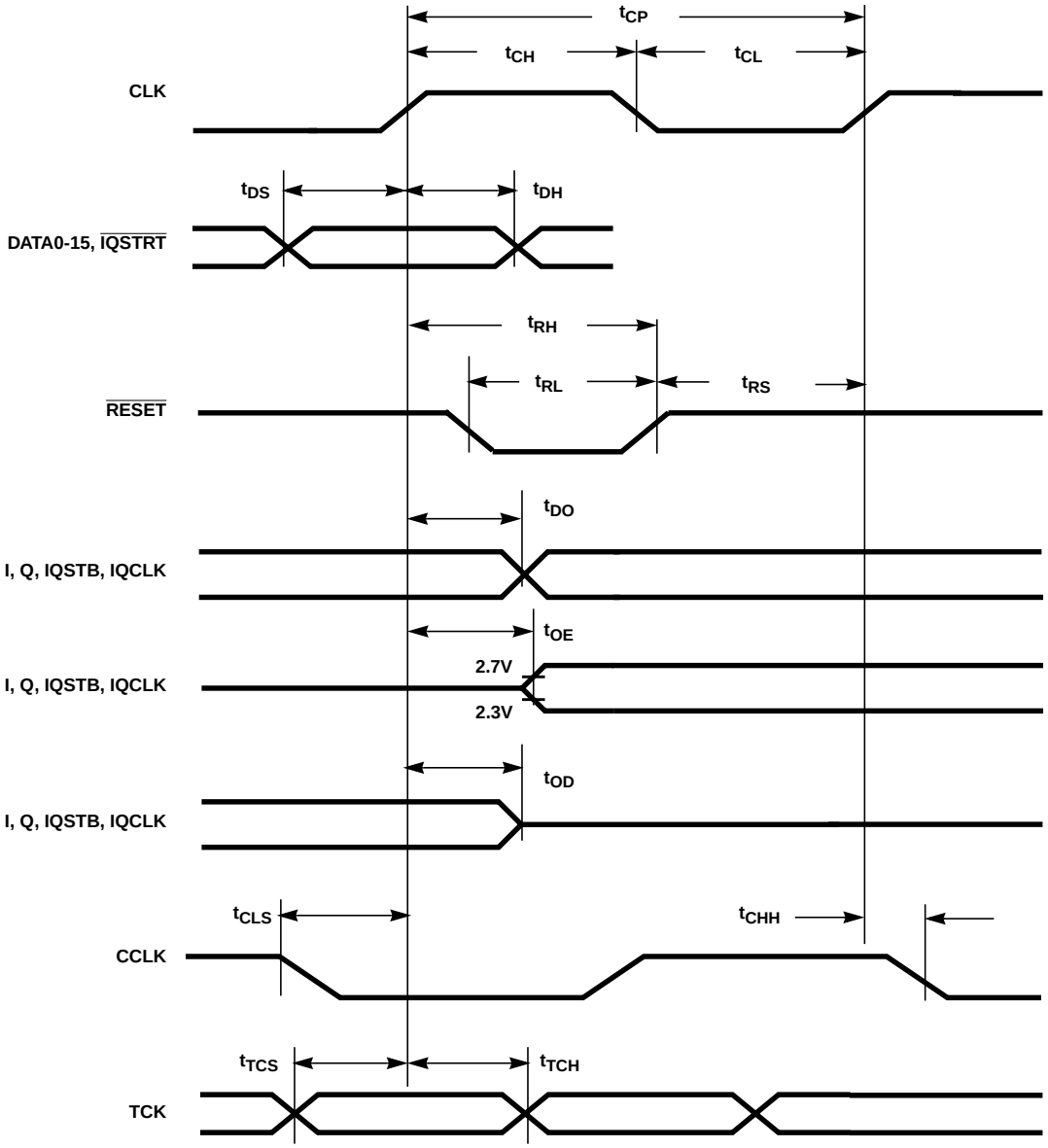


FIGURE 24. TIMING RELATIVE TO CLK

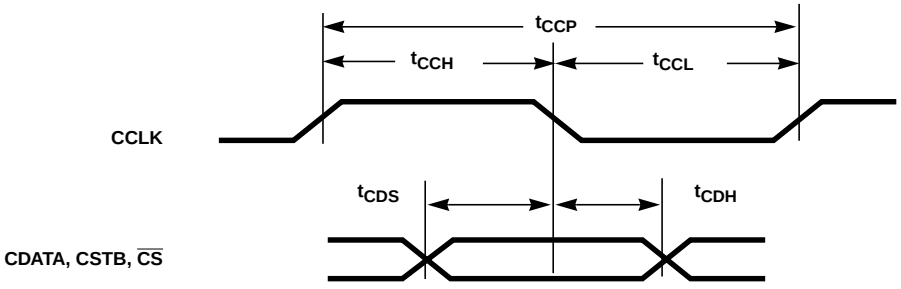


FIGURE 25. TIMING RELATIVE TO CCLK

Waveforms (Continued)

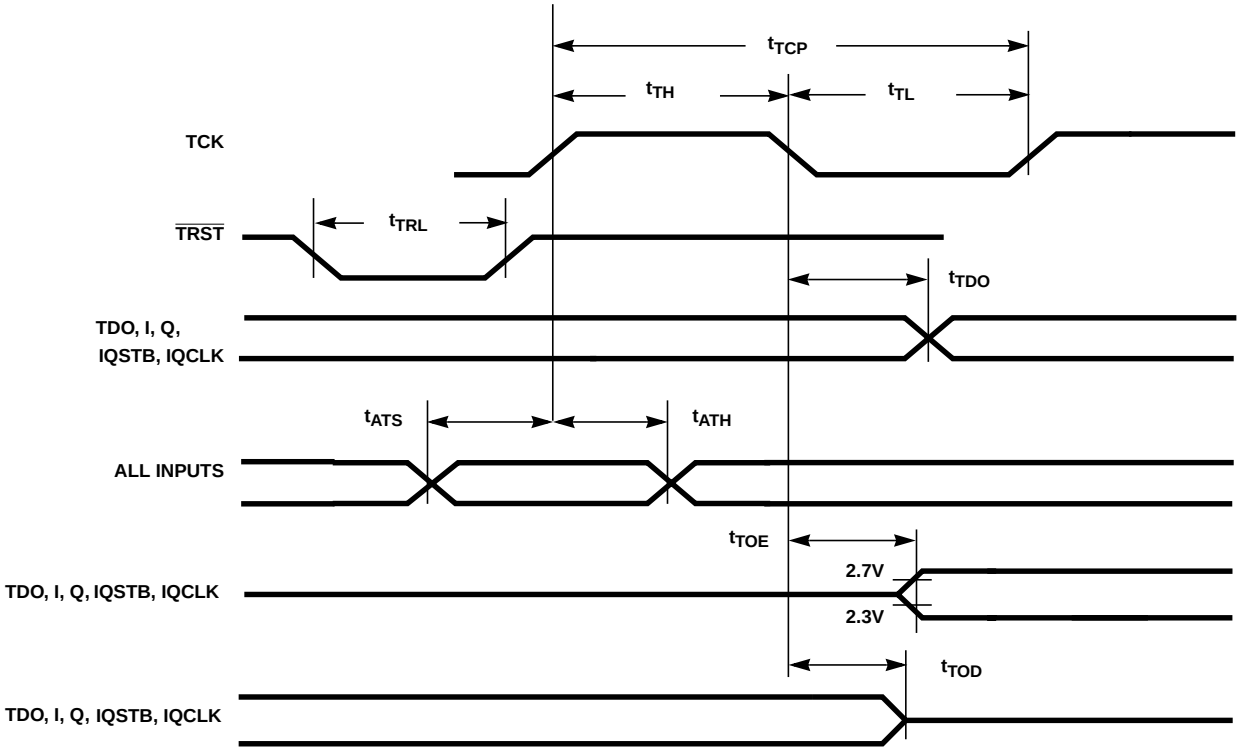


FIGURE 26. TIMING RELATIVE TO TCK

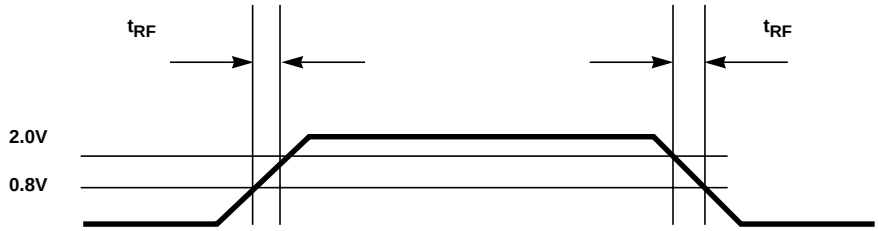


FIGURE 27. OUTPUT RISE AND FALL TIMES

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