Features

G.709 ODU - 2 Synchronous and Asynchronous mapping
- 1 x OC – 192/STM-64 mapping (239,237)
- Direct map (239,238) into ODU – 2

G.709 ODU - 1 Synchronous and Asynchronous mapping
- 1 x OC – 48/STM-16 mapping (239,237)
- Direct map (239,238) into ODU – 1

G.709 Overhead processing
- Bi-directional add-drop ODU – 1, ODU – 2
- Bi-direction G.709 Overhead Processing
- Dedicated GCC ports

Ingress and Egress SONET/SDH Performance Monitoring/ Injection
- 1 x OC-192/48/12/3 TOH add-drop and processing
- 8B/10B Monitoring
- 10GE Monitoring
- SONET/SDH section and line termination
- TOH add-drop port
- LOS, OOF, LOF detection
- B1, B2 monitoring with programmable Signal Degrade and Signal Fail thresholds
- J0 Monitoring, SDH and SONET modes
- Support for Protection Switching
- K1, K2 monitoring for APS changes, line AIS and line RDI
- Automatic, interrupt-driven, or manual AIS insertion
- Frame boundary output

Industry Standard RS(255,239) Forward Error Correction with 6.2 dB Coding Gain (at 10^{-15} CER)
- G.709 Compliant Frame Structure
- Compatible with AMCC S19203 (Hudson)

Enhanced Gain Forward Error Correction with G.709 ODU
- 10.71, 10.66, and 11.1 Gbps enhanced FEC with >8dB coding gain
- G.709 overhead processing and nominal rate expansion
- Comprehensive channel statistics gathering
- Corrected bits, bytes
- Corrected zeros, ones (with outputs)
- Uncorrectable sub-frame count

Broad Interface Compatibility
- 16 bit, 622 Mbps LVDS interface (OIF MSA compliant) 10 Gbps interface
- Compatible with AMCC Hudson, Ganges, S3091/92, S3097/98, S19211, S3193/S3094, and S3474

Client and Line side loop-back
- Client-side loopback on single 10 Gbps interface
- Line loopback on 10 Gbps interface

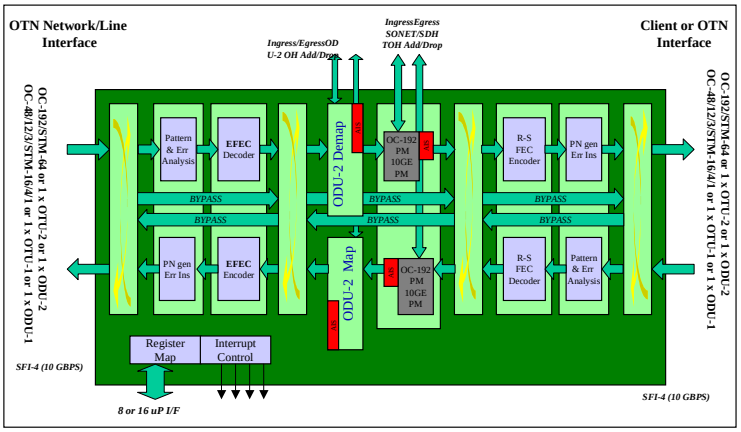
Support For System Test and Diagnostics
- Can synthesize SONET frame
- Error injection capability for verification of remote error reporting
- Test set compliant pseudo-random sequence generation/analysis

General Purpose Processor Interface
- Glueless interface to MPC860, 25 MHz to 52 MHz
- Dual Mode Interface also supports Intel processors
- Interrupt Driven or Polled mode operation

Additional Protocol Support
- FEC Frame Synchronous scrambling
- Programmable sequence detection

Low Power .18 u CMOS Technology
- 1.8 Volt core operation
- 2.5 Volt I/O

Figure 1: Block Diagram



***Final/Production Release*Information** - The information contained in this document is about a product in its fully tested and characterized phase. All features described herein are supported. Contact AMCC for updates to this document and the latest product status.

AMCC
Applied Micro Circuits Corporation

Applications

- SONET/SDH OC-48/STM-16 OC-192/STM-64 DWDM transport systems and DWDM metro networks
- Transparent Add-Drop Multiplexing Transponder applications
- Protocol Transparent Transport
- IaDI to IrDI FEC transponder chip (6.2dB gain network to >8dB gain network)

GENERAL DESCRIPTION

The AMCC Niagara device is a wide-area and metropolitan transport device aimed at next generation applications required transparent multiplexing and enhanced error correction capability. The device utilizes the ITU G.709 frame and overhead structures to enable deployment of full OTN compliant network elements. Niagara will support two gain rates, the standard G.975 based rate of 6.2dB (raw optical coding gain), and AMCC's proprietary EFEC code rated at greater than 8dB (raw optical coding gain). The Niagara device is capable of running both these gains simultaneously, providing a superb single chip transponder solution for standard gain to enhanced gain networks.

DATA INTERFACES

Both the client and network interfaces are SFI-4 compliant. Data is transferred as 16 bit LVDS parallel data with a synchronous clock. For 10 Gbps applications, the client interface rate varies between 622 Mbps and 692 Mbps, for an aggregate bandwidth of 9.95 Gbps to 10.7 Gbps. The defined low end of the parallel client interface is 31.25 Mbps (across 4 bits of the interface) for an aggregate bandwidth of 125 Mbps. The device supports OC-192/STM-64, ITU G.709 OTU-2, ITU-G.709 ODU-2, or proprietary direct map (into ODU-2) data up to a client rate of 10.3 Gbps. For 10 Gbps applications, the network side data interface operates at parallel rate of 622 Mbps and 693 Mbps for an aggregate bandwidth of 9.95 Gbps to 11.1 Gbps. The defined low end of the parallel network interface is 33.4375 Mbps (across 4 bits of the interface) for an aggregate bandwidth of 133 Gbps.

CLIENT PERFORMANCE MONITORING

A SONET/SDH performance monitor supporting OC192/48/12/3 and SDH64/16/4/1 rates is provided to perform optional section and limited-line termination functions. TOH for the SONET signal is dropped and added. On-chip processing of the critical TOH functions, such as B1, B2, and J0 is provided to enable functioning as a SONET/SDH network element. The performance monitor may also be configured to provide non-intrusive monitoring while transparently passing through the received signal with no overwrite. The 10 Gbps signal and the 2.5 Gbps signal may be synchronously or asynchronously mapped into the ODU-2 and ODU-1 payloads, respectively. FEC parity check bytes are then optionally added to form the OTU-2 or OTU-1. The device can also output the ODU-2 or OTU-1 with no parity check bytes. In the receive direction, data is de-mapped from the ODU-2 or OTU-1, and control signals provided to enable timing regeneration of the client 10 Gbps or 2.5 Gbps signal.

When operating in the ITU G.709 OTU-2/OTU-1 or ODU-2/ODU-1 mode, the SONET monitors are bypassed. On-chip processing of the G.709 overhead is provided to enable single chip G.709 section termination. G.709 overhead can be added or dropped as required. Re-mapping required for synchronization of asynchronous ODU-1 signals is not supported.

Client-signal monitoring for 8B/10B encoded data is also provided, as well as 64B/66B monitoring for 10GE-LAN traffic. A full 10GE-LAN MAC is also included in the Niagara device to support extensive 10GE monitoring.

AIS SUPPORT

For applications in which the client signal is SONET or SDH, the Niagara can generate a SONET/SDH AIS on both the client ingress and the egress.

For applications in which the client signal is G.709 compliant or for OTN regenerator applications, Line Fail and un-equipped OTN AIS is supported. For OTN edge applications, the device can be provisioned to provide either a SONET/SDH AIS or a OTN Generic AIS to the client. This facilitates convergence of the SONET/SDH and OTN functions into a single network element.

ODU MAPPING

ITU compliant client mapping of SONET OC-192 or SDH STM-64 into the ODU-2 signals (and the corresponding 2.5G signals into an ODU-1) is supported whereby a stuff column is added to every G.709 sub-frame resulting in a ODU rate expansion of (239/237). The chip can be configured to insert the G.709 compliant stuff-byte value or to insert user data into this column. The values assigned to the stuff bytes can be defined either from a register set on chip or from an external add-drop port. Coverage of these stuff columns in the BIP calculation or in the FEC is optional and can be enabled via software. When the no-coverage option is enabled, The BIP and Parity check values are calculated as if the standard stuff values were present.

A direct map mode is supported for ODU-2 and ODU-1 with no stuff columns to enable proprietary mapping with a 239/238 rate. Start of frame signals are provided at the input and output ports to enable synchronization to the ODU.

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LEGACY COMPATIBILITY

As indicated above, the Niagara also supports operation in the G.975 mode. In this mode, the G.709 overhead processing can be inhibited and direct access to the non-framing bytes in the overhead column is provided through the pins on the device. The device should be configured to operate in the 255,238 mapping mode with no stuff columns inserted in the FEC payload.

CONTROL INTERFACE

A general purpose 16-bit microprocessor interface is provided for control and monitoring. The interface supports both Intel and Motorola type microprocessors, and is capable of operating in either interrupt-driven or polled-mode configurations.

APPLICATION DIAGRAMS

Figure 2: OC-192/STM64 to OTU-2 Edge Transponder

Figure 2 shows the Niagara in an edge transponder application. An AMCC S19211 CMOS SerDes device provides the interface to the client-side optics. On the network side, the AMCC S3193 and S3094 are used to provide a high-performance interface to the network-side optics. This diagram is also the diagram for a mid-span transponder for either a standard FEC to standard FEC network or a standard FEC to enhanced FEC network. In either of these mid-span transponder applications, the client rate would increase from the standard SONET rate to the 7% overhead rate.

Figure 2: OC-192/STM64 to OTU-2 Edge Transponder

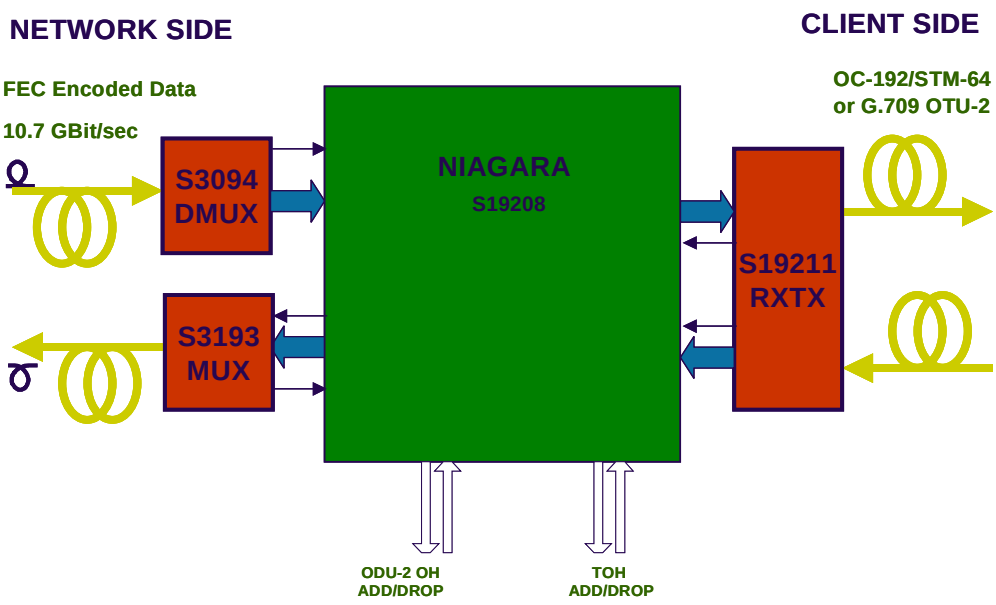
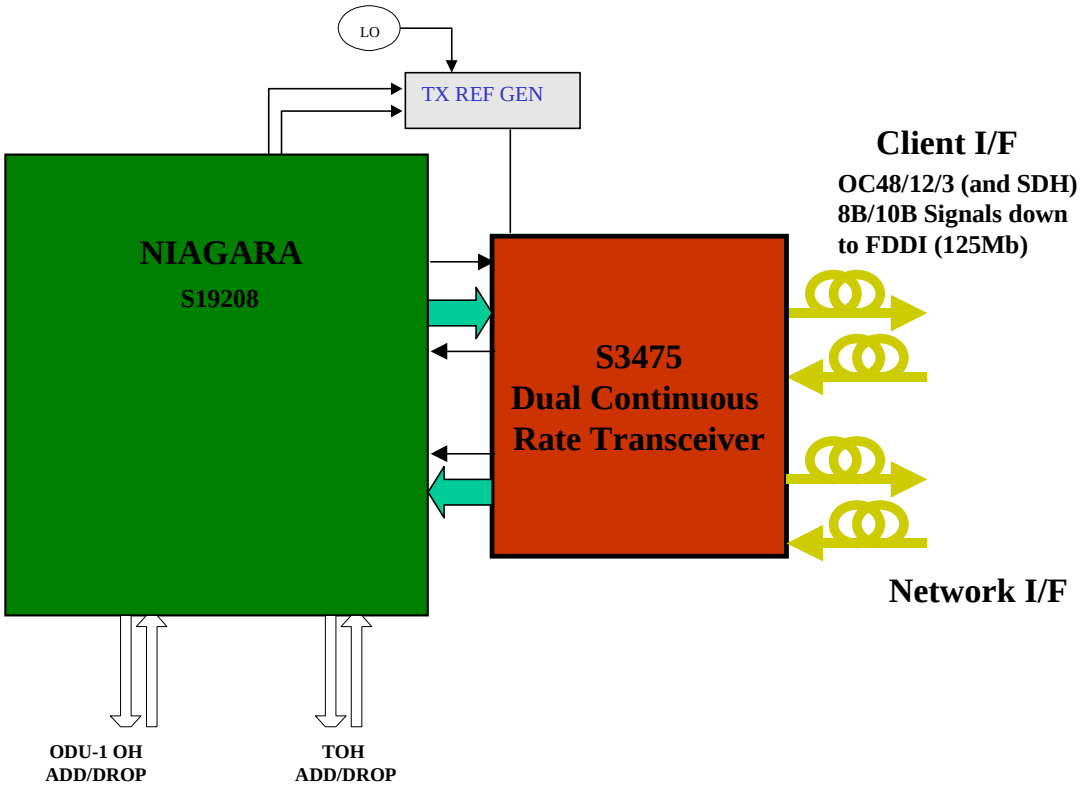


Figure 3: OC-48/STM16 (and below) to OTU-1 Edge Transponder

Figure 3 shows the Niagara in an edge transponder application. An AMCC S3474 CMOS Dual-SerDes with Continuous mode operation provides the interface to the client side and network side optics. In this application, the client half of the S3474 will run down to FDDI rates (125 Mbps). The network side of the S3474 will support the client rate plus 7% overhead for a pure FEC application, or it will support an OTU-1 rate for mapping into the Digital Wrapper frame.

Figure 3: OC-48/STM16 to OTU-1 Edge Transponder



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