TLE9871QXA20

Microcontroller with PWM Interface and BLDC MOSFET Driver for Automotive Applications

BE-Step

Data Sheet

Rev. 1.0, 2015-04-30

Automotive Power

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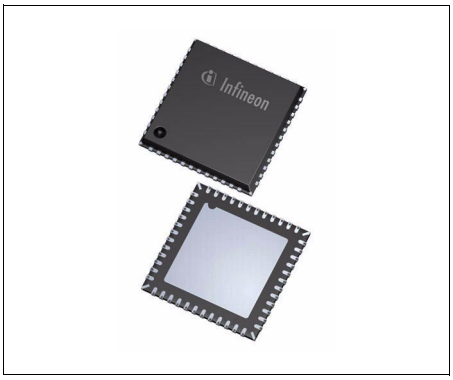
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1 Overview



VQFN-48-31

Summary of Features

- 32 bit ARM Cortex M3 Core
  - up to 24 MHz clock frequency
  - one clock per machine cycle architecture
- On-chip memory
  - 36 kByte Flash including
  - 4 kByte EEPROM (emulated in Flash)
  - 1024 Byte 100 Time Programmable Memory (100TP)
  - 3 kByte RAM
  - Boot ROM for startup firmware and Flash routines
- On-chip OSC and PLL for clock generation
  - PLL loss-of-lock detection
- MOSFET driver including charge pump
- 10 general-purpose I/O Ports (GPIO)
- 5 analog inputs, 10-bit A/D Converter (ADC1)
- 16-bit timers - GPT12, Timer 2, Timer 21 and Timer 3
- Capture/compare unit for PWM signal generation (CCU6)
- 2 full duplex serial interfaces (UART)
- 2 synchronous serial channels (SSC)
- On-chip debug support via 2-wire SWD
- Bidirectional PWM interface
- 1 high voltage monitoring input
- Single power supply from 5.5 V to 27 V
- Extended power supply voltage range from 3 V to 28 V
- Low-dropout voltage regulators (LDO)
- High speed operational amplifier for motor current sensing via shunt
- 5 V voltage supply for external loads (e.g. Hall sensor)
- Core logic supply at 1.5 V
- Programmable window watchdog (WDT1) with independent on-chip clock source
- Power saving modes
  - MCU slow-down Mode
  - Sleep Mode
  - Stop Mode
  - Cyclic wake-up Sleep Mode
- Power-on and undervoltage/brownout reset generator

Type	Package	Marking
TLE9871QXA20	VQFN-48-31	

- Overtemperature protection
- Short circuit protection
- Loss of clock detection with fail safe mode entry for low system power consumption
- Temperature Range T_J: -40 °C up to 150 °C
- Package VQFN-48 with LTI feature
- Green package (RoHS compliant)
- AEC qualified

1.1 Abbreviations

The following acronyms and terms are used within this document. List see in Table 1.

Table 1 Acronyms

Acronyms	Name
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
CCU6	Capture Compare Unit 6
CGU	Clock Generation Unit
CMU	Cyclic Management Unit
CP	Charge Pump for MOSFET driver
CSA	Current Sense Amplifier
DPP	Data Post Processing
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read Only Memory
EIM	Exceptional Interrupt Measurement
FSM	Finite State Machine
GPIO	General Purpose Input Output
H-Bridge	Half Bridge
ICU	Interrupt Control Unit
IEN	Interrupt Enable
IIR	Infinite Impulse Response
LDM	Load Instruction
LDO	Low DropOut voltage regulator
LSB	Least Significant Bit
LTI	Lead Tip Inspection
MCU	Micro Controller Unit
MF	Measurement Functions
MSB	Most Significant Bit
MPU	Memory Protection Unit
MRST	Master Receive Slave Transmit
MTSR	Master Transmit Slave Receive
MU	Measurement Unit
NMI	Non Maskable Interrupt
NVIC	Nested Vector Interrupt Controller
NVM	Non-Volatile Memory
OTP	One Time Programmable
OSC	Oscillator
PBA	Peripheral Bridge
PCU	Power Control Unit

Table 1 Acronyms

Acronyms	Name
PD	Pull Down
PGU	Power supply Generation Unit
PLL	Phase Locked Loop
PPB	Private Peripheral Bus
PU	Pull Up
PWM	Pulse Width Modulation
RAM	Random Access Memory
RCU	Reset Control Unit
RMU	Reset Management Unit
ROM	Read Only Memory
SCU-DM	System Control Unit - Digital Modules
SCU-PM	System Control Unit - Power Modules
SFR	Special Function Register
SOW	Short Open Window (for WDT)
SPI	Serial Peripheral Interface
SSC	Synchronous Serial Channel
STM	Store Instruction
SWD	ARM Serial Wire Debug
TCCR	Temperature Compensation Control Register
TMS	Test Mode Select
TSD	Thermal Shut Down
UART	Universal Asynchronous Receiver Transmitter
VBG	Voltage reference Band Gap
VCO	Voltage Controlled Oscillator
VPRE	Pre Regulator
WDT	Watchdog Timer in SCU-DM
WDT1	Watchdog Timer in SCU-PM
WMU	Wake-up Management Unit
100TP	100 Time Programmable

2 Block Diagram

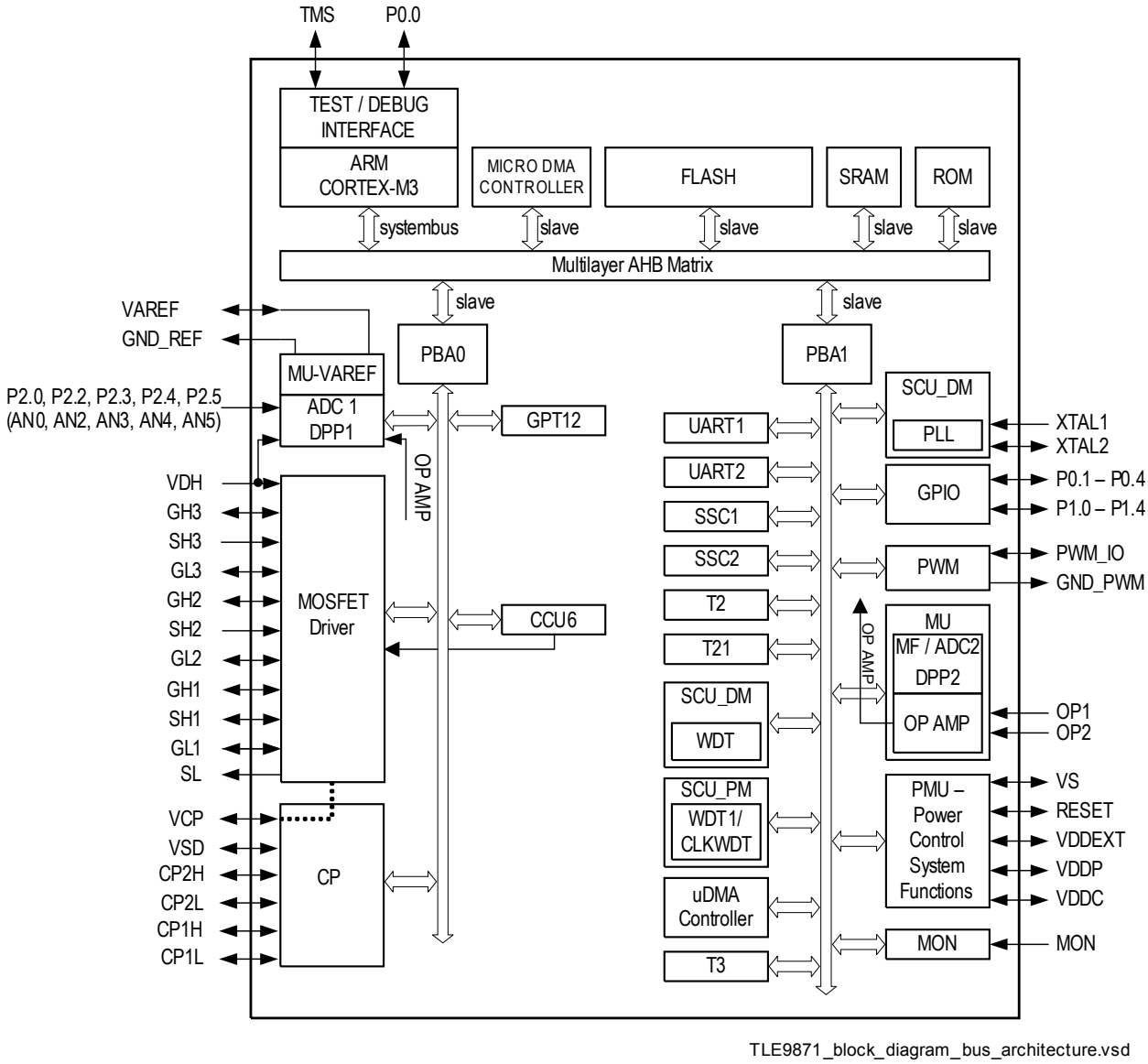


Figure 1 Block Diagram TLE9871QXA20

3 Device Pinout and Pin Configuration

3.1 Device Pinout

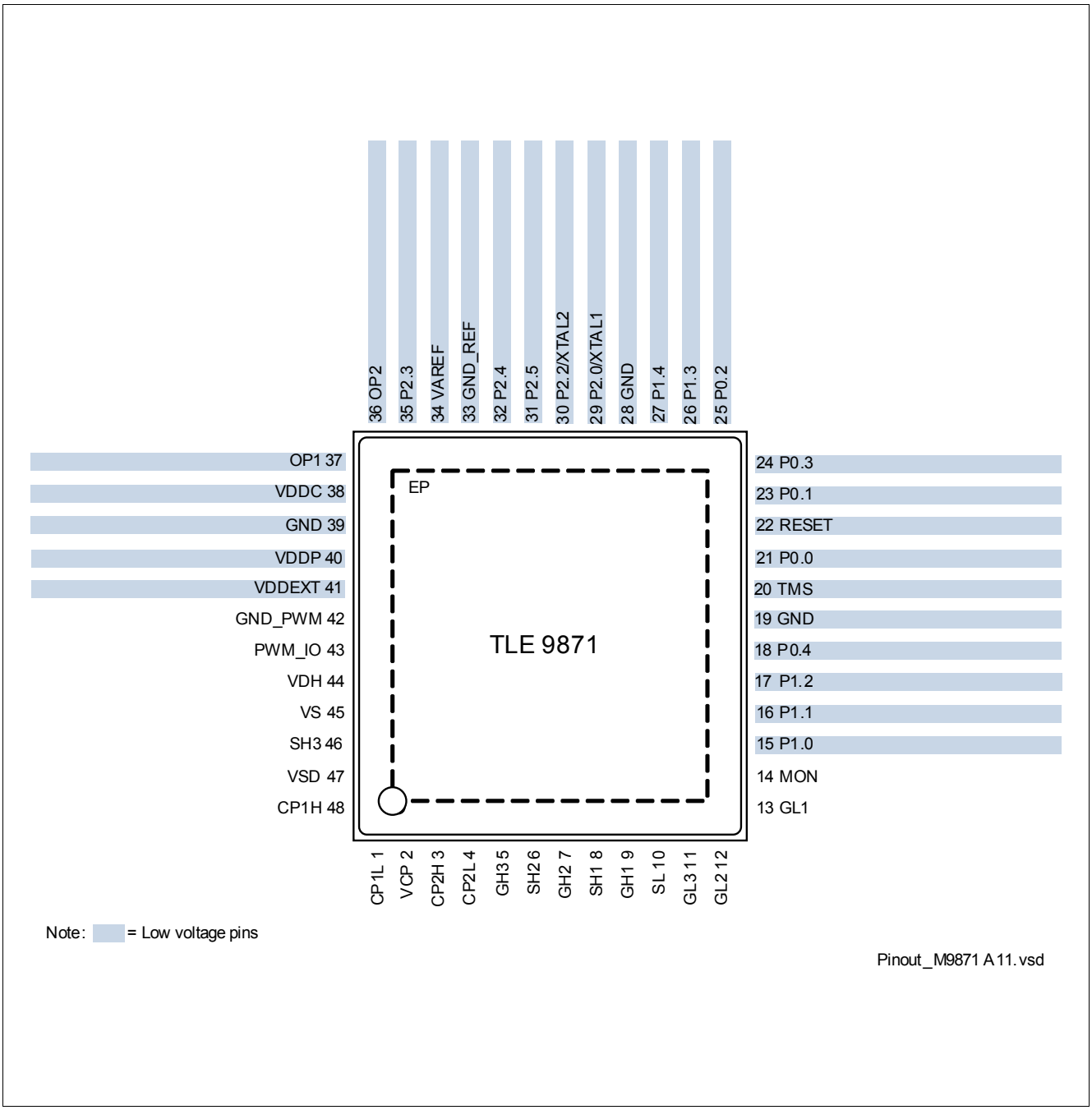


Figure 2 Device Pinout, TLE9871QXA20

3.2 Pin Configuration

After reset, all pins are configured as input (except supply pin) with one of the following settings:

- Pull-up device enabled only (PU)
- Pull-down device enabled only (PD)
- Input with both pull-up and pull-down devices disabled (I)
- Output with output stage deactivated = high impedance state (Hi-Z)

The functions and default states of the TLE9871QXA20 external pins are provided in the following table.

Type: indicates the pin type.

- I/O: Input or output
- I: Input only
- O: Output only
- P: Power supply

Not all alternate functions listed.

Table 2 Pin Definitions and Functions

Symbol	Pin Number	Type	Reset State[1)]	Function	
P0				**Port 0** Port 0 is a 5-bit bidirectional general purpose I/O port. Alternate functions can be assigned and are listed in the port description. Main function is listed below.	
P0.0	21	I/O	I/PU	SWD	Serial Wire Debug Clock
P0.1	23	I/O	I/PU	GPIO	General Purpose IO Alternate function mapping see **Table 8**
P0.2	25	I/O	I/PD	GPIO	General Purpose IO Alternate function mapping see **Table 8** *Note: For a functional SWD connection this GPIO must be tied to zero!*
P0.3	24	I/O	I/PU	GPIO	General Purpose IO Alternate function mapping see **Table 8**
P0.4	18	I/O	I/PD	GPIO	General Purpose IO Alternate function mapping see **Table 8**
P1				**Port 1** Port 1 is a 5-bit bidirectional general purpose I/O port. Alternate functions can be assigned and are listed in the Port description. The principal functions are listed below.	
P1.0	15	I/O	I	GPIO	General Purpose IO Alternate function mapping see **Table 9**
P1.1	16	I/O	I	GPIO	General Purpose IO Alternate function mapping see **Table 9**
P1.2	17	I/O	I	GPIO	General Purpose IO Alternate function mapping see **Table 9**
P1.3	26	I/O	I	GPIO	General Purpose IO, used for Inrush Transistor Alternate function mapping see **Table 9**
P1.4	27	I/O	I	GPIO	General Purpose IO Alternate function mapping see **Table 9**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State[1)]	Function
P2				**Port 2** Port 2 is a 5-bit general purpose input-only port. Alternate functions can be assigned and are listed in the Port description. Main function is listed below.
P2.0/XTAL1	29	I/I	I	AN0 ADC analog input 0 Alternate function mapping see **Table 10**
P2.2/XTAL2	30	I/O	I	AN2 ADC analog input 2 Alternate function mapping see **Table 10**
P2.3	35	I	I	AN3 ADC analog input 3 Alternate function mapping see **Table 10**
P2.4	32	I	I	AN4 ADC analog input 4 Alternate function mapping see **Table 10**
P2.5	31	I	I	AN5 ADC analog input 5 Alternate function mapping see **Table 10**
Power Supply				
VS	45	P	–	Battery supply input
VDDP	40	P	–	[2)]I/O port supply (5.0 V). Connect external buffer capacitor.
VDDC	38	P	–	[3)]Core supply (1.5 V during Active Mode). Do not connect external loads, connect external buffer capacitor.
VDDEXT	41	P	–	External voltage supply output (5.0 V, 20 mA)
GND	19	P	–	GND digital
GND	28	P	–	GND digital
GND	39	P	–	GND analog
Monitor Input				
MON	14	I	–	High Voltage Monitor Input
PWM Interface				
PWM_IO	43	I/O	–	PWM interface input/output
GND_PWM	42	P	–	PWM ground
Charge Pump				
CP1H	48	P	–	Charge Pump Capacity 1 High, connect external C
CP1L	1	P	–	Charge Pump Capacity 1 Low, connect external C
CP2H	3	P	–	Charge Pump Capacity 2 High, connect external C
CP2L	4	P	–	Charge Pump Capacity 2 Low, connect external C
VCP	2	P	–	Charge Pump Capacity
VSD	47	P	–	Battery supply input for Charge Pump
MOSFET Driver				
VDH	44	P	–	Voltage Drain High Side MOSFET Driver
SH3	46	P	–	Source High Side FET 3
SH2	6	P	–	Source High Side FET 2

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State[1)]	Function
GH2	7	P	–	Gate High Side FET 2
SH1	8	P	–	Source High Side FET 1
GH1	9	P	–	Gate High Side FET 1
SL	10	P	–	Source Low Side FET
GL2	12	P	–	Gate Low Side FET 2
GL1	13	P	–	Gate Low Side FET 1
GH3	5	P	–	Gate High Side FET 3
GL3	11	P	–	Gate Low Side FET 3
Others				
GND_REF	33	P	–	GND for VAREF
VAREF	34	I/O	–	5V ADC1 reference voltage, optional buffer or input
OP1	37	I	–	Negative operational amplifier input
OP2	36	I	–	Positive operational amplifier input
TMS	20	I I/O	I/PD	TMS Test Mode Select input SWD Serial Wire Debug input/output
RESET	22	I/O	–	Reset input, not available during Sleep Mode
EP	–	–	–	Exposed Pad, connect to GND

1) Only valid for digital IOs
2) Also named VDD5V.
3) Also named VDD1V5.

4 Modes of Operation

This highly integrated circuit contains analog and digital functional blocks. An embedded 32-bit microcontroller is available for system and interface control. On-chip, low-dropout regulators are provided for internal and external power supply. An internal oscillator provides a cost effective clock that is particularly well suited for PWM communications. A PWM interface is available as a communication interface. Driver stages for a Motor Bridge or BLDC Motor Bridge with external MOSFET are integrated, featuring PWM capability, protection features and a charge pump for operation at low supply voltage. A 10-bit SAR ADC is implemented for high precision sensor measurement. An 8-bit ADC is used for diagnostic measurements.

The Micro Controller Unit (MCU) supervision and system protection (including a reset feature) is complemented by a programmable window watchdog. A cyclic wake-up circuit, supply voltage supervision and integrated temperature sensors are available on-chip.

All relevant modules offer power saving modes in order to support automotive applications connected to terminal 30. A wake-up from power-save mode is possible via a PWM interface, via the monitoring input or using a programmable time period (cyclic wake-up).

Featuring LTI, the integrated circuit is available in a VQFN-48-31 package with 0.5 mm pitch, and is designed to withstand the severe conditions of automotive applications.

The TLE9871QXA20 has several operation modes mainly to support low power consumption requirements.

Reset Mode

The Reset Mode is a transition mode used e.g. during power-up of the device after a power-on reset, or after wake-up from Sleep Mode. In this mode, the on-chip power supplies are enabled and all other modules are initialized. Once the core supply VDDC is stable, the device enters Active Mode. If the watchdog timer WDT1 fails more than four times, the device performs a fail-safe transition to Sleep Mode.

Active Mode

In Active Mode, all modules are activated and the TLE9871QXA20 is fully operational.

Stop Mode

Stop Mode is one of two major low power modes. The transition to the low power modes is performed by setting the corresponding bits in the mode control register. In Stop Mode the embedded microcontroller is still powered, allowing faster wake-up response times. Wake-up from this mode is possible through PWM interface bus activity, by using the high-voltage monitoring pin or the corresponding 5V GPIOs.

Stop Mode with Cyclic Wake-Up

The Cyclic Wake-Up Mode is a special operating mode of the Stop Mode. The transition to the Cyclic Wake-Up Mode is done by first setting the corresponding bits in the mode control register followed by the Stop Mode command. In addition to the cyclic wake-up behavior (wake-up after a programmable time period), asynchronous wake events via the activated sources (PWM interface and/or MON) are available, as in normal Stop Mode.

Sleep Mode

The Sleep Mode is a low-power mode. The transition to the low-power mode is done by setting the corresponding bits in the MCU mode control register or in case of failure, see below. In Sleep Mode the embedded microcontroller power supply is deactivated allowing the lowest system power consumption. A wake-up from this mode is possible by PWM Interface activity, the High Voltage Monitor Input pin or Cyclic Wake-up.

Sleep Mode in Case of Failure

Sleep Mode is activated after 5 consecutive watchdog failures or in case of supply failure (5 times). In this case, MON is enabled as the wake source and Cyclic Wake-Up is activated with 1s of wake time.

Sleep Mode with Cyclic Wake-Up

The Cyclic Wake-Up Mode is a special operating mode of the Sleep Mode. The transition to Cyclic Wake-Up Mode is performed by first setting the corresponding bits in the mode control register followed by the Sleep and Stop Mode command. In addition to the cyclic wake-up behavior (wake-up after a programmable time period), asynchronous wake events via the activated sources (PWM interface and/or MON) are available, as in normal Sleep Mode.

When using Sleep Mode with cyclic wake-up the voltage regulator is switched off and started again with the wake. A limited number of registers is buffered during sleep, and can be used by SW e.g. for counting sleep/wake cycles.

MCU Slow Down Mode

In MCU Slow Down Mode the MCU frequency is reduced for saving power during operation. PWM communication is still possible. LS MOSFET can be activated.

Wake-Up Source Prioritization

All wake-up sources have the same priority. In order to handle the asynchronous nature of the wake-up sources, the first wake-up signal will initiate the wake-up sequence. Nevertheless all wake-up sources are latched in order to provide all wake-up events to the application software. The software can clear the wake-up source flags. This is to ensure that no wake-up event is lost.

As default wake-up source, the MON input is activated after power-on reset only. Additionally, the device is in Cyclic Wake-Up Mode with the max. configurable dead time setting.

The following table shows the possible power mode configurations including the Stop Mode.

Table 3 Power Mode Configurations

Module/Function	Active Mode	Stop Mode	Sleep Mode	Comment
VDDEXT	ON/OFF	ON (no dynamic load)/OFF	OFF	–
Bridge Driver	ON/OFF	OFF	OFF	
PWM TRx	ON/OFF	wake-up only/ OFF	wake-up only/ OFF	–
VS sense	ON/OFF brownout detection	brownout detection	POR on VS	brownout det. done in PCU
GPIO 5V (wake-up)	n.a.	disabled/static	OFF	–
GPIO 5V (active)	ON	ON	OFF	–
WDT1	ON	OFF	OFF	–
CYCLIC WAKE	n.a.	cyclic wake-up/ cyclic sense/OFF	cyclic wake-up/ OFF	–
Measurement	ON[1)]	OFF	OFF	–
MCU	ON/slow-down/STOP	STOP[2)]	OFF	–
CLOCK GEN (MC)	ON	OFF	OFF	–

Table 3 Power Mode Configurations (cont'd)

Module/Function	Active Mode	Stop Mode	Sleep Mode	Comment
LP_CLK (18 MHz)	ON	OFF	OFF	WDT1
LP_CLK2 (100 kHz)	ON/OFF	ON/OFF	ON/OFF	for cyclic wake-up

1) May not be switched off due to safety reasons

2) MC PLL clock disabled, MC supply reduced to 0.9 V

Wake-Up Levels and Transitions

The wake-up can be triggered by rising, falling or both signal edges for the monitor input, by PWM interface or by cyclic wake-up.

5 Power Management Unit (PMU)

5.1 Features

- System modes control (startup, sleep, stop and active)
- Power management (cyclic wake-up)
- Control of system voltage regulators with diagnosis (overload, short, over-voltage)
- Fail safe mode detection and operation in case of system errors (watchdog fail)
- Wake-up sources configuration and management (PWM Interface, MON, GPIOs)
- System error logging

5.2 Introduction

The power management unit is responsible for generating all required voltage supplies for the embedded MCU (VDDC, VDDP) and the external supply (VDDEXT). The power management unit is designed to ensure fail-safe behavior of the system IC by controlling all system modes including the corresponding transitions. Additionally, the PMU provides well defined sequences for the system mode transitions and generates hierarchical reset priorities. The reset priorities control the reset behavior of all system functionalities especially the reset behavior of the embedded MCU. All these functions are controlled by a state machine. The system master functionality of the PMU make use of an independent logic supply and system clock. For this reason, the PMU has an "Internal logic supply and system clock" module which works independently of the MCU clock.

5.2.1 Block Diagram

The following figure shows the structure of the Power Management Unit. **Table 4** describes the submodules in more detail.

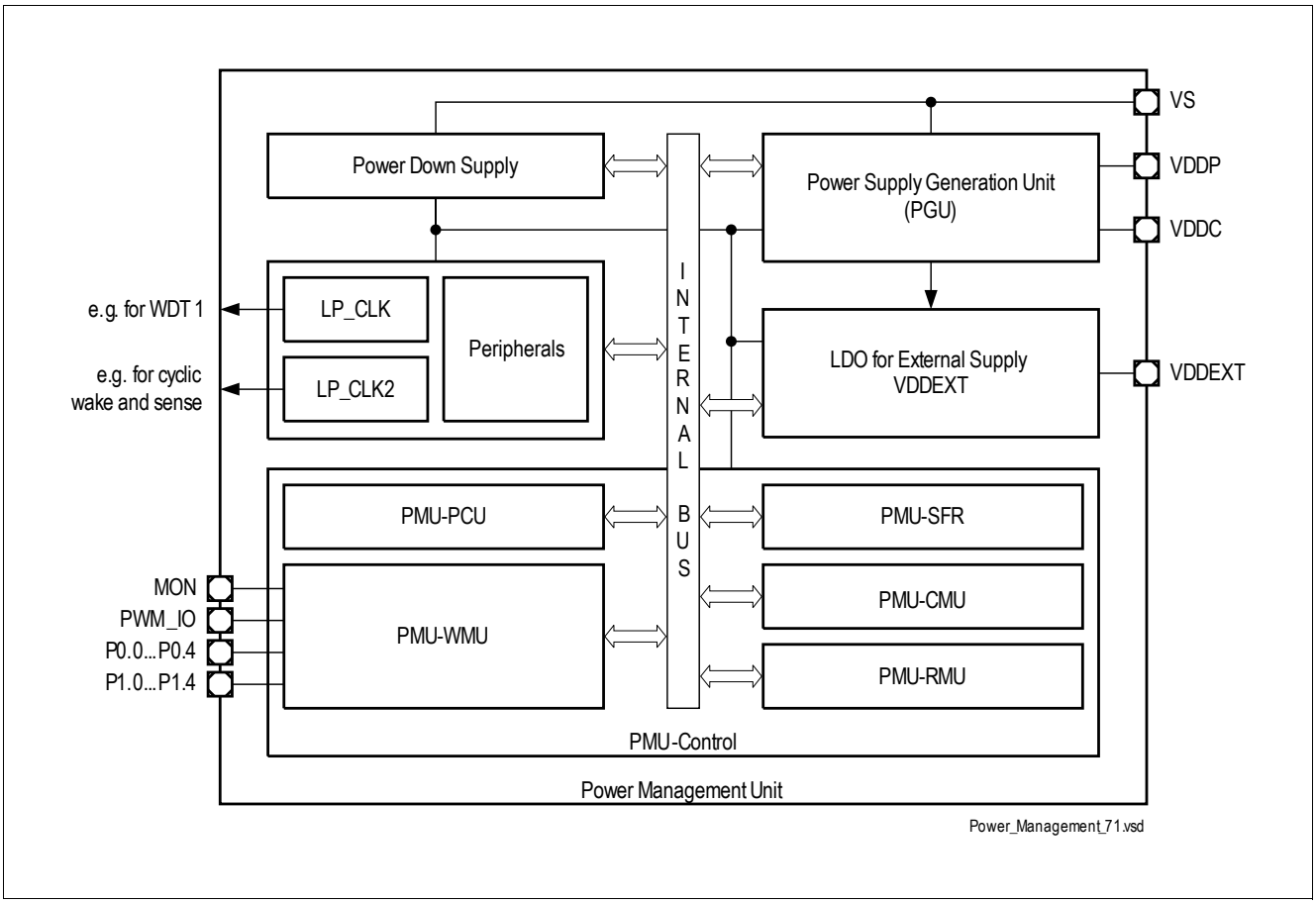


Figure 3 Power Management Unit Block Diagram

Table 4 Description of PMU Submodules

Mod. Name	Modules	Functions
Power Down Supply	Independent supply voltage generation for PMU	This supply is dedicated to the PMU to ensure an independent operation from generated power supplies (VDDP, VDDC).
LP_CLK (= 18 MHz)	- Clock source for all PMU submodules - Backup clock source for System - Clock source for WDT1	This ultra low power oscillator generates the clock for the PMU. This clock is also used as backup clock for the system in case of PLL Clock failure and as an independent clock source for WDT1.
LP_CLK2 (= 100 kHz)	Clock source for PMU	This ultra low power oscillator generates the clock for the PMU in Stop Mode and in the cyclic modes.
Peripherals	Peripheral blocks of PMU	These blocks include the analog peripherals to ensure a stable and fail-safe PMU startup and operation (bandgap, bias).

Table 4 Description of PMU Submodules (cont'd)

Mod. Name	Modules	Functions
Power Supply Generation Unit (PGU)	Voltage regulators for VDDP and VDDC	This block includes the voltage regulators for the pad supply (VDDP) and the core supply (VDDC).
VDDEXT	Voltage regulator for VDDEXT to supply external modules (e.g. Sensors)	This voltage regulator is a dedicated supply for external modules and can also be used for cyclic sense operations (e.g. with hall sensor).
PMU-SFR	All Extended Special Function registers that are relevant to the PMU.	This module contains all registers needed to control and monitor the PMU.
PMU-PCU	Power Control Unit of the PMU	This block is responsible for controlling all power related actions within the PGU Module. It also contains all regulator related diagnostics such as undervoltage and overvoltage detection as well as overcurrent and short circuit diagnostics.
PMU-WMU	Wake-Up Management Unit of the PMU	This block is responsible for controlling all wake-up related actions within the PMU Module.
PMU-CMU	Cyclic Management Unit of the PMU	This block is responsible for controlling all actions in cyclic mode.
PMU-RMU	Reset Management Unit of the PMU	This block generates resets triggered by the PMU such as undervoltage or short circuit reset, and passes all resets to the relevant modules and their register.

5.2.2 PMU Modes Overview

The following state diagram shows the available modes of the device.

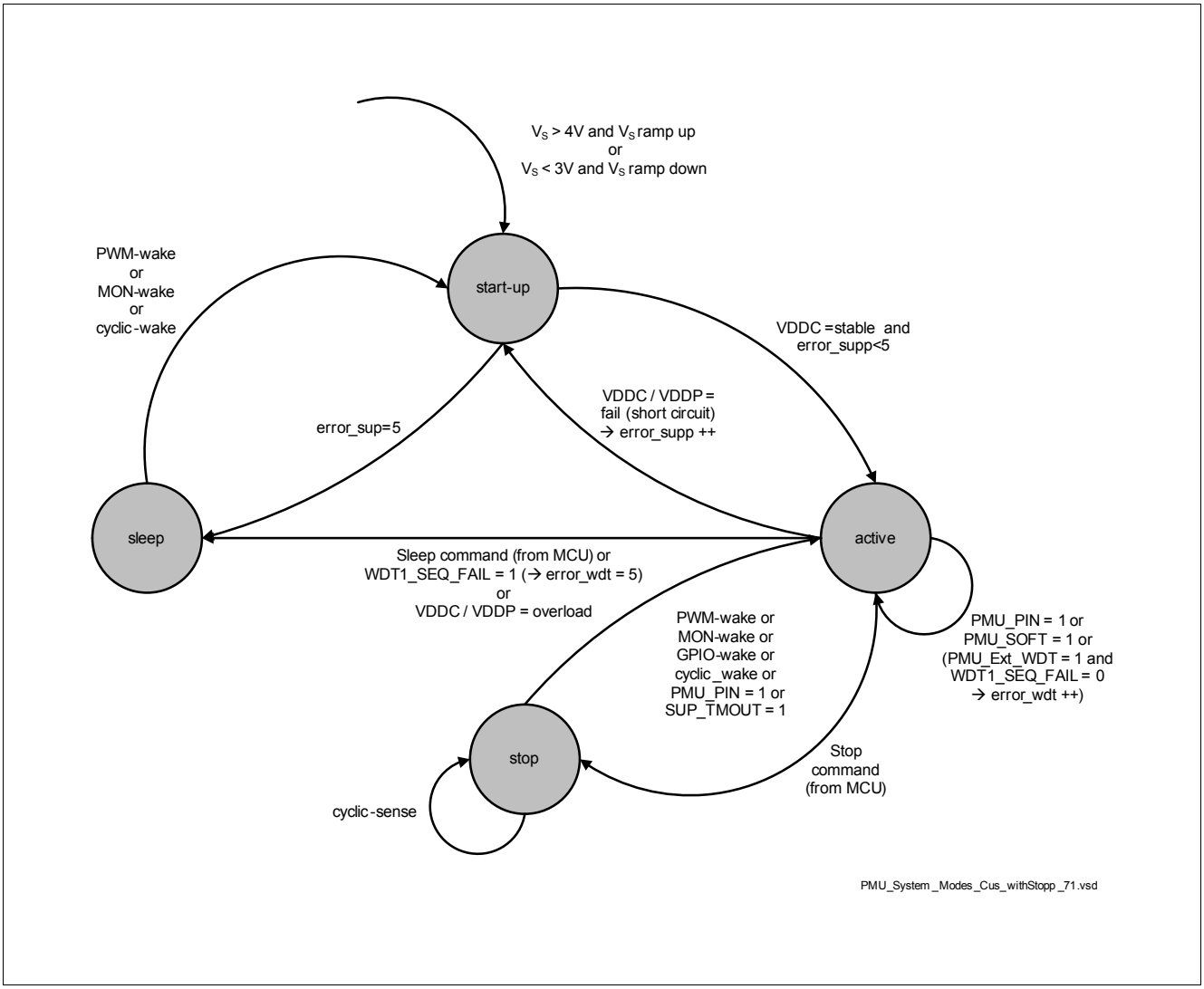


Figure 4 Power Management Unit System Modes

5.3 Power Supply Generation Unit (PGU)

5.3.1 Voltage Regulator 5.0V (VDDP)

This module represents the 5 V voltage regulator, which provides the pad supply for the parallel port pins and other 5 V analog functions (e.g. PWM Interface).

Features

- 5 V low-drop voltage regulator
- Overcurrent monitoring and shutdown with MCU signaling (interrupt)
- Overvoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with reset (Undervoltage Reset, V_{DDPUV})
- Pre-Regulator for VDDC Regulator
- GPIO Supply
- Pull Down Current Source at the output for Sleep Mode only (typ. 5 mA)

The output capacitor C_{VDDP} is mandatory to ensure proper regulator functionality.

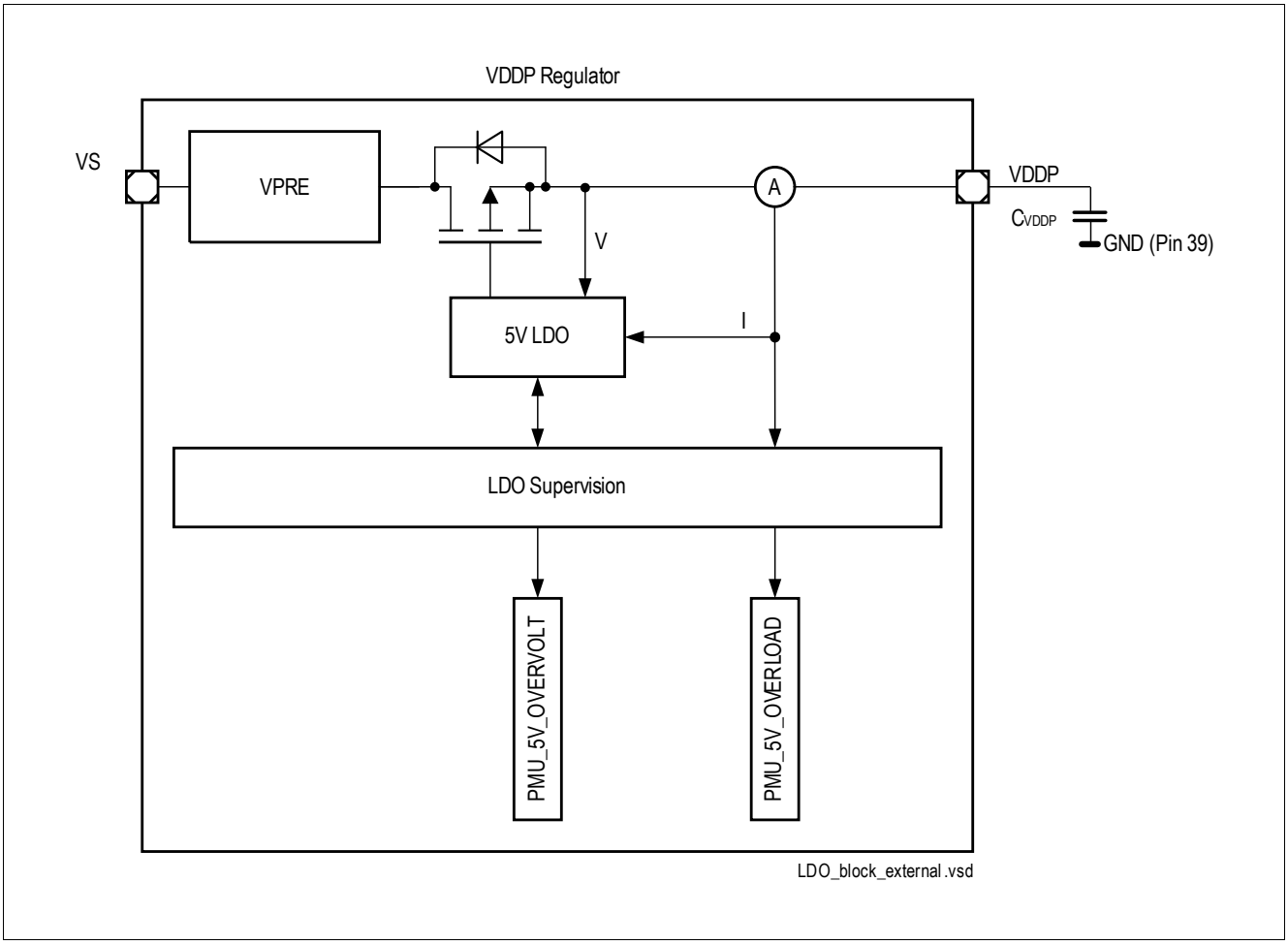


Figure 5 Module Block Diagram of VDDP Voltage Regulator

5.3.2 Voltage Regulator 1.5V (VDDC)

This module represents the 1.5 V voltage regulator, which provides the supply for the microcontroller core, the digital peripherals and other internal analog 1.5 V functions (e.g. ADC2) of the chip. To further reduce the current consumption of the MCU during Stop Mode the output voltage can be lowered to 0.9 V.

Features

- 1.5 V low-drop voltage regulator
- Overcurrent monitoring and shutdown with MCU signaling (interrupt)
- Overvoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with reset
- Pull Down Current Source at the output for Sleep Mode only (typ. 100 µA)

The output capacitor C_{VDDC} is mandatory to ensure a proper regulator functionality.

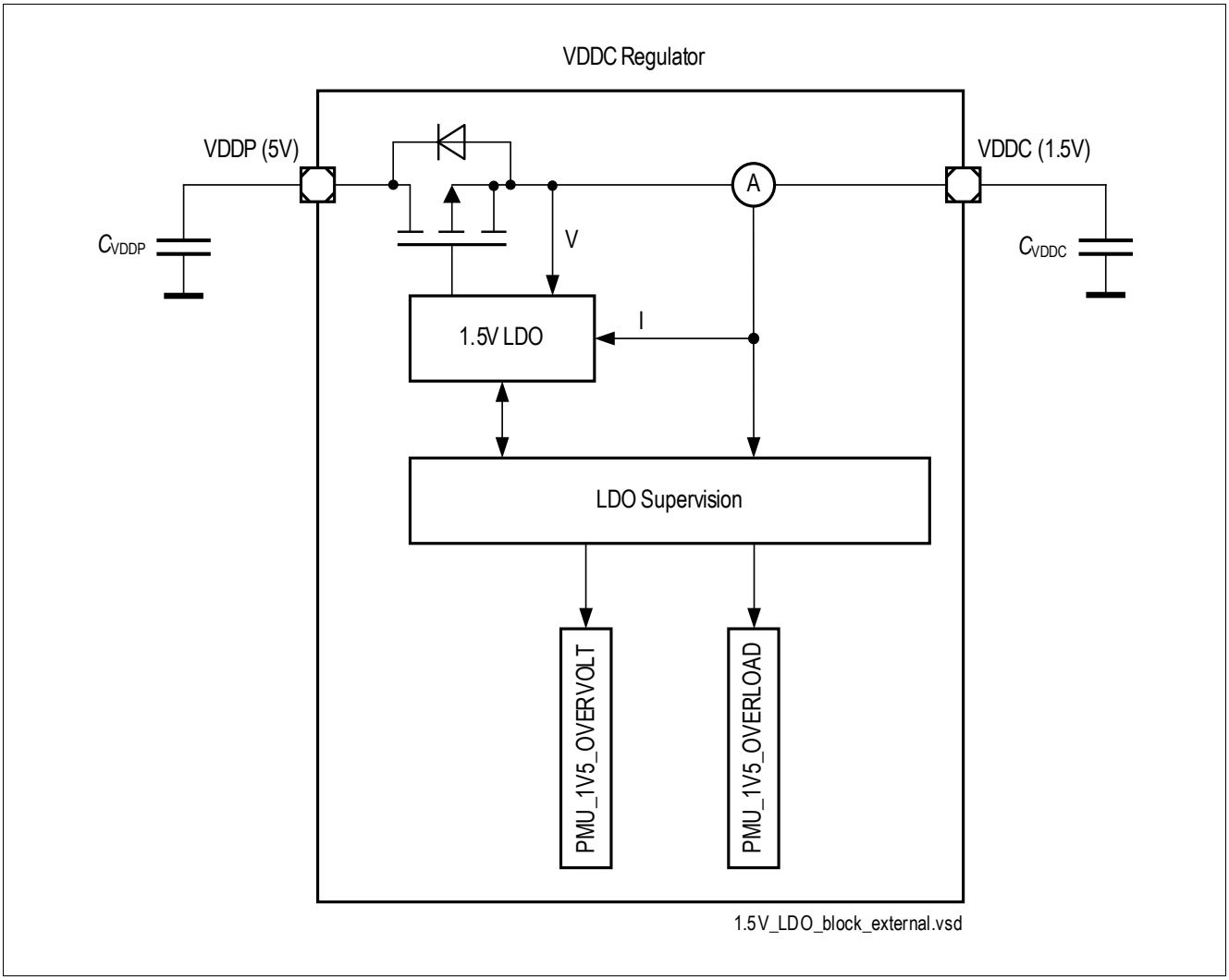


Figure 6 Module Block Diagram of VDDC Voltage Regulator

5.3.3 External Voltage Regulator 5.0V (VDDEXT)

This module represents the 5 V voltage regulator, which serves as a supply for external circuits. It can be used e.g. to supply an external sensor, LEDs or potentiometers.

Features

- Switchable +5 V, low-drop voltage regulator
- Switch-on overcurrent blanking time in order to drive small capacitive loads
- Overcurrent monitoring and shutdown with MCU signaling (interrupt)
- Overvoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with MCU signaling (interrupt)
- Pull Down current source at the output for Sleep Mode only (typ. 100 µA)
- Cyclic sense option together with GPIOs

The output capacitor C_{VDDEXT} is mandatory to ensure a proper regulator functionality.

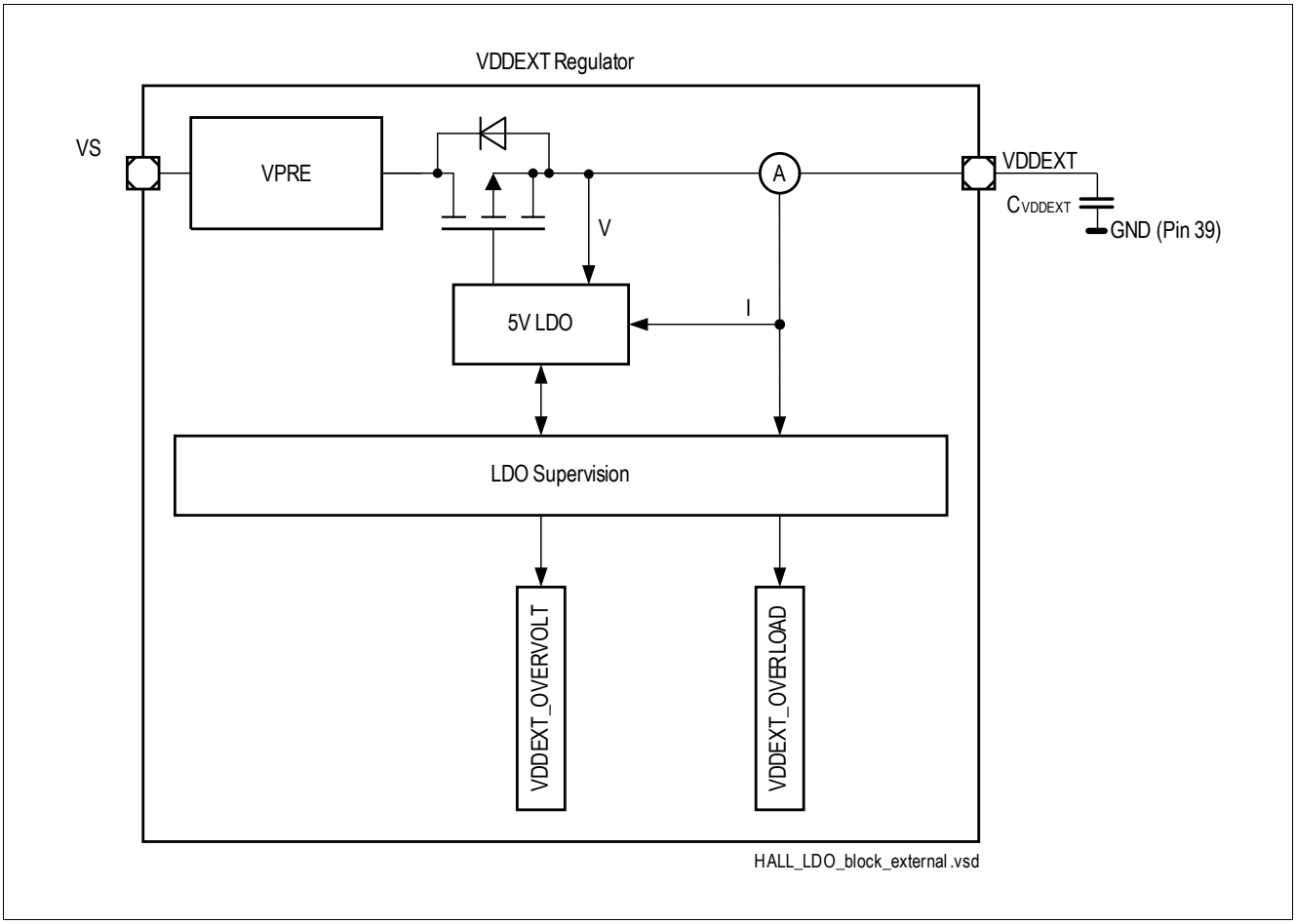


Figure 7 Module Block Diagram of External Voltage Regulator

6 System Control Unit - Digital Modules (SCU-DM)

6.1 Features

- Flexible clock configuration features
- Reset management of all system resets
- System modes control for all power modes (active, power down, sleep)
- Interrupt enabling for many system peripherals
- General purpose input output control
- Debug mode control of system peripherals

6.2 Introduction

The System Control Unit (SCU) supports all central control tasks in the TLE9871QXA20. The SCU is made up of the following sub-modules:

- Clock System and Control
- Reset Control
- Power Management
- Interrupt Management
- General Port Control
- Flexible Peripheral Management
- Module Suspend Control
- Watchdog Timer
- Error Detection and Correction in Data Memory
- Miscellaneous Control

6.2.1 Block Diagram

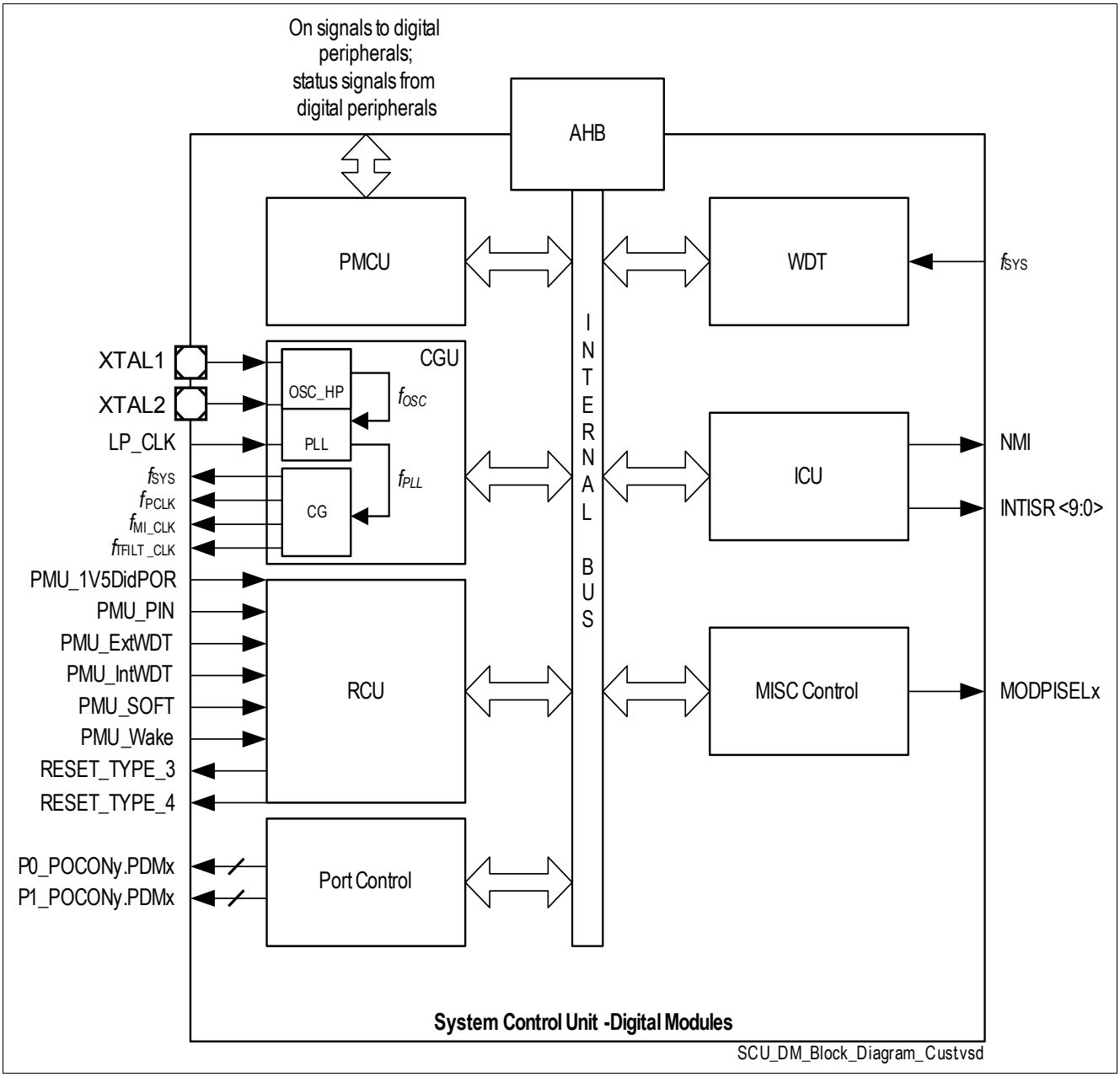


Figure 8 System Control Unit - Digital Modules Block Diagram

AMBA AHB (Advanced High-Performance Bus)

PMCU (Power Module Control Unit)

WDT (Watchdog Timer in SCU-DM)

- f_{SYS}; System clock

CGU (Clock Generation Unit)

- f_{SYS}; System clock
- f_{PCLK}; Peripheral clock

- f_{MI_CLK}; Measurement interface clock
- f_{TFILT_CLK}; Analog module filter clock
- LP_CLK; Clock source for all PMU submodules and WDT1

ICU (Interrupt Control Unit)

- NMI (Non-Maskable Interrupt)
- INTISR<15:0>; External interrupt signals

RCU (Reset Control Unit)

- PMU_1V5DidPOR; Undervoltage reset of power down supply
- PMU_PIN; Reset generated by reset pin
- PMU_ExtWDT; WDT1 reset
- PMU_IntWDT; WDT (SCU) reset
- PMU_SOFT; Software reset
- PMU_Wake; Sleep Mode/Stop Mode exit with reset
- RESET_TYPE_3; Peripheral reset (contains all resets)
- RESET_TYPE_4; Peripheral reset (without SOFT and WDT reset)

Port Control

- P0_POCONy.PDMx; driver strength control
- P1_POCONy.PDMx; driver strength control

MISC Control

- MODPISELx; Mode selection registers for UART (source section) and Timer (trigger or count selection)

6.3 Clock Generation Unit

The Clock Generation Unit (CGU) enables a flexible clock generation for TLE9871QXA20. During user program execution, the frequency can be modified to optimize the performance/power consumption ratio, allowing power consumption to be adapted to the actual application state.

The CGU in the TLE9871QXA20 consists of one oscillator circuit (OSC_HP), a Phase-Locked Loop (PLL) module with an internal oscillator (OSC_PLL), and a Clock Control Unit (CCU). The CGU can convert a low-frequency input/external clock signal to a high-frequency internal clock.

The system clock f_{SYS} is generated from of the following selectable clocks:

- PLL clock output f_{PLL}
- Direct clock from oscillator OSC_HP f_{OSC}
- Low precision clock f_{LP_CLK} (HW-enabled for startup after reset and during power-down wake-up sequence)

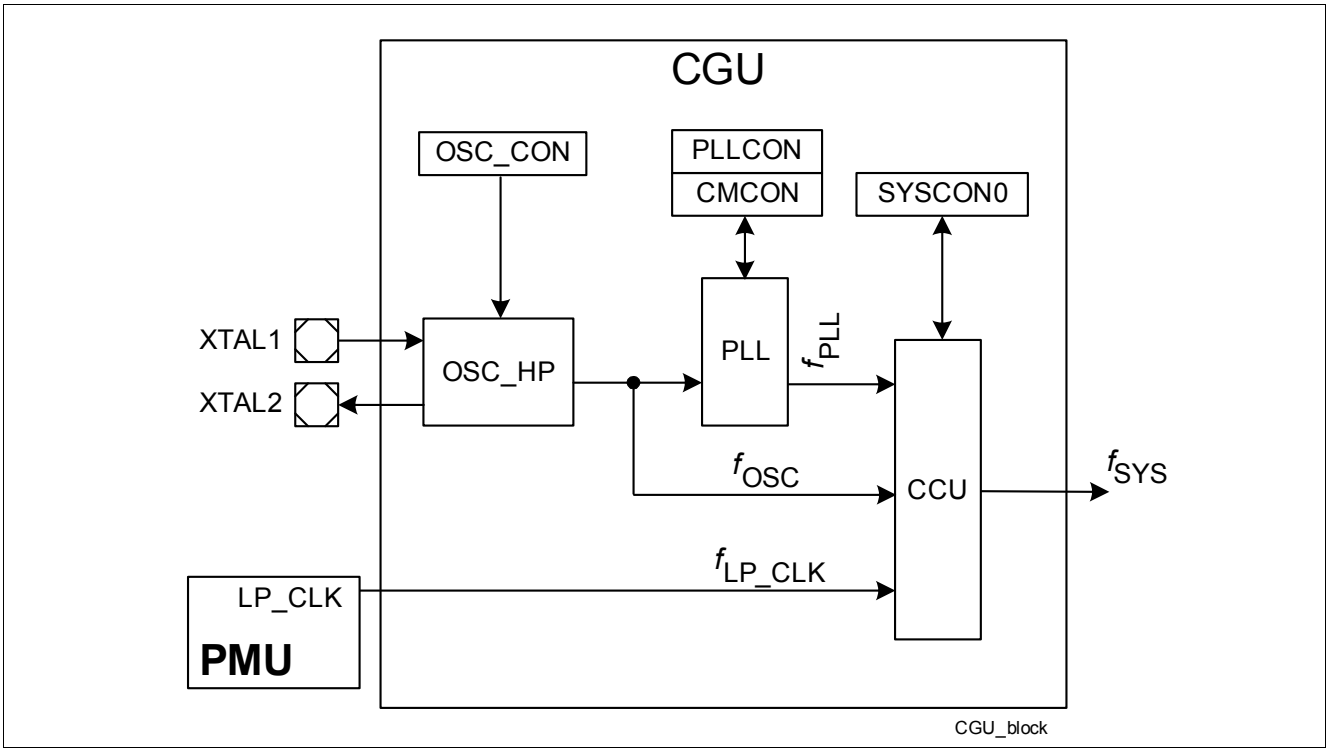


Figure 9 Clock Generation Unit Block Diagram

The following sections describe the different parts of the CGU.

6.3.1 Low Precision Clock

The clock source LP_CLK is a low-precision RC oscillator (LP-OSC) with a nominal frequency of 18 MHz that is enabled by hardware as an independent clock source for the TLE9871QXA20 startup after reset and during the power-down wake-up sequence. f_{LP_CLK} is not user configurable.

6.3.2 High Precision Oscillator Circuit (OSC_HP)

The high precision oscillator circuit, designed to work with both an external crystal oscillator or an external stable clock source, consists of an inverting amplifier with XTAL1 as the input, and XTAL2 as the output.

Figure 10 shows the recommended external circuitry for both operating modes, External Crystal Mode and External Input Clock Mode.

6.3.2.1 External Input Clock Mode

When supplying the clock signal directly, not using an external crystal and bypassing the oscillator, the input frequency needs to be equal to or greater than 4 MHz if the PLL VCO part is used.

When using an external clock signal, it must be connected to XTAL1. XTAL2 is left open (unconnected).

6.3.2.2 External Crystal Mode

When using an external crystal, its frequency can be within the range of 4 MHz to 25 MHz. An external oscillator load circuitry must be used, connected to both pins, XTAL1 and XTAL2. It normally consists of the two load capacitances C1 and C2. A series damping resistor could be required for some crystals. The exact values and the corresponding operating ranges depend on the crystal and have to be determined and optimized in cooperation with the crystal vendor using the negative resistance method. The following load cap values can be used as starting point for the evaluation:

Table 5 External CAP Capacitors

Fundamental Mode Crystal Frequency (approx., MHz)	Load Caps C_1, C_2 (pF)
4	33
8	18
12	12
16	10
20	10
25	8

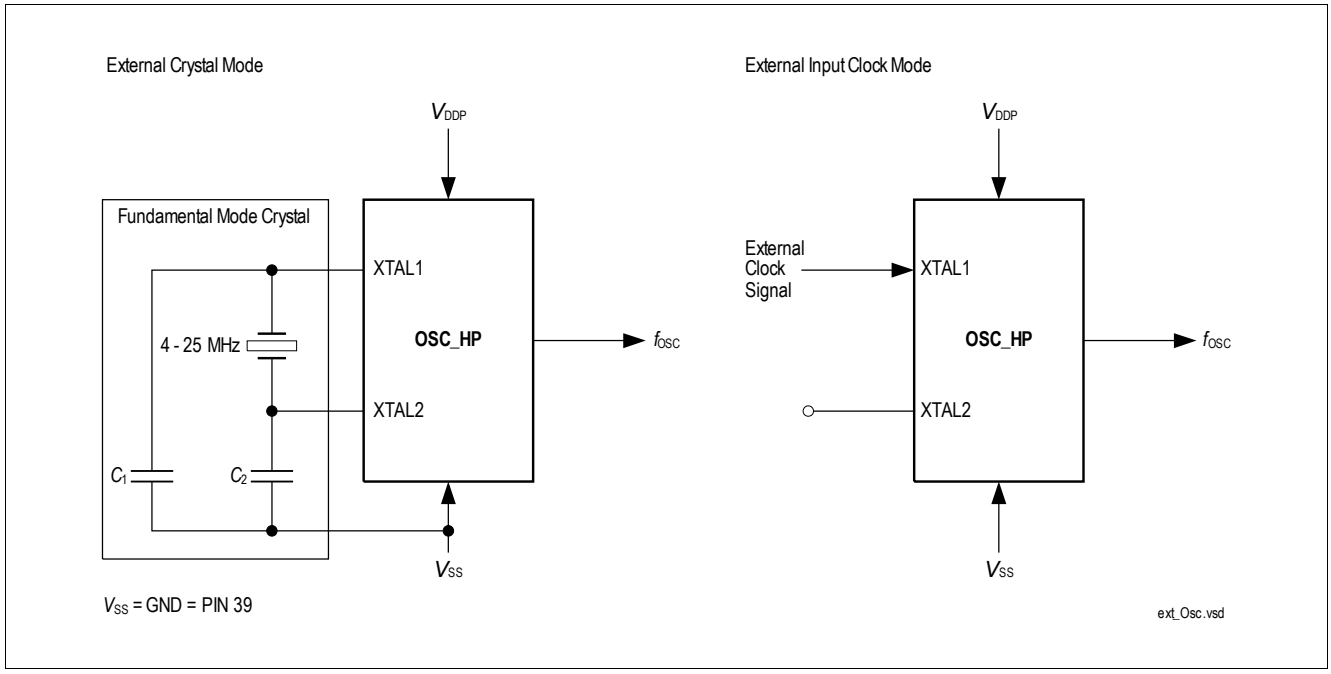


Figure 10 TLE9871QXA20 External Circuitry for the OSC_HP

7 System Control Unit - Power Modules (SCU-PM)

7.1 Features

- Clock Watchdog Unit (CWU): supervision of all clocks with NMI signaling relevant to power modules
- Interrupt Control Unit (ICU): all interrupt flags and status flags with system relevance
- Power Control Unit (PCU): takes over control when device enters and exits Sleep and Stop Mode
- External Watchdog (WDT1): independent system watchdog for monitoring system activity

7.2 Introduction

7.2.1 Block Diagram

The System Control Unit of the power modules consists of the sub-modules in the figure shown below:

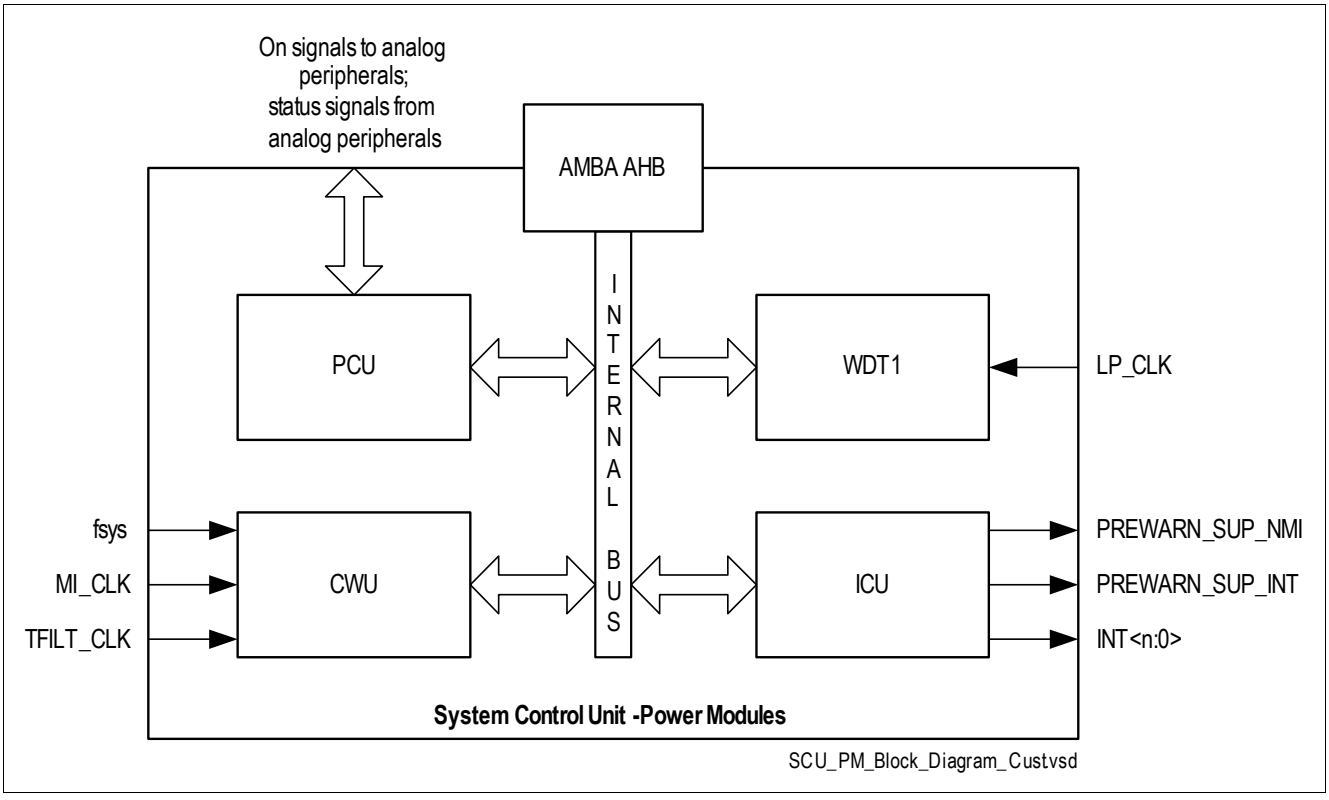


Figure 11 Block diagram of System Control Unit - Power Modules

AMBA AHB (Advanced High-Performance Bus)

CWU (Clock Watchdog Unit)

- fsys; system frequency: PLL output
- MI_CLK; measurement interface clock (analog clock): derived from fsys using division factors 1/2/3/4
- TFILT_CLK; clock used for digital filters: derived from fsys using configurable division factors

WDT1 (System Watchdog)

- LP_CLK; clock source for all PMU submodules and WDT1

ICU (Interrupt Control Unit)

- PREWARN_SUP_NMI; supply prewarning NMI request
- PREWARN_SUP_INT; supply prewarning interrupt
- grouping of peripheral interrupts for external interupt nodes:
  - grouping single peripheral interrupts for interrupt node INT<2> (Measurement Unit (MU))
  - grouping single peripheral interrupts for interrupt node INT<3> (ADC1-VAREF)
  - grouping single peripheral interrupts for interrupt node INT<10> (UART1-PWM Interface)
  - grouping single peripheral interrupts for interrupt node INT<14> (Bridge Driver)

8 ARM Cortex M3 Core

8.1 Features

The key features of the Cortex M3 implemented are listed below.

Processor Core. A low gate count core, with low latency interrupt processing:

- A subset of the Thumb®-2 Instruction Set
- Banked stack pointer (SP) only
- 32-bit hardware divide instructions, SDIV and UDIV (Thumb-2 instructions)
- Handler and Thread Modes
- Thumb and debug states
- Interruptible-continued instructions LDM/STM, Push/Pop for low interrupt latency
- Automatic processor state saving and restoration for low latency Interrupt Service Routine (ISR) entry and exit
- ARM architecture v7-M Style BE8/LE support
- ARMv6 unaligned accesses

Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing:

- Interrupts, configurable from 1 to 16
- Bits of priority (4)
- Dynamic reprioritization of interrupts
- Priority grouping. This enables selection of preemptive interrupt levels and non-preemptive interrupt levels
- Support for tail-chaining and late arrival of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead

Bus interfaces

- Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, DCode, and System bus interface
- Memory access alignment
- Write buffer for buffering of write data

8.2 Introduction

The ARM Cortex-M3 processor is a leading 32-bit processor and provides a high-performance and cost-optimized platform for a broad range of applications including microcontrollers, automotive body systems and industrial control systems. Like the other Cortex family processors, the Cortex-M3 processor implements the Thumb®-2 instruction set architecture. With the optimized feature set the Cortex-M3 delivers 32-bit performance in an application space that is usually associated with 8- and 16-bit microcontrollers.

8.2.1 Block Diagram

Figure 12 shows the functional blocks of the Cortex M3.

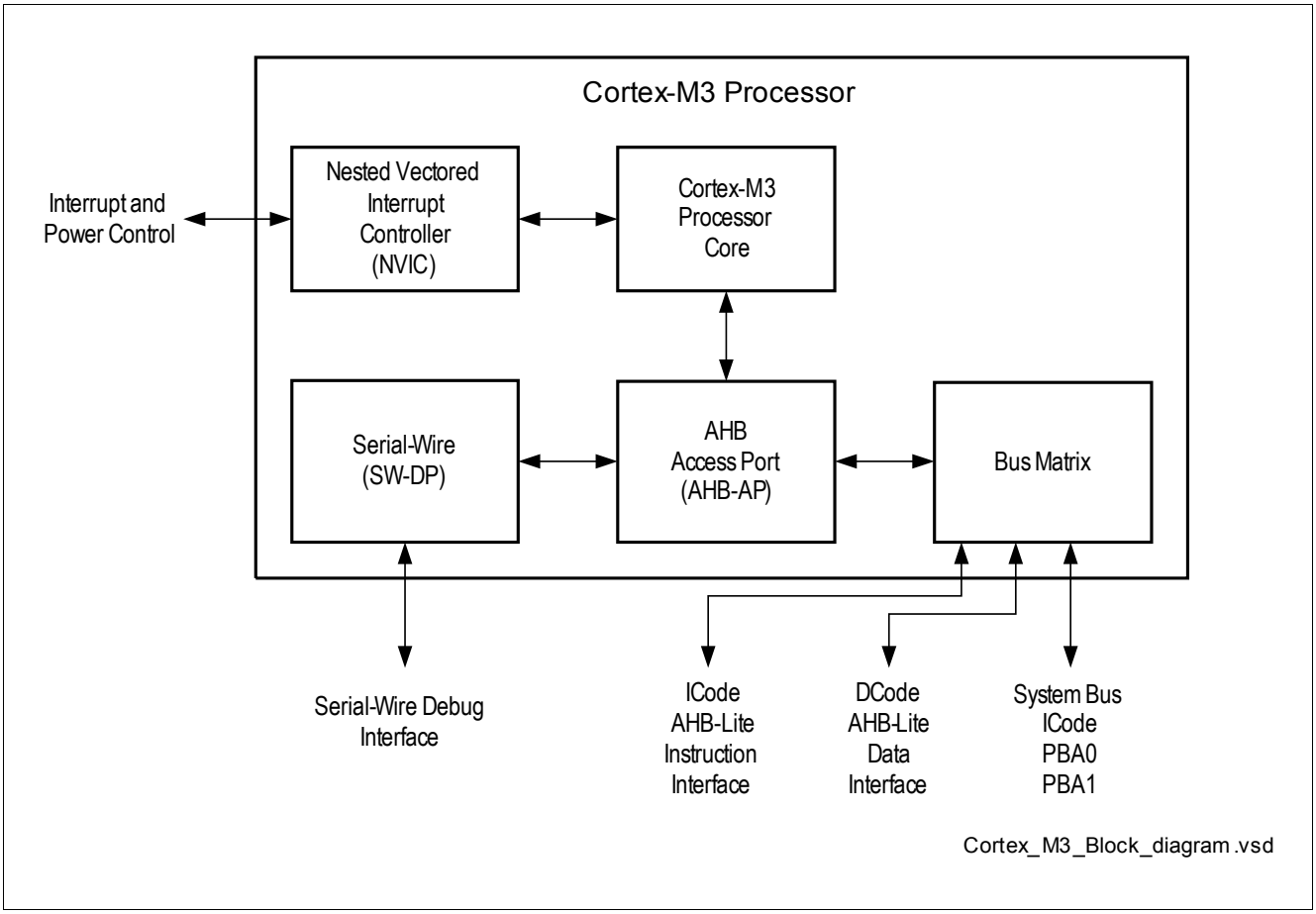


Figure 12 Cortex M3 Block Diagram

9 DMA Controller

Figure 13 shows the Top Level Block Diagram of the TLE9871QXA20.

The bus matrix allows the uDMA to access the PBA0, PBA1 and RAM.

9.1 Features

The principal features of the DMA Controller are that:

- it is compatible with AHB-Lite for the DMA transfers
- it is compatible with APB for programming the registers
- it has a single AHB-Lite master for transferring data using a 32-bit address bus and 32-bit data bus
- it supports 13 DMA channels
- each DMA channel has dedicated handshake signals
- each DMA channel has a programmable priority level
- each priority level arbitrates using a fixed priority that is determined by the DMA channel number. The DMA also supports multiple transfer types:
  - memory-to-memory
  - memory-to-peripheral
  - peripheral-to-memory
- it supports multiple DMA cycle types
- it supports multiple DMA transfer data widths
- each DMA channel can access a primary, and alternate, channel control data structure
- all the channel control data is stored in system memory (RAM) in little-endian format
- it performs all DMA transfers using the SINGLE AHB-Lite burst type. The destination data width is equal to the source data width.
- the number of transfers in a single DMA cycle can be programmed from 1 to 1024
- the transfer address increment can be greater than the data width

9.2 Introduction

Please also refer to **Chapter 9.3**, **Functional Description**.

9.2.1 Block Diagram

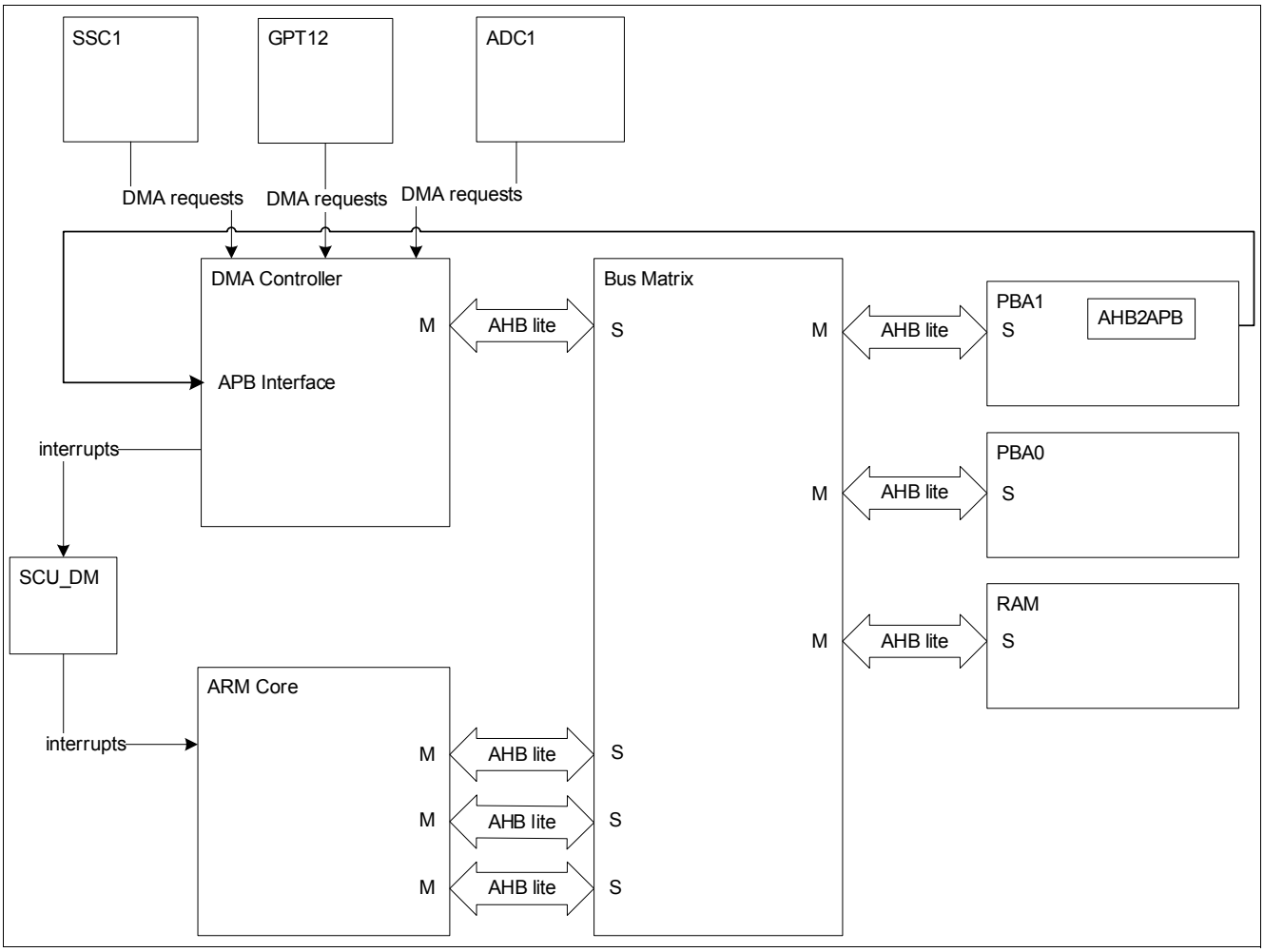


Figure 13 DMA Controller Top Level Block Diagram

9.3 Functional Description

9.3.1 DMA Mode Overview

The DMA controller implements the following 13 hardware DMA requests:

- ADC1 complete sequence 1 done: DMA transfer is requested on completion of the ADC1 channel conversion sequence.
- ADC1 exceptional sequence 2 (ESM) done: DMA transfer is requested on completion of the ADC1 conversion sequence triggered by an exceptional measurement request.
- SSC1/2 transmit byte: DMA transfer is requested upon the completion of data transmission via SSC1/2
- SSC1/2: receive byte: DMA transfer is requested upon the completion of data reception via SSC1/2.
- ADC1 channel 0 conversion done: DMA transfer is requested on completion of the ADC1 channel 0 conversion.
- ADC1 channel 1 conversion done: DMA transfer is requested on completion of the ADC1 channel 1 conversion.
- ADC1 channel 2 conversion done: DMA transfer is requested on completion of the ADC1 channel 2 conversion.
- ADC1 channel 3 conversion done: DMA transfer is requested on completion of the ADC1 channel 3 conversion.
- ADC1 channel 4 conversion done: DMA transfer is requested on completion of the ADC1 channel 4 conversion.
- ADC1 channel 5 conversion done: DMA transfer is requested on completion of the ADC1 channel 5 conversion.
- ADC1 channel 6 conversion done: DMA transfer is requested on completion of the ADC1 channel 6 conversion.
- ADC1 channel 7 conversion done: DMA transfer is requested on completion of the ADC1 channel 7 conversion.
- Timer3 ccu6_int: DMA transfer is requested following a timer trigger.

10 Address Space Organization

The TLE9871QXA20 manipulates operands in the following memory spaces:

- 36 kByte of Flash memory in code space
- 32 kByte Boot ROM memory in code space (used for boot code and IP storage)
- 3 kByte RAM memory in code space and data space (RAM can be read/written as program memory or external data memory)
- Special function registers (SFRs) in peripheral space

The figure below shows the detailed address alignment of TLE9871QXA20:

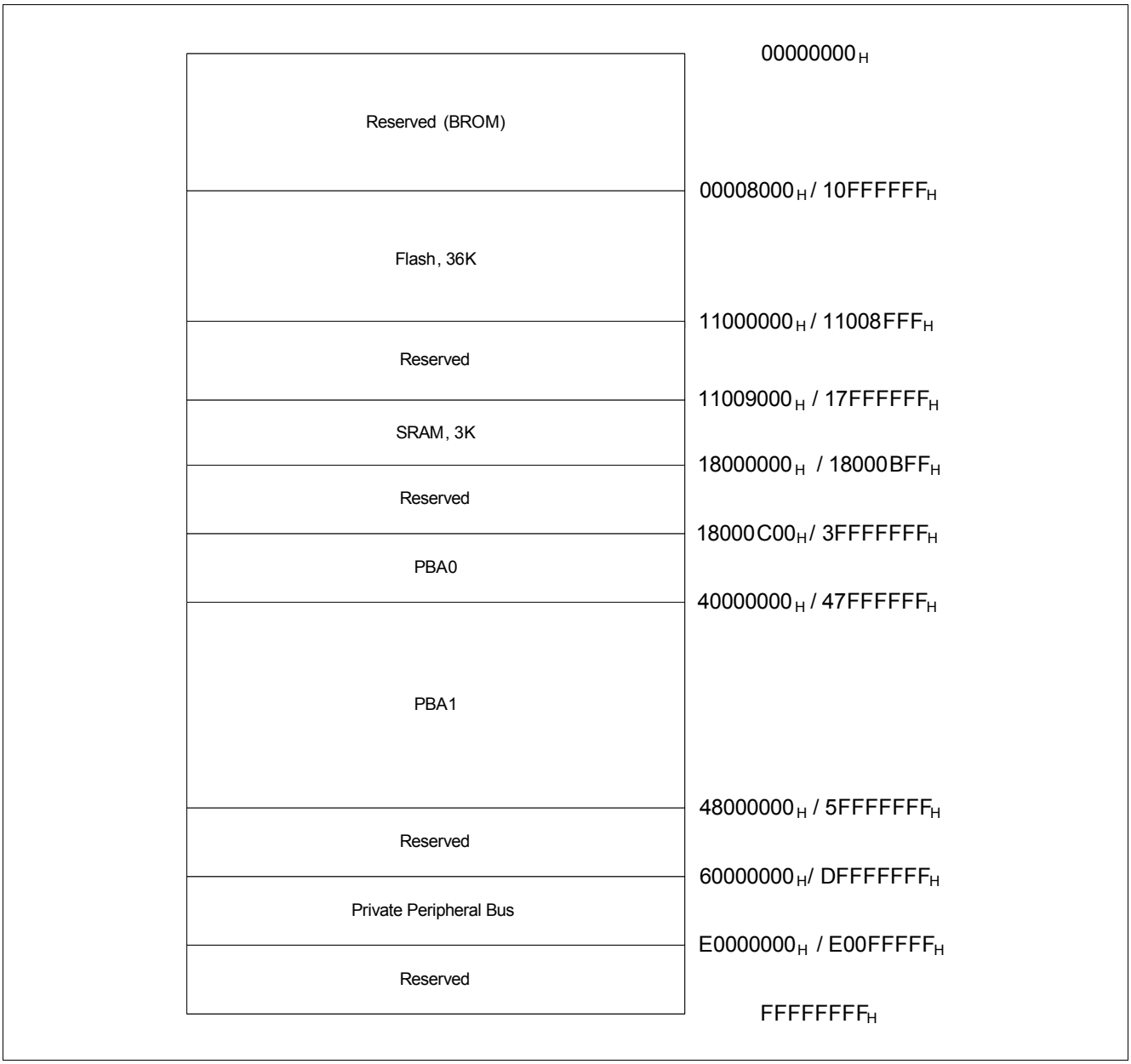


Figure 14 TLE9871QXA20 Memory Map

11 Memory Control Unit

11.1 Features

- Handles all system memories and their interaction with the CPU
- Memory protection functions for all system memories (D-Flash, P-Flash, RAM)
- Address management with access violation detection including reporting
- Linear address range for all memories (no paging)

11.2 Introduction

11.2.1 Block Diagram

The Memory Control Unit (MCU) is divided in the following sub-modules:

- NVM Memory module (embedded Flash Memory)
- RAM memory module
- BootROM memory module
- Memory Protection Unit (MPU) module

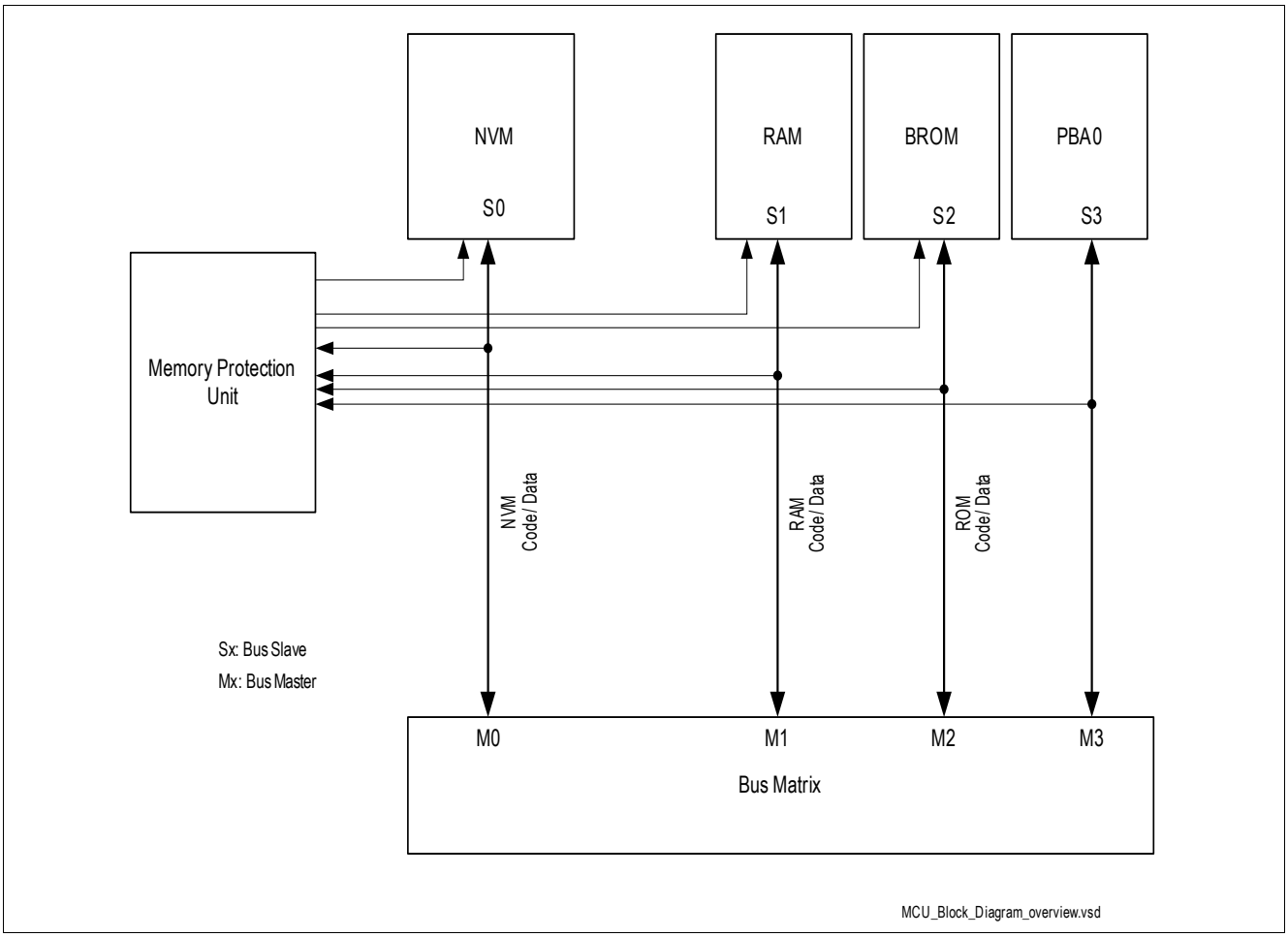


Figure 15 MCU Block View

11.3 NVM Module (Flash Memory)

The Flash Memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data.

Features

- In-system programming via PWM Interface (Flash Mode) and SWD
- Error Correction Code (ECC) for detection of single-bit and double-bit errors and dynamic correction of single Bit errors.
- Interrupts and signals double-bit error by NMI
- Program width of 128 byte (page)
- Minimum erase width of 128 bytes (page)
- Integrated hardware support for EEPROM emulation
- 8 byte read access
- Physical read access time: 75 ns
- Code read access acceleration integrated; read buffer and automatic pre-fetch
- Page program time: 3 ms
- Page erase (128 bytes) and sector erase (4K bytes) time: 4ms

Note: The user has to ensure that no flash operations which change the content of the flash get interrupted at any time.

The clock for the NVM is supplied with the system frequency fsys. Integrated firmware routines are provided to erase NVM, and other operations including EEPROM emulation are provided as well.

12 Interrupt System

12.1 Features

- Up to 16 interrupt nodes for on-chip peripherals
- Up to 8 NMI nodes for critical system events
- Maximum flexibility for all 16 interrupt nodes

12.2 Introduction

12.2.1 Overview

The TLE9871QXA20 supports 16 interrupt vectors with 16 priority levels. Fifteen of these interrupt vectors are assigned to the on-chip peripherals: GPT12, SSC, CCU6, DMA, Bridge Driver and A/D Converter are each assigned to one dedicated interrupt vector; while UART1 and Timer2 or UART2, External Interrupt 2 and Timer21 share interrupt vectors. Two vectors are dedicated for External Interrupt 0 and 1.

Table 6 Interrupt Vector Table

Service Request	Node ID	Description
GPT12	0/1	GPT interrupt (T2-T6, CAPIN)
MU- ADC8/T3	2	Measurement Unit, VBG, Timer3, BEMF
ADC1	3	ADC1 interrupt / VREF5V Overload / VREF5V OV/UV, 10-bit ADC
CCU0	4	CCU6 node 0 interrupt
CCU1	5	CCU6 node 1 interrupt
CCU2	6	CCU6 node 2 interrupt
CCU3	7	CCU6 node 3 interrupt
SSC1	8	SSC1 interrupt (receive, transmit, error)
SSC2	9	SSC2 interrupt (receive, transmit, error)
UART1	10	UART1 interrupt (receive, transmit), Timer2, PWM-Interface
UART2	11	UART2 interrupt (receive, transmit), Timer21, External interrupt (EINT2)
EXINT0	12	External interrupt (EINT0), MON
EXINT1	13	External interrupt (EINT1)
BDRV/CP	14	Bridge Driver / Charge Pump
DMA	15	DMA Controller

Table 7 NMI Interrupt Table

Service Request	Node	Description
Watchdog Timer NMI	NMI	Watchdog Timer overflow
PLL NMI	NMI	PLL Loss-of-Lock
NVM Operation Complete NMI	NMI	NVM Operation Complete
Overtemperature NMI	NMI	System Overtemperature

Table 7 NMI Interrupt Table

Service Request	Node	Description
Oscillator Watchdog NMI	NMI	Oscillator Watchdog / MI_CLK Watchdog Timer Overflow
NVM Map Error NMI	NMI	NVM Map Error
ECC Error NMI	NMI	RAM / NVM Uncorrectable ECC Error
Supply Prewarning NMI	NMI	Supply Prewarning

13 Watchdog Timer (WDT1)

13.1 Features

There are two watchdog timers in the system. The Watchdog Timer (WDT) within the System Control Unit - Digital Modules (see SCU_DM) and the Watchdog Timer (WDT1) located within the System Control Unit - Power Modules (see SCU_PM). The Watchdog Timer WDT1 is described in this section.

In Active Mode, the WDT1 acts as a windowed watchdog timer, which provides a highly reliable and safe way to recover from software or hardware failures.

The WDT1 is always enabled in Active Mode. In Sleep Mode, Low Power Mode and SWD Mode the WDT1 is automatically disabled.

Functional Features

- Windowed Watchdog Timer with programmable timing in Active Mode
- Long open window (typ. 80ms) after power-up, reset, wake-up
- Short open window (typ. 30ms) to facilitate Flash programming
- Disabled during debugging
- Safety shutdown to Sleep Mode after 5 missed WDT1 services

13.2 Introduction

The behavior of the Watchdog Timer in Active Mode is illustrated in **Figure 16**.

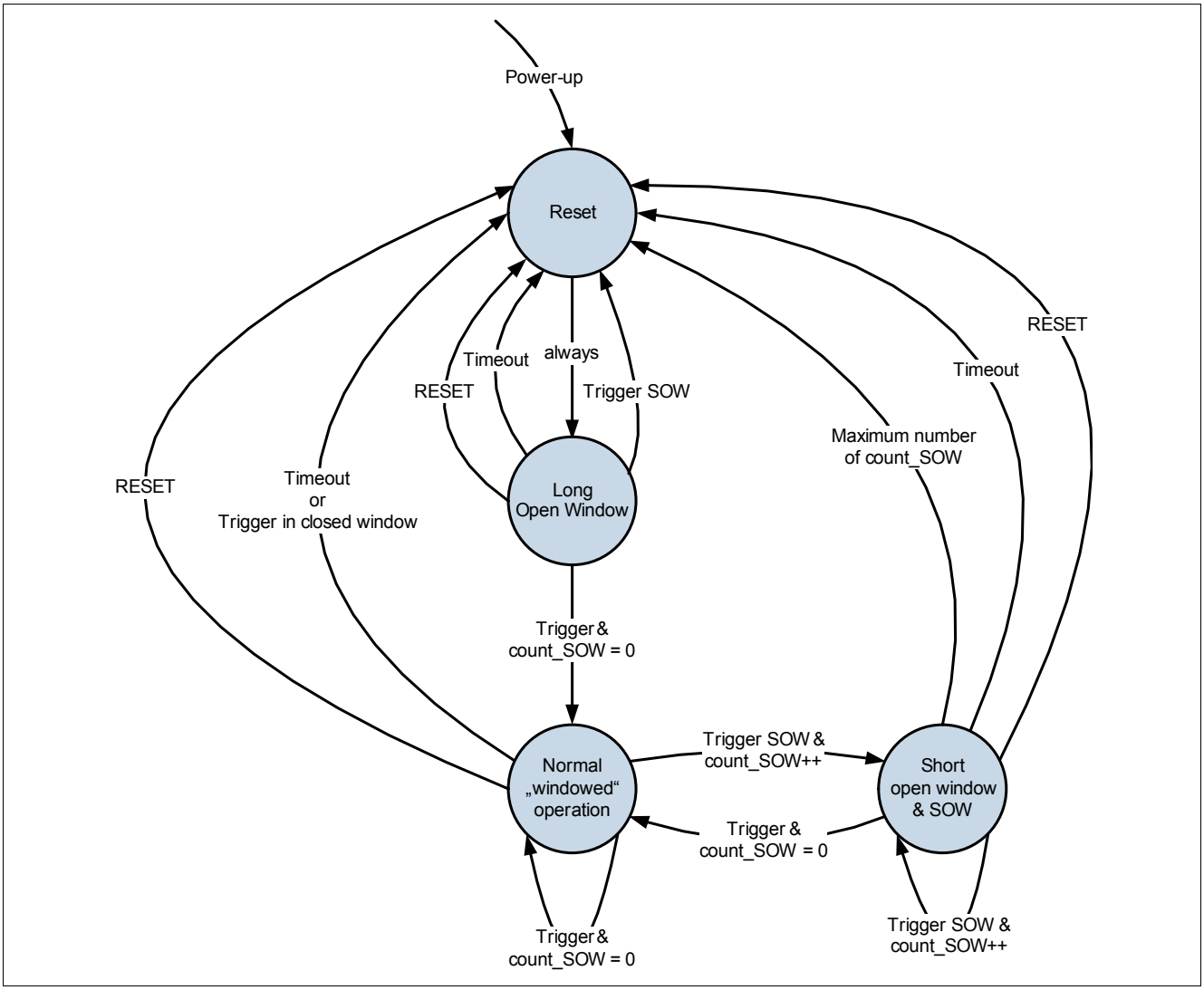


Figure 16 Watchdog Timer Behavior

14 GPIO Ports and Peripheral I/O

The TLE9871QXA20 has 15 port pins organized into three parallel ports: Port 0 (P0), Port 1 (P1) and Port 2 (P2). Each port pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. P0 and P1 are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected. On Port 2 (P2) analog inputs are shared with general purpose input.

14.1 Features

Bidirectional Port Features (P0, P1)

- Configurable pin direction
- Configurable pull-up/pull-down devices
- Configurable open drain mode
- Configurable drive strength
- Transfer of data through digital inputs and outputs (general purpose I/O)
- Alternate input/output for on-chip peripherals

Analog Port Features (P2)

- Configurable pull-up/pull-down devices
- Transfer of data through digital inputs
- Alternate inputs for on-chip peripherals

14.2 Introduction

14.2.1 Port 0 and Port 1

Figure 17 shows the block diagram of an TLE9871QXA20 bidirectional port pin. Each port pin is equipped with a number of control and data bits, thus enabling very flexible usage of the pin. By defining the contents of the control register, each individual pin can be configured as an input or an output. The user can also configure each pin as an open drain pin with or without internal pull-up/pull-down device.

Each bidirectional port pin can be configured for input or output operation. Switching between input and output mode is accomplished through the register Px_DIR (x = 0 or 1), which enables or disables the output and input drivers. A port pin can only be configured as either input or output mode at any one time.

In input mode (default after reset), the output driver is switched off (high-impedance). The actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt trigger device and can be read via the register Px_DATA.

In output mode, the output driver is activated and drives the value supplied through the multiplexer to the port pin. In the output driver, each port line can be switched to open drain mode or normal mode (push-pull mode) via the register Px_OD.

The output multiplexer in front of the output driver enables the port output function to be used for different purposes. If the pin is used for general purpose output, the multiplexer is switched by software to the data register Px_DATA. Software can set or clear the bit in Px_DATA and therefore directly influence the state of the port pin. If an on-chip peripheral uses the pin for output signals, alternate output lines (AltDataOut) can be switched via the multiplexer to the output driver circuitry. Selection of the alternate output function is defined in registers

Px_ALTSEL0 and Px_ALTSEL1. When a port pin is used as an alternate function, its direction must be set accordingly in the register Px_DIR.

Each pin can also be programmed to activate an internal weak pull-up or pull-down device. Register Px_PUDSEL selects whether a pull-up or the pull-down device is activated while register Px_PUDEN enables or disables the pull device.

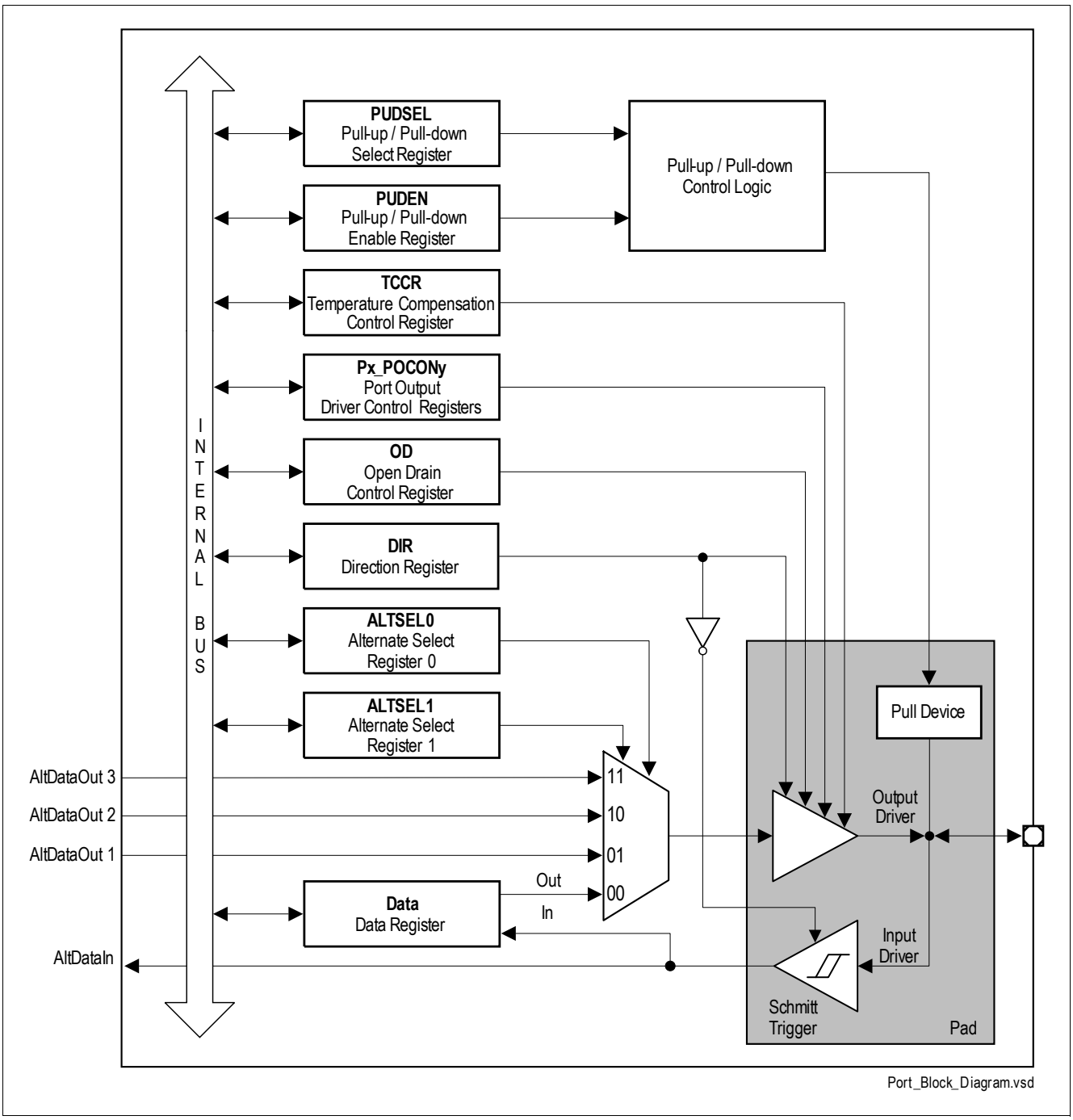


Figure 17 General Structure of Bidirectional Port (P0, P1)

14.2.2 Port 2

Figure 18 shows the structure of an input-only port pin. Each P2 pin can only function in input mode. Register P2_DIR is provided to enable or disable the input driver. When the input driver is enabled, the actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt trigger device and can be read via register P2_DATA. Each pin can also be programmed to activate an internal weak pull-up or pull-down device. Register P2_PUDSEL selects whether a pull-up or the pull-down device is activated while register P2_PUDEN enables or disables the pull device. The analog input (AnalogIn) bypasses the digital circuitry and Schmitt trigger device for direct feed-through to the ADC input channels.

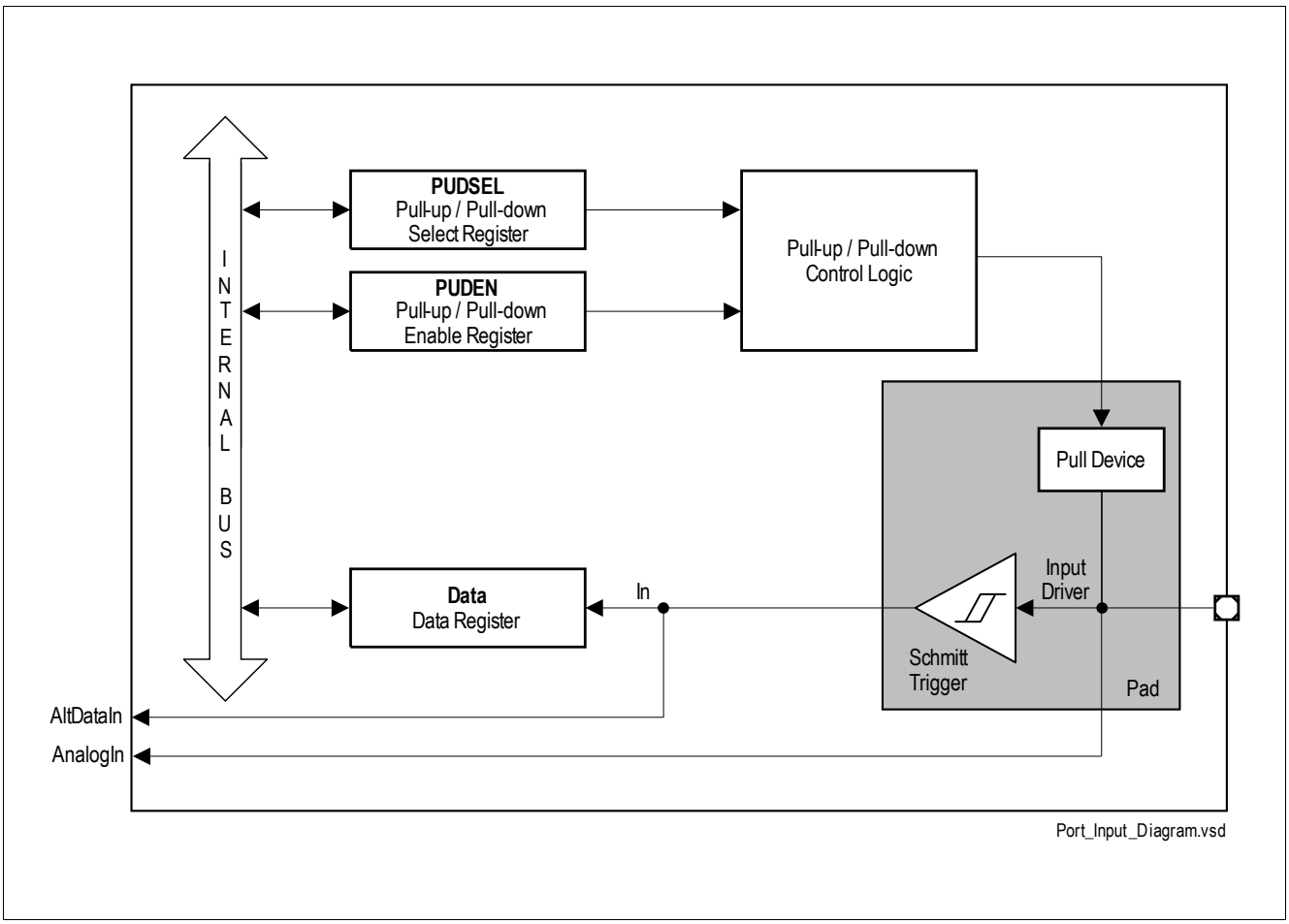


Figure 18 General Structure of Input Port (P2)

14.3 TLE9871QXA20 Port Module

14.3.1 Port 0

14.3.1.1 Port 0 Functions

Table 8 Port 0 Input/Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P0.0	Input	GPI	P0_DATA.P0	
		INP1	SWCLK / TCK_0	SW
		INP2	T12HR_0	CCU6
		INP3	T4INA	GPT12T4
		INP4	T2_0	Timer 2
		INP5	–	–
		INP6	EXINT2_3	SCU
	Output	GPO	P0_DATA.P0	
		ALT1	T3OUT	GPT12T3
		ALT2	EXF21_0	Timer 21
		ALT3	RXDO_2	UART2
P0.1	Input	GPI	P0_DATA.P1	
		INP2	T13HR_0	CCU6
		INP3	TxD1	PWM_TxD
		INP4	CAPINA	GPT12CAP
		INP5	T21_0	Timer 21
		INP6	T4INC	GPT12T4
		INP7	MRST_1_2	SSC1
		INP8	EXINT0_2	SCU
	Output	GPO	P0_DATA.P1	
		ALT1	TxD1	UART1 / PWM_TxD
		ALT2	–	–
		ALT3	T6OUT	GPT12T6

Table 8 Port 0 Input/Output Functions (cont'd)

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P0.2	Input	GPI	P0_DATA.P2	
		INP1	CCPOS2_1	CCU6
		INP2	T2EUDA	GPT12T2
		INP3	MTSR_1	SSC1
		INP4	T21EX_0	Timer 21
		INP5	T6INA	GPT12T6
	Output	GPO	P0_DATA.P2	–
		ALT1	COUT60_0	CCU6
		ALT2	MTSR_1	SSC1
		ALT3	EXF2_0	Timer 2
P0.3	Input	GPI	P0_DATA.P3	
		INP1	SCK_1	SSC1
		INP2	CAPINB	GPT12
		INP3	T5INA	GPT12T5
		INP4	T4EUDA	GPT12T4
		INP5	CCPOS0_1	CCU6
	Output	GPO	P0_DATA.P3	
		ALT1	SCK_1	SSC1
		ALT2	EXF21_2	Timer 21
		ALT3	T6OUT	GPT12T6
P0.4	Input	GPI	P0_DATA.P4	
		INP1	MRST_1_0	SSC1
		INP2	CC60_0	CCU6
		INP3	T21_2	Timer 21
		INP4	EXINT2_2	SCU
		INP5	T3EUDA	GPT12T3
		INP6	CCPOS1_1	CCU6
	Output	GPO	P0_DATA.P4	
		ALT1	MRST_1_0	SSC1
		ALT2	CC60_0	CCU6
		ALT3	CLKOUT_0	SCU

14.3.2 Port 1

14.3.2.1 Port 1 Functions

Table 9 Port 1 Input / Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P1.0	Input	GPI	P1_DATA.P0	
		INP1	T3INC	GPT12T3
		INP2	T4EUDB	GPT12T4
		INP3	CC61_0	CCU6
		INP4	SCK_2	SSC2
		INP5	EXINT1_2	SCU
	Output	GPO	P1_DATA.P0	
		ALT1	SCK_2	SSC2
		ALT2	CC61_0	CCU6
		ALT3	EXF21_3	Timer 21
P1.1	Input	GPI	P1_DATA.P1	
		INP1	–	–
		INP2	T6EUDA	GPT12T6
		INP3	–	-
		INP4	MTSR_2	SSC2
		INP5	T21_1	Timer 21
		INP6	EXINT1_0	SCU
	Output	GPO	P1_DATA.P1	–
		ALT1	MTSR_2	SSC2
		ALT2	COUT61_0	CCU6
		ALT3	TXD2_0	UART2
P1.2	Input	GPI	P1_DATA.P2	
		INP1	T2INA	GPT12T2
		INP2	T2EX_1	Timer 2
		INP3	T21EX_3	Timer 21
		INP4	MRST_2_0	SSC2
		INP5	RXD2_0	UART2
		INP6	CCPOS2_2	CCU6
		INP7	EXINT0_1	SCU
	Output	GPO	P1_DATA.P2	
		ALT1	MRST_2_0	SSC2
		ALT2	COUT63_0	CCU6
		ALT3	T3OUT	GPT12T3

Table 9 Port 1 Input / Output Functions (cont'd)

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P1.3	Input	GPI	P1_DATA.P3	
		INP1	T6INB	GPT12T6
		INP2	–	
		INP3	CC62_0	CCU6
		INP4	T6EUDB	GPT12T6
		INP5	–	
		INP6	CCPOS0_2	CCU6
		INP7	EXINT1_1	SCU
	Output	GPO	P1_DATA.P3	
		ALT1	EXF21_1	Timer 21
		ALT2	CC62_0	CCU6
		ALT3	TXD2_1	UART2
P1.4	Input	GPI	P1_DATA.P4	
		INP1	EXINT2_1	SCU
		INP2	T21EX_1	Timer 21
		INP3	T5EUDA	GPT12T5
		INP4	RxD1	UART1
		INP5	T2INB	GPT12T2
		INP6	CCPOS1_2	CCU6
		INP7	MRST_1_3	SSC1
	Output	GPO	P1_DATA.P4	
		ALT1	CLKOUT_1	SCU
		ALT2	COUT62_0	CCU6
		ALT3	RxD1	UART1 / PWM_RxD

14.3.3 Port 2

14.3.3.1 Port 2 Functions

Table 10 Port 2 Input Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P2.0	Input	GPI	P2_DATA.P0	
		INP1	CCPOS0_3	CCU6
		INP2	-	-
		INP3	T12HR_2	CCU6
		INP4	EXINT0_0	SCU
		INP5	CC61_2	CCU6
		ANALOG	AN0	ADC
			XTAL (in)	XTAL
P2.2	Input	GPI	P2_DATA.P2	
		INP1	CCPOS2_3	CCU6
		INP2	T13HR_2	CCU6
		INP3	–	
		INP4	CC62_2	CCU6
		ANALOG	AN2	ADC
		OUT	XTAL (out)	XTAL
P2.3	Input	GPI	P2_DATA.P3	
		INP1	CCPOS1_0	CCU6
		INP2	T3IND	GPT12T3
		INP3	CTRAP#_1	CCU6
		INP4	T21EX_2	Timer 21
		INP5	CC60_1	CCU6
		INP6	EXINT0_3	SCU
		ANALOG	AN3	ADC
P2.4	Input	GPI	P2_DATA.P4	
		INP1	$\overline{\text{CTRAP\#_0}}$	CCU6
		INP2	T2EUDB	GPT12T2
		INP3	MRST_1_1	SSC1
		INP4	EXINT1_3	SCU
		ANALOG	AN4	ADC
P2.5	Input	GPI	P2_DATA.P5	
		INP1	RXD2_1	UART2
		INP2	T3EUDB	GPT12T3
		INP3	MRST_2_1	SSC2
		INP4	T2_1	Timer 2
		ANALOG	AN5	ADC

15 General Purpose Timer Units (GPT12)

15.1 Features

15.1.1 Features Block GPT1

The following list summarizes the supported features:

- f_{GPT}/4 maximum resolution
- 3 independent timers/counters
- Timers/counters can be concatenated
- 4 operating modes:
  - Timer Mode
  - Gated Timer Mode
  - Counter Mode
  - Incremental Interface Mode
- Reload and Capture functionality
- Shared interrupt: Node 0

15.1.2 Features Block GPT2

The following list summarizes the supported features:

- f_{GPT}/2 maximum resolution
- 2 independent timers/counters
- Timers/counters can be concatenated
- 3 operating modes:
  - Timer Mode
  - Gated Timer Mode
  - Counter Mode
- Extended capture/reload functions via 16-bit capture/reload register CAPREL
- Shared interrupt: Node 1

15.2 Introduction

The General Purpose Timer Unit blocks GPT1 and GPT2 have very flexible multifunctional timer structures which may be used for timing, event counting, pulse width measurement, pulse generation, frequency multiplication, and other purposes.

They incorporate five 16-bit timers that are grouped into the two timer blocks GPT1 and GPT2. Each timer in each block may operate independently in a number of different modes such as Gated timer or Counter Mode, or may be concatenated with another timer of the same block.

Each block has alternate input/output functions and specific interrupts associated with it. Input signals can be selected from several sources by register PISEL.

The GPT module is clocked with clock f_{GPT}. f_{GPT} is a clock derived from f_{SYS}.

15.2.1 Block Diagram GPT1

Block GPT1 contains three timers/counters: The core timer T3 and the two auxiliary timers T2 and T4. The maximum resolution is $f_{GPT}/4$. The auxiliary timers of GPT1 may optionally be configured as reload or capture registers for the core timer.

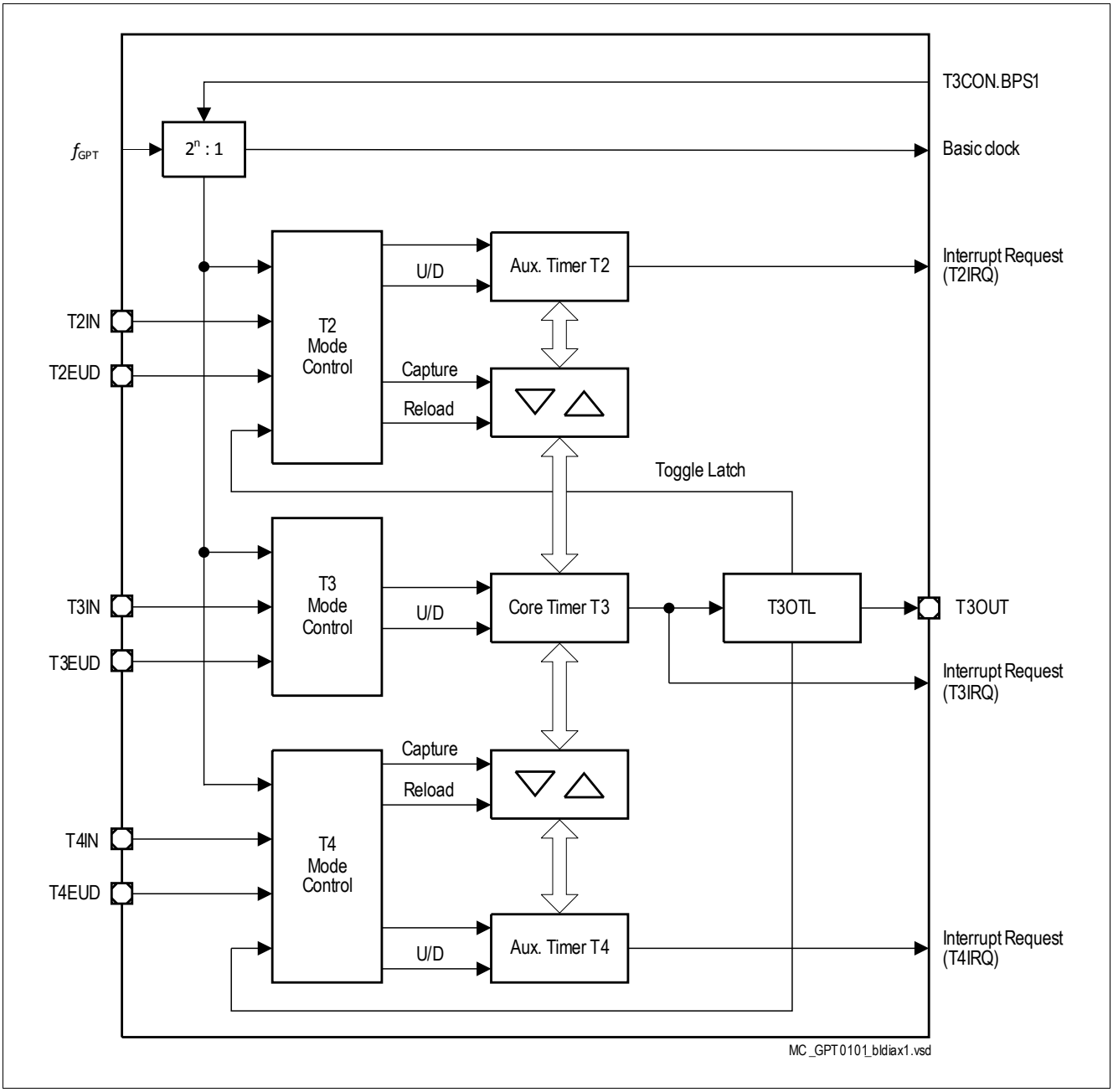


Figure 19 GPT1 Block Diagram (n = 2 … 5)

15.2.2 Block Diagram GPT2

Block GPT2 contains two timers/counters: The core timer T6 and the auxiliary timer T5. The maximum resolution is $f_{GPT}/2$. An additional Capture/Reload register (CAPREL) supports capture and reload operation with extended functionality.

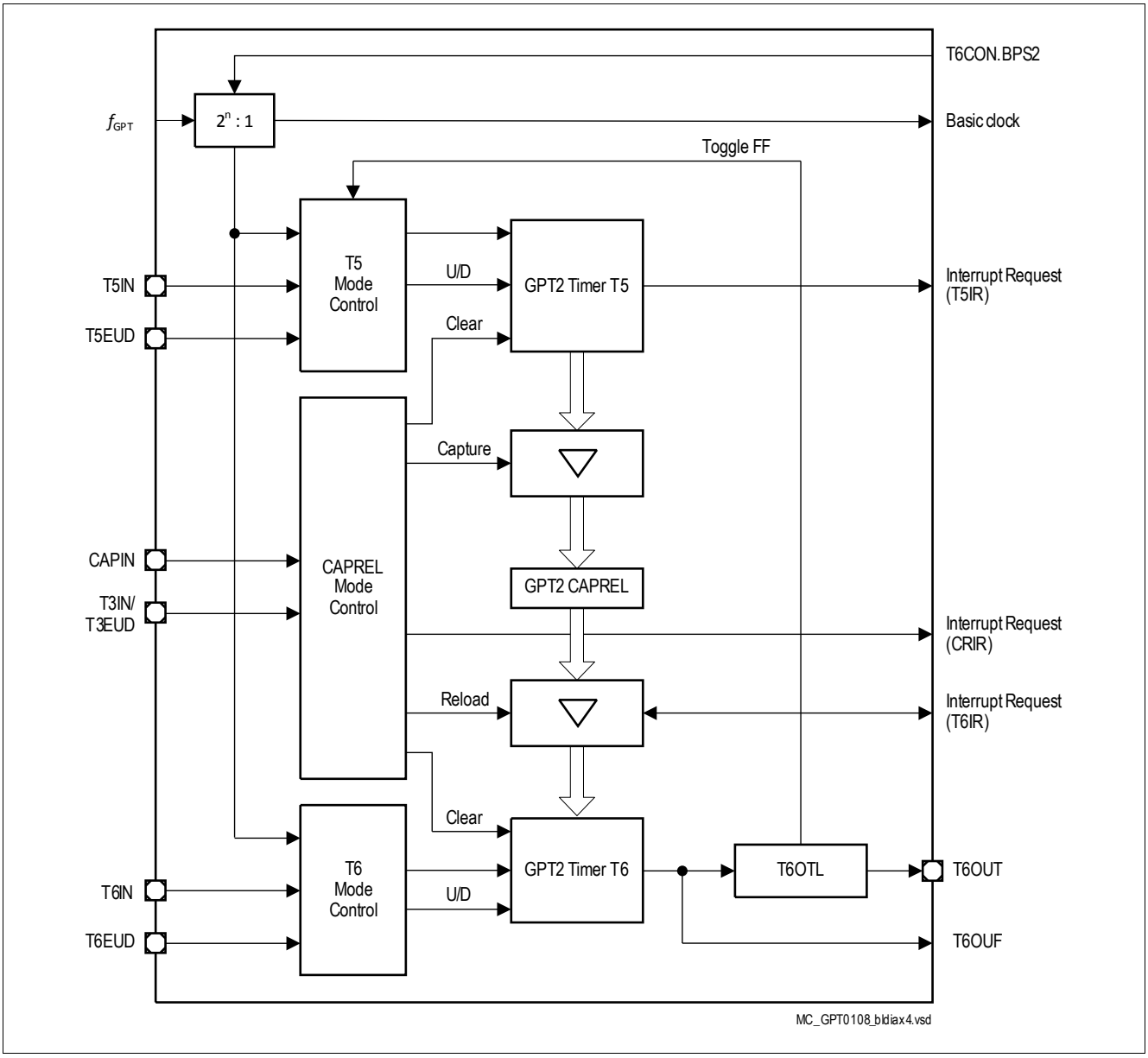


Figure 20 GPT2 Block Diagram

16 Timer2 and Timer21

16.1 Features

- 16-bit auto-reload mode
  - selectable up or down counting
- One channel 16-bit capture mode

16.2 Introduction

The timer modules are general-purpose 16-bit timers. Timer 2/21 can function as a timer or counter in each of its modes. As a timer, it counts with an input clock of $f_{PCLK}/12$ (if prescaler is disabled). As a counter, Timer 2 counts 1-to-0 transitions on pin T2. In the counter mode, the maximum resolution for the count is $f_{PCLK}/24$ (if prescaler is disabled).

16.2.1 Timer2 and Timer21 Modes Overview

Table 11 Timer2 and Timer21 Modes

Mode	Description
Auto-reload	**Up/Down Count Disabled** • Count up only • Start counting from 16-bit reload value, overflow at $FFFF_H$ • Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well • Programmable reload value in register RC2 • Interrupt is generated with reload events.
Auto-reload	**Up/Down Count Enabled** • Count up or down, direction determined by level at input pin T2EX • No interrupt is generated • Count up – Start counting from 16-bit reload value, overflow at $FFFF_H$ – Reload event triggered by overflow condition – Programmable reload value in register RC2 • Count down – Start counting from $FFFF_H$, underflow at value defined in register RC2 – Reload event triggered by underflow condition – Reload value fixed at $FFFF_H$
Channel capture	• Count up only • Start counting from 0000_H, overflow at $FFFF_H$ • Reload event triggered by overflow condition • Reload value fixed at 0000_H • Capture event triggered by falling/rising edge at pin T2EX • Captured timer value stored in register RC2 • Interrupt is generated by reload or capture events

17 Timer3

17.1 Features

- 16-bit incremental timer/counter (counting up)
- Counting frequency up to f_{sys}
- Selectable clock prescaler
- 6 modes of operation
- Interrupt up on overflow
- Interrupt on compare

17.2 Introduction

The possible applications for the timer include measuring the time interval between events, counting events and generating a signal at regular intervals.

Timer3 can function as timer or counter. When functioning as a timer, Timer3 is incremented in periods based on the MI_CLK or LP_CLK clock. When functioning as a counter, Timer3 is incremented in response to a 1-to-0 transition (falling edge) at its respective input. Timer3 can be configured in four different operating modes to use in a variety of applications, see **Table 12**.

Several operating modes can be used for different tasks such as the following:

- simple time measurement between two events
- triggering of the measuring unit upon PWM/CCU6 unit
- measurement of the 100kHz LP_CLK2

17.3 Functional Description

Six modes of operation are provided to fulfill various tasks using this timer. In every mode the clocking source can be selected between MI_CLK and LP_CLK. A prescaler provides in addition capability to divide the selected clock source by 2, 4 or 8. The timer counts upwards, starting with the value in the timer count registers, until the maximum count value which depends on the selected mode of operation. Timer 3 provides two individual interrupts upon counter overflow, one for the low-byte and one for the high-byte counter register.

17.3.1 Timer3 Modes Overview

The following table provides an overview of the timer modes together with the reasonable configuration options in **Table 12**.

Table 12 Timer3 Modes

Mode	Sub-Mode	Operation
0	**No Sub-Mode**	**13-bit Timer** The timer is essentially an 8-bit counter with a divide-by-32 prescaler.
1	**a**	**16-bit Timer** The timer registers, TL3 and TH3, are concatenated to form a 16-bit counter.
1	**b**	**16-bit Timer triggered by an event** The timer registers, TL3 and TH3, are concatenated to form a 16-bit counter, which is triggered by an event to enable a single shot measurement on a preset channel with the measurement unit.

Table 12 Timer3 Modes (cont'd)

Mode	Sub-Mode	Operation
2	**No Sub-Mode**	**8-bit Timer with auto-reload** The timer register TL3 is reloaded with a user-defined 8-bit value in TH3 upon overflow.
3	**a**	**Timer3 operates as two 8-bit timers** The timer registers TL3 and TH3, operate as two separate 8-bit counters.
3	**b**	**Timer3 operates as Two 8-bit timers for clock measurement** The timer registers, TL3 and TH3 operate as two separate 8-bit counters. In this mode the LP_CLK2 Low Power Clock can be measured. TL3 acts as an edge counter for the clock edges and TH3 as a counter which counts the time between the edges.

18 Capture/Compare Unit 6 (CCU6)

18.1 Feature Set Overview

This section gives an overview over the different building blocks and their main features.

Timer 12 Block Features

- Three capture/compare channels, each channel can be used either as capture or as compare channel
- Generation of a three-phase PWM supported (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of T12 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events
- Multiple interrupt request sources
- Hysteresis-like control mode

Timer 13 Block Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Concurrent update of T13 registers
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events

Additional Specific Functions

- Block commutation for brushless DC-drives implemented
- Position detection via hall-sensor pattern
- Noise filter supported for position input signals
- Automatic rotational speed measurement and commutation control for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

18.2 Introduction

The CCU6 unit is made up of a Timer T12 block with three capture/compare channels and a Timer T13 block with one compare channel. The T12 channels can independently generate PWM signals or accept capture triggers, or they can jointly generate control signal patterns to drive DC-motors or inverters.

A rich set of status bits, synchronized updating of parameter values via shadow registers, and flexible generation of interrupt request signals provide efficient software-control.

Note: The capture/compare module itself is referred to as CCU6 (capture/compare unit 6). A capture/compare channel inside this module is referred to as CC6x.

The timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined (e.g. a channel works in compare mode, whereas another channel works in capture mode). The timer T13 can work in compare mode only. The multi-channel control unit generates output patterns which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

18.2.1 Block Diagram

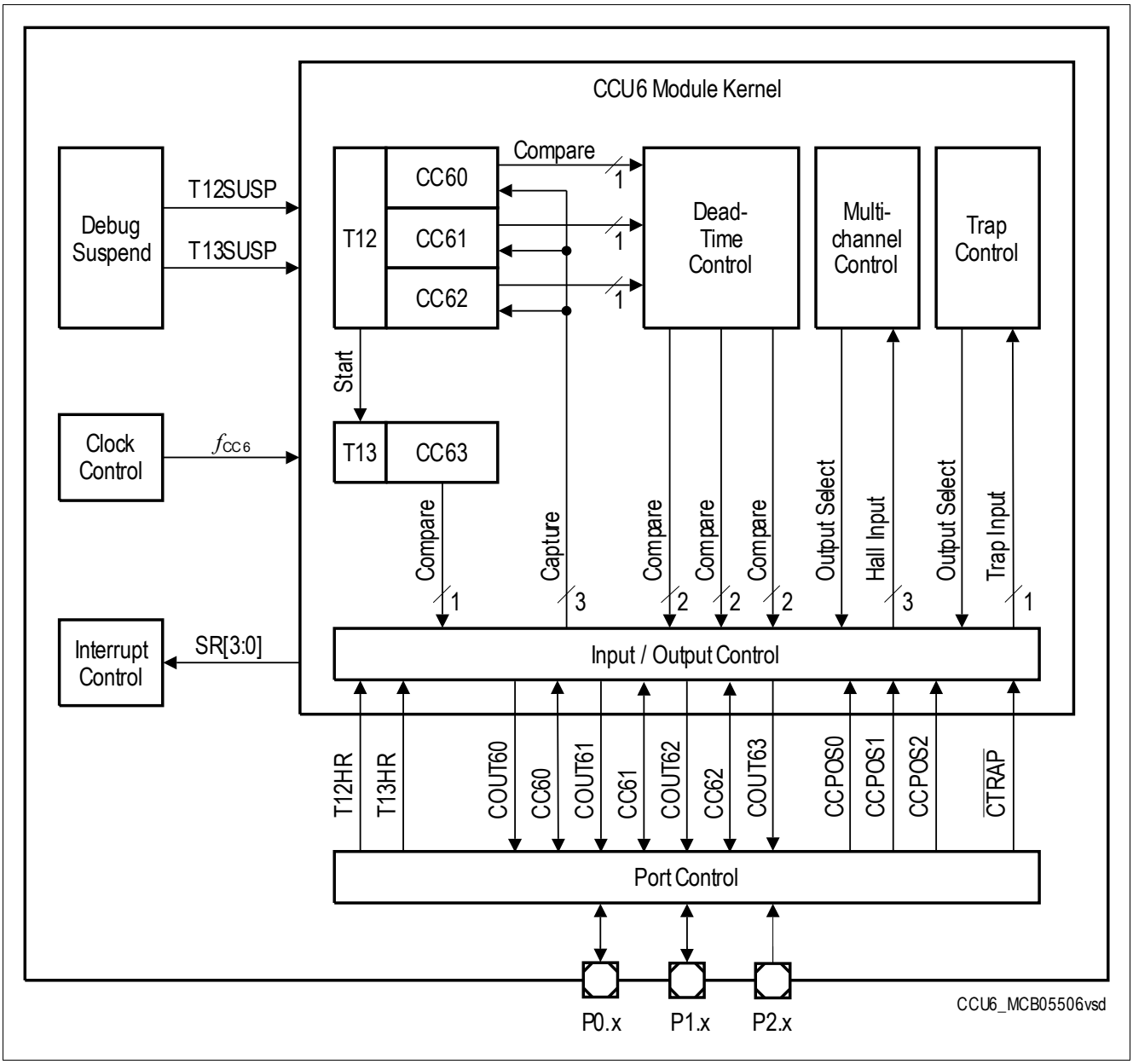


Figure 21 CCU6 Block Diagram

19 UART1/UART2

19.1 Features

- Full-duplex asynchronous modes
  - 8-bit or 9-bit data frames, LSB first
  - fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception
- Baud-rate generator with fractional divider for generating a wide range of baud rates
- Hardware logic for break and synch byte detection

19.2 Introduction

The UART provides a full-duplex asynchronous receiver/transmitter, i.e., it can transmit and receive simultaneously. It is also receive-buffered, i.e., it can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost. The serial port receive and transmit registers are both accessed at Special Function Register (SFR) SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

19.2.1 Block Diagram

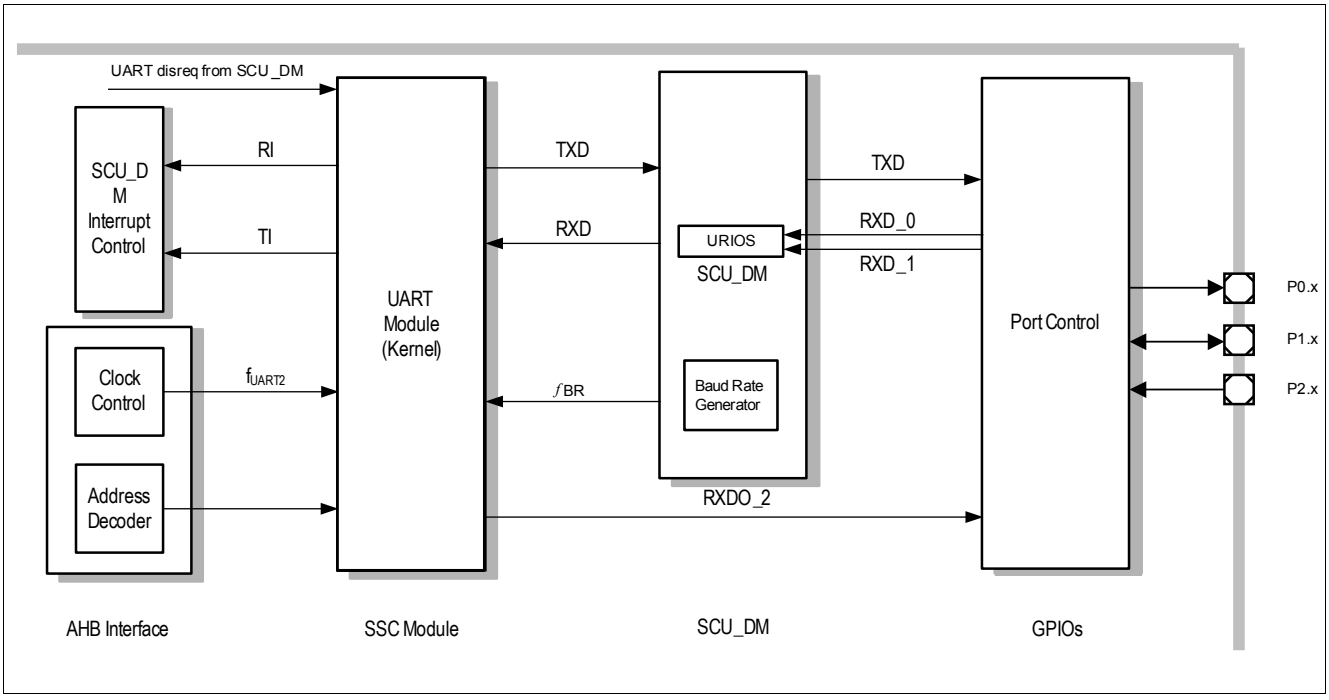


Figure 22 UART Block Diagram

19.3 UART Modes

The UART can be used in four different modes. In mode 0, it operates as an 8-bit shift register. In mode 1, it operates as an 8-bit serial port. In modes 2 and 3, it operates as a 9-bit serial port. The only difference between mode 2 and mode 3 is the baud rate, which is fixed in mode 2 but variable in mode 3. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator.

The different modes are selected by setting bits SM0 and SM1 to their corresponding values, as shown in Table 13.

Table 13 UART Modes

SM0	SM1	Operating Mode	Baud Rate
0	0	Mode 0: 8-bit shift register	$f_{PCLK}/2$
0	1	Mode 1: 8-bit shift UART	Variable
1	0	Mode 2: 9-bit shift UART	$f_{PCLK}/64$
1	1	Mode 3: 9-bit shift UART	Variable

The UART1 is connected to the integrated PWM interface, and to GPIO for test purpose. The UART2 is connected to GPIO only.

20 High Voltage PWM Interface

20.1 Features

General Functional Features

- Bidirectional High Voltage PWM interface

Special Features

- PWM interface can be used as a high voltage input/output with dedicated SFR control bits.

Operation Modes Features

- High Voltage Input / Output Mode (HVIO)

Supported Baudrates

- up to 57.6 kHz

Slope Modes Features

- Normal Slope Mode (10 kHz)
- Low Slope Mode (5.2 kHz)
- Flash Mode (57.6 kHz)

Wake-Up Features

- High Voltage PWM Interface wake-up

20.2 Introduction

The high voltage bidirectional PWM Module is a robust physical layer interface for PWM communication.

The bidirectional PWM Module offers two different operation modes, including a Sleep Mode and the High Voltage Input Output Mode.

20.2.1 Block Diagram

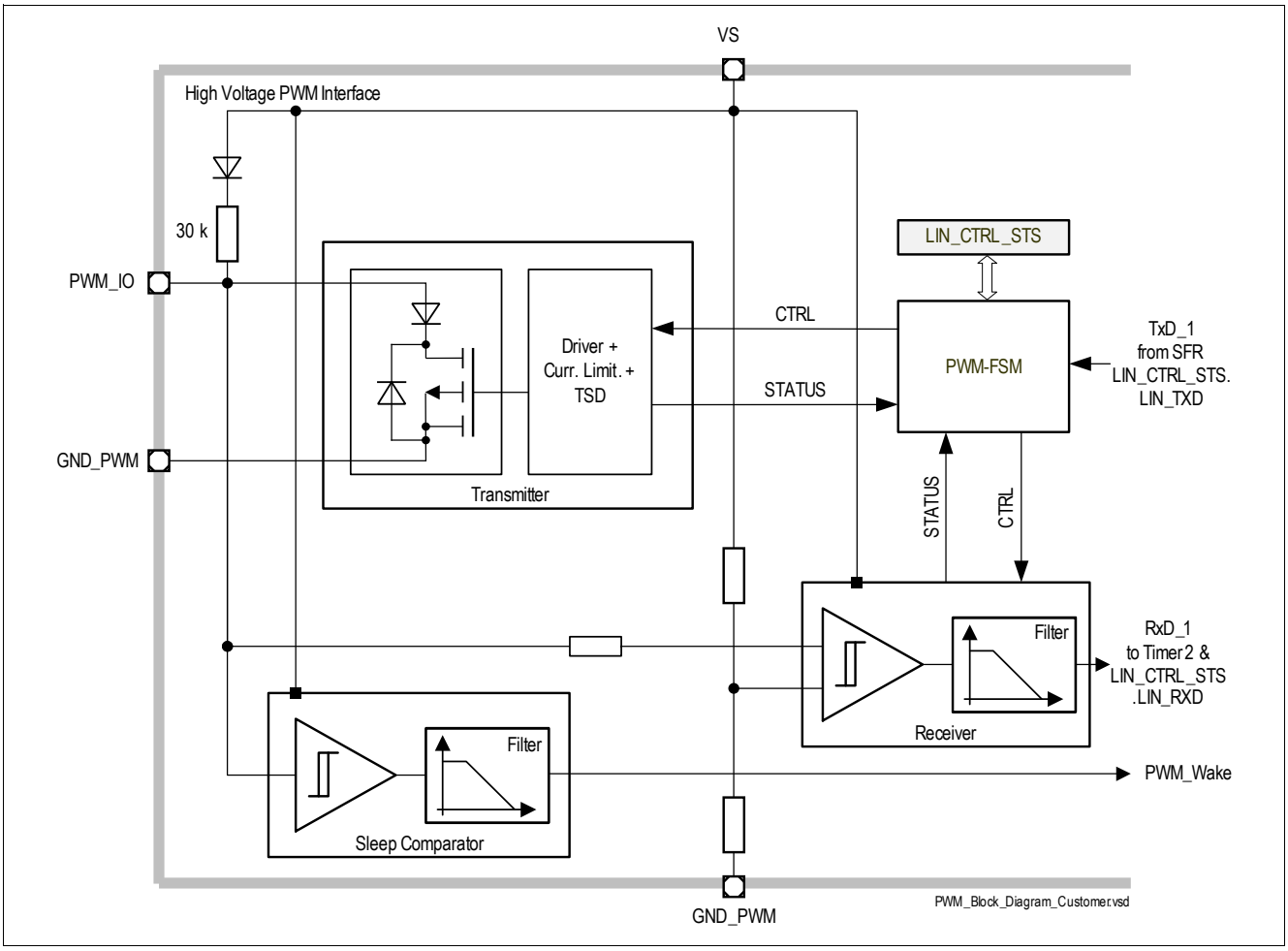


Figure 23 PWM Interface Block Diagram

21 High-Speed Synchronous Serial Interface (SSC1/SSC2)

21.1 Features

- Master and Slave Mode operation
  - Full-duplex or half-duplex operation
- Transmit and receive buffered
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: Least Significant Bit (LSB) or Most Significant Bit (MSB) shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
  - On a transmitter empty condition
  - On a “receiver full” condition
  - On an error condition (receive, phase, baud rate, transmission error)

21.2 Introduction

The High-Speed Synchronous Serial Interface (SSC) supports both full-duplex and half-duplex serial synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-bit baud rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity, and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

Data is transmitted or received on TXD and RXD lines, which are normally connected to the MTSR (MasterTransmit/Slave Receive) and MRST (Master Receive/Slave Transmit) pins. The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

21.2.1 Block Diagram

Figure 24 shows all functional relevant interfaces associated with the SSC Kernel.

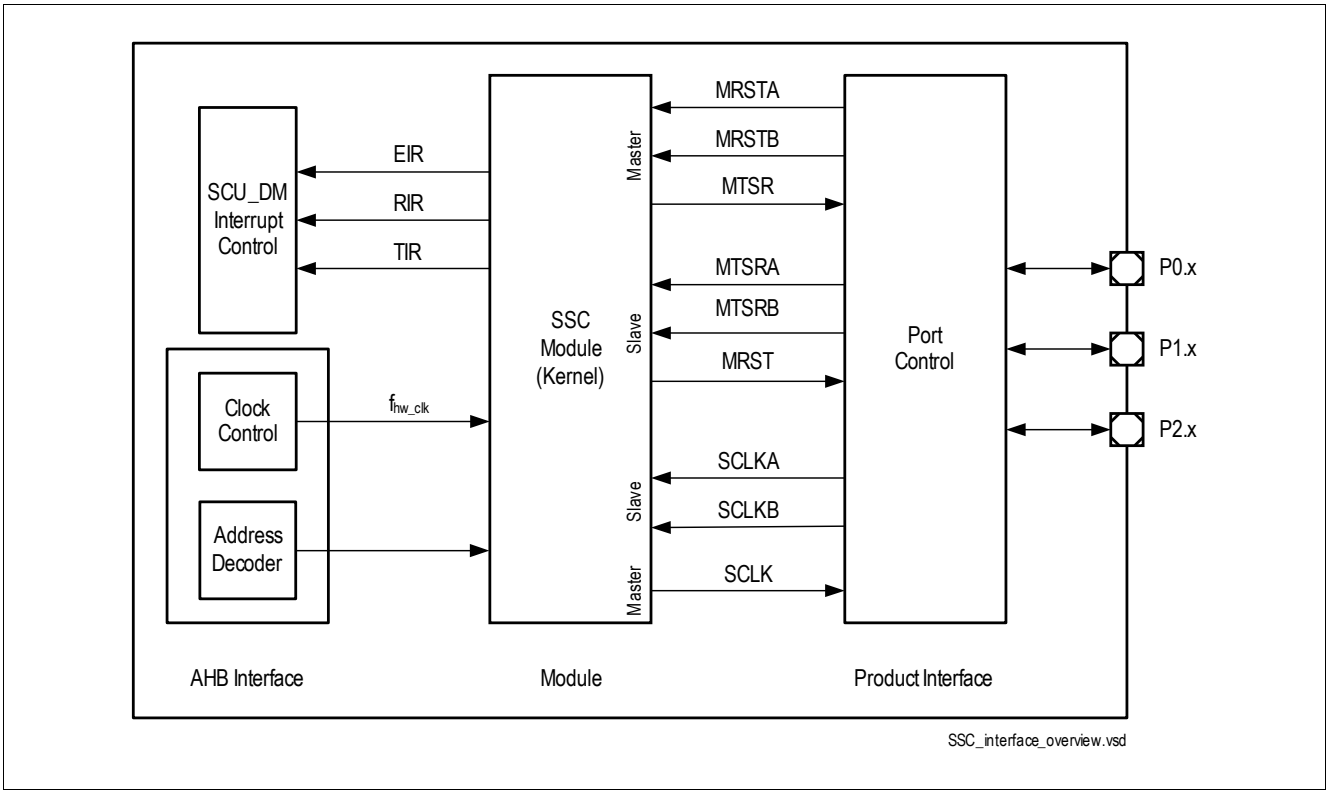


Figure 24 SSC Interface Diagram

22 Measurement Unit

22.1 Features

- 1 x 8-bit ADC with 10 Inputs including attenuator allowing measurement of high voltage input signals
- Supply Voltage Attenuators with attenuation of **VS**, **VDDP** and **VDDC**.
- VBG monitoring of 8-bit ADC to guarantee functional safety requirements.
- Bridge Driver Diagnosis Measurement (VDH, VCP).
- Temperature Sensor for monitoring the chip temperature and PMU Regulator temperature.
- BEMF Comparators for commutation triggering inside BLDC Applications.
- Supplement Block with Reference Voltage Generation, Bias Current Generation, Voltage Buffer for NVM Reference Voltage, Voltage Buffer for Analog Module Reference Voltage and Test Interface.

22.2 Introduction

The measurement unit is a functional unit that comprises the following associated sub-modules:

Table 14 Measurement Functions and Associated Modules

Module Name	Modules	Functions
Central Functions Unit	Bandgap reference circuit	The bandgap-reference sub-module provides two reference voltages 1. a trimmable reference voltage for the 8-bit ADCs. A local dedicated bandgap circuit is implemented to avoid deterioration of the reference voltage arising e.g. from crosstalk or ground voltage shift. 2. the reference voltage for the NVM module
8-bit ADC (ADC2)	8-bit ADC module with 10 multiplexed inputs, including HV input attenuator	5 high voltage full supply range capable inputs (2.5V...30,7V(FS)) 2 medium voltage inputs (0..5V/7V FS). 3 low voltage inputs (0..1.2V/1.6V FS) (allocation see following overview figure)
10-bit ADC (ADC1)	10-bit ADC module with 8 multiplexed inputs	Five (5V) analog inputs from Port 2.x
VDH Input Voltage Attenuator	VDH input voltage attenuator	Scales down V(VDH) to the input voltage range of ADC1.CH6
Temperature Sensor	Temperature sensor with two multiplexed sensing elements: • PMU located sensor • Central chip located sensor	Generates output voltage which is a linear function of the local chip (junction) temperature.

Table 14 Measurement Functions and Associated Modules

Module Name	Modules	Functions
BEMF - Comparators	Back Electromotive Force Comparators	Comparators are used to detect the Back Electromotive Force (Zero Crossing Event), which can be used as a commutation trigger for BLDC applications.
Measurement Core Module	Digital signal processing and ADC2 control unit	1. Generates the control signal for the 8-bit ADC2 and the synchronous clock for the switched capacitor circuits, 2. Performs digital signal processing functions and provides status outputs for interrupt generation.

22.2.1 Block Diagram

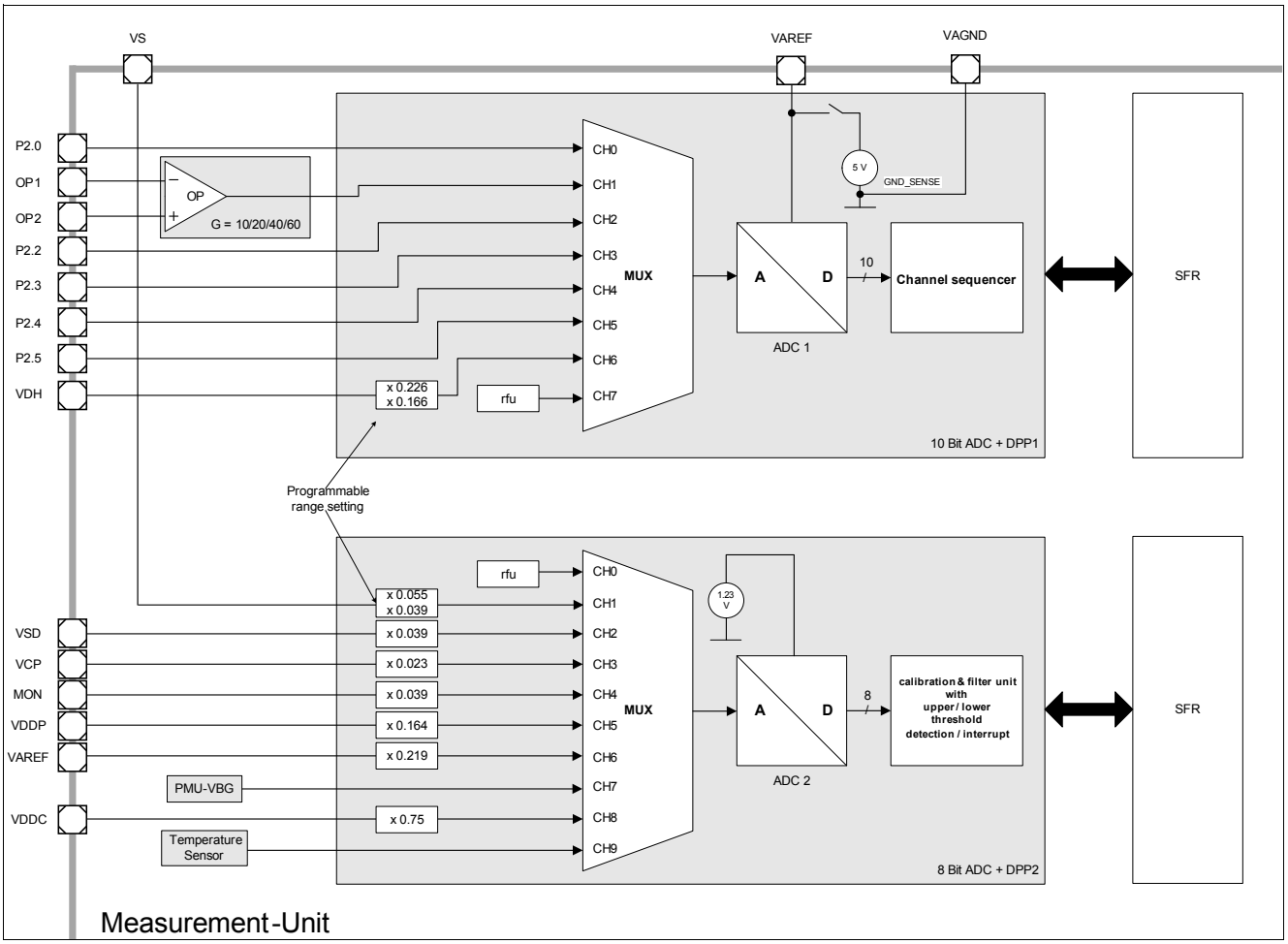


Figure 25 Measurement Unit-Overview (with opamp)

22.2.1.1 Block Diagram BEMF Comparator

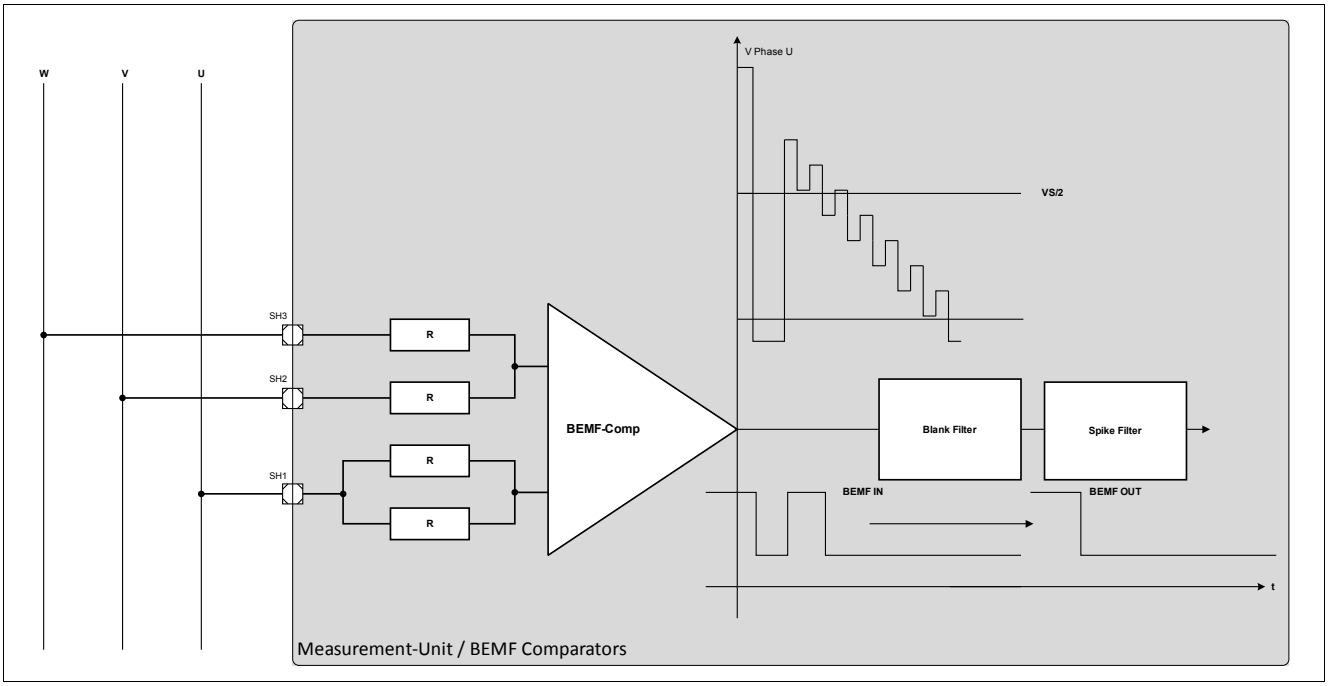


Figure 26 3 Times BEMF Comparator

23 Measurement Core Module (incl. ADC2)

23.1 Features

- 8 individually programmable channels split into two groups of user configurable and non user configurable
- Individually programmable channel prioritization scheme for measurement unit
- Two independent filter stages with programmable low-pass and time filter characteristics for each channel
- Two channel configurations:
  - Programmable upper- and lower trigger thresholds comprising a fully programmable hysteresis
  - Two individually programmable trigger thresholds with limit hysteresis settings
- Individually programmable interrupts and statuses for all channel thresholds

23.2 Introduction

The basic function of this block is the digital postprocessing of several analog digitized measurement signals by means of filtering, level comparison and interrupt generation. The measurement postprocessing block consists of ten identical channel units attached to the outputs of the 10-channel 8-bit ADC (ADC2). It processes ten channels, where the channel sequence and prioritization is programmable within a wide range.

23.2.1 Block Diagram

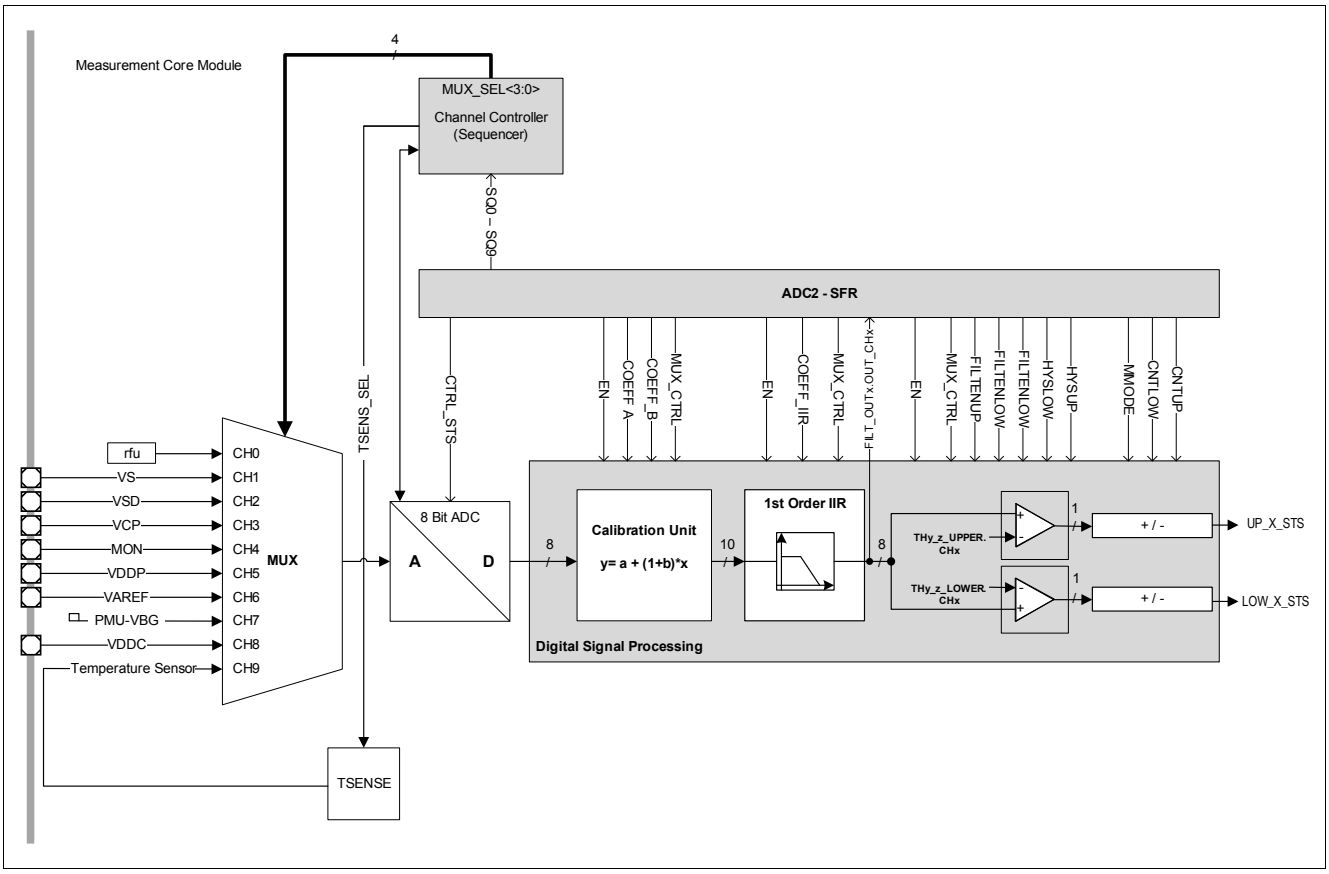


Figure 27 Module Block Diagram

23.2.2 Measurement Core Module Modes Overview

The basic function of this unit, is the digital signal processing of several analog digitized measurement signals by means of filtering, level comparison and interrupt generation. The Measurement Core module processes ten channels in a quasi parallel process.

As shown in the figure above, the ADC2 postprocessing unit consists of a channel controller (Sequencer), an 10-channel demultiplexer and the signal processing block, which filters and compares the sampled ADC2 values for each channel individually. The channel control block controls the multiplexer sequencing on the analog side before the ADC2 and on the digital domain after the ADC2. As described in the following section, the channel sequence can be controlled in a flexible way, which allows a certain degree of channel prioritization.

This capability can be used e.g. to set a higher priority to supply voltage channels compared to the other channel measurements. The Measurement Core Module offers additionally two different post-processing measurement modes for over-/undervoltage detection and for two-level threshold detection.

The channel controller (sequencer) runs in one of the following modes:

“Normal Sequencer Mode” – channels are selected according to the 10 sequence registers which contain individual enablers for each of the 10 channels.

“Exceptional Interrupt Measurement” – following a hardware event, a high priority channel is inserted into the current sequence. The current actual measurement is not destroyed.

“Exceptional Sequence Measurement” – following a hardware event, a complete sequence is inserted after the current measurement is finished. The current sequence is interrupted by the exception sequence.

24 10-Bit Analog Digital Converter (ADC1)

24.1 Features

The principal features of the ADC1 are:

- Up to 8 analog input channels (channel 7 reserved for future use)
- Flexible results handling
  - 8-bit and 10-bit resolution
- Flexible source selection due to sequencer
  - insert one exceptional sequence (ESM)
  - insert one interrupt measurement into the current sequence (EIM), single or up to 128 times
  - software mode
- Conversion sample time (separate for each channel) adjustable to adapt to sensors and reference
- Standard external reference (VAREF) to support ratiometric measurements and different signal scales
- DMA support, transfer ADC conversion results via DMA into RAM
- Support of suspend and power saving modes
- Result data protection for slow CPU access (wait-for-read mode)
- Programmable clock divider
- Integrated sample and hold circuitry

24.2 Introduction

The TLE9871QXA20 includes a high-performance 10-bit Analog-to-Digital Converter (ADC1) with eight multiplexed analog input channels. The ADC1 uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC1 are available at AN0, AN2 - AN5.

24.2.1 Block Diagram

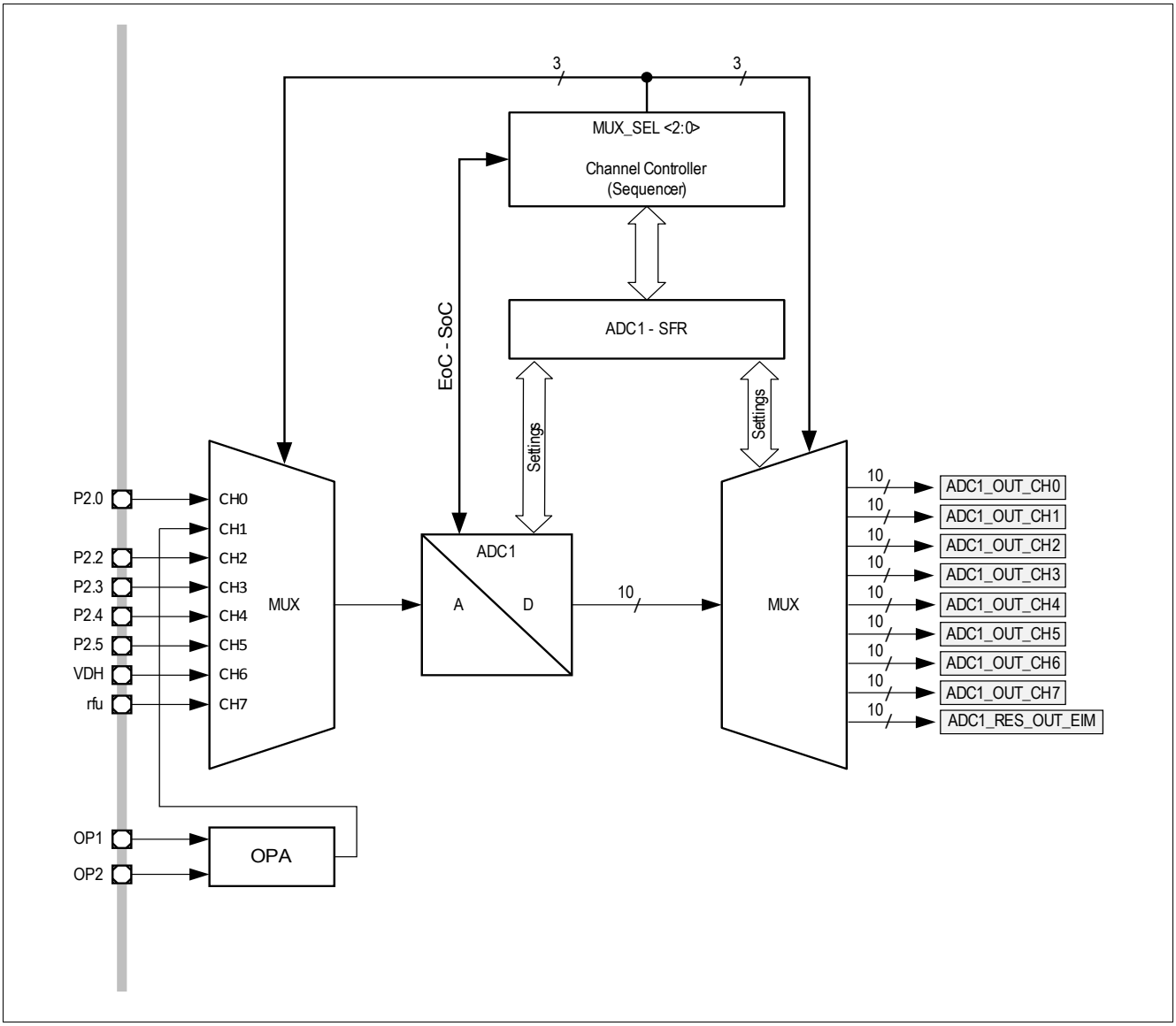


Figure 28 ADC1 Top Level Block Diagram

As shown in the figure above, the ADC1 postprocessing consists of a channel controller (Sequencer) and an 8-channel demultiplexer. The channel control block controls the multiplexer sequencing on the analog side before the ADC1 and on the digital domain after the ADC1. As described in the following section, the channel sequence can be controlled in a flexible way, which allows a certain degree of channel prioritization.

This capability can be used e.g. to give a higher priority to some channels compared to the other channel measurements.

25 High-Voltage Monitor Input

25.1 Features

- High-voltage input with V_S/2 threshold voltage
- Integrated selectable pull-up and pull-down current sources
- Wake capability for power saving modes
- Level change sensitivity configurable for transitions from low to high, high to low or both directions

25.2 Introduction

This module is dedicated to monitor external voltage levels above or below a specified threshold or it can be used to detect a wake-up event at the high-voltage MON pin in low-power mode. The input is sensitive to a input level monitoring, this is available when the module is switched to active mode with the SFR bit EN.

To use the Wake function during low power mode of the IC, the monitoring pin is switched to Sleep Mode via the SFR bit EN.

25.2.1 Block Diagram

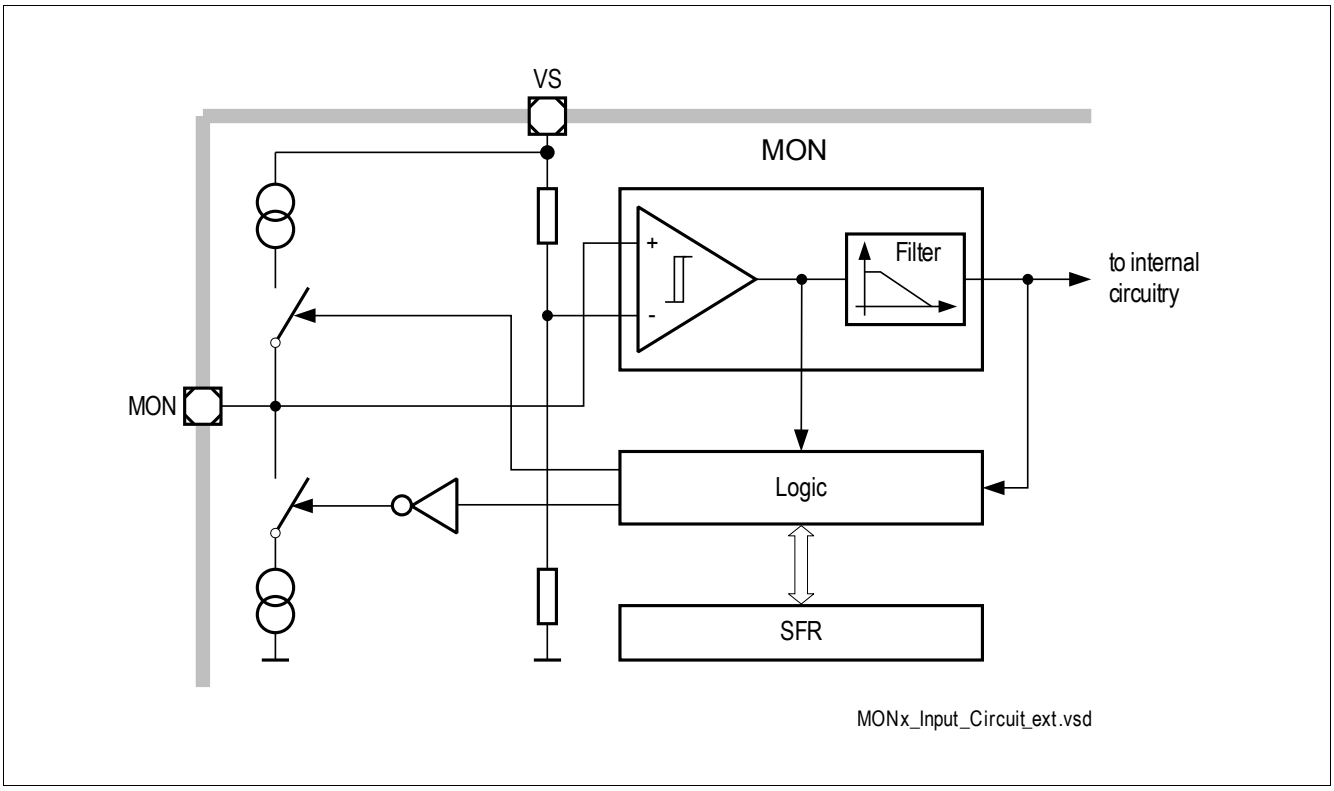


Figure 29 Monitoring Input Block Diagram

26 Bridge Driver (incl. Charge Pump)

26.1 Features

The MOSFET Driver is intended to drive external normal level NFET transistors in bridge configuration. The driver provides many diagnostic possibilities to detect faults.

Functional Features

- External Power NFET Transistor Driver Stage with driver capability for max. 100 nC gate charge @ 25 kHz switching frequency.
- Implemented adjustable cross conduction protection.
- Supply voltage (VSD) monitoring incl. adjustable over- and undervoltage shutdown with configurable interrupt signalling.
- VSD operating range down to 5.4 V
- VDS comparators for short circuit detection in on- and off-state
- Open-Load detection in off-state
- Flexible PWM frequency range, rates above 25 kHz require power dissipation and duty cycle resolution analysis

26.2 Introduction

The MOSFET Driver Stage can be used for controlling external Power NFET Transistors (normal level). The module output is controlled by SFR or System PWM Machine (CCU6).

26.2.1 Block Diagram

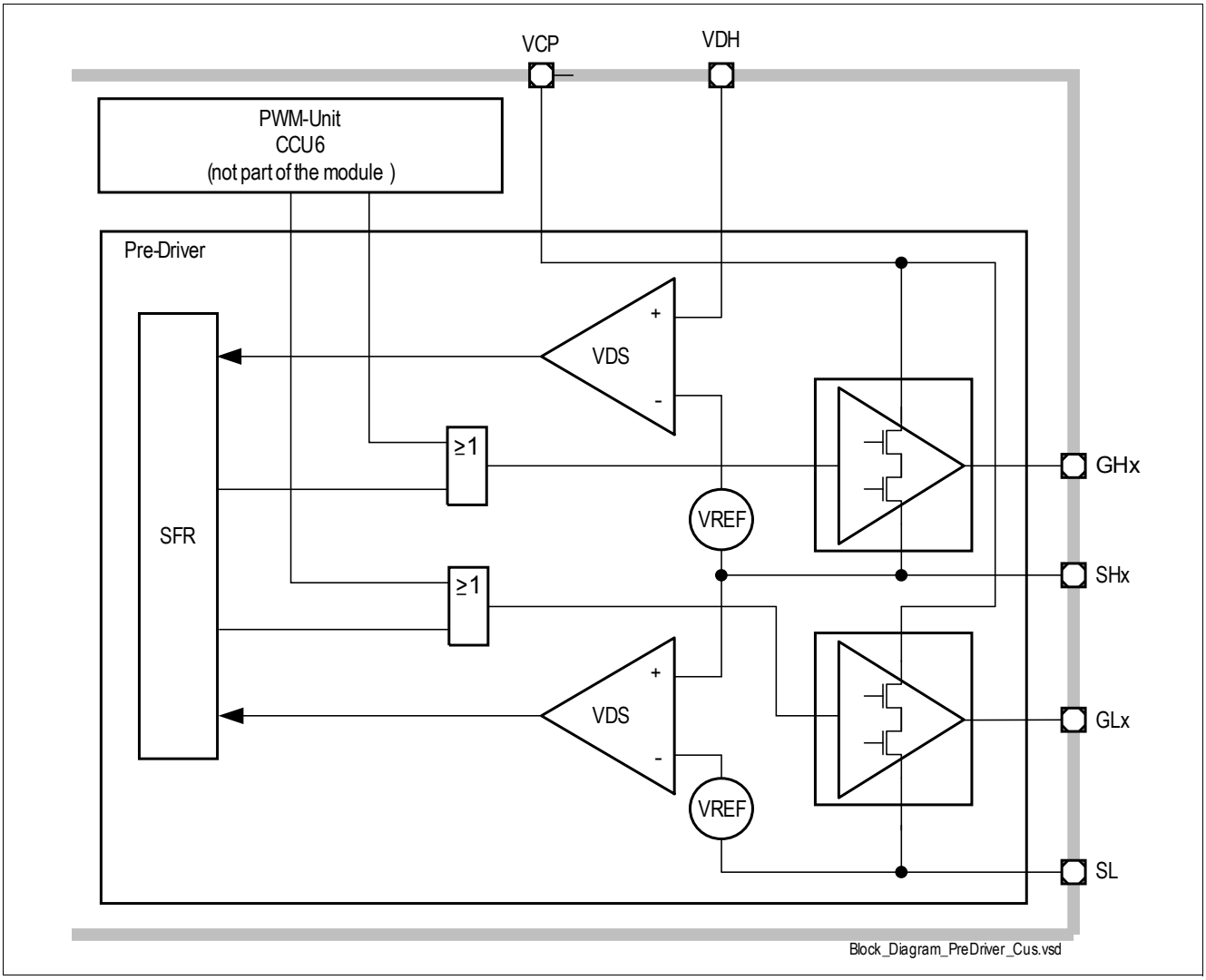


Figure 30 Driver Module Block Diagram (incl. system connections)

26.2.2 General

The Driver can be controlled in two different ways:

- In Normal Mode the output stage is fully controllable through the SFR registers CTRLx (x = 1,2,3). Protection functions such as overcurrent and open-load detection are available.
- The PWM Mode can also be enabled by the corresponding bit in CTRL1 and CTRL2. The PWM must be configured in the System PWM Module (CCU6). All protection functions are available in PWM mode as well.

Protection Functions

- Overcurrent detection and shutdown feature for external MOSFET by Drain Source measurement
- Programmable minimum cross current protection time
- Open-load detection feature in Off-state for external MOSFET.

27 Current Sense Amplifier

27.1 Features

Main Features

- Programmable gain settings: G = 10, 20, 40, 60
- Differential input voltage: ± 1.5V / G
- Wide common mode input range ± 2 V
- Low setting time < 1.4 µs

27.2 Introduction

The current sense amplifier in **Figure 31** can be used to measure near ground differential voltages via the 10-bit ADC. Its gain is digitally programmable through internal control registers.

Linear calibration has to be applied to achieve high gain accuracy, e.g. end-of-line calibration including the shunt resistor.

Figure 31 shows how the current sense amplifier can be used as a low-side current sense amplifier where the motor current is converted to a voltage by means of a shunt resistor R_{SH}. A differential amplifier input is used in order to eliminate measurement errors due to voltage drop across the stray resistance R_{Stray} and differences between the external and internal ground. If the voltage at one or both inputs is out of the operating range, the input circuit is overloaded and requires a certain specified **recovery time**.

In general, the external low pass filter should provide suppression of EMI.

27.2.1 Block Diagram

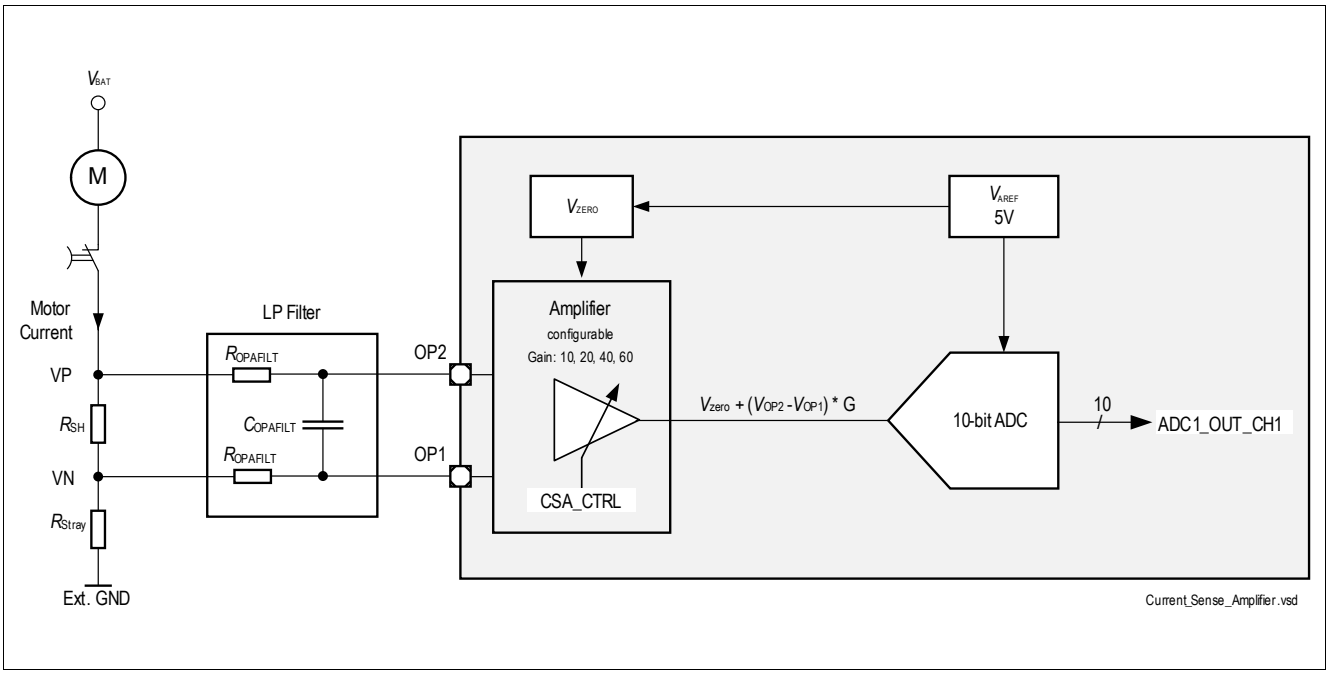


Figure 31 Simplified Application Diagram

28 Application Information

28.1 BLDC Driver

Figure 32 shows the TLE9871QXA20 in an electric drive application setup controlling a BLDC motor.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

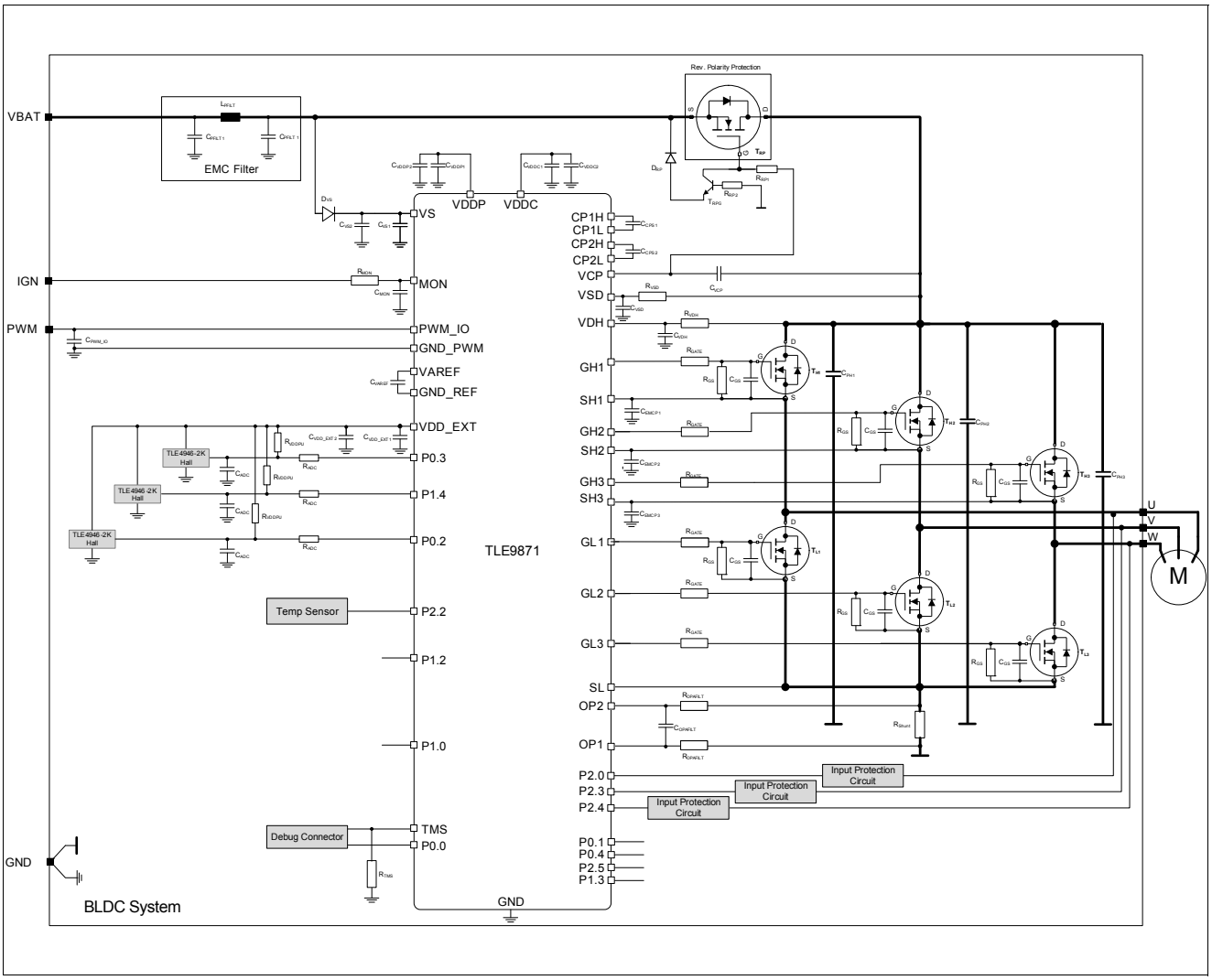


Figure 32 Simplified Application Diagram Example

Note: This is a very simplified example of an application circuit and bill of materials. The function must be verified in the actual application.

Table 15 External Components (BOM)

Symbol	Function	Component
C_{VS1}	Blocking capacitor at VS pin	≥ 100 nF Ceramic, ESR < 1Ω
C_{VS2}	Blocking capacitor at VS pin	> 2.2 µF Elco[1)]
C_{VDDP}	Blocking capacitor at VDDP pin	470 nF + 100 nF Ceramic, ESR < 1Ω
C_{VDD_EXT}	Blocking capacitor at VDDEXT pin	100nF, Ceramic ESR < 1Ω
C_{VDDC}	Blocking capacitor at VDDC pin	470 nF + 100 nF Ceramic, ESR < 1Ω
C_{VAREF}	Blocking capacitor at VAREF pin	100 nF, Ceramic ESR < 1Ω
C_{PWM_IO}	Standard C for PWM Interface slave	–
C_{VSD}	Filter C for charge pump end driver	1 µF
C_{CPS1}	Charge pump capacitor	220 nF
C_{CP2S}	Charge pump capacitor	220 nF
C_{VCP}	Charge pump capacitor	470 nF
C_{MON}	Filter C for ISO pulses	10nF
C_{VDH}	Capacitor	3.3 nF
C_{PH1}	Capacitor	220 µF
C_{PH2}	Capacitor	220 µF
C_{PH3}	Capacitor	220 µF
$C_{OPAFILT}$	Capacitor	100 nF
C_{EMCP1}	Capacitor	1 nF
C_{EMCP2}	Capacitor	1 nF
C_{EMCP3}	Capacitor	1 nF
C_{PFILT1}, C_{PFILT2}	Capacitor	
R_{MON}	Resistor at MON pin	3.9kΩ
R_{VSD}	Limitation of reverse current due to transient (-2V, 8ms)	2Ω
R_{VDH}	Resistor	1kΩ
R_{GATE}	Resistor	2Ω
$R_{OPAFILT}$	Resistor	12Ω
R_{SH1}	Resistor	optional
R_{SH2}	Resistor	optional
R_{SH3}	Resistor	optional
L_{PFILT}		–
D_{VS}	Reverse-polarity protection diode	–

1) The capacitor must be dimensioned so as to ensure that flash operations modifying the content of the flash are never interrupted (e.g. in case of power loss).

28.2 ESD Immunity According to IEC61000-4-2

Note: Tests for ESD immunity according to IEC61000-4-2 “Gun test” (150pF, 330Ω) has been performed. The results and test condition will be available in a test report.

Table 16 ESD “Gun Test”

Performed Test	Result	Unit	Remarks
ESD at pin PWM_IO, versus GND[1)]	> 6	kV	positive pulse
ESD at pin PWM_IO, versus GND[1)]	< -6	kV	negative pulse

1) ESD test “ESD GUN” is specified with external components; see application diagram: C_{MON} = 100nF, R_{MON} = 1kΩ, C_{PWM_IO} = 220pF, C_{VS} = >20µF ELCO + 100nF ESR < 1Ω, C_{VSD} = 1µF, R_{VSD} = 2Ω.

29 Electrical Characteristics

This chapter includes all relevant electrical characteristics of the product TLE9871QXA20.

29.1 General Characteristics

29.1.1 Absolute Maximum Ratings

Table 17 Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltages – Supply Pins							
Supply voltage – VS	V_S	-0.3	–	40	V	Load dump	P_1.1.1
Supply voltage – VSD	V_{SD}	-0.3	–	48	V	–	P_1.1.2
Supply voltage – VSD	$V_{SD_max_extend}$	-2.8	–	48	V	Series resistor R_{VSD} = 2.2 Ω, t = 8 ms [2)]	P_1.1.32
Voltage range – VDDP	V_{DDP}	-0.3	–	5.5	V	–	P_1.1.3
Voltage range – VDDP	$V_{DDP_max_extend}$	-0.3	–	7	V	In case of voltage transients on V_S with dV_S/dt ≤ 1V/µs; duration: t ≤ 150µs; C_{VDDP} ≤ 570 nF	P_1.1.41
Voltage range – VDDEXT	V_{DDEXT}	-0.3	–	5.5	V	–	P_1.1.4
Voltage range – VDDEXT	$V_{DDEXT_max_extend}$	-0.3	–	7	V	In case of voltage transients on V_S with dV_S/dt ≤ 1V/µs; duration: t ≤ 150µs; C_{VDDEXT} ≤ 570 nF	P_1.1.42
Voltage range – VDDC	V_{DDC}	-0.3	–	1.6	V	–	P_1.1.5
Voltages – High Voltage Pins							
Input voltage at PWM_IO	V_{PWM_IO}	-28	–	40	V	–	P_1.1.7
Input voltage at MON	$V_{MON_maxrate}$	-28	–	40	V	[3)]	P_1.1.8
Input voltage at VDH	$V_{VDH_maxrate}$	-2.8	–	40	V	[4)]	P_1.1.38
Voltage range at GHx	V_{GH}	-6.0	–	48	V	[5)]	P_1.1.9
Voltage range at GHx vs. SHx	V_{GHvsSH}	14	16	19	V	–	P_1.1.44
Voltage range at SHx	V_{SH}	-6.0	–	48	V	–	P_1.1.11
Voltage range at GLx	V_{GL}	-6.0	–	48	V	[6)]–	P_1.1.13
Voltage range at GLx vs. SL	V_{GLvsSL}	14	16	19	V	–	P_1.1.45

Table 17 Absolute Maximum Ratings[1)] (cont'd)

T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltage range at charge pump pins CP1H, CP1L, CP2H, CP2L, VCP	V_{CPx}	-0.3	–	48	V	7)	P_1.1.15
Voltages – GPIOs							
Voltage on any port pin	V_{in}	-0.3	–	V_{DDP} +0.3	V	$V_{IN} < V_{DDPmax}$ 8)	P_1.1.16
Current at VCP Pin							
Max. current at VCP pin	I_{VCP}	-15	–	–	mA	–	P_1.1.35
Injection Current at GPIOs							
Injection current on any port pin	I_{GPIONM}	-5	–	5	mA	9)	P_1.1.34
Sum of all injected currents in Normal Mode	I_{GPIOAM_sum}	-50	–	50	mA	9)	P_1.1.30
Sum of all injected currents in Power Down Mode (Stop Mode)	I_{GPIOPD_sum}	-5000	–	50	µA	9)	P_1.1.36
Sum of all injected currents in Sleep Mode	$I_{GPIOSleep_sum}$	-5	–	5	mA	9)	P_1.1.37
Other Voltages							
Input voltage VAREF	V_{AREF}	-0.3	–	V_{DDP} +0.3	V	–	P_1.1.17
Input voltage OP1, OP2	V_{OAI}	-7	–	7	V	–	P_1.1.23
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_1.1.18
Storage temperature	T_{stg}	-55	–	150	°C	–	P_1.1.19
ESD Susceptibility							
ESD susceptibility all pins	V_{ESD1}	-2	–	2	kV	HBM 10)	P_1.1.20
ESD susceptibility pins MON, VS, VSD vs.GND	V_{ESD2}	-4	–	4	kV	HBM 11)	P_1.1.21
ESD susceptibility pins PWM_IO vs. GND_PWM	V_{ESD3}	-6	–	6	kV	HBM 10)	P_1.1.22
ESD susceptibility **CDM** all pins vs. GND	V_{ESD_CDM1}	-500	–	500	V	12)	P_1.1.28
ESD susceptibility **CDM** pins 1, 12, 13, 24, 25, 36, 37, 48 (corner pins) vs. GND	V_{ESD_CDM2}	-750	–	750	V	12)	P_1.1.43

1) Not subject to production test, specified by design.

2) Conditions and min. value is derived from application condition for reverse polarity event.

3) Min voltage -28V with external 3.9kΩ series resistor only.

4) Min voltage -2.8V with external 1kΩ series resistor only.
5) To achieve max. ratings on this pin, Parameter P_1.1.44 has to be taken into account resulting in the following dependency: $V_{GH} < V_{SH} + V_{GHvsSH}$ and additionally $V_{SH} < V_{GH} + 0.3V$.
6) To achieve max. ratings on this pin, Parameter P_1.1.45 has to be taken into account resulting in the following dependency: $V_{GL} < V_{SL} + V_{GLvsSL}$ and additionally $V_{SL} < V_{GL} + 0.3V$.
7) These limits can be kept if max current drawn out of pin does not exceed limit of 200 µA.
8) Includes TMS and RESET.
9) Maximum rating for injection current of GPIO with V_{IN} respected.
10) ESD susceptibility HBM according to ANSI/ESDA/JEDEC JS-001 (1.5kΩ, 100pF)
11) MON with external circuitry of a series resistor of 3.9kΩ and 10nF (at connector); VS with an external ceramic capacitor of 100nF; VSD with an external capacitor of 470nF; VDH with external circuitry of a series resistor of 1kΩ and 3.3nF (at pin).
12) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JESD22-C101F

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

29.1.2 Functional Range

Table 18 Functional Range

T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage in Active Mode	V_{S_AM}	5.5	–	28	V	–	P_1.2.1
Extended supply voltage in Active Mode	$V_{S_AM_extend}$	28	–	40	V	1) Functional with parameter deviation	P_1.2.16
Supply voltage in Active Mode for MOSFET Driver Supply	V_{SD_AM}	5.4	–	28	V		P_1.2.18
Extended supply voltage in Active Mode for MOSFET Driver Supply	$V_{SD_AM_extend}$	28	–	32	V	1)Functional with parameter deviation	P_1.2.17
Specified supply voltage for PWM interface	$V_{S_AM_PWM_IO}$	5.5	–	18	V	Parameter Specification	P_1.2.2
Extended supply voltage for PWM interface	$V_{S_AM_PWM_IO}$	4.8	–	28	V	Functional with parameter deviation	P_1.2.14
Supply voltage in Active Mode with reduced functionality (Microcontroller / Flash with full operation)	V_{S_AMmin}	3.0	–	5.5	V	2)	P_1.2.3
Supply voltage in Sleep Mode	V_{S_Sleep}	3.0	–	28	V	–	P_1.2.4
Supply voltage transients slew rate	dV_S/dt	-1	–	1	V/µs	3)	P_1.2.5
Output sum current for all GPIO pins	$I_{GPIO,sum}$	-50	–	50	mA	–	P_1.2.7
Operating frequency	f_{sys}	5	–	24	MHz	4)	P_1.2.15
Junction temperature	T_j	-40	–	150	°C	–	P_1.2.9

1) This operation voltage range is only allowed for a short duration: $t_{max} \leq 400$ ms, f_{sys} = 24 MHz, I_{VDDP} = 10 mA, I_{VDDEXT} = 5 mA.

2) Reduced functionality (e.g. cranking pulse) - Parameter deviation possible.

3) Not subject to production test, specified by design.

4) Function not specified when limits are exceeded.

29.1.3 Current Consumption

Table 19 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption @VS pin							
Current consumption in Active Mode at pin VS	I_{Vs}	–	30	35	mA	f_{sys} = 20 MHz no loads on pins, PWM interface in recessive state[1)]	P_1.3.1
Current consumption in Active Mode at pin VSD	I_{VSD}	–	–	40	mA	20 kHz PWM on Bridge Driver	P_1.3.8
Current consumption in Sleep Mode	I_{Sleep}	–	30	35	µA	System in Sleep Mode, microcontroller not powered, Wake capable via PWM interface and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND: T_J = -40°C to 85°C; V_S = 5.5 V to 18V;[2)]	P_1.3.3
Current consumption in Sleep Mode extended range	I_{Sleep_extend}	–	90	200	µA	System in Sleep Mode, microcontroller not powered, Wake capable via PWM interface and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND: T_J = -40°C to 150°C; V_S = 5.5 V to 18V;[2)]	P_1.3.15
Current consumption in Sleep Mode	I_{Sleep}	–	–	33	µA	System in Sleep Mode, microcontroller not powered, Wake capable via PWM interface and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND: T_J = -40°C to 40°C; V_S = 5.5 V to 18V;[2)]	P_1.3.9

Table 19 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current consumption in Sleep Mode with cyclic wake	I_{Cyclic}	–	–	110	µA	T_J = -40°C to 85°C; V_S = 5.5 V to 18V; t_{Cyclic_ON} = 4ms; t_{Cyclic_OFF} = 2048 ms;2)	P_1.3.4
Current consumption in Stop Mode	I_{Stop}	–	100	150	µA	System in Stop Mode, microcontroller not clocked, Wake capable via PWM interface and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND; T_J = -40°C to 85°C; V_S = 5.5V to 18V	P_1.3.10

1) Current on V_S, ADC1/2 active, timer running, PWM interface active (recessive).

2) Incl. leakage currents form VDH, VSD and MON

Note: Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

29.1.4 Thermal Resistance

Table 20 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	R_{thJSP}	–	6	–	K/W	1) measured to Exposed Pad	P_1.4.1
Junction to Ambient	R_{thJA}	–	33	–	K/W	2)	P_1.4.2

1) Not subject to production test, specified by design.

2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board. Board: 76.2x114.3x1.5mm³ with 2 inner copper layers (35µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300mm^2 cooling area on the bottom layer (70µm).

29.1.5 Timing Characteristics

The transition times between the system modes are specified here. Generally the timings are defined from the time when the corresponding bits in register PMCON0 are set until the sequence is terminated.

Table 21 System Timing1)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Wake-up over battery	t_{start}	–	–	3	ms	Battery ramp-up time to code execution	P_1.5.6
Wake-up over battery	$t_{startSW}$	–	–	1.5	ms	Battery ramp-up time to till MCU reset is released; V_S > 3 V and RESET = 1	P_1.5.1
Sleep-Exit	$t_{sleep\ -\ exit}$	–	–	1.5	ms	Rising/falling edge of any wake-up signal (PWM interface, MON) till MCU reset is released;	P_1.5.2
Sleep-Entry	$t_{sleep\ -\ entry}$	–	–	330	µs	2)	P_1.5.3

1) Not subject to production test, specified by design.

2) Wake events during Sleep-Entry are stored and lead to wake-up after Sleep Mode is reached.

29.2 Power Management Unit (PMU)

This chapter includes all electrical characteristics of the Power Management Unit

29.2.1 PMU I/O Supply (VDDP) Parameters

This chapter describes all electrical parameters which are observable on SoC level. For this purpose only the pad-supply VDDP and the transition times between the system modes are specified here.

Table 22 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified output current	I_{VDDP}	0	–	50	mA	1)	P_2.1.1
Specified output current	I_{VDDP}	0	–	30	mA	1)2)	P_2.1.22
Required decoupling capacitance	C_{VDDP1}	0.47	–	2.2	µF	3)4) ESR < 1Ω; the specified capacitor value is a typical value.	P_2.1.2
Required buffer capacitance for stability (load jumps)	C_{VDDP2}	1	–	2.2	µF	3)4) The specified capacitor value is a typical value.	P_2.1.20
Output voltage including line and load regulation @ Active Mode	V_{DDPOUT}	4.9	5.0	5.1	V	5) I_{load} < 90mA; V_S > 5.5V	P_2.1.3
Output voltage including line and load regulation @ Active Mode	V_{DDPOUT}	4.9	5.0	5.1	V	2)5) I_{load} < 70mA; V_S > 5.5V	P_2.1.23
Output voltage including line and load regulation @ Stop Mode	$V_{DDPOUTSTOP}$	4.5	5.0	5.5	V	5) I_{load} is only internal; V_S > 5.5V	P_2.1.21
Output drop @ Active Mode	$V_{SVDDPout}$	–	50	400	mV	I_{VDDP} = 30mA6); 3.5V < V_S < 5.0V	P_2.1.4
Load regulation @ Active Mode	$V_{VDDPLOR}$	-50	–	50	mV	2 ... 90mA; C = 570nF	P_2.1.5
Line regulation @ Active Mode	$V_{VDDPLIR}$	-50	–	50	mV	V_S = 5.5 ... 28V	P_2.1.6
Overvoltage detection	V_{DDPOV}	5.14	–	5.4	V	V_S > 5.5V; Overvoltage leads to SUPPLY_NMI	P_2.1.7
Overvoltage detection filter time	t_{FILT_VDDPOV}	–	735	–	µs	3)7)	P_2.1.24
Voltage OK detection	V_{DDPOK}	–	3	–	V	3)	P_2.1.25
Voltage stable detection range8)	ΔV_{DDPSTB}	- 220	–	+ 220	mV	3)	P_2.1.26
Undervoltage reset	V_{DDPUV}	2.5	2.6	2.7	V	–	P_2.1.8
Overcurrent diagnostic	I_{VDDPOC}	91	–	220	mA	–	P_2.1.9

Table 22 Electrical Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Overcurrent diagnostic filter time	t_{FILT_VDDPOC}	–	27	–	µs	3)7)	P_2.1.27
Overcurrent diagnostic shutdown time	$t_{FILT_VDDPOC_SD}$	–	290	–	µs	3)7)9)	P_2.1.28

1) Specified output current for port supply and additional other external loads already excluding VDDC current.
2) This use case applies to cases where output current on VDDEXT is max. 40 mA.
3) Not subject to production test, specified by design.
4) Ceramic capacitor.
5) Load current includes internal supply.
6) Output drop for IVDDP without internal supply current.
7) This filter time and its variation is derived from the time base $t_{LP_CLK} = 1 / f_{LP_CLK}$.
8) The absolute voltage value is the sum of parameters $V_{DDP} + V_{DDPSTB}$.
9) After $t_{FILT_VDDCOC_SD}$ is passed and the overcurrent condition is still present the device will enter sleep mode.

29.2.2 PMU Core Supply (VDDC) Parameters

This chapter describes all electrical parameters which are observable on SoC level. For this purpose only the core-supply VDDC and the transition times between the system modes are specified here.

Table 23 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Required decoupling capacitance	C_{VDDC1}	0.1	–	1	µF	1)2) ESR < 1Ω; the specified capacitor value is a typical value.	P_2.2.1
Required buffer capacitance for stability (load jumps)	C_{VDDC2}	0.33	–	1	µF	2)the specified capacitor value is a typical value.	P_2.2.17
Output voltage including line regulation @ Active Mode/Stop Mode	V_{DDCOUT}	1.44	1.5	1.56	V	I_{load} < 40mA	P_2.2.2
Load Regulation @ Active Mode	V_{DDCLOR}	-50	–	50	mV	2 ... 40mA; C =430nF	P_2.2.3
Line regulation @ Active Mode	V_{DDCLIR}	-25	–	25	mV	V_{DDP} = 2.5 ... 5.5V	P_2.2.4
Overvoltage detection	V_{DDCOV}	1.59	1.62	1.68	V	Overvoltage leads to SUPPLY_NMI	P_2.2.5
Overvoltage detection filter time	t_{FILT_VDDCOV}	–	735	–	µs	1)3)	P_2.2.18
Voltage OK detection range[4)]	ΔV_{DDCOK}	- 280	–	+ 280	mV	1)	P_2.2.19
Voltage stable detection range[5)]	ΔV_{DDCSTB}	- 110	–	+ 110	mV	1)	P_2.2.20
Undervoltage reset	V_{DDVUV}	1.136	1.20	1.264	V	–	P_2.2.6
Overcurrent diagnostic	I_{VDDCOC}	45	–	100	mA	–	P_2.2.7
Overcurrent diagnostic filter time	t_{FILT_VDDCOC}	–	27	–	µs	1)3)	P_2.2.21
Overcurrent diagnostic shutdown time	$t_{FILT_VDDCOC_SD}$	–	290	–	µs	1)3)6)	P_2.2.22

1) Not subject to production test, specified by design.
2) Ceramic capacitor.
3) This filter time and its variation is derived from the time base $t_{LP_CLK} = 1 / f_{LP_CLK}$.
4) The absolute voltage value is the sum of parameters $V_{DDC} + V_{DDCSTB}$.
5) The absolute voltage value is the sum of parameters $V_{DDC} + V_{DDCOK}$.
6) After $t_{FILT_VDDCOC_SD}$ is passed and the overcurrent condition is still present the device will enter sleep mode.

29.2.3 VDDEXT Voltage Regulator (5.0V) Parameters

Table 24 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified output current	I_{VDDEXT}	0	–	20	mA	–	P_2.3.1
Specified output current	I_{VDDEXT}	0	–	40	mA	1)	P_2.3.21
Required decoupling capacitance	$C_{VDDEXT1}$	0.1	–	2.2	µF	3) 2)ESR < 1 Ω; the specified capacitor value is a typical value.	P_2.3.22
Required buffer capacitance for stability (load jumps)	$C_{VDDEXT2}$	1	–	2.2	µF	3)2)the specified capacitor value is a typical value.	P_2.3.20
Output voltage including line and load regulation	V_{DDEXT}	4.9	5.0	5.1	V	3) I_{load}<20mA; V_S > 5.5V	P_2.3.3
Output voltage including line and load regulation	V_{DDEXT}	4.8	5.0	5.2	V	I_{load}<40mA; V_S > 5.5V	P_2.3.23
Output drop @ Active Mode	V_S-V_{DDEXT}		50	+300	mV	3) I_{load} < 20mA; 3V < V_S < 5.0V	P_2.3.4
Output drop @ Active Mode	V_S-V_{DDEXT}		–	+400	mV	I_{load} < 40mA; 3V < V_S < 5.0V	P_2.3.14
Load regulation @ Active Mode	$V_{DDEXTLOR}$	-50	–	50	mV	2 ... 40mA; C =200nF	P_2.3.5
Line regulation @ Active Mode	$V_{VDDEXTLIR}$	-50	–	50	mV	V_S = 5.5 ... 28V	P_2.3.6
Power supply ripple rejection @ Active Mode	$P_{SSRVDDEXT}$	50	–	–	dB	3) V_S = 13.5V; f =0 ... 1KHz; Vr=2Vpp	P_2.3.7
Overvoltage detection	$V_{VDDEXTOV}$	5.18	–	5.4	V	V_S > 5.5V	P_2.3.8
Overvoltage detection filter time	$t_{FILT_VDDEXTOV}$	–	735	–	µs	3)4)	P_2.3.24
Voltage OK detection range	$V_{VDDEXTOK}$	–	3	–	V	3)	P_2.3.25
Voltage stable detection range[5)]	$\Delta V_{VDDEXTSTB}$	- 220	–	+ 220	mV	3)	P_2.3.26
Undervoltage trigger	$V_{VDDEXTUV}$	2.6	2.8	3.0	V	6)	P_2.3.9
Overcurrent diagnostic	$I_{VDDEXTOC}$	50	–	160	mA	–	P_2.3.10
Overcurrent diagnostic filter time	t_{FILT_VDDCOC}	–	27	–	µs	3)4)	P_2.3.27
Overcurrent diagnostic shutdown time	$t_{FILT_VDDCOC_SD}$	–	290	–	µs	3)4)	P_2.3.28

1) This use case requires the reduced utilization of VDDP output current by 20 mA, see P_2.1.22.
2) Ceramic capacitor.
3) Not subject to production test, specified by design.
4) This filter time and its variation is derived from the time base t_{LP_CLK} = 1 / f_{LP_CLK}.

5) The absolute voltage value is the sum of parameters V_{DDEXT} + $V_{DDEXTSTB}$.
6) When the condition is met, the Bit VDDEXT_CTRL.bit.SHORT will be set.

29.2.4 VPRE Voltage Regulator (PMU Subblock) Parameters

The PMU VPRE Regulator acts as a supply of VDDP and VDDEXT voltage regulators.

Table 25 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified output current	I_{VPRE}	–	–	110	mA	1)	P_2.4.1

1) Not subject to production test, specified by design.

29.2.4.1 Load Sharing Scenarios of VPRE Regulator

The figure below shows the possible load sharing scenarios of VPRE regulator.

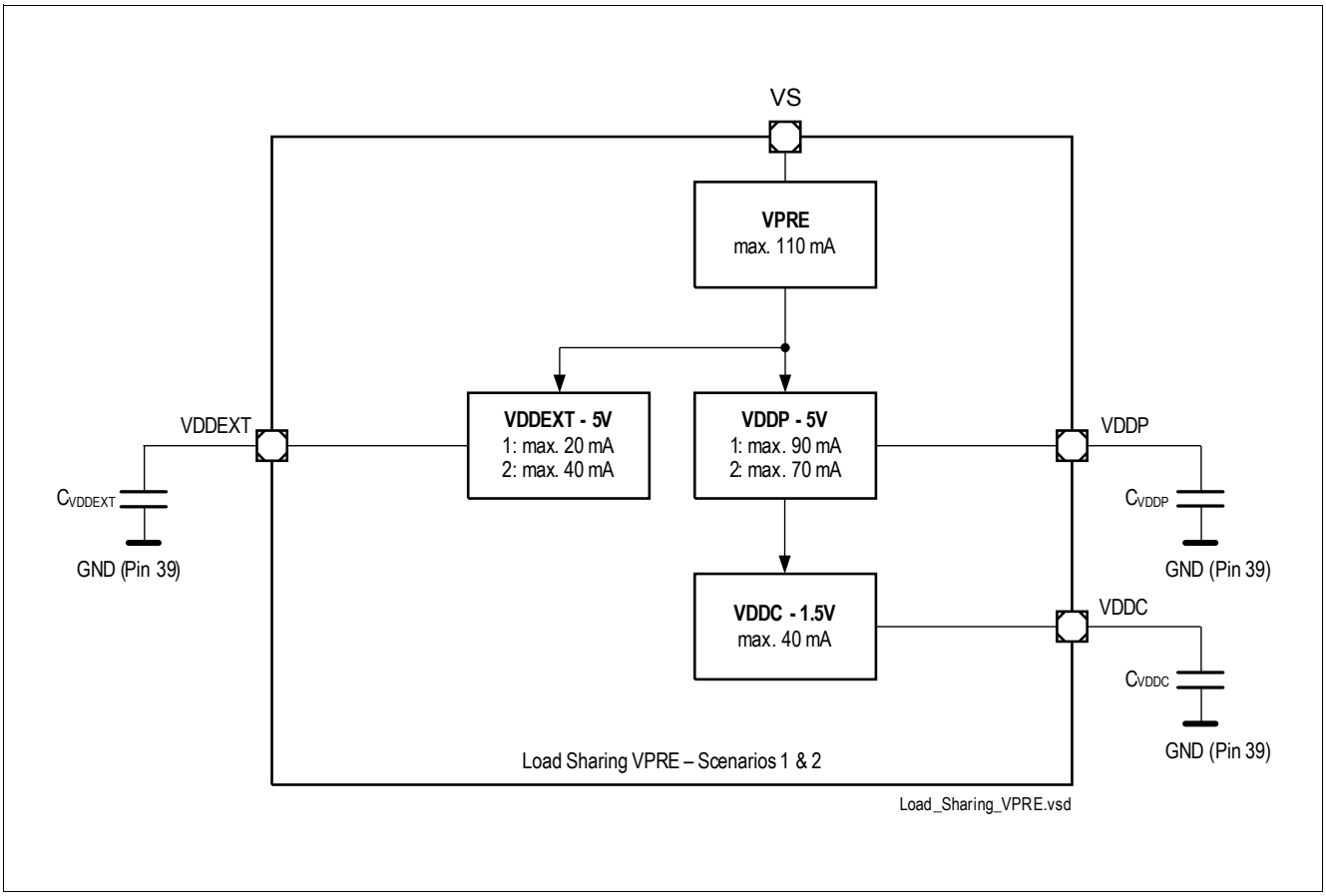


Figure 33 Load Sharing Scenarios of VPRE Regulator

29.2.5 Power Down Voltage Regulator (PMU Subblock) Parameters

The PMU Power Down voltage regulator consists of two subblocks:

- Power Down Pre regulator: VDD5VPD
- Power Down Core regulator: VDD1V5_PD (Supply used for GPUDATAxy registers)

Both regulators are used as purely internal supplies. The following table contains all relevant parameters:

Table 26 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
VDD1V5_PD							
Power-On Reset Threshold	$V_{DD1V5_PD_RSTTH}$	1.2	–	1.5	V	1)	P_2.5.1

1) Not subject to production test, specified by design

29.3 System Clocks

29.3.1 Oscillators and PLL Parameters

Table 27 Electrical Characteristics System Clocks

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
PMU Oscillators (Power Management Unit)							
Frequency of LP_CLK	f_{LP_CLK}	14	18	22	MHz	This clock is used at startup and can be used in case the PLL fails	P_3.1.1
Frequency of LP_CLK2	f_{LP_CLK2}	70	100	130	kHz	This clock is used for cyclic wake	P_3.1.2
CGU Oscillator (Clock Generation Unit Microcontroller)							
Short term frequency deviation[1)]	f_{TRIMST}	-0.4	–	+0.4	%	[2)3)] Within any 10 ms, e.g. after synchronization to a PWM signal (PLL settings untouched within 10 ms)	P_3.1.3
Absolute accuracy	$f_{TRIMABSA}$	-1.5	–	+1.5	%	Including temperature and lifetime deviation	P_3.1.4
CGU-OSC Start-up time	t_{OSC}	–	–	10	µs	[3)] Startup time OSC from Sleep Mode, power supply stable	P_3.1.5
PLL (Clock Generation Unit Microcontroller) [3)]							
VCO frequency range Mode 0	f_{VCO-0}	48	–	112	MHz	VCOSEL =”0”	P_3.1.6
VCO frequency range Mode 1	f_{VCO-1}	96	–	160	MHz	VCOSEL =”1”	P_3.1.7
Input frequency range	f_{OSC}	4	–	16	MHz	–	P_3.1.8
XTAL1 input freq. range	f_{OSC}	4	–	16	MHz	–	P_3.1.9
Output freq. range	f_{PLL}	0.04687	–	80	MHz	–	P_3.1.10
Free-running frequency Mode 0	$f_{VCOfree_0}$	–	–	38	MHz	VCOSEL =”0”	P_3.1.11
Free-running frequency Mode 1	$f_{VCOfree_1}$	–	–	76	MHz	VCOSEL =”1”	P_3.1.12
Input clock high/low time	$t_{high/low}$	10	–	–	ns	–	P_3.1.13
Peak period jitter	t_{jp}	-500	–	500	ps	[4)] for K=1	P_3.1.14
Accumulated jitter	jacc	–	–	5	ns	[4)] for K=1	P_3.1.15
Lock-in time	t_L	–	–	200	µs	–	P_3.1.16

1) The typical oscillator frequency is 5 MHz
2) V_{DDC} = 1.5 V, T_j = 25°C
3) Not subject to production test, specified by design.
4) This parameter is valid for PLL operation with an external clock source and thus reflects the real PLL performance.

29.4 Flash Memory

This chapter includes the parameters for the 36 kByte embedded flash module.

29.4.1 Flash Parameters

Table 28 Flash Characteristics[1)]

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Programming time per 128 byte page	t_{PR}	–	3[2)]	3.5	ms	3V < V_S < 28V	P_4.1.1
Erase time per sector/page	t_{ER}	–	4[2)]	4.5	ms	3V < V_S < 28V	P_4.1.2
Data retention time	t_{RET}	20	–	–	years	1,000 erase / program cycles	P_4.1.3
Data retention time	t_{RET}	50	–	–	years	1,000 erase / program cycles T_j = 30°C[3)]	P_4.1.9
Flash erase endurance for user sectors	N_{ER}	30	–	–	kcycles	Data retention time 5 years	P_4.1.4
Flash erase endurance for security pages	N_{SEC}	10	–	–	cycles	[4)]Data retention time 20 years	P_4.1.5
Drain disturb limit	N_{DD}	32	–	–	kcycles	[5)]	P_4.1.6

1) Not subject for production test, specified by design.
2) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. The requirement is only relevant for extremely low system frequencies.
3) Derived by extrapolation of lifetime tests.
4) Temperature: 25 °C
5) This parameter limits the number of subsequent programming operations within a physical sector without a given page in this sector being (re-)programmed. The drain disturb limit is applicable if wordline erase is used repeatedly. For normal sector erase/program cycles this limit will not be violated. For data sectors the integrated EEPROM emulation firmware routines handle this limit automatically, for wordline erases in code sectors (without EEPROM emulation) it is recommended to execute a software based refresh, which may make use of the integrated random number generator NVMBRNG to statistically start a refresh.

29.5 Parallel Ports (GPIO)

29.5.1 Description of Keep and Force Current

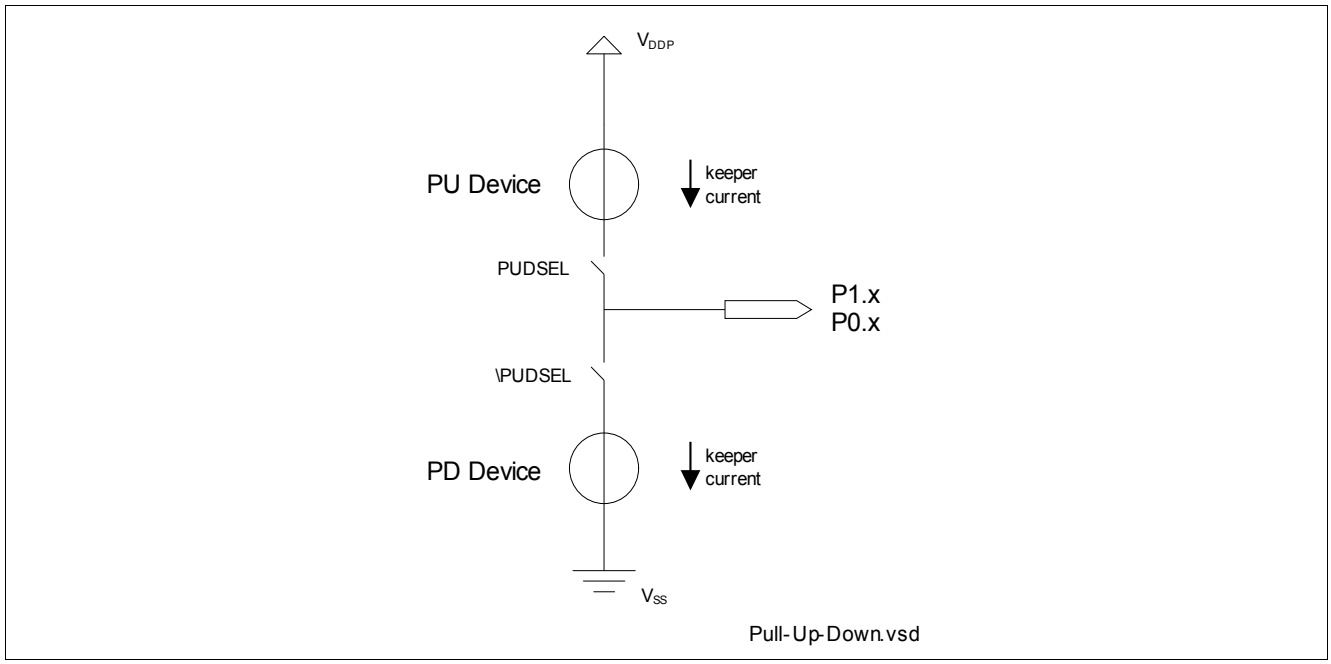


Figure 34 Pull-Up/Down Device

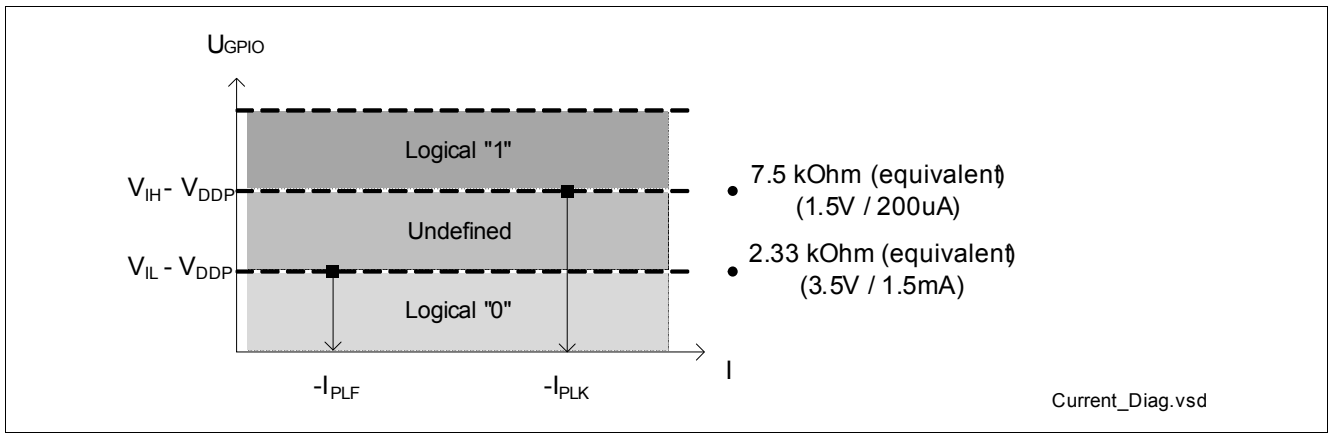


Figure 35 Pull-Up Keep and Forced Current

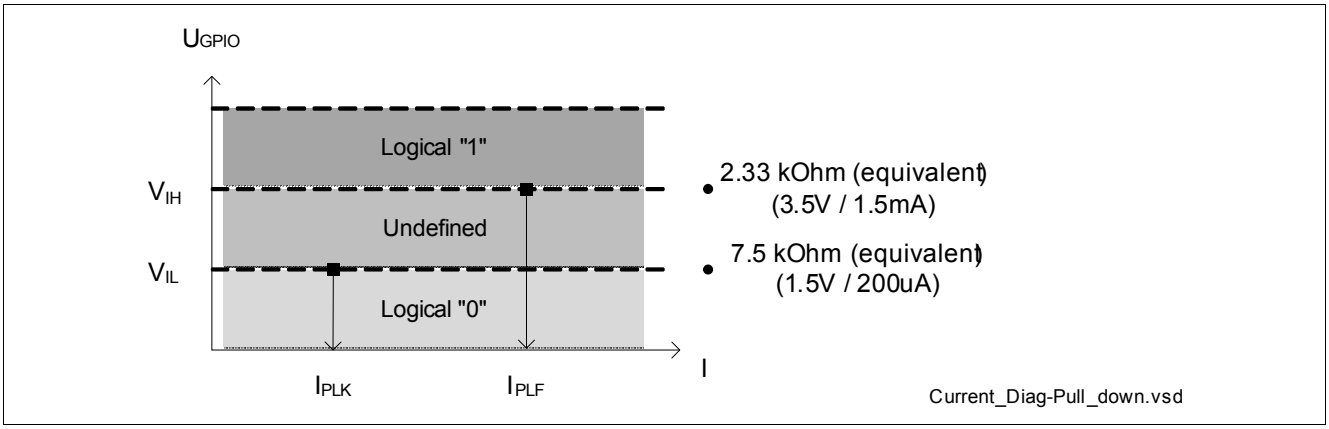


Figure 36 Pull-Down Keep and Force Current

29.5.2 DC Parameters of Port 0, Port 1, TMS and Reset

Note: Operating Conditions apply.
Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the maximum allowed ocurrent which can be taken out of VDDP.

Table 29 Current Limits for Port Output Drivers[1)]

Port Output Driver Mode	Maximum Output Current (I_{OLmax} , - I_{OHmax})		Maximum Output Current (I_{OLnom} , - I_{OHnom})		Number
	V_{DDP} ≥ 4.5V	2.6V < V_{DDP} < 4.5V	V_{DDP} ≥ 4.5V	2.6V < V_{DDP} < 4.5V	
Strong driver[2)]	5 mA	3 mA	1.6 mA	1.0 mA	P_5.1.15
Medium driver[3)]	3 mA	1.8 mA	1.0 mA	0.8 mA	P_5.1.1
Weak driver[3)]	0.5 mA	0.3 mA	0.25 mA	0.15 mA	P_5.1.2

1) Not subject to production test, specified by design.
2) Not available for port pins P0.4, P1.0, P1.1 and P1.2
3) All P0.x and P1.x

Table 30 DC Characteristics Port0, Port1

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input hysteresis	HYS_{P0_P1}	0.11 x V_{DDP}	–	–	V	[1)] Series resistance = 0 Ω; 4.5V ≤ V_{DDP} ≤ 5.5V	P_5.1.5
Input hysteresis	$HYS_{P0_P1_exend}$	–	0.09 x V_{DDP}	–	V	[1)] Series resistance = 0 Ω; 2.6V ≤ V_{DDP} ≤ 4.5V	P_5.1.16

Table 30 DC Characteristics Port0, Port1 (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage	V_{IL}	-0.3	–	0.3 x V_{DDP}	V	2)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.1.3
Input low voltage	V_{IL_extend}	-0.3	0.42 x V_{DDP}	–	V	1)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.1.17
Input high voltage	V_{IH}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	2)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.1.4
Input high voltage	V_{IH_extend}	–	0.52 x V_{DDP}	V_{DDP} + 0.3	V	1)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.1.18
Output low voltage	V_{OL}	–	–	1.0	V	3) 4) I_{OL} ≤ I_{OLmax}	P_5.1.6
Output low voltage	V_{OL}	–	–	0.4	V	3) 5) I_{OL} ≤ I_{OLnom}	P_5.1.7
Output high voltage	V_{OH}	V_{DDP} - 1.0	–	–	V	3) 4) I_{OH} ≥ I_{OHmax}	P_5.1.8
Output high voltage	V_{OH}	V_{DDP} - 0.4	–	–	V	3) 5) I_{OH} ≥ I_{OHnom}	P_5.1.9
Input leakage current	I_{OZ2}	-5	–	+5	µA	6) T_J ≤ 85°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.10
Input leakage current	I_{OZ2}	-15	–	+15	µA	T_J ≤ 150°C, 0.45 V < V_{IN} < V_{DDP}	P_5.1.11
Pull level keep current	I_{PLK}	-200	–	+200	µA	7) V_{PIN} ≥ V_{IH} (up) V_{PIN} ≤ V_{IL} (dn)	P_5.1.12
Pull level force current	I_{PLF}	-1.5	–	+1.5	mA	7) V_{PIN} ≤ V_{IL} (up) V_{PIN} ≥ V_{IH} (dn)	P_5.1.13
Pin capacitance	C_{IO}	–	–	10	pF	1)	P_5.1.14
Reset Pin Timing							
Reset Pin Input Filter Time	T_{filt_RESET}	–	5	–	µs	1)	P_5.1.19

1) Not subject to production test, specified by design.

2) Tested at V_{DDP} = 5V, specified for 4.5V < V_{DDP} < 5.5V.

3) The maximum deliverable output current of a port driver depends on the selected output driver mode. The limit for pin groups must be respected.

4) Tested at 4.9V < V_{DDP} < 5.1V, I_{OL} = 4mA, I_{OH} = -4mA, specified for 4.5V < V_{DDP} < 5.5V.

5) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL}→GND, V_{OH}→V_{DDP}). Tested at 4.9V < V_{DDP} < 5.1V, I_{OL} = 1mA, I_{OH} = -1mA.

6) The given values are worst-case values. In production tests, this leakage current is only tested at 150°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_J = junction temperature [°C]):
I_{OZ} = 0.05 × $e^{(1.5 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 95°C the resulting leakage current is 3.2 µA.
Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]):
I_{OZ} = $I_{OZtempmax}$ - (1.6 × DV) [µA]
This voltage derating formula is an approximation which applies for maximum temperature.

7) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pull-up; $V_{PIN} \leq V_{IL}$ for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pull-up; $V_{PIN} \geq V_{IH}$ for a pull-down.
These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.

29.5.3 DC Parameters of Port 2

These parameters apply to the IO voltage range, 4.5 V ≤ V_{DDP} ≤ 5.5 V.

Note: Operating Conditions apply.
Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Table 31 DC Characteristics Port 2

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage	V_{IL}	-0.3	–	0.3 x V_{DDP}	V	1)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.2.1
Input low voltage	V_{IL_extend}	-0.3	0.42 x V_{DDP}	–	V	2)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.2.10
Input high voltage	V_{IH}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	1)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.2.2
Input high voltage	V_{IH_extend}	–	0.52 x V_{DDP}	V_{DDP} + 0.3	V	2)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.2.11
Input hysteresis	HYS_{P2}	0.11 x V_{DDP}	–	–	V	2)Series resistance = 0 Ω; 4.5V ≤ V_{DDP} ≤ 5.5V	P_5.2.3
Input hysteresis	HYS_{P2_extend}	–	0.09 x V_{DDP}	–	V	2)Series resistance = 0 Ω; 2.6V ≤ VDDP < 4.5V	P_5.2.12
Input leakage current	I_{OZ1}	-400	–	+400	nA	T_J ≤ 85°C, 0 V < V_{IN} < V_{DDP}	P_5.2.4
Pull level keep current	I_{PLK}	-30	–	+30	µA	3) $V_{PIN} \geq V_{IH}$ (up) $V_{PIN} \leq V_{IL}$ (dn)	P_5.2.5
Pull level force current	I_{PLF}	-750	–	+750	µA	3) $V_{PIN} \leq V_{IL}$ (up) $V_{PIN} \geq V_{IH}$ (dn)	P_5.2.6
Pin capacitance (digital inputs/outputs)	C_{IO}	–	–	10	pF	2)	P_5.2.7

1) Tested at V_{DDP} = 5V, specified for 4.5V < V_{DDP} < 5.5V.
2) Not subject to production test, specified by design.
3) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pull-up; $V_{PIN} \leq V_{IL}$ for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pull-up; $V_{PIN} \geq V_{IH}$ for a pull-down.

29.6 PWM Interface

29.6.1 Electrical Characteristics

Table 32 Electrical Characteristics PWM Interface

V_s = 5.5V to 18V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Bus Receiver Interface							
Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.45 × V_S	0.53 x V_S	V	SAE J2602	P_6.1.1
Receiver dominant state	V_{BUSdom}	-27	–	0.4 × V_S	V	–	P_6.1.2
Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	0.47 x V_S	0.55 × V_S	0.6 × V_S	V	SAE J2602	P_6.1.3
Receiver recessive state	V_{BUSrec}	0.6 × V_S	–	1.15 × V_S	V	1)	P_6.1.4
Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	2)	P_6.1.5
Receiver hysteresis	V_{HYS}	0.07 V_S	0.12 × V_S	0.175 × V_S	V	3)	P_6.1.6
Wake-up threshold voltage	$V_{BUS,wk}$	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	–	P_6.1.7
Dominant time for bus wake-up (internal analog filter delay)	$t_{WK,bus}$	3	–	15	µs	The overall dominant time for bus wake-up is a sum of $t_{WK,bus}$ + adjustable digital filter time.	P_6.1.8
Bus Transmitter Interface							
Bus recessive output voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	V_{TxD} = high Level	P_6.1.9
Bus short circuit current	$I_{BUS,sc}$	40	100	150	mA	Current Limitation for driver dominant state driver on V_{BUS} = 18 V;	P_6.1.10
Bus short circuit filter time	$t_{BUS,sc}$	–	1	–	µs	The overall bus short circuit filter time is a sum of $t_{BUS,sc}$ + digital filter time. The digital filter time is 4 µs (typ.)	P_6.1.71
Leakage current (loss of ground)	$I_{BUS_NO_GND}$	-1000	-450	1000	µA	V_S = 12 V; 0 < V_{BUS} < 18 V;	P_6.1.11
Leakage current	$I_{BUS_NO_BAT}$	–	10	20	µA	V_S = 0 V; V_{BUS} = 18 V;	P_6.1.12

Table 32 Electrical Characteristics PWM Interface (cont'd)

V_s = 5.5V to 18V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Leakage current	$I_{BUS_PAS_dom}$	-1	–	–	mA	V_S = 18 V; V_{BUS} = 0 V;	P_6.1.13
Leakage current	$I_{BUS_PAS_rec}$	–	–	20	µA	V_S = 8 V; V_{BUS} = 18 V;	P_6.1.14
Bus pull-up resistance	R_{BUS}	20	30	47	kΩ	Normal mode	P_6.1.15
AC Characteristics - Transceiver Normal Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	–	P_6.1.16
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	–	P_6.1.17
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$;	P_6.1.18
Duty cycle D1 Normal Slope Mode (for worst case at 20 kbit/s)	t_{duty1}	0.396	–	–		[4] duty cycle 1 TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 5.5 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus_rec(min)}$/2 t_{bit};	P_6.1.19
Duty cycle D2 Normal Slope Mode (for worst case at 20 kbit/s)	t_{duty2}	–	–	0.581		[4] duty cycle 2 TH_{Rec}(min) = 0.422 × V_S; TH_{Dom}(min) = 0.284 × V_S; V_S = 5.5 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus_rec(max)}$/2 t_{bit};	P_6.1.20
AC Characteristics - Transceiver Low Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	–	P_6.1.21
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	–	P_6.1.22
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R} = t_{d(L),R} - t_{d(H),R}$;	P_6.1.23

Table 32 Electrical Characteristics PWM Interface (cont'd)

V_s = 5.5V to 18V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Duty cycle D3 (for worst case at 10,4 kbit/s)	t_{duty1}	0.417	–	–		[4] duty cycle 3 TH_{Rec}(max) = 0.778 × V_S; TH_{Dom}(max) = 0.616 × V_S; V_S = 5.5 … 18 V; t_{bit} = 96 µs; D3 = $t_{bus_rec(min)}$/2 t_{bit};	P_6.1.24
Duty cycle D4 (for worst case at 10,4 kbit/s)	t_{duty2}	–	–	0.590		[4] duty cycle 4 TH_{Rec}(min) = 0.389 × V_S; TH_{Dom}(min) = 0.251 × V_S; V_S = 5.5 … 18 V; t_{bit} = 96 µs; D4 = $t_{bus_rec(max)}$/2 t_{bit}	P_6.1.25
AC Characteristics - Transceiver Fast Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	–	P_6.1.26
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	–	P_6.1.27
Receiver delay symmetry	$t_{sym,R}$	-1.5	–	1.5	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$;	P_6.1.28
AC Characteristics - Flash Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	–	P_6.1.31
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	–	P_6.1.32
Receiver delay symmetry	$t_{sym,R}$	-1.0	–	1.5	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$;	P_6.1.33
Duty cycle D7 (for worst case at 115 kbit/s) for +1 µs Receiver delay symmetry	t_{duty1}	0.399	–	–		[5] duty cycle D7 THRec(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 13.5 V; t_{bit} = 8.7 µs; D7 = $t_{bus_rec(min)}$/2 t_{bit};	P_6.1.34
Duty cycle D8 (for worst case at 115 kbit/s) for +1 µs Receiver delay symmetry	t_{duty2}	–	–	0.578		[6] duty cycle 8 TH_{Rec}(min) = 0.422 × V_S; TH_{Dom}(min) = 0.284 × V_S;V_S = 13.5 V; t_{bit} = 8.7 µs; D8 = $t_{bus_rec(max)}$/2 t_{bit};	P_6.1.35
PWM interface input capacity	C_{PWM_IN}	–	15	30	pF	[6]	P_6.1.69

Table 32 Electrical Characteristics PWM Interface (cont'd)

V_s = 5.5V to 18V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
TxD dominant time out	$t_{timeout}$	6	12	20	ms	V_{TxD} = 0 V	P_6.1.36
Thermal Shutdown (Junction Temperature)							
Thermal shutdown temp.	T_{jSD}	160	180	200	°C	7)	P_6.1.65
Thermal shutdown hyst.	ΔT	–	10	–	K	7)	P_6.1.66

1) Maximum limit specified by design.
2) $V_{BUS_CNT} = (V_{th_dom} + V_{th\ rec})/2$
3) $V_{HYS} = V_{BUSrec} - V_{BUSdom}$
4) Bus load :
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
   Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS}
   Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}
5) Bus load
   Load 1 = 1 nF / 500 Ω = C_{BUS} / R_{BUS}
6) Not subject to production test, specified by design.

29.7 High-Speed Synchronous Serial Interface

29.7.1 SSC Timing Parameters

The table below provides the SSC timing in the TLE9871QXA20.

Table 33 SSC Master Mode Timing (Operating Conditions apply; CL = 50 pF)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
SCLK clock period	t_0	1) 2 * T_{SSC}	–	–		2) V_{DDP} > 2.7 V	P_7.1.1
MTSR delay from SCLK	t_1	10	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.2
MRST setup to SCLK	t_2	10	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.3
MRST hold from SCLK	t_3	15	–	–	ns	2) V_{DDP} > 2.7 V	P_7.1.4

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. If f_{CPU} = 20 MHz, t_0 = 100 ns. T_{CPU} is the CPU clock period.
2) Not subject to production test, specified by design.

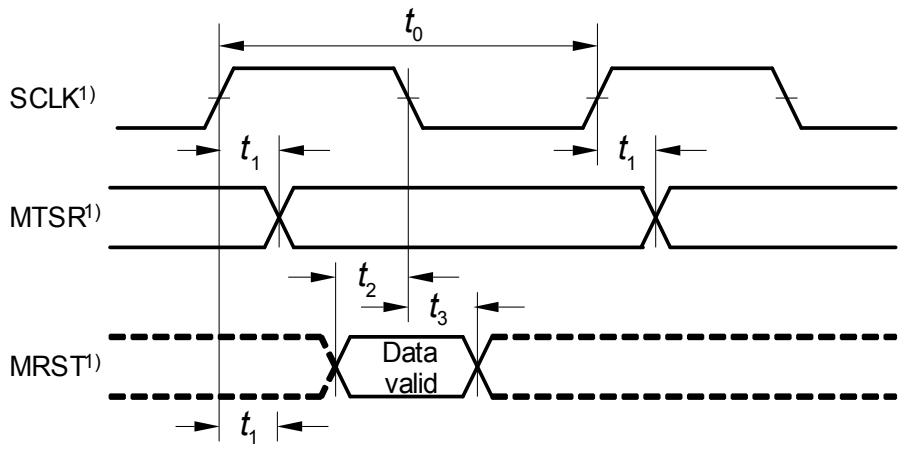


Figure 37 SSC Master Mode Timing

29.8 Measurement Unit

29.8.1 System Voltage Measurement Parameters

Table 34 Supply Voltage Signal Conditioning

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Measurement output voltage range @ VAREF5	V_{A5}	0	–	5	V	–	P_8.1.15
Measurement output voltage range @ VAREF1V2	V_{A1V2}	0	–	1.23	V	–	P_8.1.16
Battery / Supply Voltage Measurement							
Input to output voltage attenuation: V_S	ATT_{VS_1}	–	0.055	–		SFR setting 1	P_8.1.41
Nominal operating input voltage range V_S	$V_{S,range1}$	3	–	22	V	[1]SFR setting 1; Max. value corresponds to typ. ADC full scale input; 3V < V_S < 28V	P_8.1.1
Accuracy of V_S after calibration	$V_{S,range1}$	-312	–	312	mV	SFR setting 1, V_S = 5.5 V to 18V, T_j = -40..85°C	P_8.1.70
Input to output voltage attenuation: V_S	ATT_{VS_2}	–	0.039	–		SFR setting 2	P_8.1.42
Nominal operating input voltage range V_S	$V_{S,range2}$	3	–	31	V	[1]SFR setting 2; Max. value corresponds to typ. ADC full scale input 3V < V_S < 28V	P_8.1.40
Accuracy of V_S after calibration	$V_{S,range2}$	-440	–	440	mV	SFR setting 2, V_S = 5.5V to 18V, T_j = -40..85°C	P_8.1.44
Driver Supply Voltage Measurement V_{SD}							
Input to output voltage attenuation: V_{SD}	ATT_{VSD}	–	0.039	–		–	P_8.1.21
Nominal operating input voltage range V_{SD}	$V_{SD,range}$	2.5	–	31	V	[1]	P_8.1.2

Table 34 Supply Voltage Signal Conditioning (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Accuracy of V_{SD} sense after calibration	ΔV_{SD}	-440	–	440	mV	V_S = 5.5V to 18V, T_j = -40..85°C	P_8.1.47
Charge Pump Voltage Measurement V_{CP}							
Input to output voltage attenuation: V_{CP}	ATT_{VCP}	–	0.023	–		–	P_8.1.56
Nominal operating input voltage range V_{CP}	$V_{CP,range}$	2.5	–	52	V	1)	P_8.1.7
Accuracy of V_{CP} sense after calibration	ΔV_{CP}	-747	–	747	mV	V_S = 5.5V to 18V, T_j = -40..85°C	P_8.1.62
Monitoring Input Voltage Measurement V_{MON}							
Input to output voltage attenuation: V_{MON}	ATT_{VMON}	–	0.039	–		–	P_8.1.49
Nominal operating input voltage range V_{MON}	$V_{MON,range}$	2.5	–	31	V	1)	P_8.1.8
Accuracy of V_{MON} sense after calibration	ΔV_{MON}	-440	–	440	mV	V_S = 5.5V to 18V, T_j = -40..85°C	P_8.1.68
Pad Supply Voltage Measurement V_{VDDP}							
Input-to-output voltage attenuation: V_{DDP}	ATT_{VDDP}	–	0.164	–		–	P_8.1.33
Nominal operating input voltage range V_{DDP}	$V_{DDP,range}$	0	–	7.50	V	1)	P_8.1.50
Accuracy of V_{DDP} sense after calibration	ΔV_{DDP_SENSE}	-105	–	105	mV	2) V_S = 5.5 to 18V, T_j = -40..85°C	P_8.1.5
10-Bit ADC Reference Voltage Measurement V_{AREF}							
Input to output voltage attenuation: V_{AREF}	ATT_{VAREF}	–	0.219	–		–	P_8.1.22
Nominal operating input voltage range V_{AREF}	$V_{AREF,range}$	0	–	5.62	V	1)	P_8.1.51
Accuracy of V_{AREF} sense after calibration	ΔV_{AREF}	-79	–	79	mV	V_S = 5.5V to 18V, T_j = -40..85°C	P_8.1.48
8-Bit ADC Reference Voltage Measurement V_{BG}							
Input-to-output voltage attenuation: V_{BG}	ATT_{VBG}	–	0.75	–		–	P_8.1.57

Table 34 Supply Voltage Signal Conditioning (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating input voltage range V_{BG}	$V_{BG,range}$	0.8	–	1.64	V	1)	P_8.1.52
Core supply Voltage Measurement V_{DDC}							
Input-to-output voltage attenuation: V_{DDC}	ATT_{VDDC}	–	0.75	–		–	P_8.1.34
Nominal operating input voltage range V_{DDC}	$V_{DDC,range}$	0.8	–	1.64	V	1)	P_8.1.53
Accuracy of V_{DDC} sense after calibration	ΔV_{DDC_SENSE}	-22	–	22	mV	V_S = 5.5 to 18V, T_j = -40..85°C	P_8.1.6
VDH Input Voltage Measurement $V_{VDH10BITADC}$							
VDH Input to output voltage attenuation:	ATT_{VDH_1}	–	0.1666667	–		SFR setting 1	P_8.1.64
VDH Input to output voltage attenuation:	ATT_{VDH_2}	–	0.22600	–		SFR setting 2	P_8.1.65
Nominal operating input voltage range V_{VDH}, Range 1	$V_{VDH,range1}$	–	–	30		SFR setting 1	P_8.1.66
Nominal operating input voltage range V_{VDH}, Range 2	$V_{VDH,range2}$	–	–	20		SFR setting 2	P_8.1.67
V_{VDH} 10-bit ADC, Range 1	$\Delta V_{VDHADC10B}$	-300	–	300	mV	V_S= 5.5 to 18V, T_j = -40..85°C	P_8.1.39
V_{VDH} 10-bit ADC, Range 2	$\Delta V_{VDHADC10B}$	-200	–	200	mV	V_S= 5.5V to 18V, T_j = -40..85°C	P_8.1.71
10-Bit ADC measurement input resistance for VDH	$R_{in_VDH,measure}$	200	390	470	kΩ	PD_N=1 (on-state)	P_8.1.3
Measurement input leakage current for V_{VDH}	$I_{leak_VDH,\ measure}$	0	–	2.0	µA	PD_N=0 (off-state),	P_8.1.10

1) Not subject to production test, specified by design.

2) Accuracy is valid for a calibrated device.

29.8.2 Central Temperature Sensor Parameters

Table 35 Electrical Characteristics Temperature Sensor Module

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output voltage V_{TEMP} at T_0=273 K (0°C)	a	–	0.666	–	V	1) T_0=273 K (0°C)	P_8.2.2
Temperature sensitivity b	b	–	2.31	–	mV/K	1)	P_8.2.4
Accuracy_1	Acc_1	-10	–	10	°C	2)1) -40°C < Tj < 85°C	P_8.2.5
Accuracy_2	Acc_2	-10	–	10	°C	2)1) 125°C < Tj < 150°C	P_8.2.6
Accuracy_3	Acc_3	-5	–	5	°C	2)1) 85°C < Tj < 125°C	P_8.2.7

1) Not subject to production test, specified by design

2) Accuracy with reference to on-chip temperature calibration measurement, valid for Mode1

29.8.3 ADC2

29.8.3.1 ADC2 Specifications

Table 36 DC Specifications

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Resolution	RES	–	8	–	Bits	Full	P_8.3.18
Guaranteed offset error	–	-2.0	±0.3	2.0	LSB	not calibrated	P_8.3.19
Gain error	–	-2.0	±0.5	2.0	%FSR	not calibrated	P_8.3.20
Differential non-linearity (DNL)	–	-0.8	±0	0.8	LSB	Full	P_8.3.21
Integral non-linearity (INL)	–	-1.2	±0	1.2	LSB	–	P_8.3.22
Input referred noise	–	–	0.5	1.5	LSBrms	1)@ T_J = 27°C	P_8.3.23

1) Not subject to production test, specified by design.

29.9 ADC1 - VAREF

29.9.1 Electrical Characteristics VAREF

Table 37 Electrical Characteristics VAREF

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Required buffer capacitance	C_{VAREF}	0.1	–	1	µF	ESR < 1Ω	P_9.1.1
Reference output voltage	V_{AREF}	4.95	5	5.05	V	V_S > 5.5V	P_9.1.2
DC supply voltage rejection	$DC_{PSRVAREF}$	30	–	–	dB	1) –	P_9.1.3
Supply voltage ripple rejection	$AC_{PSRVAREF}$	26	–	–	dB	1) V_S = 13.5V; f = 0 ... 1KHz; V_r = 2Vpp	P_9.1.4
Turn ON time	t_{so}	–	–	200	µs	1) C_{ext} = 100nF PD_N to 99.9% of final value	P_9.1.5
Input resistance at VAREF Pin	$R_{IN,VAREF}$	–	100	–	kΩ	1)input impedance in case of VAREF is applied from external	P_9.1.20

1) Not subject to production test, specified by design.

29.9.2 Electrical Characteristics ADC1 (10-Bit)

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 38 A/D Converter Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Analog reference supply	V_{AREF}	V_{AGND} + 1.0	–	V_{DDPA} + 0.05	V	1)	P_9.2.1
Analog reference ground	V_{AGND}	V_{SS} - 0.05	–	1.5	V	–	P_9.2.2
Analog input voltage range	V_{AIN}	V_{AGND}	–	V_{AREF}	V	2)	P_9.2.3
Analog clock frequency	f_{ADCI}	5	–	24	MHz	3)	P_9.2.4
Conversion time for 10-bit result	t_{C10}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	(13 + STC) × t_{ADCI} + 2 x t_{SYS}	–	4)	P_9.2.5
Conversion time for 8-bit result	t_{C8}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	(11 + STC) × t_{ADCI} + 2 × t_{SYS}	–	–	P_9.2.6
Wakeup time from analog powerdown, fast mode	t_{WAF}	–	–	4	µs	1)	P_9.2.7
Wakeup time from analog powerdown, slow mode	t_{WAS}	–	–	15	µs	5)	P_9.2.8
Total unadjusted error (8 bit)	TUE_{8B}	–	±1	±2	counts	6)7) V_{AREF} = 5.0 V	P_9.2.9
Total unadjusted error (10 bit)	TUE_{10B}	–	±6	±12	counts	7)8) V_{AREF} = 5.0 V	P_9.2.22
DNL error	EA_{DNL}	–	±0.8	±3	counts	–	P_9.2.10
INL error with internal 5V reference VAREF	$EA_{INL_int_VAREF}$	–	±0.8	±5	counts	–	P_9.2.11
Gain error with internal 5V reference VAREF	$EA_{GAIN_int_VAREF}$	–	±0.4	±10	counts	–	P_9.2.12
Offset error	EA_{OFF}	–	±0.5	±2	counts	–	P_9.2.13
Total capacitance of an analog input	C_{AINT}	–	–	10	pF	5)9)	P_9.2.14
Switched capacitance of an analog input	C_{AINS}	–	–	4	pF	5)9)	P_9.2.15
Resistance of the analog input path	R_{AIN}	–	–	2	kΩ	5)9)	P_9.2.16

Table 38 A/D Converter Characteristics (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Total capacitance of the reference input	C_{AREFT}	–	–	15	pF	5)9)	P_9.2.17
Switched capacitance of the reference input	C_{AREFS}	–	–	7	pF	5)9)	P_9.2.18
Resistance of the reference input path	R_{AREF}	–	–	2	kΩ	5)9)	P_9.2.19

1) Not subject to production test, specified by design.
2) V_{AIN} may exceed V_{AGND} or V_{AREFx} up to the absolute maximum ratings. However, the conversion result in these cases will be 0000_H or $03FF_H$, respectively.
3) The limit values for f_{ADCI} must not be exceeded when selecting the peripheral frequency and the prescaler setting.
4) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result.
5) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 µs.
6) The total unadjusted error TUE is the maximum deviation from the ideal ADC transfer curve, not the sum of individual errors.
   All error specifications are based on measurement methods standardized by IEEE 1241.2000.
7) The specified TUE is valid only if the absolute sum of input overload currents (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.
8) The total unadjusted error TUE is the maximum deviation from the ideal ADC transfer curve, not the sum of individual errors.
   All error specifications are based on measurement methods standardized by IEEE 1241.2000.
9) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used:
   $C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 5 pF, R_{AINtyp} = 1.0 kΩ, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 10 pF, $R_{AREFtyp}$ = 1.0 kΩ.

29.10 Reserved

29.11 High-Voltage Monitoring Input

29.11.1 Electrical Characteristics

Table 39 Electrical Characteristics Monitoring Input

T_j = -40 °C to +150 °C; V_S = 5.5 V to 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
MON Input Pin characteristics							
Wake-up/monitoring threshold voltage	V_{MONth}	0.4*V_S	0.5*V_S	0.6*V_S	V	Without external serial resistor R_s (with R_s:DV = $I_{PD/PU}$ * R_s); V_S = 5.5V to 18V; T_J = -40°C to 85°C	P_11.1.1
Wake-up/monitoring threshold voltage extended range	V_{MONth_extend}	0.44*V_S	0.53*V_S	0.64*V_S	V	Without external serial resistor R_s (with R_s:DV = $I_{PD/PU}$ * R_s)	P_11.1.11
Threshold hysteresis	$V_{MONth,hys}$	0.015*V_S	0.05*V_S	0.1*V_S	V	In all modes; without external serial resistor R_s (with R_s:dV = $I_{PD/PU}$ * R_s); V_S = 5.5V to 18V;	P_11.1.12
Threshold hysteresis	$V_{MONth,hys}$	0.02*V_S	0.06*V_S	0.12*V_S	V	In all modes; without external serial resistor R_s (with R_s:dV = $I_{PD/PU}$ * R_s); V_S = 18V to 28V;	P_11.1.2
Pull-up current	$I_{PU, MON}$	-20	-10	-1	µA	0.6*V_S	P_11.1.3
Pull-down current	$I_{PD, MON}$	3	10	20	µA	0.4*V_S	P_11.1.4
Input leakage current	$I_{LK,MON}$	-2.5	–	2.5	µA	[1] 0 V < V_{MON_IN} < 28 V	P_11.1.5
Timing							
Wake-up filter time (internal analog filter delay)	$t_{FT,MON}$	–	500	–	ns	[2] The overall filter time for MON wake-up is a sum of $t_{FT,MON}$ + adjustable digital filter time. The digital filter time can be adjusted by PMU.CNF_WAKE_FILTER.CNF_MON_FT;	P_11.1.6

1) Input leakage is valid for disabled state.

2) With pull-up, pull down current disabled.

29.12 MOSFET Driver

29.12.1 Electrical Characteristics

Table 40 Electrical Characteristics MOSFET Driver

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
MOSFET Driver Output							
Source current - Charge current (low gate voltage)	I_{Soumax}	200	250	420	mA	V_{SD} > 8 V, C_{Load} = 10 nF, I_{SOU} = C_{Load} * slew rate, (= (20%-50%) / t_{SLEW}), I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.44
Sink current - Discharge current	$I_{Sinkmax}$	200	250	420	mA	V_{SD} > 8 V, C_{Load} = 10 nF, I_{SOU} = C_{Load} * slew rate, (= (50%-20%) / t_{SLEW}), I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.45
High level output voltage Gxx vs. Sxx	V_{Gxx1}	10	–	14	V	V_{SD} > 8V[1], C_{Load} = 10 nF	P_12.1.3
High level output voltage GHx vs. SHx	V_{Gxx2}	8	–	–	V	V_{SD} = 6.4 V[1)2)], C_{Load} = 10 nF	P_12.1.4
High level output voltage GHx vs. SHx	V_{Gxx3}	7	–	–	V	V_{SD} = 5.4 V[1)], C_{Load} = 10 nF	P_12.1.5
High level output voltage GLx vs. GND	V_{Gxx6}	8	–	–	V	V_{SD} = 6.4 V[1)2)], C_{Load} = 10 nF	P_12.1.6
High level output voltage GLx vs. GND	V_{Gxx7}	7	–	–	V	V_{SD} = 5.4 V[1)], C_{Load} = 10 nF	P_12.1.7
Rise time	t_{rise3_3nf}	–	200	–	ns	[2)]C_{Load} = 3.3 nF, V_{SD} > 8 V, 25-75%, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.8
Fall time	t_{fall3_3nf}	–	200	–	ns	[2)]C_{Load} = 3.3 nF, V_{SD} > 8 V, 75-25%, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.9
Rise time	$t_{risemax}$	100	250	450	ns	C_{Load} = 10 nF, V_{SD} > 8 V, 25-75%, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.57

Table 40 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Fall time	$t_{fallmax}$	100	250	450	ns	C_{Load} = 10 nF, V_{SD} > 8 V, 75-25%, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.58
Rise time	$t_{risemin}$	1.25	2.5	5	µs	2) C_{Load} = 10 nF, V_{SD} > 8 V, 25-75%, I_{CHARGE} = I_{DISCHG} = 3(min)	P_12.1.14
Fall time	$t_{fallmin}$	1.25	2.5	5	µs	2) C_{Load} = 10 nF, V_{SD} > 8 V, 75-25%, I_{CHARGE} = I_{DISCHG} = 3(min)	P_12.1.15
Absolute rise - fall time difference for all LSx	$t_{r_f(diff)LSx}$	–	–	100	ns	C_{Load} = 10 nF, V_{SD} > 8 V, 25-75%, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.35
Absolute rise - fall time difference for all HSx	$t_{r_f(diff)HSx}$	–	–	100	ns	C_{Load} = 10 nF, V_{SD} > 8 V, 25-75%, I_{CHARGE} = I_{DISCHG} = 31(max)	P_12.1.36
Resistor between GHx/GLx and GND	R_{GGND}	30	40	50	kΩ	2) –	P_12.1.11
Resistor between SHx and GND	R_{SHGN}	30	40	50	kΩ	2)3) This resistance is the resistance between GHx and GND connected through a diode to SHx. As a consequence, the voltage at SHx can rise up to 0,6V typ. before it is discharged through the resistor.	P_12.1.10
Low RDSON mode (boosted discharge mode)	R_{ONCCP}	–	9	12	Ω	V_{VSD} = 13.5 V, V_{VCP} = V_{VSD} + 14.0 V; I_{CHARGE} = I_{DISCHG} = 31(max); 50mA forced into Gx, Sx grounded	P_12.1.50
Resistance between VDH and VSD	I_{BSH}	–	4	–	kΩ	2)	P_12.1.24
Input propagation time (LS on)	$t_{P(ILN)min}$	–	1.5	3	µs	C = 10 nF, (25%) / t_{SLEWon} 2)4)	P_12.1.37

Table 40 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input propagation time (LS off)	$t_{P(ILF)min}$	–	1.5	3	µs	C = 10 nF, (75%) / $t_{SLEWoff}$ 2)4)	P_12.1.38
Input propagation time (HS on)	$t_{P(IHN)min}$	–	1.5	3	µs	C = 10 nF, (25%) / t_{SLEWon} 2)4)	P_12.1.39
Input propagation time (HS off)	$t_{P(IHF)min}$	–	1.5	3	µs	C = 10 nF, (75%) / $t_{SLEWoff}$ 2)4)	P_12.1.40
Input propagation time (LS on)	$t_{P(ILN)max}$	–	200	350	ns	C = 10 nF, (25%) / t_{SLEWon} 5)	P_12.1.26
Input propagation time (LS off)	$t_{P(ILF)max}$	–	200	300	ns	C = 10 nF, (75%) / $t_{SLEWoff}$ 5)	P_12.1.27
Input propagation time (HS on)	$t_{P(IHN)max}$	–	200	350	ns	C = 10 nF, (25%) / t_{SLEWon} 5)	P_12.1.28
Input propagation time (HS off)	$t_{P(IHF)max}$	–	200	300	ns	C = 10 nF, (75%) / $t_{SLEWoff}$ 5)	P_12.1.29
Absolute input propagation time difference between propagation times for all LSx (LSx on)	$t_{Pon(diff)LSx}$	–	–	100	ns	C = 10 nF, (25%) / t_{SLEWon} 5)	P_12.1.30
Absolute input propagation time difference between propagation times for all LSx (LSx off)	$t_{Poff(diff)LSx}$	–	–	100	ns	C = 10 nF, (75%) / $t_{SLEWoff}$ 5)	P_12.1.41
Absolute input propagation time difference between propagation times for all HSx (HSx on)	$t_{Pon(diff)HSx}$	–	–	100	ns	C = 10 nF, (25%) / t_{SLEWon} 5)	P_12.1.42
Absolute input propagation time difference between propagation times for all HSx (HSx off)	$t_{Poff(diff)HSx}$	–	–	100	ns	C = 10 nF, (75%) / $t_{SLEWoff}$ 5)	P_12.1.43
Drain source monitoring							
Drain source monitoring threshold	$V_{DSMONVTH}$	–	– 0.25 0.50 0.75 1.00 1.25 1.5 1.75 2.00	–	V	DRV_CTRL3.DSMONVTH<2:0> 000 001 010 011 100 101 110 111	P_12.1.46

Table 40 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Open load diagnosis currents							
Pull-up diagnosis current	I_{PUDiag}	-220	-370	-520	µA	I_{DISCHG} = 1; V_{SHx} = 5.0 V	P_12.1.47
Pull-down diagnosis current	I_{PDDiag}	650	900	1100	µA	I_{DISCHG} = 1; V_{SHx} = 5.0 V	P_12.1.48
Charge pump							
Output voltage VCP vs. VSD	V_{CPmin1}	8.5	–	–	V	V_{VSD} = 5.4V, I_{CP}=5 mA, Bridge Driver enabled	P_12.1.53
Regulated output voltage VCP vs. VSD	V_{CP}	12	14	16	V	8 V < V_{VSD} < 28, I_{CP}=10mA, @250kHz f_{CP}	P_12.1.49
Turn ON Time	t_{ON_VCP}	80	88	120	us	8 V < V_{VSD} < 28, (25%)[2)6)], C_{CP1}, C_{CP2} = 220 nF, f_{CP} = 250kHz	P_12.1.59
Rise time	t_{rise_VCP}	60	72	88	us	8 V < V_{VSD} < 28, (25-75%)[2)7)], C_{CP1}, C_{CP2} = 220 nF, f_{CP} = 250kHz	P_12.1.60

1) Specification for BLDC Drive, 6 MOSFET switching with 25 KHz. Test condition: I_{Gx} = - 100 µA, ICHARGE = IDISCHARGE = 31(max), IDISCHARGEDIV2_N = 1 and ICHARGEDIV2_N = 1.
2) Not subject to production test.
3) This resistance is connected through a diode between SHx and GHx to ground.
4) ICHARGE = IDISCHARGE = 3(min).
5) ICHARGE = IDISCHARGE = 31(max).
6) This time applies when Bit DRV_CP_CTRL_STS.bit.CP_EN is set
7) This time applies when Bit DRV_CP_CLK_CTRL.bit.CPCLK_EN is set

29.13 Operational Amplifier

29.13.1 Electrical Characteristics

Table 41 Electrical Characteristics Operational Amplifier

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Differential gain (uncalibrated)	G	 9.5 19 38 57	 10 20 40 60	 10.5 21 42 63		Gain settings GAIN<1:0>: 00 01 10 11	P_13.1.6
Differential input operating voltage range OP2 - OP1	V_{IX}	-1.5 / G	–	1.5 / G	V	G is the Gain specified below	P_13.1.1
Operating. common mode input voltage range (referred to GND (OP2 - GND) or (OP1 - GND)	V_{CM}	-2.0	–	2.0	V	Input common mode has to be checked in evaluation if it fits the required range	P_13.1.2
Max. input voltage range (referred to GND (OP_2 - GND) or (OP1 - GND)	V_{IX}	-7.0	–	7.0	V	Max. rating of operational amplifier inputs, where measurement is not done	P_13.1.3
Single ended output voltage range (linear range)	V_{OUT}	V_{ZERO} - 1.5	–	V_{ZERO} + 1.5	V	[1)2)] Offset output voltage 2 V ± 1.5V	P_13.1.4
Linearity error	E_{PWM}	-15	–	15	mV	Maximum deviation from best fit straight line divided by max. value of differential output voltage range (0.5V - 3.5V); this parameter is determined at G = 10.	P_13.1.5
Linearity error	$E_{PWM_\%}$	-1.0	–	1.0	%	Maximum deviation from best fit straight line divided by max. value of differential output voltage range (0.5V - 3.5V); this parameter is determined at G = 10.	P_13.1.24
Gain drift		-1	–	1	%	Gain drift after calibration at G = 10.	P_13.1.7

Table 41 Electrical Characteristics Operational Amplifier (cont'd)

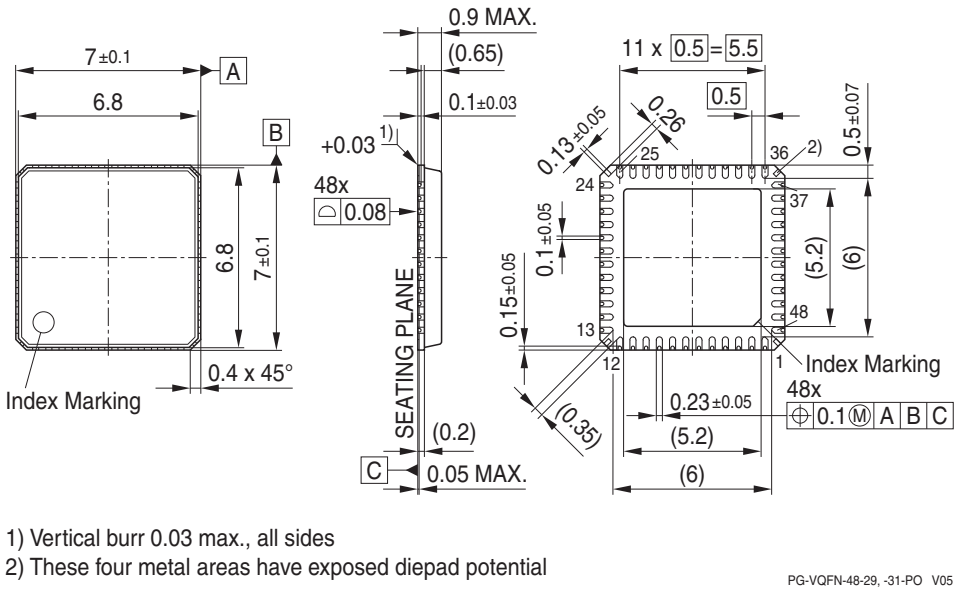
V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
DC input voltage common mode rejection ratio	DC-CMRR	58	80	–	dB	CMRR (in dB)=-20*log (differential mode gain/ common mode gain) V_{CMI}= -2V... 2V, V_{AIP}-V_{AIN}=0V	P_13.1.8
Settling time to 98%	T_{SET}	–	800	1400	ns	Derived from 80 - 20 % rise fall times for ± 2V overload condition (3 Tau value of settling time constant)[2]	P_13.1.9
Current Sense Amplifier Input Resistance @ OP1, OP2	$R_{in_OP1_OP2}$	1	1.25	1.5	kΩ	[2]–	P_13.1.25

1) Typical V_{ZERO} = 0,4 * **VAREF**.

2) This parameter is not subject to production test.

30 Package Outlines



1) Vertical burr 0.03 max., all sides
2) These four metal areas have exposed diepad potential

PG-VQFN-48-29, -31-PO V05

Figure 38 Package outline VQFN-48-31 (with LTI)

Notes

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.*
2. *Dimensions in mm.*

31 Revision History

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Rev. 1.0, 2015-04-30	
all	Initial Release.

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