Dual Precision, Low Cost, High Speed BiFET Op Amp

AD712

FEATURES

- **Enhanced replacement for LF412 and TL082**
- **AC performance**
  - **Settles to ±0.01% in 1.0 µs**
  - **16 V/µs minimum slew rate (AD712J)**
  - **3 MHz minimum unity-gain bandwidth (AD712J)**
- **DC performance**
  - **200 V/mV minimum open-loop gain (AD712K)**
  - **Surface mount available in tape and reel in accordance with the EIA-481A standard**
  - **MIL-STD-883B parts available**
  - **Single version available: AD711**
  - **Quad version: AD713**
  - **Available in PDIP, SOIC_N, and CERDIP packages**

CONNECTION DIAGRAM

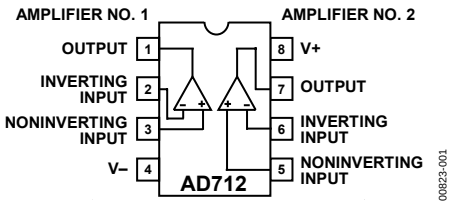


Figure 1. 8-Lead PDIP (N-Suffix), SOIC_N (R-Suffix), and CERDIP (Q-Suffix)

GENERAL DESCRIPTION

The AD712 is a high speed, precision, monolithic operational amplifier offering high performance at very modest prices. Its very low offset voltage and offset voltage drift are the results of advanced laser wafer trimming technology. These performance benefits allow the user to easily upgrade existing designs that use older precision BiFETs and, in many cases, bipolar op amps.

The superior ac and dc performance of this op amp makes it suitable for active filter applications. With a slew rate of 16 V/µs and a settling time of 1 µs to ±0.01%, the AD712 is ideal as a buffer for 12-bit digital-to-analog and analog-to-digital converters and as a high speed integrator. The settling time is unmatched by any similar IC amplifier.

The combination of excellent noise performance and low input current also make the AD712 useful for photo diode preamps. Common-mode rejection of 88 dB and open-loop gain of 400 V/mV ensure 12-bit performance even in high speed unity-gain buffer circuits.

The AD712 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD712J and AD712K are rated over the commercial temperature range of 0°C to 70°C. The AD712A is rated over the industrial temperature range of −40°C to +85°C. The AD712S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, in addition to other environmental and physical tests.

The AD712 is available in 8-lead PDIP, SOIC_N, and CERDIP packages.

PRODUCT HIGHLIGHTS

1. The AD712 offers excellent overall performance at very competitive prices.
2. The Analog Devices, Inc. advanced processing technology and 100% testing guarantee a low input offset voltage (3 mV maximum, J grade). Input offset voltage is specified in the warmed-up condition.
3. Together with precision dc performance, the AD712 offers excellent dynamic response. It settles to ±0.01% in 1 µs and has a minimum slew rate of 16 V/µs. Thus, this device is ideal for applications such as DAC and ADC buffers that require a combination of superior ac and dc performance.

Rev. G
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REVISION HISTORY

8/06—Rev. F to Rev. G

Edits to Figure 1 1
Change to 9-Pole Chebychev Filter Section 18

6/06—Rev. E to Rev. F

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Deleted B, C, and T Models ..... Universal
Changes to General Description 1
Changes to Product Highlights 1
Changes to Specifications Section 3
Changes to Figure 43 15

7/02—Rev. D to Rev. E

Edits to Features 1

9/01—Rev. C to Rev. D

Edits to Features 1
Edits to General Description 1
Edits to Connection Diagram 1
Edits to Ordering Guide 3
Deleted Metalization Photograph 3
Edits to Absolute Maximum Ratings 3
Edits to Figure 7 9
Edits to Outline Dimensions 15

SPECIFICATIONS

V_S = ±15 V @ T_A = 25°C, unless otherwise noted. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Table 1.

	AD712J/A/S			AD712K			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT OFFSET VOLTAGE[1]							
Initial Offset		0.3	**3/1/1**		0.2	**1.0**	mV
T_{MIN} to T_{MAX}			4/2/**2**			**2.0**	mV
vs. Temp		7	20/20/**20**		7	**10**	µV/°C
vs. Supply	**76**	95		**80**	100		dB
T_{MIN} to T_{MAX}	76/76/**76**			**80**			dB
Long-Term Offset Stability		15			15		µV/month
INPUT BIAS CURRENT[2]							
V_{CM} = 0 V		25	**75**		20	**75**	pA
V_{CM} = 0 V @ T_{MAX}		0.6/1.6/26	1.7/4.8/77		0.5	1.7	nA
V_{CM} = ±10 V			**100**			**100**	pA
INPUT OFFSET CURRENT							
V_{CM} = 0 V		10	**25**		5	**25**	pA
V_{CM} = 0 V @ T_{MAX}		0.3/0.7/11	0.6/1.6/26		0.1	0.6	nA
MATCHING CHARACTERISTICS							
Input Offset Voltage			**3/1/1**			**1.0**	mV
T_{MIN} to T_{MAX}			4/2/**2**			**2.0**	mV
Input Offset Voltage Drift			20/20/**20**			**10**	µV/°C
Input Bias Current			**25**			**25**	pA
Crosstalk							
@ f = 1 kHz		120			120		dB
@ f = 100 kHz		90			90		dB
FREQUENCY RESPONSE							
Small Signal Bandwidth	3.0	4.0		3.4	4.0		MHz
Full Power Response		200			200		kHz
Slew Rate	**16**	20		**18**	20		V/µs
Settling Time to 0.01%		1.0	1.2		1.0	1.2	µs
Total Harmonic Distortion		0.0003			0.0003		%
INPUT IMPEDANCE							
Differential		3×10^{12}||5.5			3×10^{12}||5.5		Ω||pF
Common Mode		3×10^{12}||5.5			3×10^{12}||5.5		Ω||pF
INPUT VOLTAGE RANGE							
Differential[3]		±20			±20		V
Common-Mode Voltage[4]		+14.5, −11.5			+14.5, −11.5		V
T_{MIN} to T_{MAX}	**$-V_S$ + 4**		**$+V_S$ − 2**	**$-V_S$ + 4**		**$+V_S$ − 2**	V
Common-Mode Rejection Ratio							
V_{CM} = ±10 V	**76**	88		**80**	88		dB
T_{MIN} to T_{MAX}	76/76/**76**	84		**80**	84		dB
V_{CM} = ±11 V	**70**	84		**76**	84		dB
T_{MIN} to T_{MAX}	70/70/**70**	80		**74**	80		dB
INPUT VOLTAGE NOISE		2			2		µV p-p
		45			45		nV/√Hz
		22			22		nV/√Hz
		18			18		nV/√Hz
		16			16		nV/√Hz

Parameter	AD712J/A/S Min	AD712J/A/S Typ	AD712J/A/S Max	AD712K Min	AD712K Typ	AD712K Max	Unit
INPUT CURRENT NOISE		0.01			0.01		pA/√Hz
OPEN-LOOP GAIN	**150**	400		**200**	400		V/mV
	100/100/**100**			**100**			V/mV
OUTPUT CHARACTERISTICS							
Voltage	**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		V
	±12/±12/**±12**	+13.8, −13.1		**±12**	+13.8, −13.1		V
Current		+25			+25		mA
POWER SUPPLY							
Rated Performance		±15			±15		V
Operating Range	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		+5.0	**+6.8**		+5.0	**+6.0**	mA

[1] Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = 25°C.
[2] Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = 25°C. For higher temperatures, the current doubles every 10°C.
[3] Defined as voltage between inputs, such that neither exceeds ±10 V from ground.
[4] Typically exceeding −14.1 V negative common-mode voltage on either input results in an output phase reversal.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation[1]	
Input Voltage[2]	±18 V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range	
Q-Suffix	−65°C to +150°C
N-Suffix and R-Suffix	−65°C to +125°C
Operating Temperature Range	
AD712J/K	0°C to 70°C
AD712A	−40°C to +85°C
AD712S	−55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C

[1] Thermal characteristics:
8-lead PDIP package: θ_{JA} = 165°C/W
8-lead CERDIP package: θ_{JC} = 22°C/W; θ_{JA} = 110°C/W
8-lead SOIC package: θ_{JA} = 100°C/W

[2] For supply voltages less than ±18 V, the absolute maximum voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

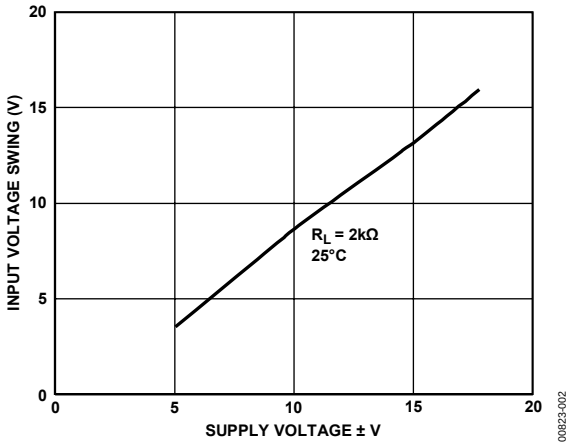


Figure 2. Input Voltage Swing vs. Supply Voltage

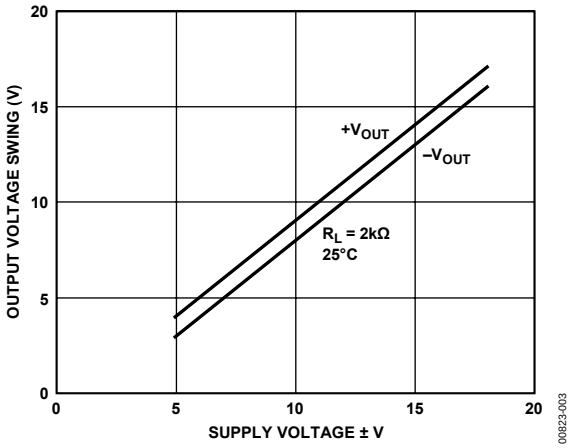


Figure 3. Output Voltage Swing vs. Supply Voltage

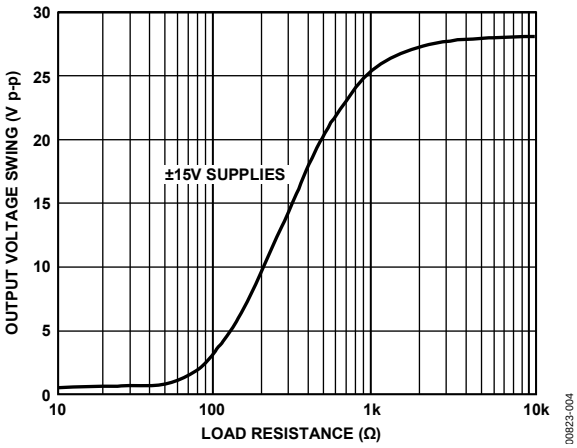


Figure 4. Output Voltage Swing vs. Load Resistance

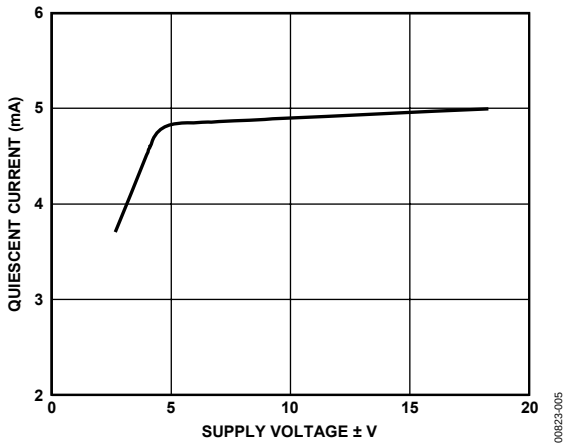


Figure 5. Quiescent Current vs. Supply Voltage

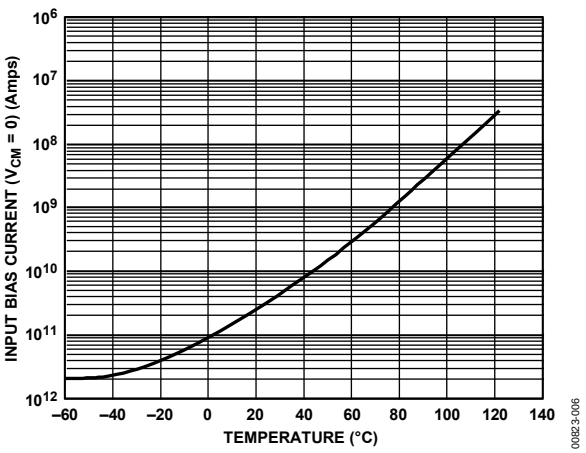


Figure 6. Input Bias Current vs. Temperature

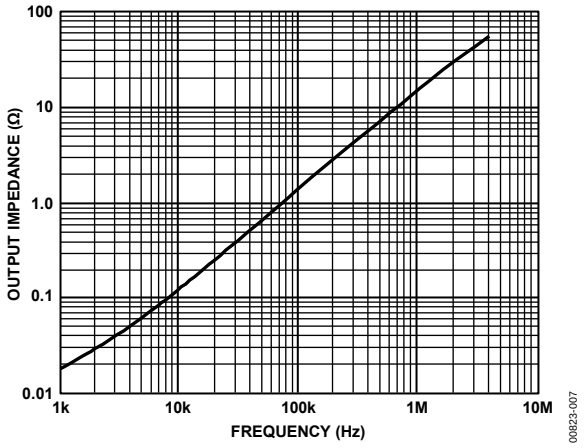


Figure 7. Output Impedance vs. Frequency

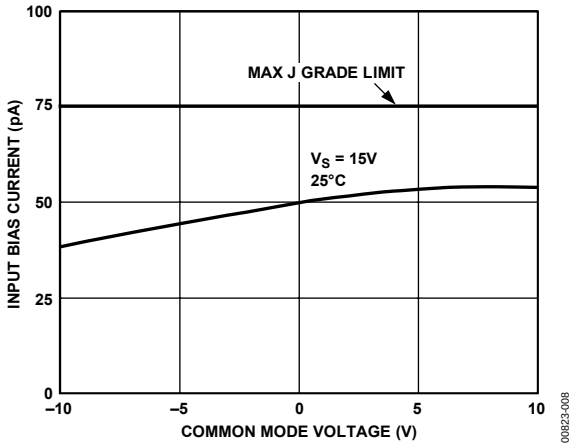


Figure 8. Input Bias Current vs. Common-Mode Voltage

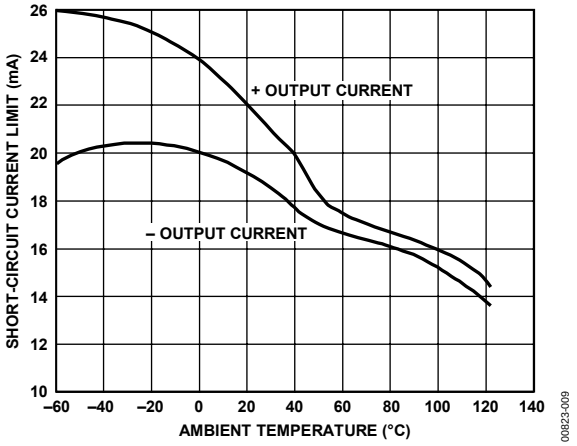


Figure 9. Short-Circuit Current Limit vs. Temperature

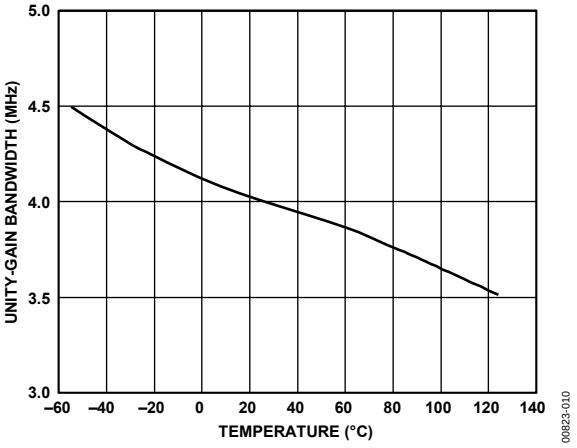


Figure 10. Unity-Gain Bandwidth vs. Temperature

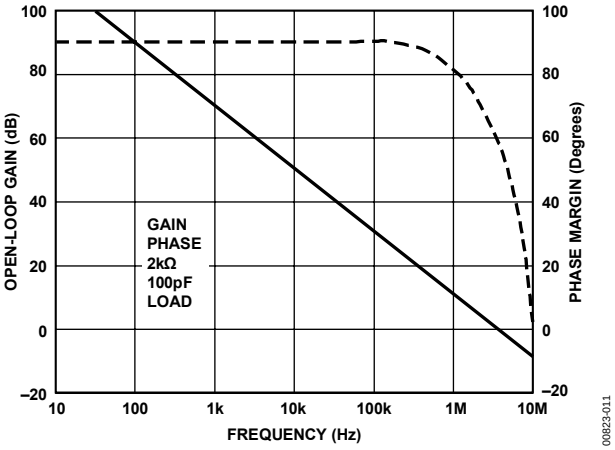


Figure 11. Open-Loop Gain and Phase Margin vs. Frequency

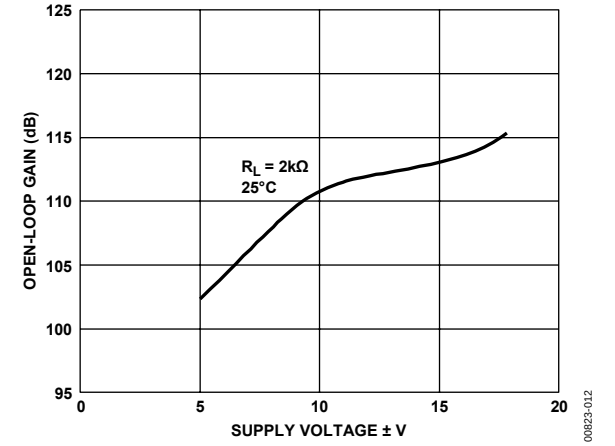


Figure 12. Open-Loop Gain vs. Supply Voltage

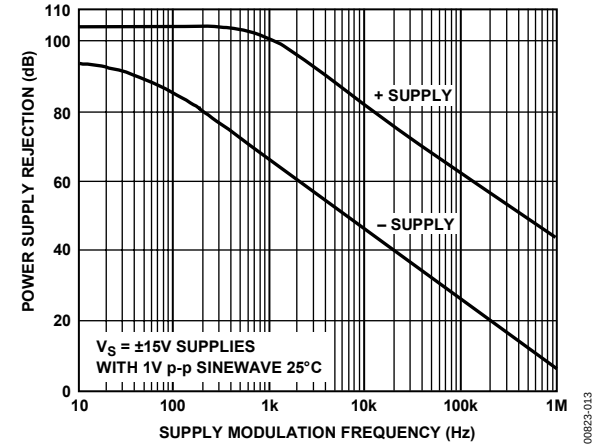


Figure 13. Power Supply Rejection vs. Frequency

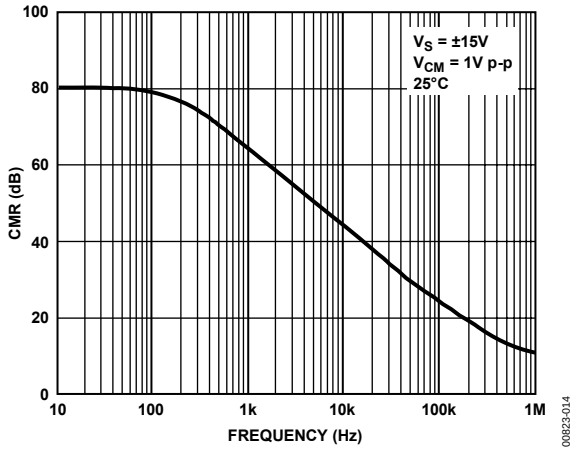


Figure 14. Common-Mode Rejection vs. Frequency

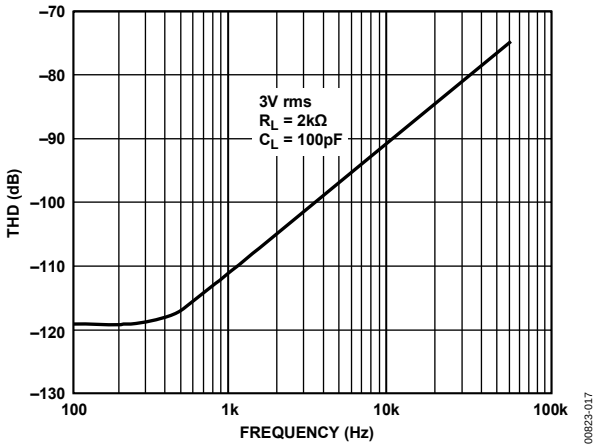


Figure 17. Total Harmonic Distortion vs. Frequency

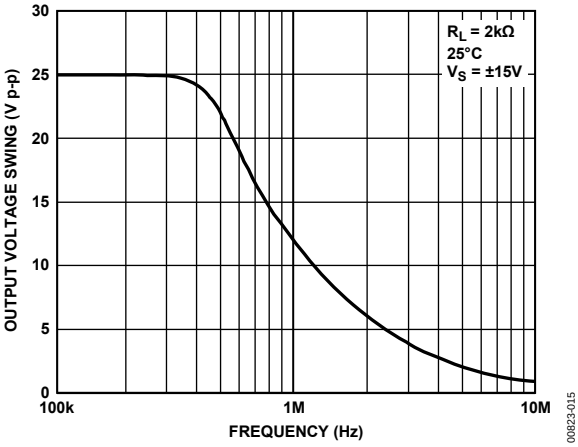


Figure 15. Large Signal Frequency Response

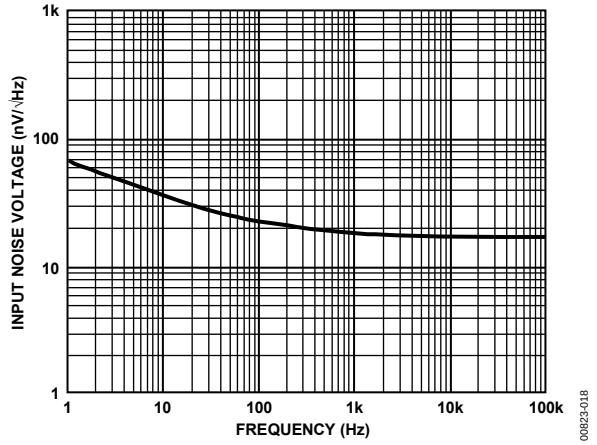


Figure 18. Input Noise Voltage Spectral Density

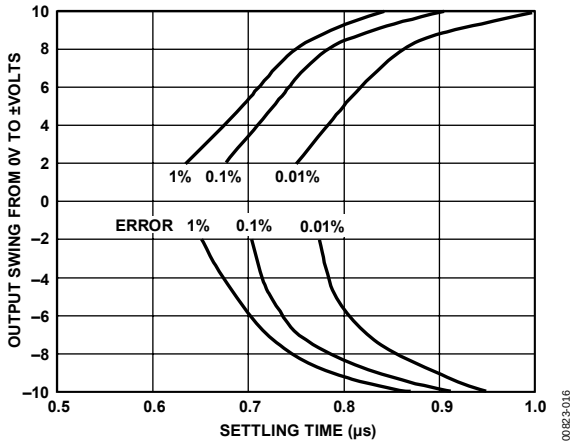


Figure 16. Output Swing and Error vs. Settling Time

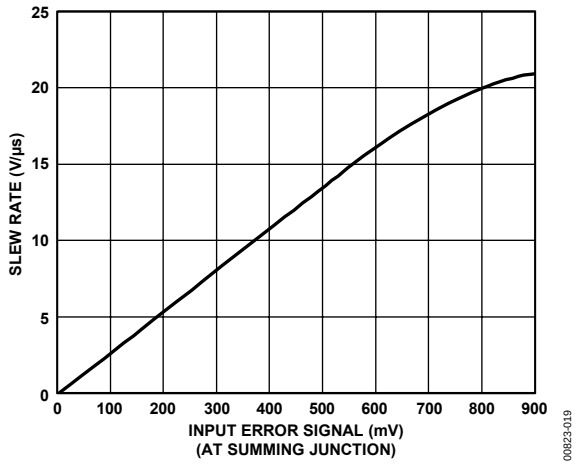


Figure 19. Slew Rate vs. Input Error Signal

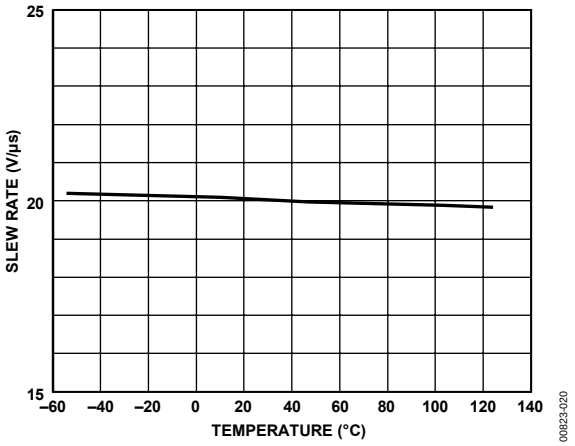


Figure 20. Slew Rate vs. Temperature

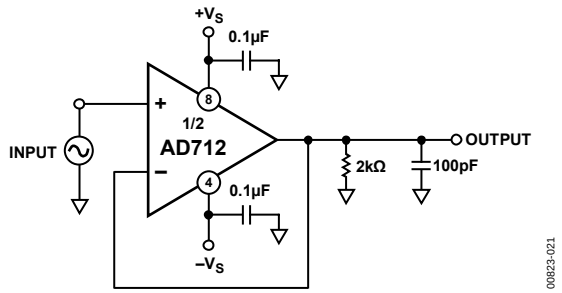


Figure 21. THD Test Circuit

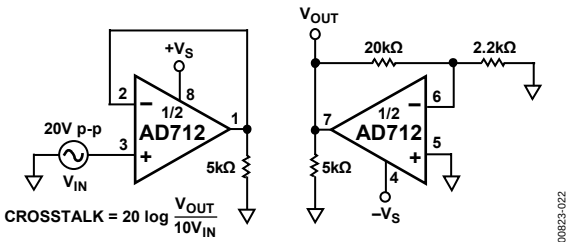


Figure 22. Crosstalk Test Circuit

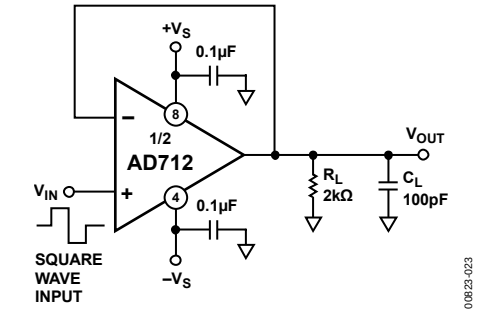


Figure 23. Unity-Gain Follower

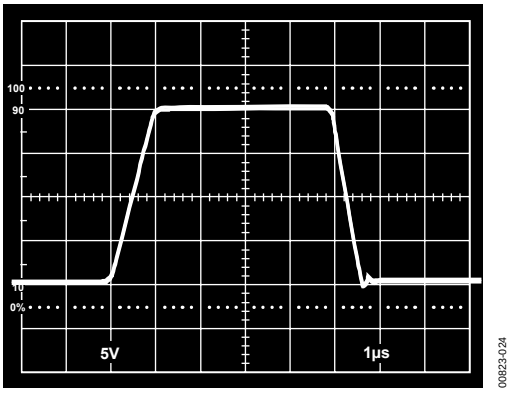


Figure 24. Unity-Gain Follower Pulse Response (Large Signal)

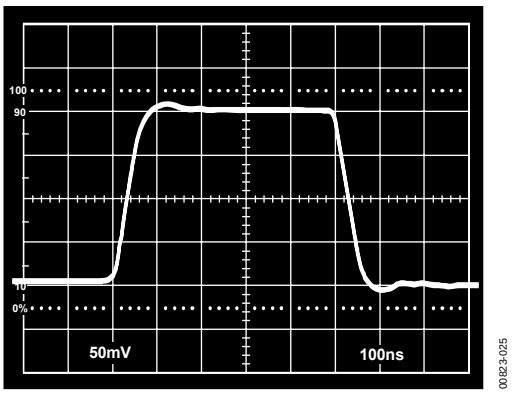


Figure 25. Unity-Gain Follower Pulse Response (Small Signal)

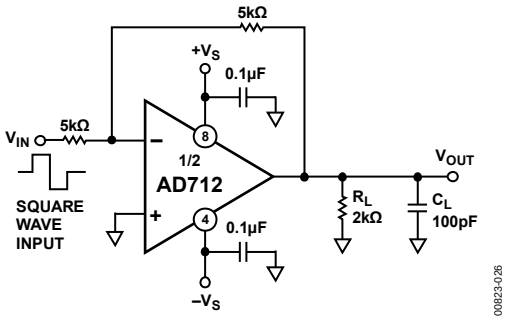


Figure 26. Unity-Gain Inverter

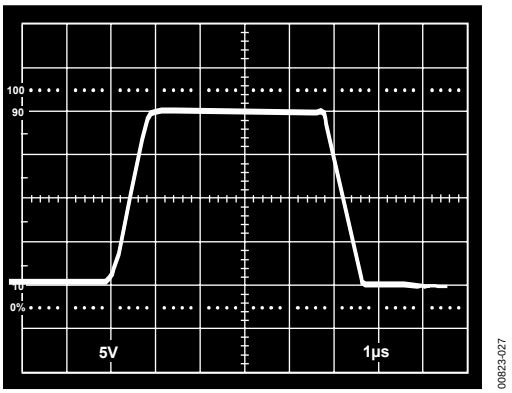


Figure 27. Unity-Gain Inverter Pulse Response (Large Signal)

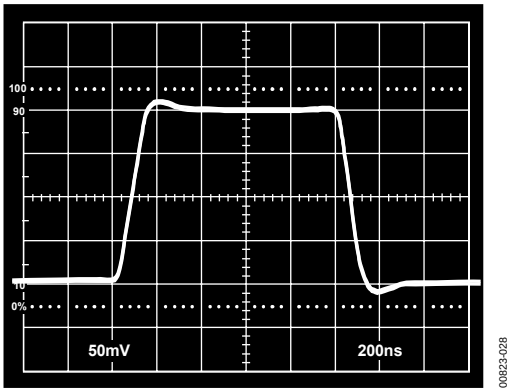


Figure 28. Unity-Gain Inverter Pulse Response (Small Signal)

SETTLING TIME

OPTIMIZING SETTLING TIME

Most bipolar high speed digital-to-analog converters (DACs) have current outputs; therefore, for most applications, an external op amp is required for a current-to-voltage conversion. The settling time of the converter/op amp combination depends on the settling time of the DAC and output amplifier. A good approximation is

$$t_S\,Total = \sqrt{(t_S\,DAC)^2 + (t_S\,AMP)^2}$$

The settling time of an op amp DAC buffer varies with the noise gain of the circuit, the DAC output capacitance, and the amount of external compensation capacitance across the DAC output scaling resistor.

Settling time for a bipolar DAC is typically 100 ns to 500 ns. Previously, conventional op amps have required much longer settling times than have typical state-of-the-art DACs; therefore, the amplifier settling time has been the major limitation to a high speed, voltage output, digital-to-analog function. The introduction of the AD71x family of op amps with their 1 µs (to ±0.01% of final value) settling time permits the full high speed capabilities of most modern DACs to be realized.

In addition to a significant improvement in settling time, the low offset voltage, low offset voltage drift, and high open-loop gain of the AD71x family assure 12-bit accuracy over the full operating temperature range.

The excellent high speed performance of the AD712 is shown in the oscilloscope photos in Figure 30 and Figure 31. Measurements were taken using a low input capacitance amplifier connected directly to the summing junction of the AD712 and both figures show a worst-case situation: full-scale input transition. The 4 kΩ [10 kΩ||8 kΩ = 4.4 kΩ] output impedance of the DAC, together with a 10 kΩ feedback resistor, produce an op amp noise gain of 3.25. The current output from the DAC produces a 10 V step at the op amp output (0 to −10 V shown in Figure 30, and −10 V to 0 V shown in Figure 31).

Therefore, with an ideal op amp, settling to ±1/2 LSB (±0.01%) requires that 375 µV or less appears at the summing junction. This means that the error between the input and output (that voltage which appears at the AD712 summing junction) must be less than 375 µV. As shown in Figure 30, the total settling time for the AD712/AD565A combination is 1.2 microseconds.

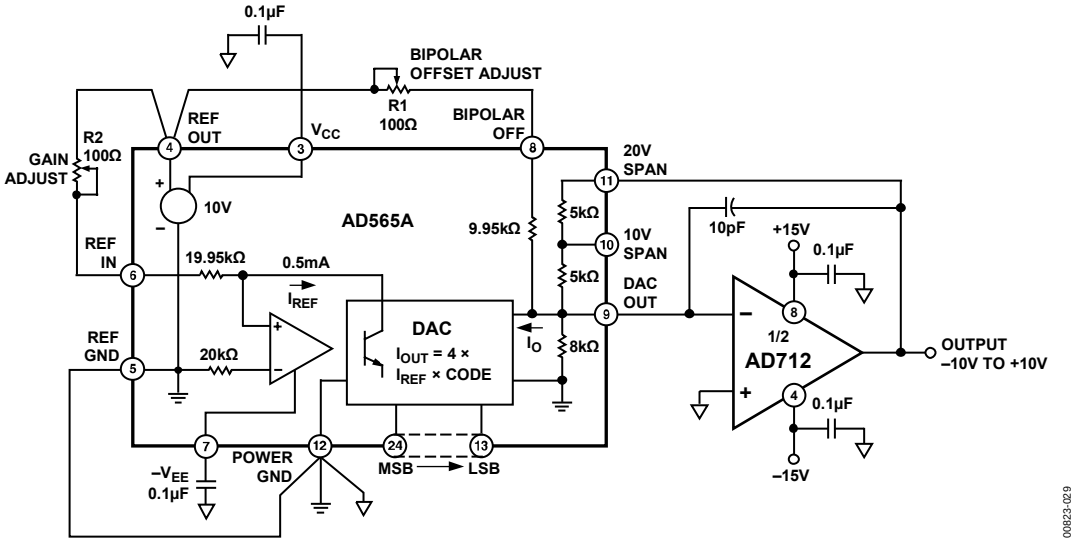


Figure 29. ±10 V Voltage Output Bipolar DAC

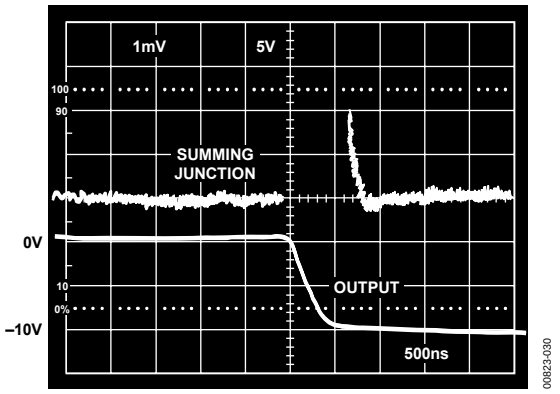


Figure 30. Settling Characteristics for AD712 with AD565A, Full-Scale Negative Transition

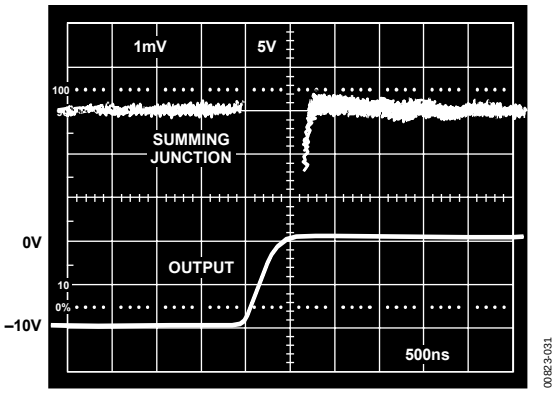


Figure 31. Settling Characteristics for AD712 with AD565A, Full-Scale Positive Transition

OP AMP SETTLING TIME—A MATHEMATICAL MODEL

The design of the AD712 gives careful attention to optimizing individual circuit components; in addition, a careful trade-off was made: the gain bandwidth product (4 MHz) and slew rate (20 V/μs) were chosen to be high enough to provide very fast settling time but not too high to cause a significant reduction in phase margin (and therefore, stability). Thus designed, the AD712 settles to ±0.01%, with a 10 V output step, in under 1 μs, while retaining the ability to drive a 250 pF load capacitance when operating as a unity-gain follower.

If an op amp is modeled as an ideal integrator with a unity-gain crossover frequency of $\omega_O/2\pi$, then Equation 1 accurately describes the small signal behavior of the circuit of Figure 32, consisting of an op amp connected as an I-to-V converter at the output of a bipolar or CMOS DAC. This equation would completely describe the output of the system if not for the finite slew rate and other nonlinear effects of the op amp.

$$\frac{V_O}{I_{IN}} = \frac{-R}{\frac{R(C_X)}{\omega_O}s^2 + \left(\frac{G_N}{\omega_O} + RC_f\right)s + 1} \quad (1)$$

Where

$\frac{\omega_O}{2\pi}$ = unity-gain frequency of the op amp.

G_N = noise gain of circuit $\left(1+\frac{R}{R_O}\right)$.

This equation can then be solved for C_f

$$C_X = \frac{2 - G_N}{R\omega_O} + 2\sqrt{\frac{RC_X\omega_O + (1 - G_N)}{R\omega_O}} \quad (2)$$

In these equations, Capacitance C_X is the total capacitance appearing at the inverting terminal of the op amp. When modeling a DAC buffer application, the Norton equivalent circuit shown in Figure 32 can be used directly; Capacitance C_X is the total capacitance of the output of the DAC plus the input capacitance of the op amp (because the two are in parallel).

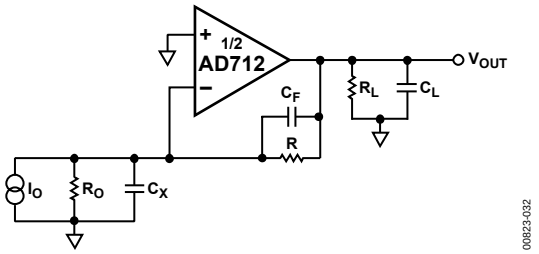


Figure 32. Simplified Model of the AD712 Used as a Current-Out DAC Buffer

When R_O and I_O are replaced with their Thevenin V_{IN} and R_{IN} equivalents, the general-purpose inverting amplifier shown in Figure 33 is created. Note that when using this general model, Capacitance C_X is either the input capacitance of the op amp, if a simple inverting op amp is being simulated, or the combined capacitance of the DAC output and the op amp input if the DAC buffer is being modeled.

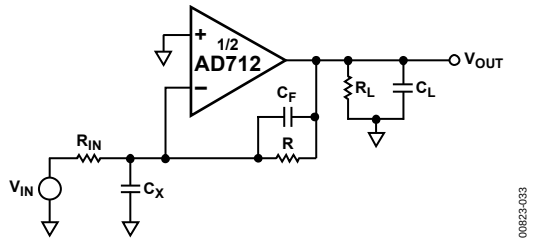


Figure 33. Simplified Model of the AD712 Used as an Inverter

In either case, Capacitance C_X causes the system to go from a one-pole to a two-pole response; this additional pole increases settling time by introducing peaking or ringing in the op amp output. Because the value of C_X can be estimated with reasonable accuracy, Equation 2 can be used to choose a small capacitor (C_F) to cancel the input pole and optimize amplifier response. Figure 34 is a graphical solution of Equation 2 for the AD712 with R = 4 kΩ.

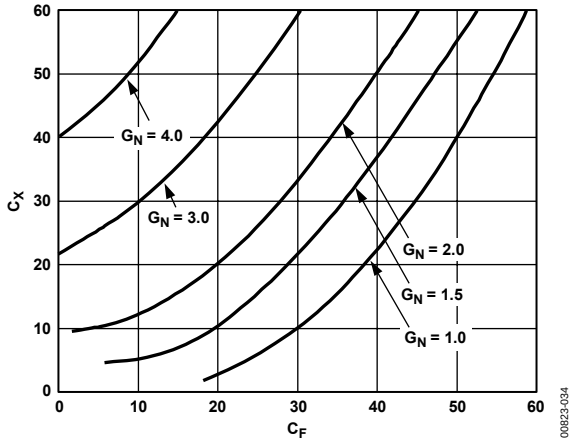


Figure 34. Value of Capacitor C_F vs. Value of C_X

The photos of Figure 35 and Figure 36 show the dynamic response of the AD712 in the settling test circuit of Figure 37.

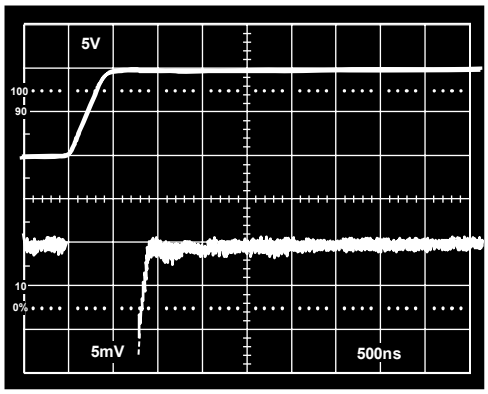


Figure 35. Settling Characteristics 0 V to +10 V Step
Upper Trace: Output of AD712 Under Test (5 V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

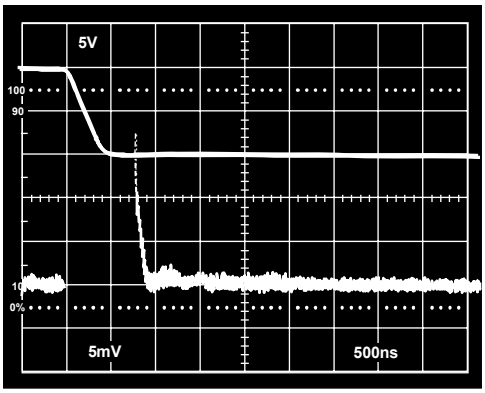


Figure 36. Settling Characteristics 0 V to −10 V Step
Upper Trace: Output of AD712 Under Test (5 V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

The input of the settling time fixture is driven by a flat top pulse generator. The error signal output from the false summing node of A1 is clamped, amplified by A2, and then clamped again. The error signal is thus clamped twice: once to prevent overloading Amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. The Tektronix oscilloscope preamp type 7A26 was carefully chosen because it does not overload with these input levels. Amplifier A2 needs to be a very high speed FET-input op amp; it provides a gain of 10, amplifying the error signal output of A1.

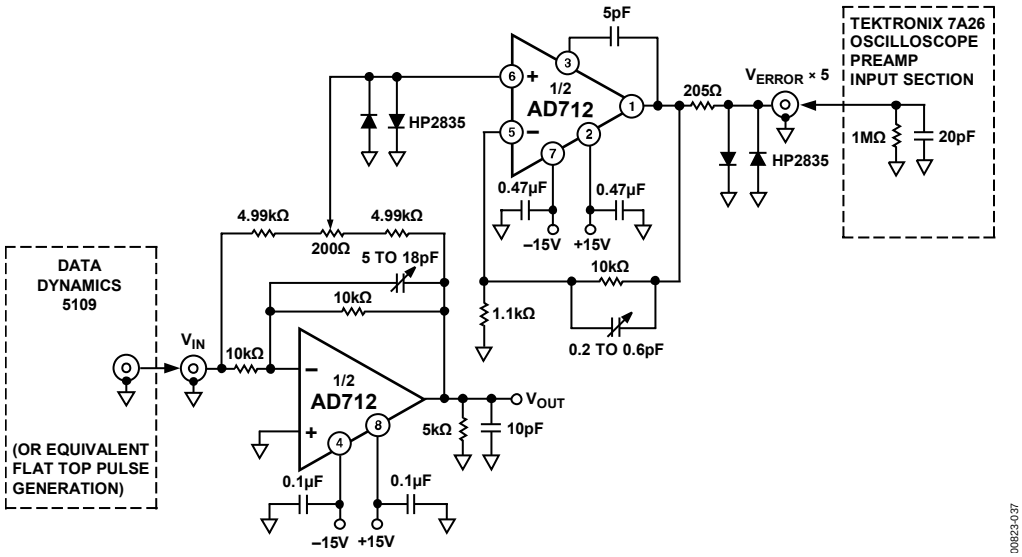


Figure 37. Settling Time Test Circuit

APPLICATIONS INFORMATION

GUARDING

The low input bias current (15 pA) and low noise characteristics of the AD712 BiFET op amp make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of a guarding technique, such as that shown in Figure 38, in printed circuit board layout and construction is critical to minimize leakage currents. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on the printed circuit board.

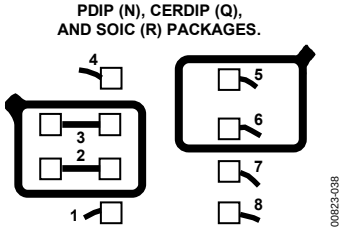


Figure 38. Board Layout for Guarding Inputs

DIGITAL-TO-ANALOG CONVERTER APPLICATIONS

The AD712 is an excellent output amplifier for CMOS DACs. It can be used to perform both 2-quadrant and 4-quadrant operations. The output impedance of a DAC using an inverted R-2R ladder approaches R for codes containing many 1s, and 3R for codes containing a single 1. For codes containing all 0s, the output impedance is infinite.

For example, the output resistance of the AD7545 modulates between 11 kΩ and 33 kΩ. Therefore, with an 11 kΩ DAC internal feedback resistance, the noise gain varies from 2 to 4/3. This changing noise gain modulates the effect of the input offset voltage of the amplifier, resulting in nonlinear DAC amplifier performance.

The AD712K with guaranteed 700 μV offset voltage minimizes this effect to achieve 12-bit performance.

Figure 39 and Figure 40 show the AD712 and AD7545 (12-bit CMOS DAC) configured for unipolar binary (2-quadrant multiplication) or bipolar (4-quadrant multiplication) operation. Capacitor C1 provides phase compensation to reduce overshoot and ringing.

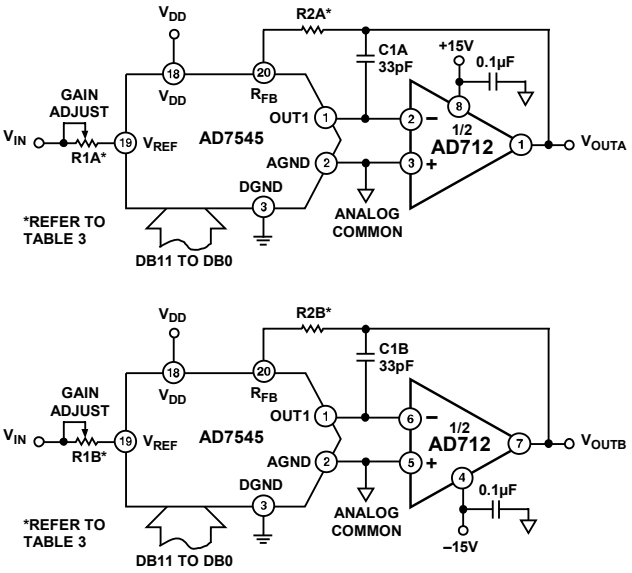


Figure 39. Unipolar Binary Operation

R1 and R2 calibrate the zero offset and gain error of the DAC. Specific values for these resistors depend upon the grade of AD7545 and are listed in Table 3.

Table 3. Recommended Trim Resistor Values vs. Grades of the AD7545 for V_{DD} = 5 V

Trim Resistor	JN/AQ	KN/BQ	LN	GLN
R1	500 Ω	200 Ω	100 Ω	20 Ω
R2	150 Ω	68 Ω	33 Ω	6.8 Ω

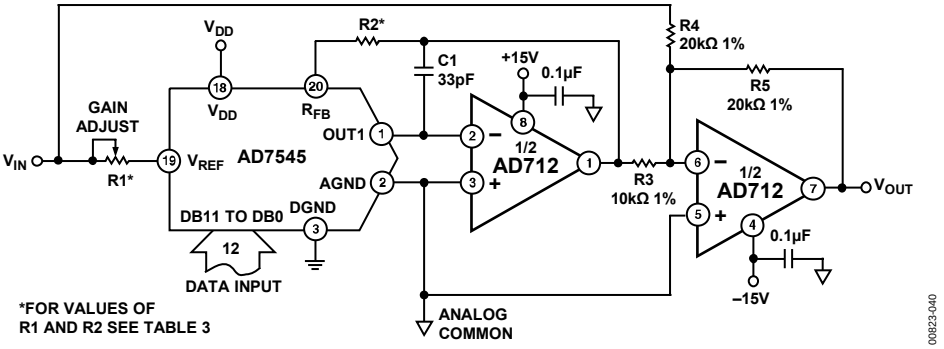


Figure 40. Bipolar Operation

Figure 41 and Figure 42 show the settling time characteristics of the AD712 when used as a DAC output buffer for the AD7545.

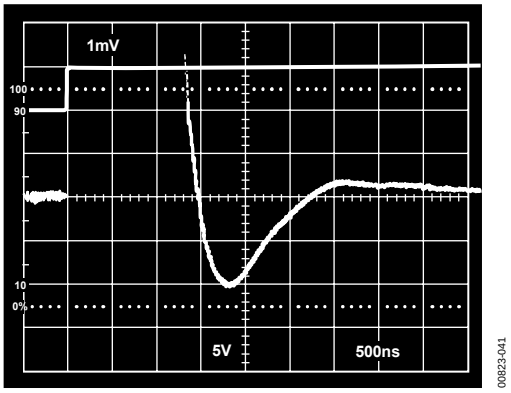


Figure 41. Positive Settling Characteristics for AD712 with AD7545

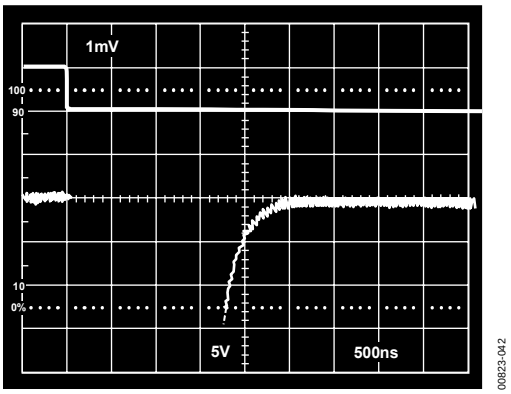


Figure 42. Negative Settling Characteristics for AD712 with AD7545

NOISE CHARACTERISTICS

The random nature of noise, particularly in the flicker noise region, makes it difficult to specify in practical terms. At the same time, designers of precision instrumentation require certain guaranteed maximum noise levels to realize the full accuracy of their equipment. All grades of the AD712 are sample tested on an AQL basis to a limit of 6 µV p-p, 0.1 Hz to 10 Hz.

DRIVING THE ANALOG INPUT OF AN ANALOG-TO-DIGITAL CONVERTER

An op amp driving the analog input of an ADC, such as that shown in Figure 43, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped, but can deviate several hundred millivolts resulting in high frequency modulation of analog-to-digital input current. The output impedance of a feedback amplifier is made artificially low by the loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open-loop value. Most IC amplifiers exhibit a minimum open-loop output impedance of 25 Ω due to current-limiting resistors.

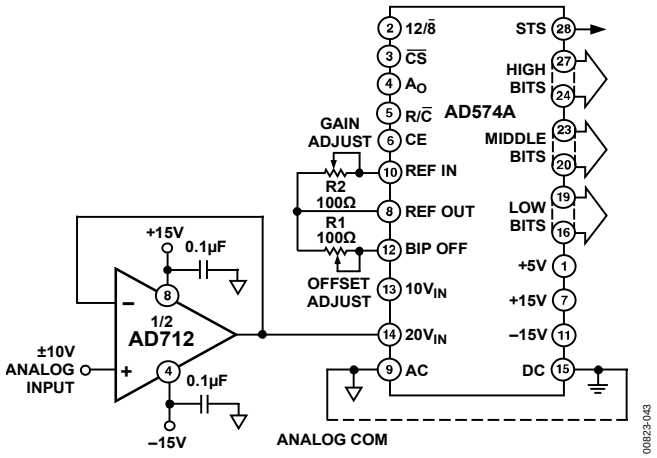


Figure 43. AD712 as An ADC Unity-Gain Buffer

A few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the analog-to-digital conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier output returns to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidth yielding slow recovery from output transients. The AD712 is ideally suited to drive high speed analog-to-digital converters because it offers both wide bandwidth and high open-loop gain.

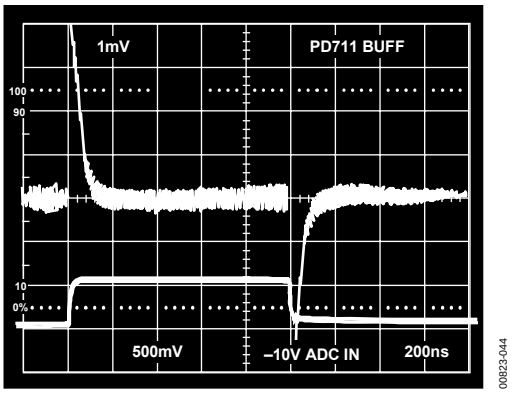


Figure 44. ADC Input Unity Gain Buffer Recovery Times, –10 V ADC IN

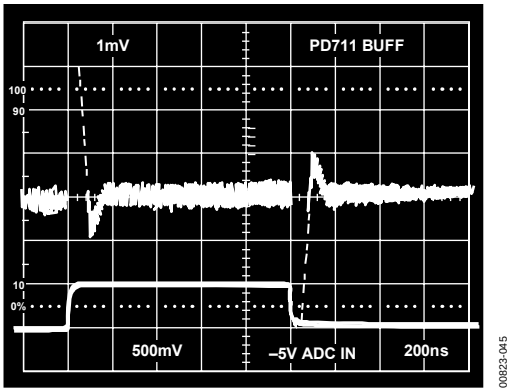


Figure 45. ADC Input Unity Gain Buffer Recovery Times, –5 V ADC IN

DRIVING A LARGE CAPACITIVE LOAD

The circuit in Figure 46 uses a 100 Ω isolation resistor that enables the amplifier to drive capacitive loads exceeding 1500 pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low-pass filter formed by the 100 Ω series resistor and the Load Capacitance C_L. Figure 47 shows a typical transient response for this connection.

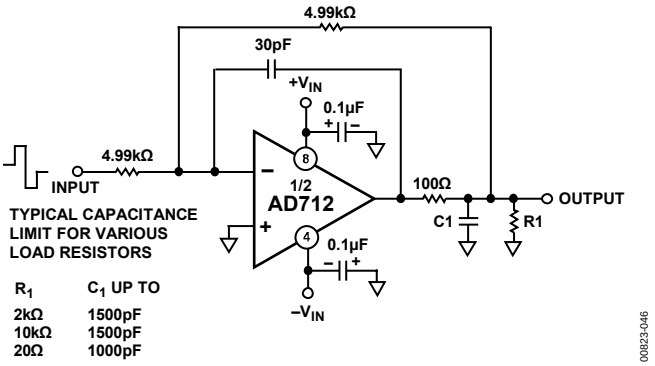


Figure 46. Circuit for Driving a Large Capacitive Load

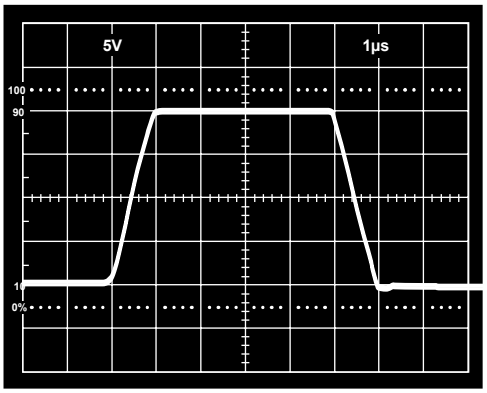


Figure 47. Transient Response R_L = 2 kΩ, C_L = 500 pF

FILTERS

ACTIVE FILTER APPLICATIONS

In active filter applications using op amps, the dc accuracy of the amplifier is critical to optimal filter performance. The amplifier offset voltage and bias current contribute to output error. Offset voltage is passed by the filter and can be amplified to produce excessive output offset. For low frequency applications requiring large value input resistors, bias currents flowing through these resistors also generate an offset voltage.

In addition, at higher frequencies, the op amp dynamics must be carefully considered. Here, slew rate, bandwidth, and open-loop gain play a major role in op amp selection. The slew rate must be fast as well as symmetrical to minimize distortion. The amplifier bandwidth in conjunction with the filter gain dictates the frequency response of the filter.

The use of a high performance amplifier such as the AD712 minimizes both dc and ac errors in all active filter applications.

SECOND-ORDER LOW-PASS FILTER

Figure 48 depicts the AD712 configured as a second-order, Butterworth low-pass filter. With the values as shown, the corner frequency is 20 kHz; however, the wide bandwidth of the AD712 permits a corner frequency as high as several hundred kilohertz. Equations for component selection are as follows:

R1 = R2 = A user selected value (10 kΩ to 100 kΩ, typical)

$$C1 \text{ (in farads)} = \frac{1.414}{(2\pi)(f_{cutoff})(R1)}$$

$$C2 = \frac{0.707}{(2\pi)(f_{cutoff})(R1)}$$

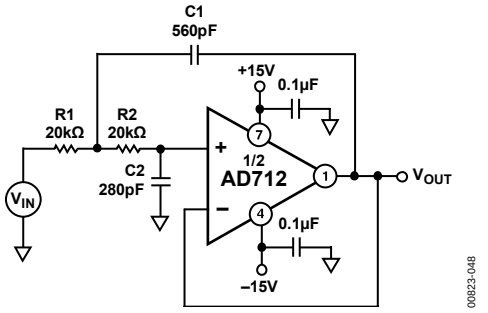


Figure 48. Second-Order Low-Pass Filter

An important property of filters is their out-of-band rejection. The simple 20 kHz low-pass filter shown in Figure 48, can be used to condition a signal contaminated with clock pulses or sampling glitches that have considerable energy content at high frequencies.

The low output impedance and high bandwidth of the AD712 minimize high frequency feedthrough as shown in Figure 49. The upper trace is that of another low cost BiFET op amp showing 17 dB more feedthrough at 5 MHz.

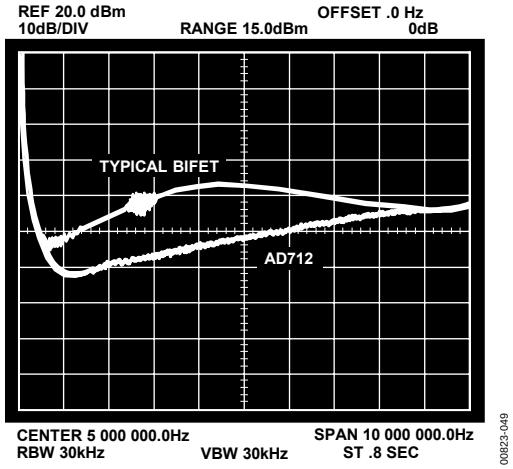


Figure 49. High Frequency Feedthrough

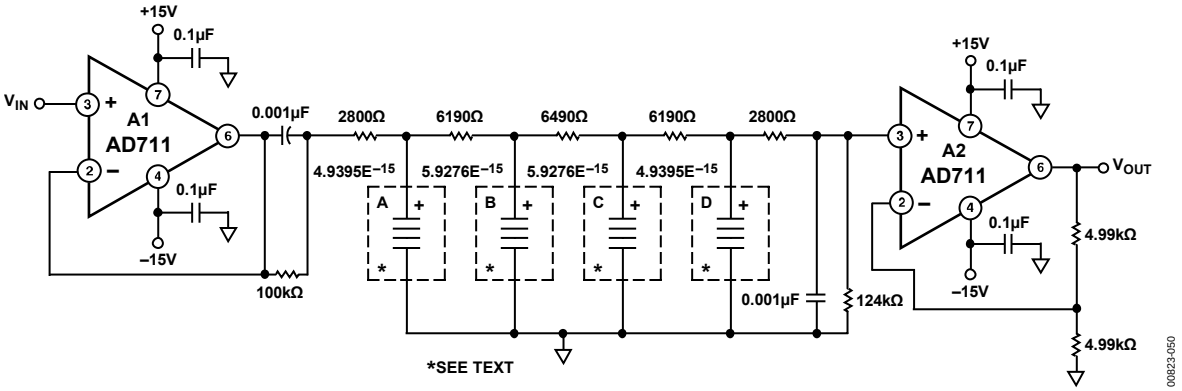


Figure 50. 9-Pole Chebychev Filter

9-POLE CHEBYCHEV FILTER

Figure 50 and Figure 51 show the AD712 and its dual counterpart, the AD711, as a 9-pole Chebychev filter using active frequency dependent negative resistors (FDNRs). With a cutoff frequency of 50 kHz and better than 90 dB rejection, it can be used as an antialiasing filter for a 12-bit data acquisition system with 100 kHz throughput.

As shown in Figure 50, the filter is comprised of four FDNRs (A, B, C, D) having values of 4.9395×10^{-15} and 5.9276×10^{-15} farad-seconds. Each FDNR active network provides a two-pole response for a total of eight poles. The ninth pole consists of a 0.001 µF capacitor and a 124 kΩ resistor at Pin 3 of Amplifier A2. Figure 51 depicts the circuits for each FDNR with the proper selection of R. To achieve optimal performance, the 0.001 µF capacitors must be selected for 1% or better matching and all resistors should have 1% or better tolerance.

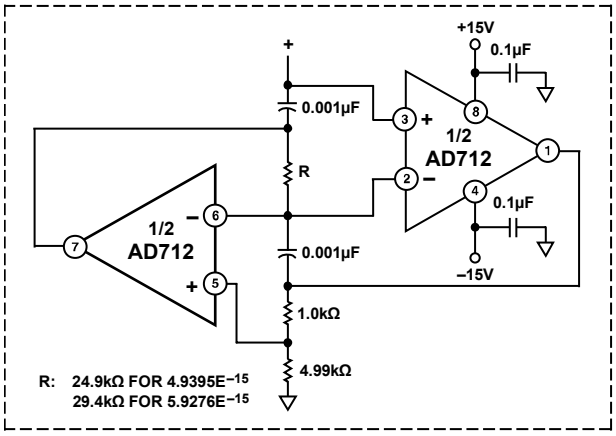


Figure 51. FDNR for 9-Pole Chebychev Filter

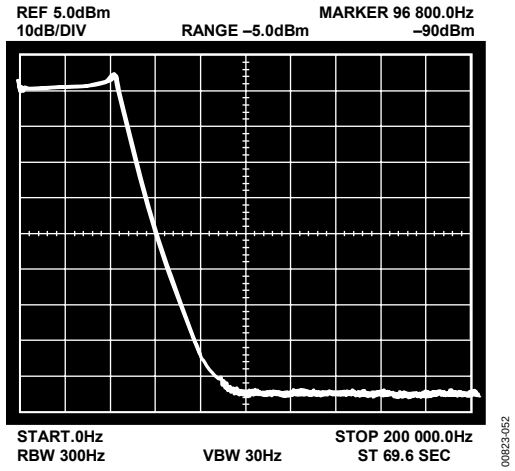
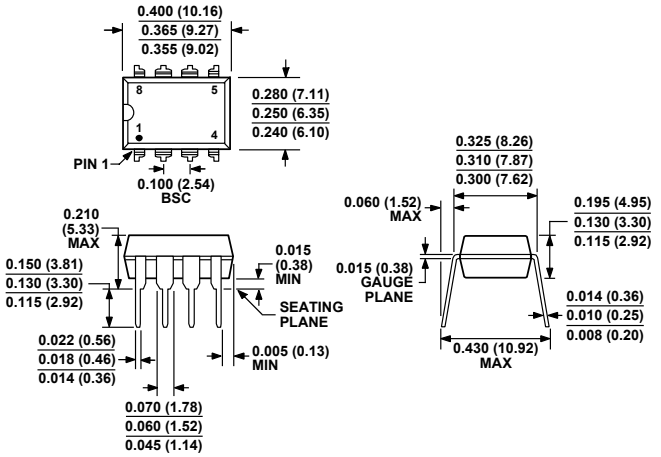


Figure 52. High Frequency Response for 9-Pole Chebychev Filter

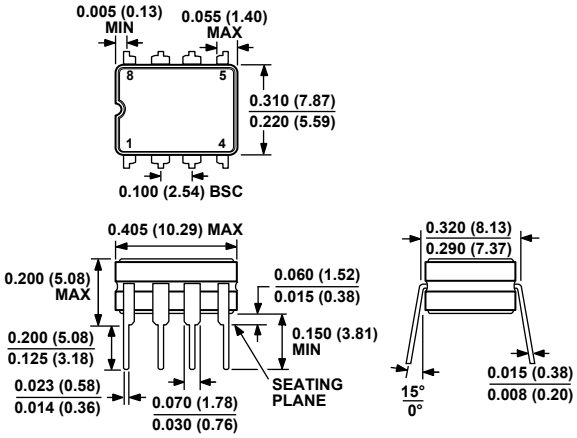
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-BA

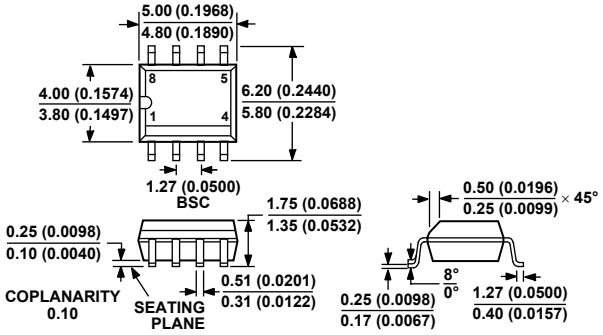
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 53. 8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 54. 8-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 55. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD712AQ	−40°C to +85°C	8-Lead CERDIP	Q-8
AD712JN	0°C to 70°C	8-Lead PDIP	N-8
AD712JNZ[1]	0°C to 70°C	8-Lead PDIP	N-8
AD712JR	0°C to 70°C	8-Lead SOIC_N	R-8
AD712JR-REEL	0°C to 70°C	8-Lead SOIC_N	R-8
AD712JR-REEL7	0°C to 70°C	8-Lead SOIC_N	R-8
AD712JRZ[1]	0°C to 70°C	8-Lead SOIC_N	R-8
AD712JRZ-REEL[1]	0°C to 70°C	8-Lead SOIC_N	R-8
AD712JRZ-REEL7[1]	0°C to 70°C	8-Lead SOIC_N	R-8
AD712KN	0°C to 70°C	8-Lead PDIP	N-8
AD712KNZ[1]	0°C to 70°C	8-Lead PDIP	N-8
AD712KR	0°C to 70°C	8-Lead SOIC_N	R-8
AD712KR-REEL	0°C to 70°C	8-Lead SOIC_N	R-8
AD712KR-REEL7	0°C to 70°C	8-Lead SOIC_N	R-8
AD712KRZ[1]	0°C to 70°C	8-Lead SOIC_N	R-8
AD712KRZ-REEL[1]	0°C to 70°C	8-Lead SOIC_N	R-8
AD712KRZ-REEL7[1]	0°C to 70°C	8-Lead SOIC_N	R-8
AD712SQ/883B	−55°C to +125°C	8-Lead CERDIP	Q-8

[1] Z = Pb-free part.

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