Final Datasheet

PE3282A

1.1 GHz/510 MHz Dual Fractional-N PLL IC for Frequency Synthesis

Applications

- Cellular handsets
- Cellular base stations
- Spread-spectrum radio
- Cordless phones
- Pagers

Features

- Modulo-32 fractional-N main counters
- On-board fractional spur compensation: no tuning required, stable over temperature
- Improved phase noise compared to integer-N architectures
- Low power—8.5 mA at 3 V
- Integrated 1.1 GHz ÷ 32/33 prescaler
- Integrated 510 MHz ÷ 16/17 prescaler

Description

The PE3282A is a dual fractional-N phase-locked loop integrated circuit designed for frequency synthesis and fabricated on Peregrine's patented UTSi® CMOS process. Each PLL includes a prescaler, phase detector, charge pump and on-board fractional spur compensation. The 32/33 RF prescaler (PLL1) operates up to 1.1 GHz and the 16/17 IF prescaler (PLL2) operates up to 510 MHz.

The PE3282A provides fractional-N division with power-of-two denominator values up to 32. This allows comparison frequencies up to 32 times the channel spacing, providing a lower phase-noise floor than integer PLLs.

Figure 1. PE3282A Block Diagram

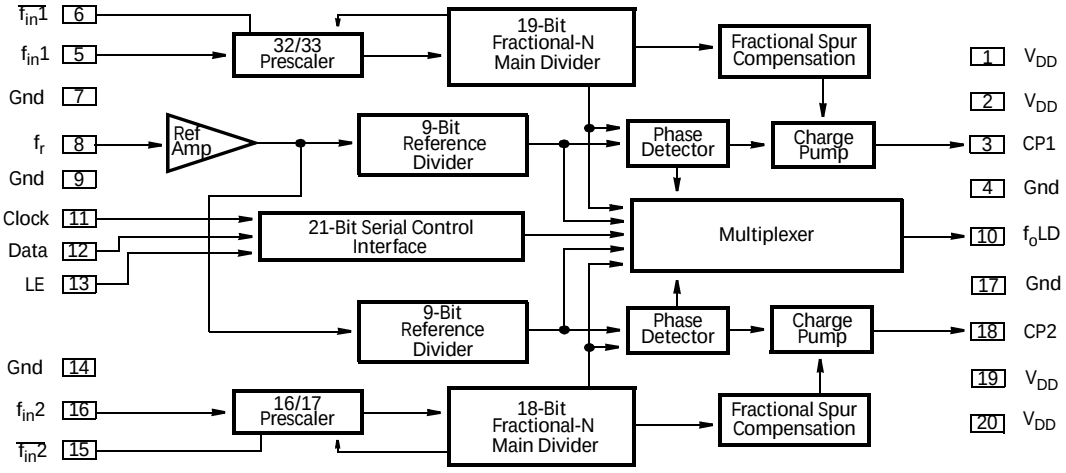

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Figure 2. Pin Configuration TSSOP (JEDEC MO-153-AC)

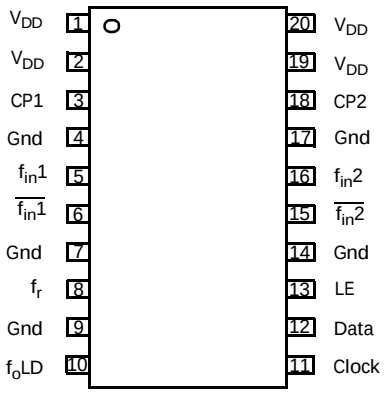


Table 1. PE3282A Pin Description

Pin No.	Pin Name	Type	Description
1	V_{DD}	(Note 1)	Power supply voltage input. Input may range from 2.7 V to 3.6 V. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.
2	V_{DD}	(Note 1)	Same as pin 1.
3	CP1	Output	Internal charge-pump output for PLL1. For connection to a loop filter for driving the input of an external VCO.
4	Gnd		Ground.
5	$f_{in}1$	Input	Prescaler input from the PLL1 (RF) VCO. 1.1 GHz max frequency.
6	$\overline{f_{in}1}$	Input	1.1 GHz prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with some loss of sensitivity.
7	Gnd		Ground.
8	f_r	Input	Reference frequency input.
9	Gnd		Ground.
10	f_oLD	Output	Multiplexed output of the PLL1 and PLL2 main counters or reference counters, Lock Detect signals, and data out of the shift register. CMOS output (see Table 10, f_oLD Programming Truth Table).
11	Clock	Input	CMOS clock input. Serial data for the various counters is clocked in on the rising edge into the 21-bit shift register. A pull-down resistor is recommended.
12	Data	Input	Binary serial data input. CMOS input data entered MSB first. The two LSBs are the control bits. A pull-down resistor is recommended.
13	LE	Input	Load Enable CMOS input. When LE is high, data word stored in the 21-bit serial shift register is loaded into one of the four appropriate latches (as assigned by the control bits). A pull-down resistor is recommended.
14	Gnd		Ground.
15	$\overline{f_{in}2}$	Input	510 MHz prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with some loss of sensitivity.
16	$f_{in}2$	Input	Prescaler input from the PLL2 (IF) VCO. 510 MHz max frequency.
17	Gnd		Ground.
18	CP2	Output	Internal charge-pump output for PLL2. For connection to a loop filter for driving the input of an external VCO.
19	V_{DD}	(Note 1)	Same as pin 1.
20	V_{DD}	(Note 1)	Same as pin 1.

Note 1: V_{DD} pins 1, 2, 19, and 20 are connected by diodes and must be supplied with the same voltage level.

Ratings and Operating Ranges

Table 2. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Unit
V_{DD}	Supply voltage	–0.3	4.0	V
V_I	Voltage on any input	–0.3	V_{DD} + 0.3	V
I_I	DC into any input or output	–10	+10	mA
T_{stg}	Storage temperature range	–65	150	°C

Table 3. Operating Ranges

Symbol	Parameter/Conditions	Min	Max	Unit
V_{DD}	Supply voltage	2.7	3.6	V
T_A	Operating ambient temperature range	–40	85	°C

Table 4. ESD Ratings

Symbol	Parameter/Conditions	Min	Max	Unit
V_{ESD}	ESD Voltage, Human body model (Note 1)	2000		V

Note 1: Periodically sampled, not 100% tested. Tested per MIL-STD-883, M3015 C2; 2KV.

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 4.

Latch-up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Table 5. DC Characteristics

V_{DD} = 3.0 V, –40° C < T_A < 85° C, unless specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Operational supply current; PLL1 (RF) enabled PLL2 (IF) enabled PLL1 and PLL2 enabled	V_{DD} = 2.7 to 3.6 V		 5.5 3.0 8.5		 mA mA mA
I_{stby}	Total standby current				25	mA
Digital inputs: Clock, Data, LE						
V_{IH}	High level input voltage	V_{DD} = 2.7 to 3.6 V	0.7 x V_{DD}			V
V_{IL}	Low level input voltage	V_{DD} = 2.7 to 3.6 V			0.3 x V_{DD}	V
I_{IH}	High level input current	V_{IH} = V_{DD} = 3.6 V	–1		+1	mA
I_{IL}	Low level input current	V_{IL} = 0, V_{DD} = 3.6 V	–1		+1	mA
Reference Divider input: f_r						
I_{IHR}	Input current	V_{IH} = V_{DD} = 3.6 V			+100	mA
I_{ILR}	Input current	V_{IL} = 0, V_{DD} = 3.6 V	–100			mA
Digital output: f_oLD						
V_{OLD}	Output voltage LOW	I_{out} = 1 mA			0.4	V
V_{OHD}	Output voltage HIGH	I_{out} = –1 mA	V_{DD} – 0.4			V
Charge Pump outputs: CP1, CP2						
$I_{CP - Source}$	Drive current	V_{CP} = V_{DD}/2, T_A = 25° C		–70		mA
$I_{CP - Sink}$				70		mA
I_{CPL}	Leakage current	0.5 < V_{CP} < V_{DD} - 0.5 V	–5		5	nA
$I_{CP - Source}$ vs. $I_{CP - Sink}$	Sink vs. source mismatch	V_{CP} = V_{DD}/2, T_A = 25° C			20	%
I_{CP} vs. T_A	Output current vs. temperature	V_{CP} = V_{DD}/2 + 85° C		–18		%
		V_{CP} = V_{DD}/2 - 40° C		+8		%
I_{CP} vs. V_{CP}	Output current magnitude variation vs. voltage	0.5 < V_{CP} < V_{DD} - 0.5 V, T_A = 25° C			20	%

Table 6. AC Characteristics

V_{DD} = 3.0 V, –40° C < T_A < 85° C, unless specified

Symbol	Parameter	Conditions	Min	Max	Unit
Serial Control Interface (see Figure 3)					
f_{Clock}	Serial data clock frequency			10	MHz
t_{ClockH}	Serial clock HIGH time		50		ns
t_{ClockL}	Serial clock LOW time		50		ns
t_{DSU}	Data set-up time to Clock rising edge		50		ns
t_{DHLD}	Data hold time after Clock rising edge		10		ns
t_{LEW}	LE pulse width		50		ns
t_{CLE}	Clock falling edge to LE rising edge		50		ns
t_{LEC}	LE falling edge to Clock rising edge		50		ns
$t_{Data\ Out}$	Data Out delay after Clock falling edge (f_oLD pin)	C_L = 50 pf		90	ns
Main Divider (Including Prescaler)					
$f_{in}1$	Operating frequency		100	1,100	MHz
$f_{in}2$	Operating frequency		45	510	MHz
$P_{fin}1$	Input level range	External AC coupling	–10	5	dBm
$P_{fin}2$	Input level range	External AC coupling	–10	5	dBm
f_c	Comparison frequency			10	MHz
Reference Divider					
f_r	Operating frequency			50	MHz
V_{fr}	Input sensitivity	External AC coupling (Note 1)	0.5		V_{P-P}

Note 1: CMOS logic levels may be used if DC coupled.

Functional Description

The Functional Block Diagram in Figure 2 shows a 21-bit serial control register, a multiplexed output, and PLL sections PLL1 and PLL2. Each PLL contains a fractional-N main counter chain, a reference counter, a phase detector, and an internal charge pump with on-chip fractional spur compensation. Each fractional-N main counter chain includes an internal dual modulus prescaler, supporting counters and a fractional accumulator.

Serial input data is clocked on the rising edge of Clock, MSB first. The last two bits are the address bits that determine the register address. Data is transferred into the counters as shown in Table 7, PE3282A Register Set. If the f_oLD pin is configured as data out, then the contents of shift register bit S_{20} are clocked on the falling edge of Clock onto the f_oLD pin. This feature allows the PE3282A and compatible devices to be connected in a daisy-chain configuration.

The PLL1 (RF) VCO frequency $f_{in}1$ is related to the reference frequency f_r by the following equation:

$$f_{in}1 = [(32 \times M_1) + A1 + (F_1/32)] \times (f_r/R_1)$$

(1) Note that A_1 must be less than M_1. Also, $f_{in}1$ must be greater than or equal to $1024 \times (f_r/R_1)$ to obtain contiguous channels.

The PLL2 (IF) VCO frequency $f_{in}2$ is related to the reference frequency f_r by the following equation:

$$f_{in}2 = [(16 \times M_2) + A2 + (F_2/32)] \times (f_r/R_2)$$

(2) Note that A_2 must be less than M_2. Also, $f_{in}2$ must be greater than or equal to $256 \times (f_r/R_2)$ to obtain contiguous channels.

F_1 sets PLL1 fractionality. If F_1 is an even number, PE3282A automatically reduces the fraction. For example, if $F_1 = 12$, then the fraction 12/32 is automatically reduced to 3/8. In this way, fractional denominators of 2, 4, 8, 16 and 32 are available. F_2 sets the fractionality for PLL2 in the same manner.

Figure 3. PE3282A Functional Block Diagram

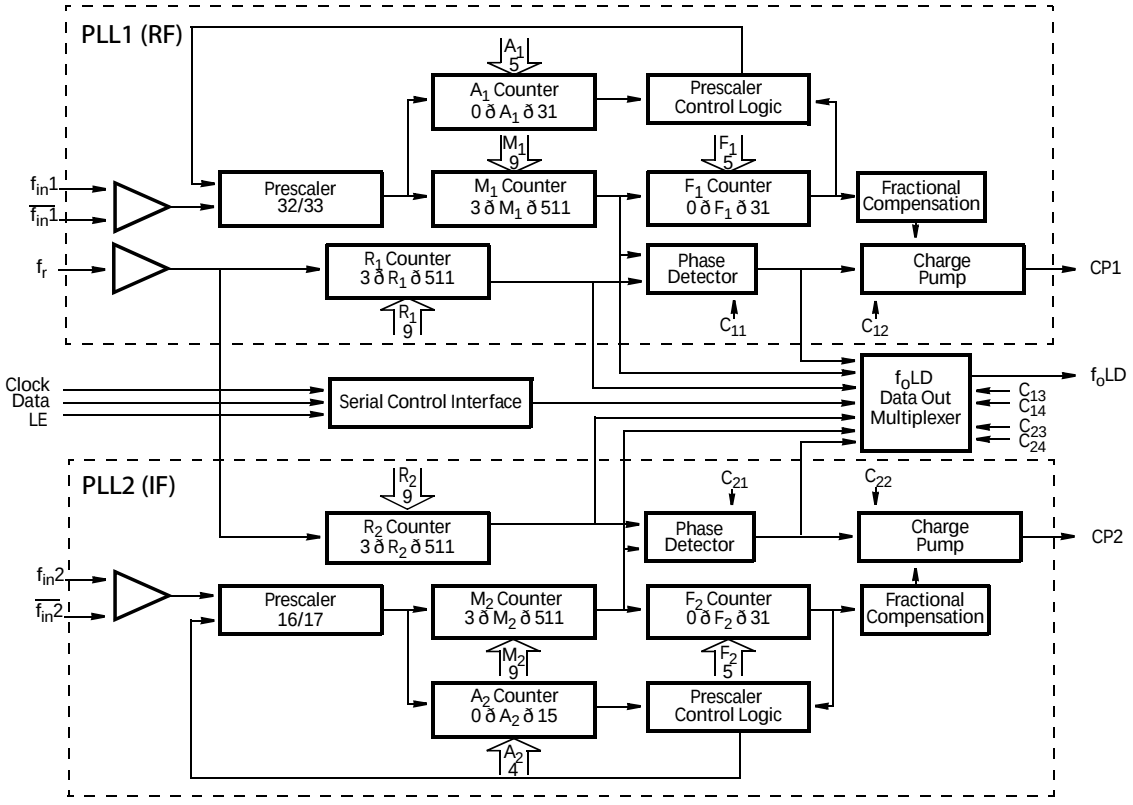
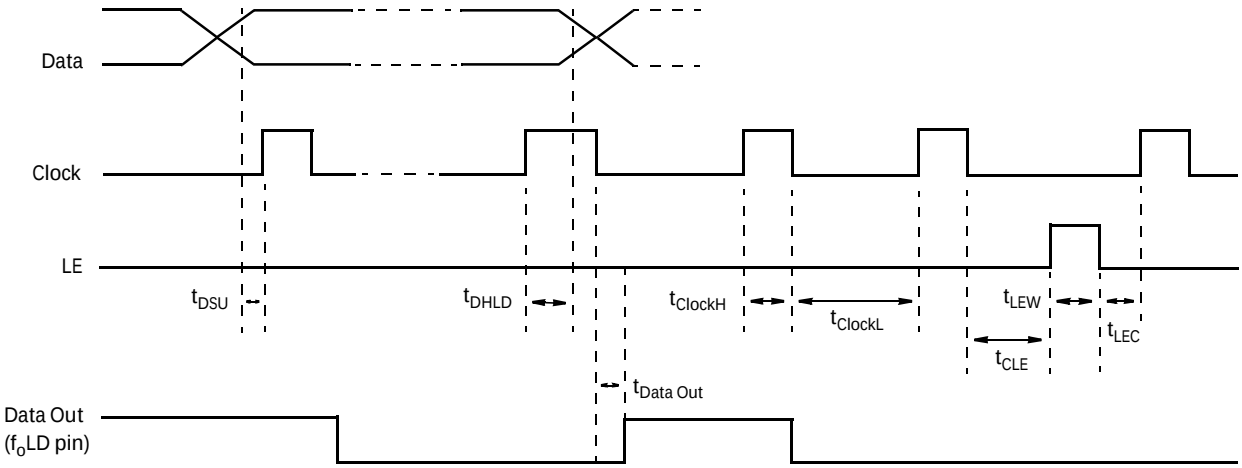


Table 7. PE3282A Register Set

S_{20}	S_{19}	S_{18}	S_{17}	S_{16}	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0
Reserved				Test	PLL2 Synthesizer control					PLL2 Reference counter R_2 divide ratio									Address	
				0	C_{24}	C_{23}	C_{22}	C_{21}	C_{20}	R_{28}	R_{27}	R_{26}	R_{25}	R_{24}	R_{23}	R_{22}	R_{21}	R_{20}	0	0
Res.	PLL2 Main counter M_2 divide ratio									PLL2 Swallow counter A_2 divide ratio				PLL2 Fractional counter F_2 numerator value					Address	
	M_{28}	M_{27}	M_{26}	M_{25}	M_{24}	M_{23}	M_{22}	M_{21}	M_{20}	A_{23}	A_{22}	A_{21}	A_{20}	F_{24}	F_{23}	F_{22}	F_{21}	F_{20}	0	1
Reserved					PLL1 Synthesizer control					PLL1 Reference counter R_1 divide ratio									Address	
					C_{14}	C_{13}	C_{12}	C_{11}	C_{10}	R_{18}	R_{17}	R_{16}	R_{15}	R_{14}	R_{13}	R_{12}	R_{11}	R_{10}	1	0
PLL1 Main counter M_1 divide ratio										PLL1 Swallow counter A_1 divide ratio				PLL1 Fractional counter F_1 numerator value					Address	
M_{18}	M_{17}	M_{16}	M_{15}	M_{14}	M_{13}	M_{12}	M_{11}	M_{10}		A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	F_{14}	F_{13}	F_{12}	F_{11}	F_{10}	1	1

MSB (first in) — (last in) LSB

Figure 4. Serial Control Interface Data Timing Diagram



Programmable Divide Values ($R_1, R_2, F_1, F_2, A_1, A_2, M_1, M_2$)

Data is clocked into the 21-bit shift register, MSB first. When LE is asserted HIGH, data is latched into the registers addressed by the last two bits shifted into the 21-bit shift register, according to Table 7. For example, to program the PLL1 (RF) swallow counter, A_1, the last two bits shifted into the register (S_0, S_1) would be (1, 1). The 5-bit A_1 counter would then be programmed according to Table 8. For normal operation, S_{16} of address (0, 0) (the Test bit) must be programmed to 0 even if PLL2 (IF) is not used.

Table 8. PE3282A Counter Programming Example

Divide Value	MSB				LSB	Address	
	S_{11}	S_{10}	S_9	S_8	S_7	S_1	S_0
	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	1	1
0	0	0	0	0	0	1	1
1	0	0	0	0	1	1	1
2	0	0	0	1	0	1	1
•	•	•	•	•	•	1	1
31	1	1	1	1	1	1	1

Programmable Modes

Several modes of operation can be programmed with bits C_{10} - C_{14} and C_{20} - C_{24}, including the phase detector polarity, charge pump high impedance, output of the f_oLD pin and power-down modes. The truth table for the programmable modes is shown in Table 9. The truth table for the f_oLD output is shown in Table 10.

Table 9. PE3282A Programmable Modes

S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_1	S_0
C_{24} see Table 10	C_{23} see Table 10	C_{22} 0 = PLL2 CP normal 1 = PLL2 CP High Z	C_{21} (Note 2) 0 = PLL2 Phase Detector inverted 1 = PLL2 Phase Detector normal	C_{20} (Note 1) 0 = PLL2 on 1 = PLL2 off	0	0
C_{14} see Table 10	C_{13} see Table 10	C_{12} 0 = PLL1 CP normal 1 = PLL1 CP High Z	C_{11} (Note 2) 0 = PLL1 Phase Detector inverted 1 = PLL1 Phase Detector normal	C_{10} (Note 1) 0 = PLL1 on 1 = PLL1 off	1	0

Note 1: The PLL1 power-down mode disables all of PLL1's components except the R_1 counter and the reference frequency input buffer, with CP1 (pin 3) and $f_{in}1$ (pin 5) becoming high impedance. The power down of PLL2 has similar results with CP2 (pin 18) and $f_{in}2$ (pin 16) becoming high impedance. Power down of both PLL1 and PLL2 further disables counters R_1 and R_2, the reference frequency input, and the f_oLD output, causing f_r (pin 8) and f_oLD (pin 10) to become high impedance. The Serial Control Interface remains active at all times.

Note 2: The C_{11} and C_{21} bits should be set according to the voltage versus frequency slope of the VCO as shown in Figure 4. This relationship presumes the use of a passive loop filter. If an inverting active loop filter is used the relationship is also inverted.

- When VCO1 (RF) slope is positive like (1), C_{11} should be set HIGH.
- When VCO1 (RF) slope is negative like (2), C_{11} should be set LOW.
- When VCO2 (IF) slope is positive like (1), C_{21} should be set HIGH.
- When VCO2 (IF) slope is negative like (2), C_{21} should be set LOW.

Figure 5. VCO Characteristics

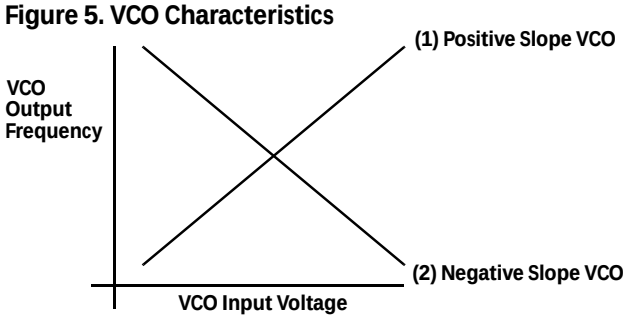


Table 10. f_oLD Programming Truth Table

X = don't care condition

f_oLD Output State	C_{14} (PLL1 f_o)	C_{13} (PLL1 LD)	C_{24} (PLL2 f_o)	C_{23} (PLL2 LD)
Disabled (Note 1)	0	0	0	0
PLL1 Lock detect (Note 2) (LD1)	0	1	0	0
PLL2 Lock detect (Note 2) (LD2)	0	0	0	1
PLL1/PLL2 Lock detect (Note 2)	0	1	0	1
PLL1 Reference divider output (f_c1)	1	X	0	0
PLL2 Reference divider output (f_c2)	0	X	1	0
PLL1 Programmable divider output (f_p1)	1	X	0	1
PLL2 Programmable divider output (f_p2)	0	X	1	1
Serial data out	1	0	1	0
Reserved	1	0	1	1
Reserved	1	1	1	0
Counter reset (Note 3)	1	1	1	1

Note 1: When the f_oLD is disabled the output is a CMOS LOW.

Note 2: Lock detect indicates when the VCO frequency is in "lock". When PLL1 is in lock and PLL1 lock detect is selected, the f_oLD pin will be HIGH, with narrow pulses LOW. When PLL2 is in lock and PLL2 lock detect is selected, the f_oLD pin will be HIGH, with narrow pulses LOW. When PLL1/PLL2 lock detect is selected the f_oLD pin will be HIGH with narrow pulses LOW, only when both PLL1 and PLL2 are in lock.

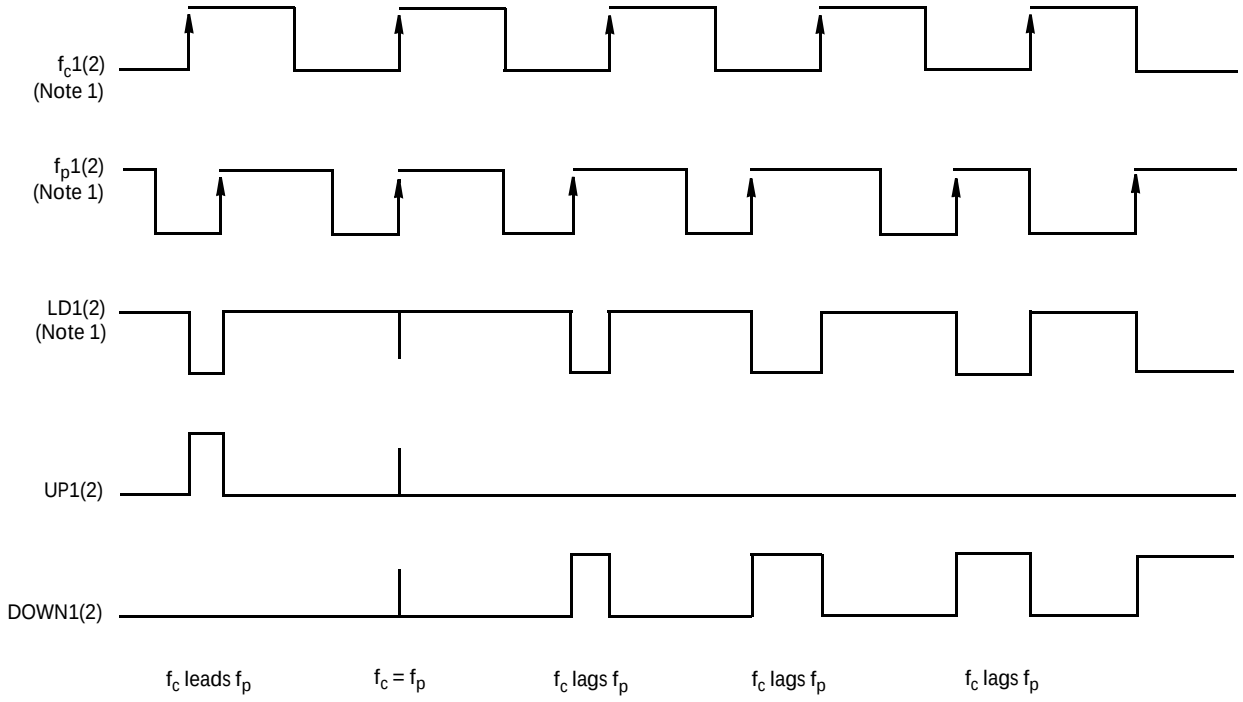
Note 3: The counter reset state when activated resets all counters. Upon removal of the reset, counters M, A, and F resume counting in close alignment with the R counter (the maximum error is one prescaler cycle). The reset bits can be activated to allow smooth acquisition upon powering up.

Phase Comparator Characteristics

PLL1 has the timing relationships shown below for f_c1, f_p1, LD1, UP1, and DOWN1. When C_{11} = HIGH, UP1 directs the internal PLL1 charge pump to source current and DOWN1 directs the PLL1 internal charge pump to sink current. If C_{11} = LOW, UP1 and DOWN1 are interchanged.

PLL2 has the timing relationships shown below for f_c2, f_p2, LD2, UP2, and DOWN2. When C_{21} = HIGH, UP2 directs the internal PLL2 charge pump to source current and DOWN2 directs the PLL2 internal charge pump to sink current. If C_{21} = LOW, UP2 and DOWN2 are interchanged.

Figure 6. Phase Comparator Timing Diagram



Note 1: $f_c1(2)$, $f_p1(2)$, and LD1(2) are accessible via the f_oLD pin per programming in Table 10.

Figure 7. Typical Application Example

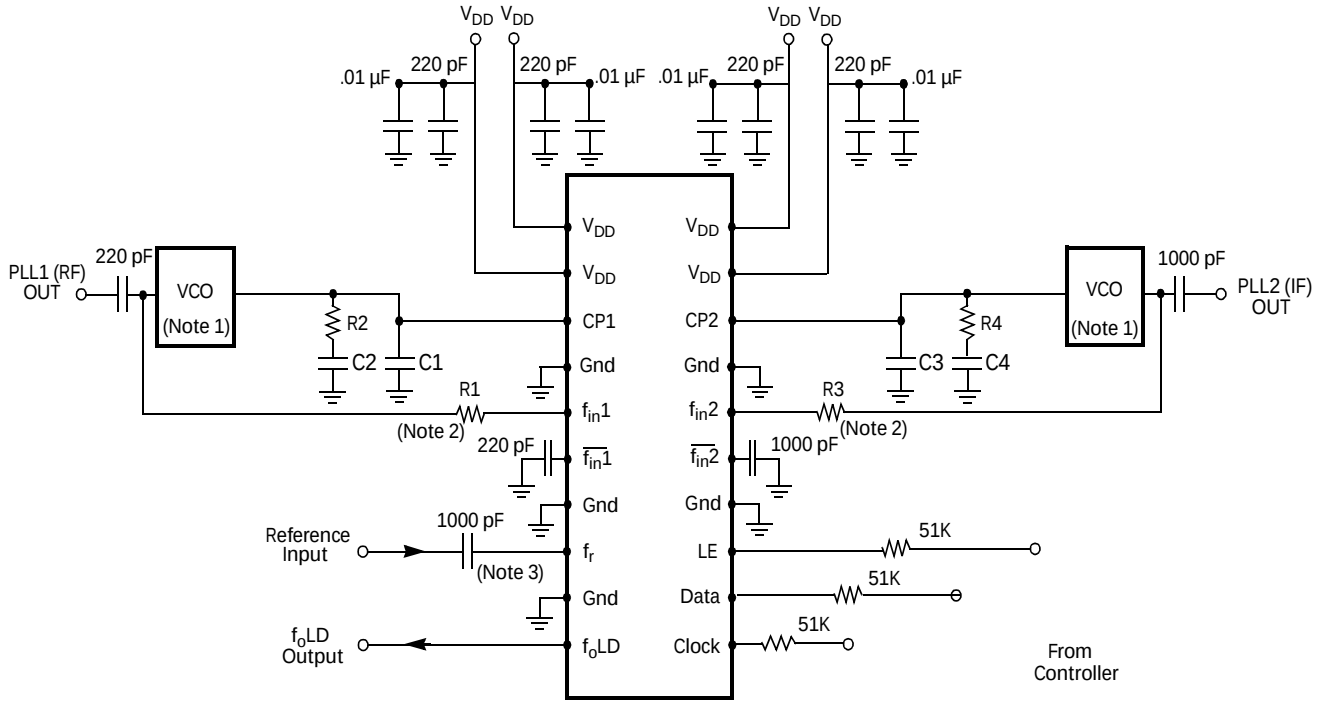


Table 11. PLL1 (RF)

Operating Conditions	Loop Filter Values (Note 4)
f_{out} = 948.075 MHz	R2 = 30 k ohm
f_{ref} = 14.4 MHz	C2 =.0043 µF
f_{comp} = 800 kHz	C1 = 900 pF
Fractionality = 32	
Step Size = 25 kHz	
ω_n = 3.0 kHz	
Phase Margin = 45°	
N = 1,185 + 3/32 (M = 37, A = 1, F = 3)	
K_{VCO} = 13 MHz/V	
Kpd = 70 µA/2 ¼ rad	

Table 12. PLL2 (IF)

Operating Conditions	Loop Filter Values (Note 4)
f_{out} = 130.45 MHz	R4 = 7.1 k ohm
f_{ref} = 14.4 MHZ	C4 =.027 µF
f_{comp} = 800 kHz	C3 =.0056 µF
Fractionality = 16	
Step Size = 50 kHz	
ω_n = 2.0 kHz	
Phase Margin = 45°	
N = 163 + 1/16 (M = 10, A = 3, F = 2)	
K_{VCO} = 5 MHz/V	
Kpd = 70 µA/2 ¼ rad	

Note 1: VCO output assumed to be AC coupled.

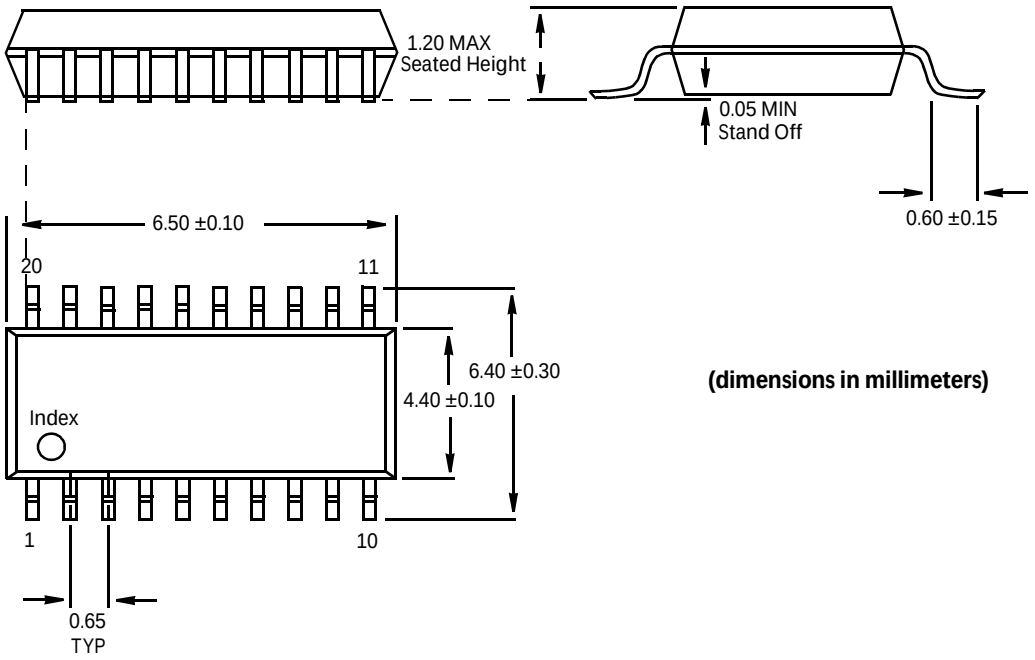
Note 2: R1 and R3 are chosen to set the input drive to pins $f_{in}1$ and $f_{in}2$. R1 and R3 also allow a larger proportion of the VCO output to be delivered to the load and attenuate reflected energy from the PLL inputs.

Note 3: The f_r input may be DC coupled if driven by an appropriate CMOS level signal. A 50 ohm terminating resistor can be used when driving the f_r pin from an external 50 ohm signal source.

Note 4: The unity gain bandwidth is recommended to be less than or equal to 10 percent of the step size.

Mechanical Information

Figure 8. Package Dimensions: TSSOP (JEDEC MO-153-AC)



Ordering Information

Peregrine Semiconductor Corp. standard products are often available in several packages and performance ranges. Part numbers for ordering the various configurations are defined as follows:

Table 13.Valid ordering number combinations for PE3282A:

Order Code	Part Marking	Package	Temperature	Shipping Method
3282-11	PE3282A	20 lead TSSOP	–40 to 85° C	Tube 74 Units/Tube
3282-12	PE3282A	20 lead TSSOP	–40 to 85° C	Tape and Reel 2500 Units/Reel
3282-00	PE3282A-EK	Evaluation Kit	–40 to 85° C	1/Box

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Data Sheet Identification

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