

PE42721

UltraCMOS® SPDT RF Switch
5–2200 MHz

Product Description

The PE42721 is a HaRP™ technology-enhanced absorptive 75Ω SPDT RF switch developed on the UltraCMOS® process technology.

PE42721 is a highly linear device delivering high isolation and very low insertion loss performance. It is designed for broadband applications such as TV tuner modules, CATV signal switching and distribution, DTV, multi-tuner digital video recorders (DVRs) and set-top boxes.

PE42721 supports +1.8V control logic and offers high ESD protection. PE42721 is pin compatible to PE42750. In addition, no blocking capacitors are required if DC voltage is not present on the RF ports.

Peregrine's HaRP™ technology enhancement is an innovative feature of the UltraCMOS® process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Features

- HaRP™ technology enhanced
 - High linearity
 - CTB of -99 dBc
 - CSO better than -105 dBc
- Supports +1.8V control logic
- Low insertion loss
 - 0.40 dB @ 220 MHz
 - 0.50 dB @ 870 MHz
 - 0.65 dB @ 2200 MHz
- High isolation
 - 85 dB @ 220 MHz
 - 68 dB @ 870 MHz
 - 53 dB @ 2200 MHz
- ESD performance
 - 3kV HBM on RF pins to GND
 - 2kV HBM on all other pins
 - 1kV CDM on all pins

Figure 1. Functional Diagram

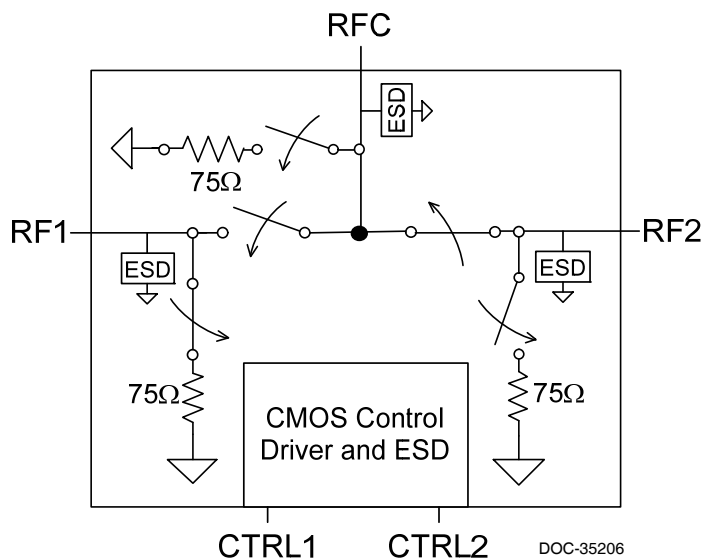


Figure 2. Package Type

12-lead 3x3 mm QFN

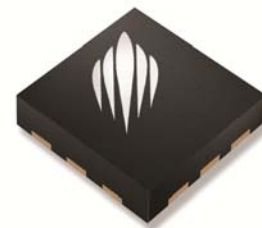


Table 1. Electrical Specifications Temp = 25°C, V_{DD} = 3.3V (Z_S = Z_L = 75Ω)

Parameter	Path	Condition	Min	Typ	Max	Unit
Operational frequency			5		2200	MHz
Insertion loss	RFC–RFX	5–220 MHz		0.40	0.55	dB
		221–870 MHz		0.50	0.70	dB
		871–2200 MHz		0.65	0.85	dB
Isolation	RFX–RFX	5–220 MHz	81	85		dB
		221–870 MHz	65	68		dB
		871–2200 MHz	52	53		dB
Isolation	RFC–RFX	5–220 MHz	68	70		dB
		221–870 MHz	57	59		dB
		871–2200 MHz	53	55		dB
Return loss	All ports	870 MHz		18		dB
		2200 MHz		15		dB
Input 0.1 dB compression ^{1,2}	RFC–RFX	45–1000 MHz		27		dBm
IIP2 ³	RFX	45–2200 MHz		110		dBm
IIP3	RFX	5–2200 MHz		60		dBm
CTB		159 channels; 42 dBmV per channel output power		-99		dBc
CSO		159 channels; 42 dBmV per channel output power		< -105		dBc
Cross modulation distortion		159 channels; 42 dBmV per channel output power		-89.5		dBc
Video feedthrough		DC measurement		4		mV _{PP}
Switching time		50% CTRL to 90% or 10% RF		1	1.5	μs

Notes: 1. The input 0.1 dB compression point (P0.1dB) is a linearity figure of merit. Refer to *Table 3* for the RF input power P_{IN}
2. P0.1dB = 25 dBm @ 2.2 GHz
3. IIP2 = 83 dBm @ 5 MHz

Figure 3. Pin Configuration (Top View)

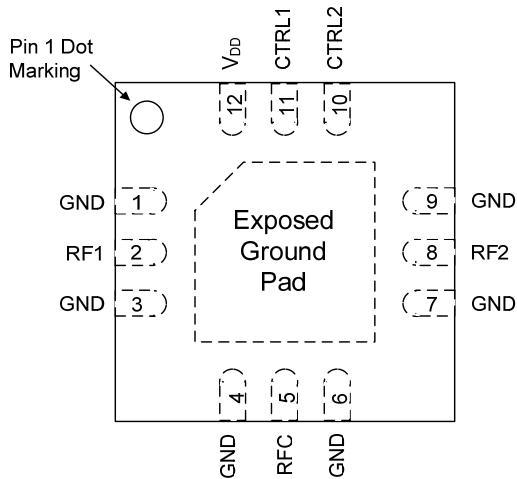


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	GND	RF Ground
2	RF1 ¹	RF Port 1
3	GND	RF Ground
4	GND	RF Ground
5	RFC ¹	RF Common
6	GND	RF Ground
7	GND	RF Ground
8	RF2 ¹	RF Port 2
9	GND	RF Ground
10	CTRL2	Digital control logic input 2
11	CTRL1	Digital control logic input 1
12	V_{DD}	Supply Voltage
Pad	GND	Exposed pad: Ground for proper operation

Note 1: RF pins 2, 5, and 8 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper operation if the 0V DC requirement is met

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 3. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.3	3.3	5.5	V
Supply current	I_{DD}		110	200	μA
Digital input high (CTRL1, CTRL2)	V_{IH}	1.17		3.6	V
Digital input low (CTRL1, CTRL2)	V_{IL}	-0.3		0.6	V
Digital input current	I_{CTRL}			1	μA
RF input power (RFC–RFX) ¹	P_{IN}			18 22	dBm dBm
5 ≤ 45 MHz					
45 ≤ 2200 MHz					
RF input power into terminated ports (RFX) ¹	$P_{IN,TERM}$			16 16	dBm dBm
5 ≤ 45 MHz					
45 ≤ 2200 MHz					
Operating temperature range	T_{OP}	-40	+25	+85	°C

Note 1: 100% duty cycle, all bands, 75 Ω

Table 4. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage	V_{CTRL}	-0.3	3.6	V
RF input power (RFC–RFX) ¹	P_{IN}		18 22	dBm dBm
5 ≤ 45 MHz				
45 ≤ 2200 MHz				
RF input power into terminated ports (RFX) ¹	$P_{IN,TERM}$		16 16	dBm dBm
5 ≤ 45 MHz				
45 ≤ 2200 MHz				
Storage temperature range	T_{ST}	-65	+150	°C
ESD voltage HBM ²	$V_{ESD,HBM}$		3000 2000	V V
RF pins to GND				
All other pins				
ESD voltage MM ³ , all pins	$V_{ESD,MM}$		100	V
ESD Voltage CDM ⁴ , all pins	$V_{ESD,CDM}$		1000	V

Notes: 1. 100% duty cycle, all bands, 75 Ω
2. Human Body Model (MIL-STD-883 Method 3015)
3. Machine Model (JEDEC JESD22-A115)
4. Charged Device Model (JEDEC JESD22-C101)

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Switching Frequency

The PE42721 has a maximum 25 kHz switching rate.

Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value. Switching time is provided in *Table 1*.

Table 5. Truth Table¹

C1	C2	RFC – RF1	RFC – RF2
Low	Low	ON	OFF
Low	High	OFF	ON
High	Low	OFF	ON
High	High	ON	OFF

Note 1: A versatile logic table has been established to allow either C1 or C2 to act as a single pin control and in either polarity

Spurious Performance

The typical spurious performance of the PE42721 is –124 dBm.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42721 in the 12-lead 3x3 mm QFN package is MSL1.

Typical Performance Data @ 25°C and $V_{DD} = 3.3V$ unless otherwise specified

Figure 4. Insertion Loss (RFC-RFX)

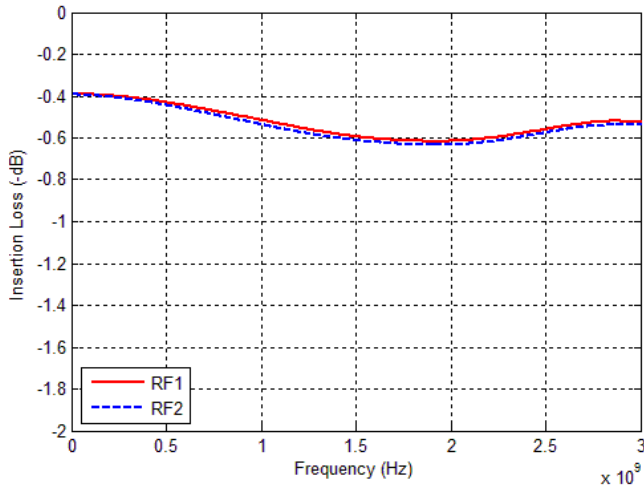


Figure 5. Insertion Loss vs. Temp (RFC-RFX)

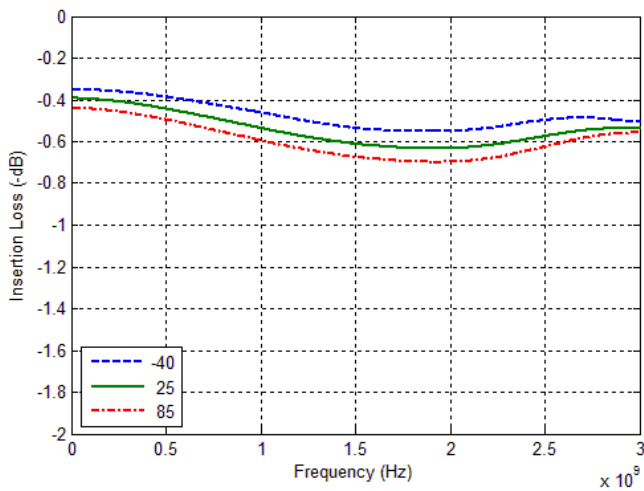
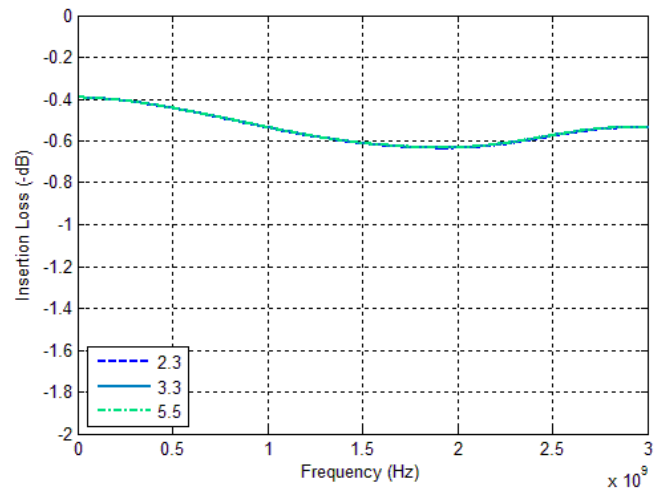


Figure 6. Insertion Loss vs. V_{DD} (RFC-RFX)



Typical Performance Data @ 25°C and $V_{DD} = 3.3V$ unless otherwise specified

Figure 7. RFC Port Return Loss vs. Temp (RF1 Active)

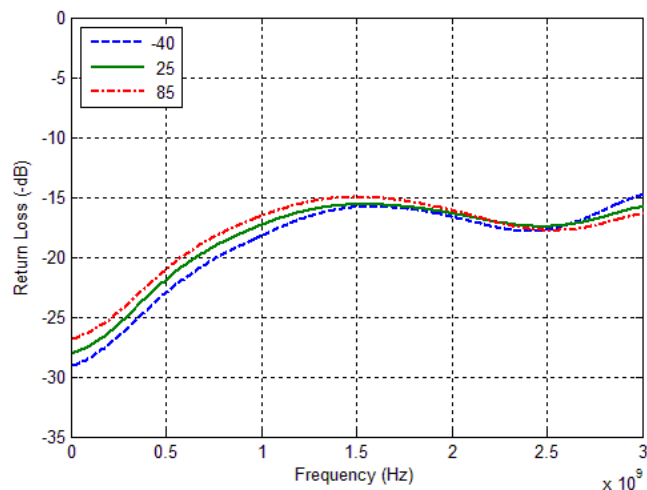


Figure 8. RFC Port Return Loss vs. V_{DD} (RF1 Active)

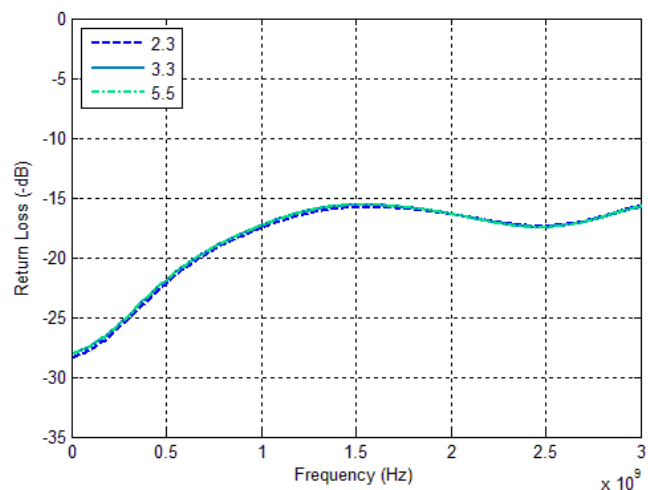


Figure 9. RFC Port Return Loss vs. Temp (RF2 Active)

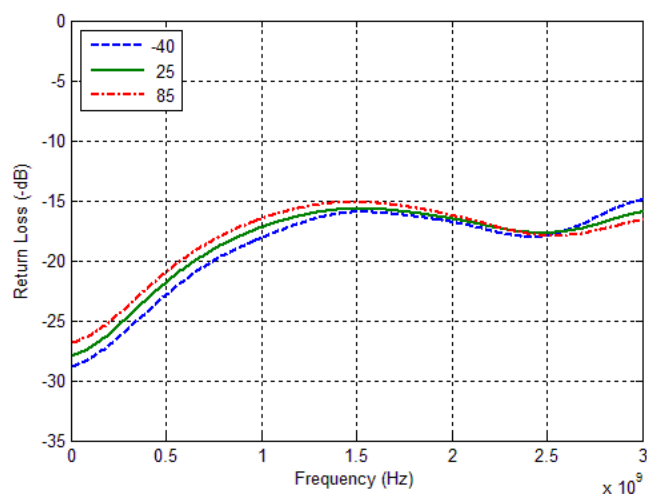
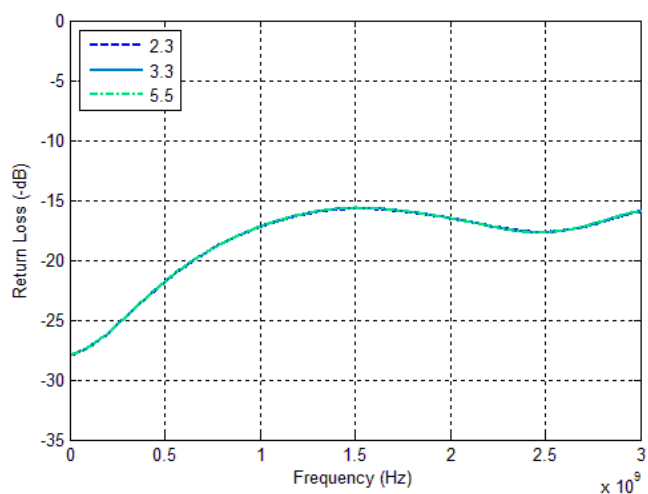


Figure 10. RFC Port Return Loss vs. V_{DD} (RF2 Active)



Typical Performance Data @ 25°C and $V_{DD} = 3.3V$ unless otherwise specified

Figure 11. Active Port Return Loss vs. Temp (RF1 Active)

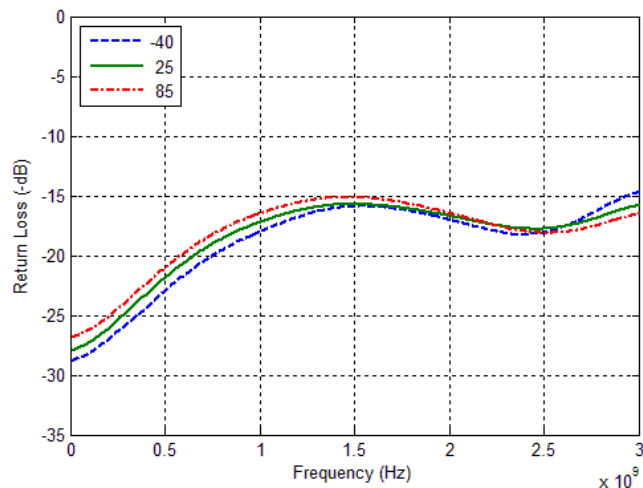


Figure 12. Active Port Return Loss vs. V_{DD} (RF1 Active)

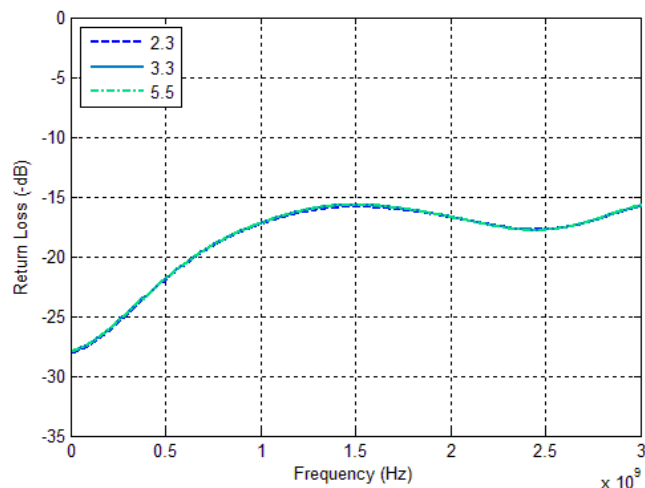


Figure 13. Active Port Return Loss vs. Temp (RF2 Active)

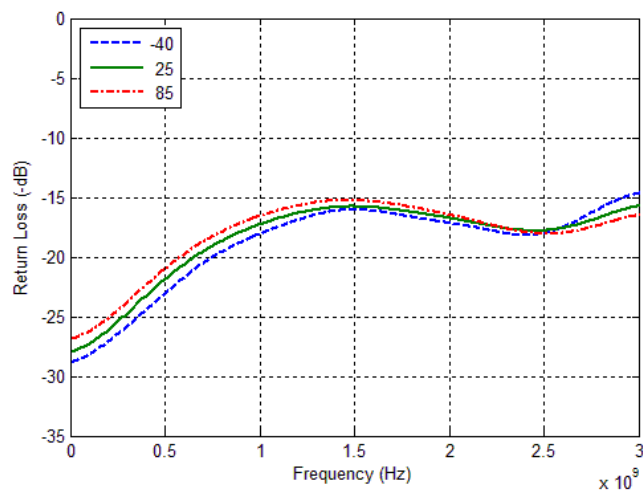
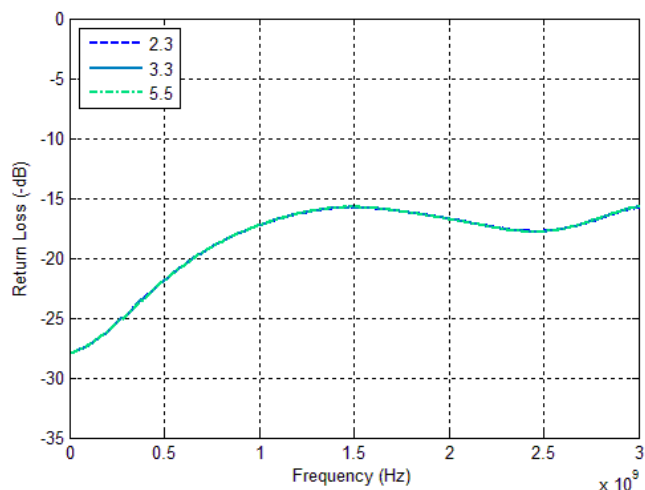


Figure 14. Active Port Return Loss vs. V_{DD} (RF2 Active)



Typical Performance Data @ 25°C and $V_{DD} = 3.3V$ unless otherwise specified

Figure 15. Isolation vs. Temp (RFX-RFX)

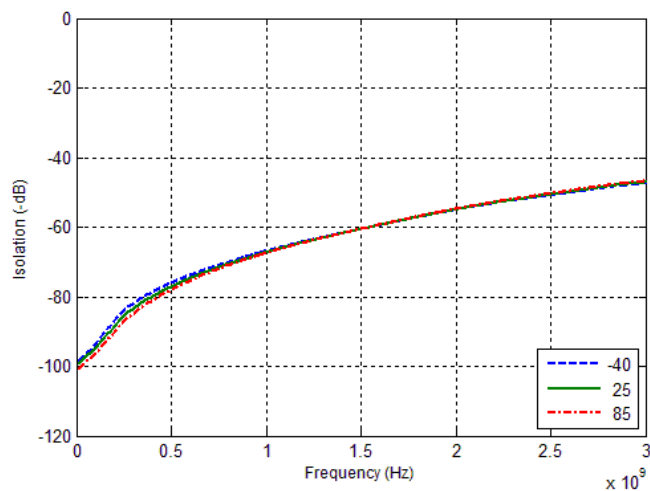


Figure 16. Isolation vs. V_{DD} (RFX-RFX)

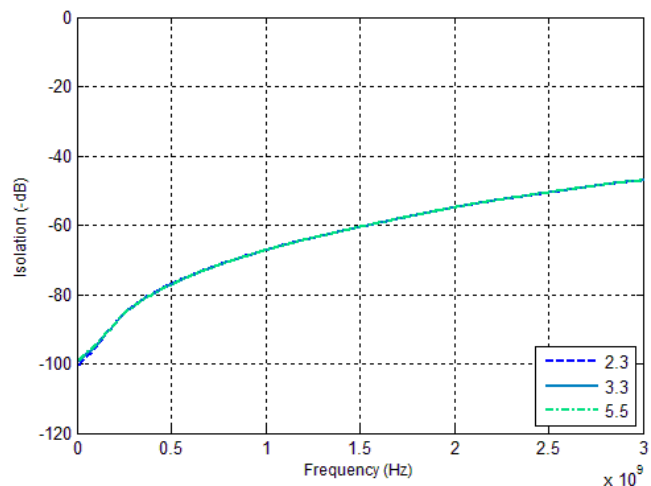


Figure 17. Isolation vs. Temp (RFC-RFX)

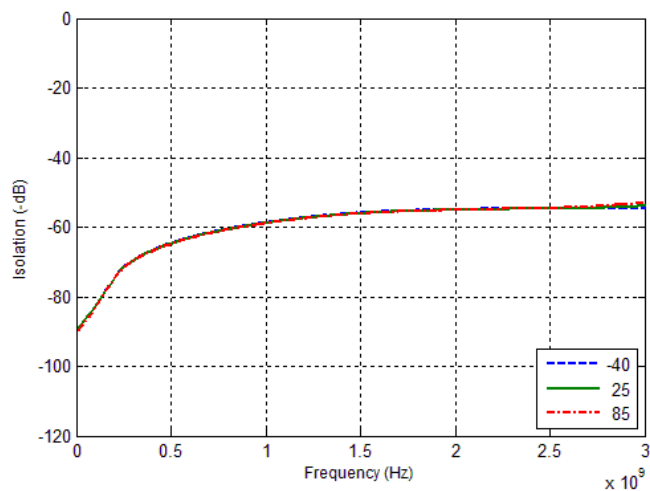
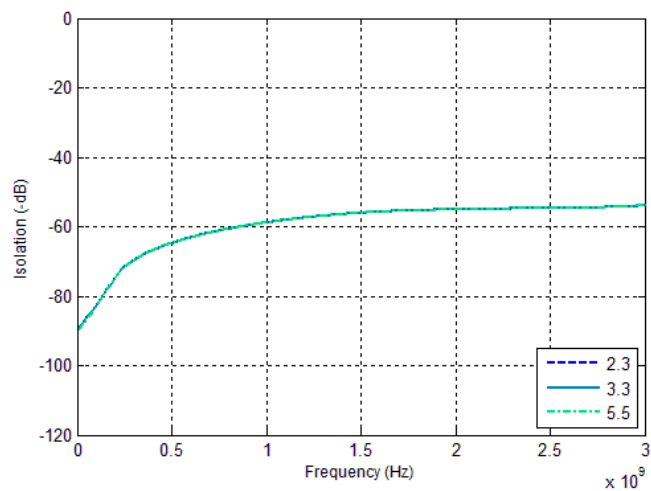


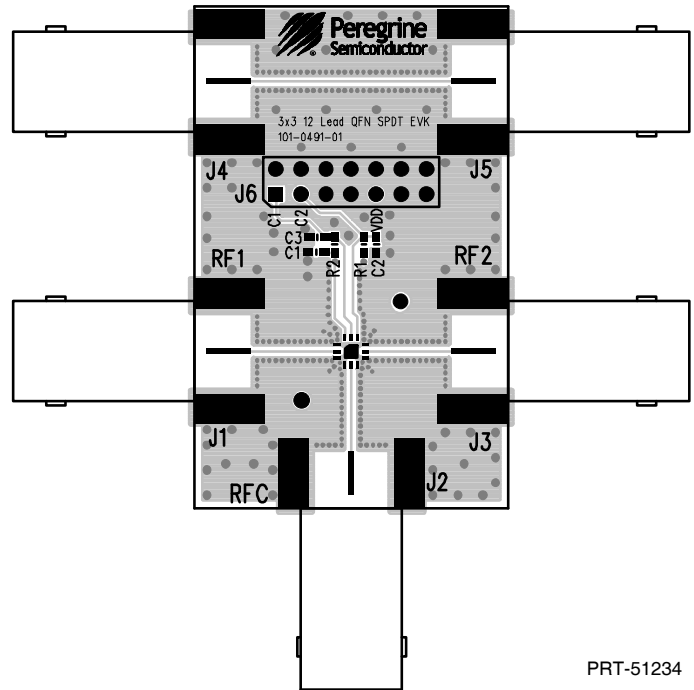
Figure 18. Isolation vs. V_{DD} (RFC-RFX)



Evaluation Board

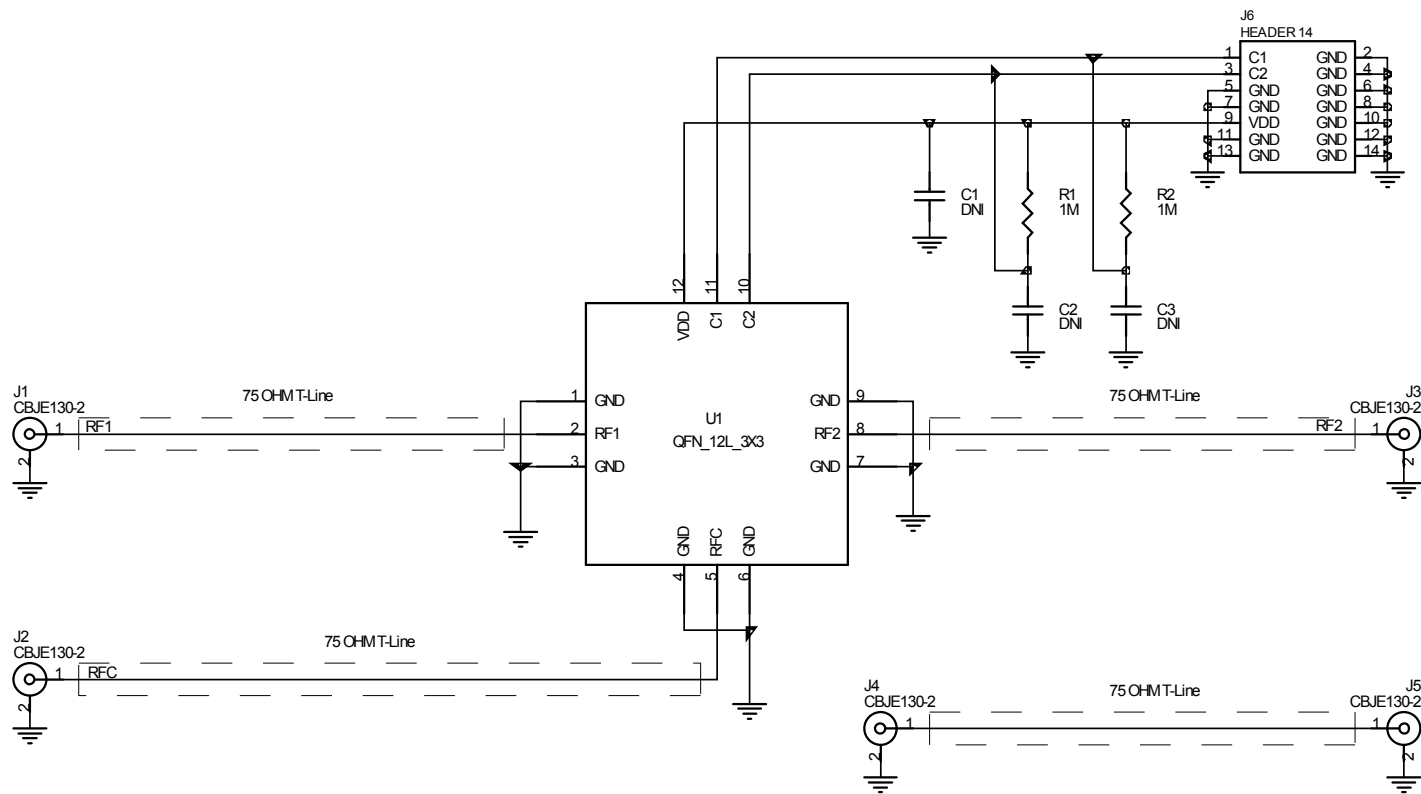
The SPDT switch evaluation board was designed to ease customer evaluation of Peregrine's PE42721. The RF common port is connected through a 75Ω transmission line via the F-Type connector, J2. RF1 and RF2 ports are connected through 75Ω transmission lines via F-Type connectors J1 and J3, respectively. A 75Ω through transmission line is available via F-Type connectors J4 and J5, which can be used to de-embed the loss of the PCB. J6 provides DC and digital inputs to the device.

Figure 19. Evaluation Board Layout



PRT-51234

Figure 20. Evaluation Board Schematic



DOC-02571

NOTES:

1. USE 101-0491-01

2. CAUTION:
CONTAINS PARTS AND ASSEMBLIES SUSCEPTIBLE
TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)

3. ALL TRANSMISSION LINES ARE:
12MIL WIDTH, 12MIL GAPS, 28MIL CORE DIELECTRIC
4.3 Er AND 2.1MIL Cu THICKNESS.

Technical drawing of a square pin with dimensions and surface finish requirements.

TOP VIEW

- Overall width: 3.00
- Overall height: 3.00
- Surface finish: 0.10 C (2X)
- Pin #1 Corner

BOTTOM VIEW

- Overall width: 3.40
- Overall height: 3.40
- Surface finish: 0.65 (x8)
- Chamfer: $0.30 \times 45^\circ$
- Dimensions: 1.50 ± 0.05 , $0.40 \pm 0.05 \text{ (x12)}$, 1.30 Ref. , $0.30 \pm 0.05 \text{ (x12)}$

RECOMMENDED LAND PATTERN

- Overall width: 3.40
- Overall height: 3.40
- Surface finish: 0.65 (x8)
- Dimensions: 0.35 (x12) , 0.60 (x12) , 1.55

SIDE VIEW

- Overall width: 3.00
- Overall height: 3.00
- Surface finish: 0.10 C
- Seating Plane
- Dimensions: 0.203 Ref. , 0.80 MAX , 0.05

ALL FEATURES

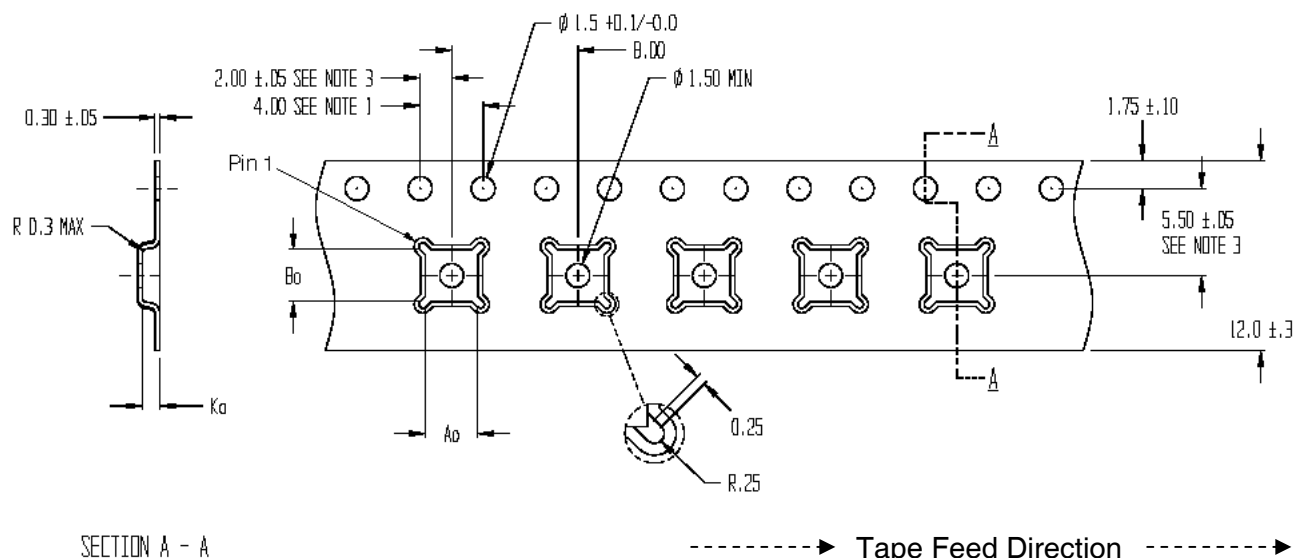
- Surface finish: 0.10 (M) C A B
- Surface finish: 0.05 (M) C

DOC-0011

42721
YYWW
ZZZZZ

● = Pin 1 designator
AAAAA = Five digit part number
YYWW = Date Code, last two digits of the year and work week
ZZZZZ = Five digits of the lot number

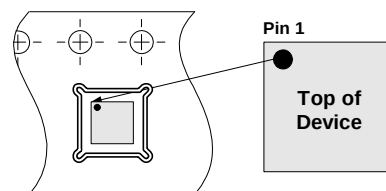
Figure 23. Tape and Reel Drawing



NOTES:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

$$\begin{aligned} A_o &= 3.30 \pm 0.1 \text{ mm} \\ B_o &= 3.30 \pm 0.1 \text{ mm} \\ K_o &= 1.10 \pm 0.1 \text{ mm} \end{aligned}$$



Device Orientation in Tape

Table 6. Ordering Information

Order Code	Description	Package	Shipping Method
PE42721MLBA-Z	PE42721 SPDT RF switch	Green 12-lead 3x3 mm QFN	3000 units/T&R
EK42721-02	PE42721 Evaluation kit	Evaluation kit	1/Box

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice. **Preliminary Specification:** The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. **Product Specification:** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form). The information in this datasheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this datasheet are implied or granted to any third party. Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications. The Peregrine name, logo, UltraCMOS and UTSi are registered trademarks and HaRP, MultiSwitch and DuNE are trademarks of Peregrine Semiconductor Corp. Peregrine products are protected under one or more of the following U.S. Patents: <http://patents.psemi.com>.