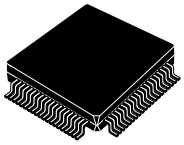
TDA7550/R TDA7551 TDA7552 TDA7553

DIGITAL SIGNAL PROCESSING IC FOR SPEECH AND AUDIO APPLICATIONS

PRODUCT PREVIEW

- 24-BIT, FIXED POINT, 50 MIPS DSP CORE
- LARGE ON-BOARD PROGRAM ROM AND DATA RAM (UP TO 16Kw ROM/RAM AND 16Kw RAM)
- INTEGRATED STEREO A/D AND D/A, 16-BIT SIGMA-DELTA
- PROGRAMMABLE CODEC SAMPLE RATE FROM 4 TO 48 kHz
- ON-BOARD PLL FOR CORE CLOCK AND CONVERTERS
- MANAGEMENT OF EXTERNAL FLASH/SRAM/DRAM MEMORY BANK
- I^2C OR SPI SERIAL INTERFACE FOR EXTERNAL CONTROL
- 80-PIN TQFP, 0.65 mm PITCH
- AUTOMOTIVE GRADE (FROM -40° C to +85°C)

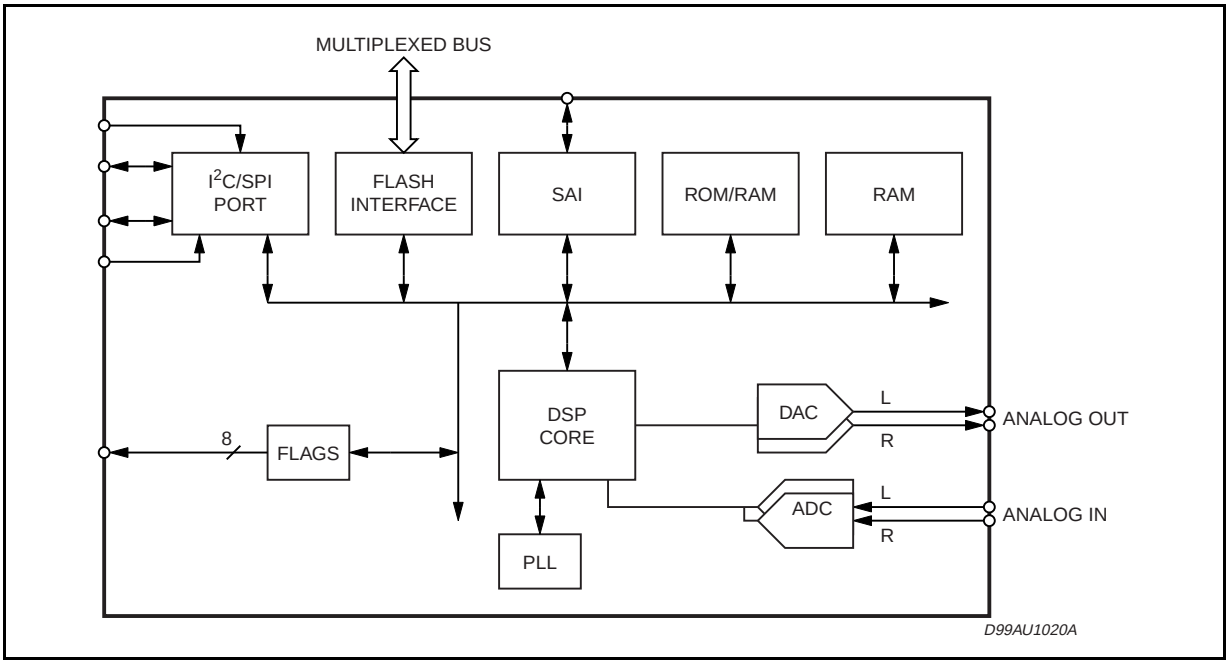


TQFP80

DESCRIPTION

The TDA755X family is a high performances, fully programmable 24-bit, 50 MIPS Digital Signal Processor (DSP), designed to support several speech and audio applications, as Automatic Speech Recognition, Speech Synthesis, Speaker Verification, Echo and Noise Cancellation. Software for these applications is licenced by Lernout & Hauspie and NCTI.
It offers an effective solution for this kind of applications because of the A/D and D/A converters and the big amount of memory integrated on chip.

BLOCK DIAGRAM



This is preliminary information on a new product now in development. Details are subject to change without notice.

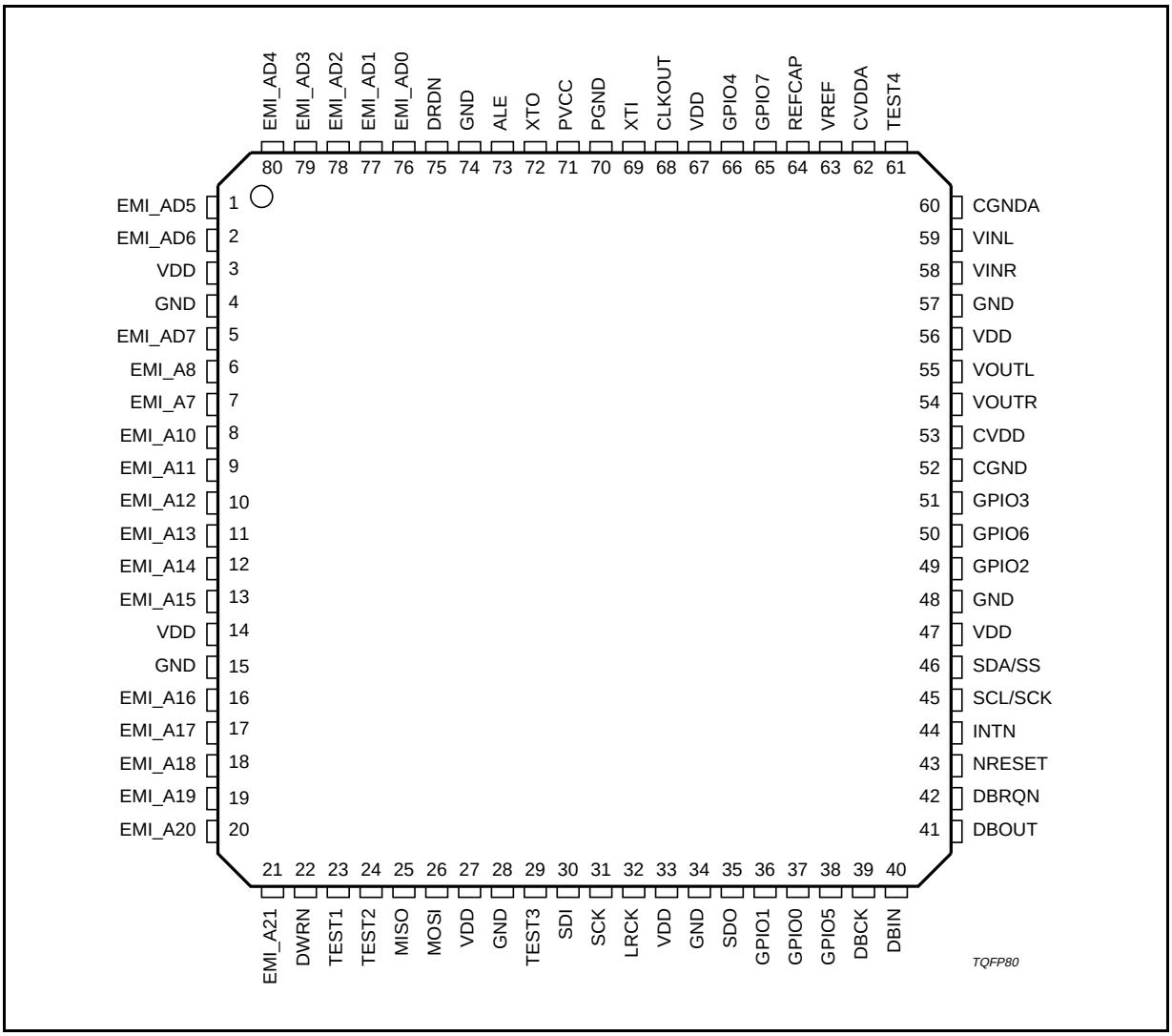
APPLICATIONS

Real time digital speech and audio processing: speech recognition, speech synthesis, speech compression, echo cancelling, noise cancelling, speaker verification.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DDP}	Pads DC Supply Voltage	–0.3 to V_{DD} +0.3	V
V_D, V_{IN}	Digital or Analog Input Voltage	–0.3 to V_{DDP} +0.3	V
T_{op}	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature Range	–55 to +150	°C
P_{tot}	Total Maximum Power Dissipation		mW

PIN CONNECTION



PIN FUNCTIONS

N.	Name	Type	Description
1	EMI_AD5	I/O	EMI Multiplexed Address/Data Line 5. these pin acts as the EMI multiplexed address and data line 5
2	EMI_AD6	I/O	EMI Multiplexed Address/Data Line 6. these pin acts as the EMI multiplexed address and data line 6
3	VDD	I	Digital power supply
4	GND	I	Ground
5	EMI_AD7	I/O	EMI Multiplexed Address/Data Line 7. these pin acts as the EMI multiplexed address and data line 7
6	EMI_A8	O	EMI Address Line 8. these pin acts as the EMI address line 8. The interface is designed to address up to 4 Mbytes of External Flash, EPROM or SRAM.
7	EMI_A9	O	EMI Address Line 9. these pin acts as the EMI address line 9.
8	EMI_A10	O	EMI Address Line 10. these pin acts as the EMI address line 10.
9	EMI_A11	O	EMI Address Line 11. these pin acts as the EMI address line 11.
10	EMI_A12	O	EMI Address Line 12. these pin acts as the EMI address line 12.
11	EMI_A13	O	EMI Address Line 13. these pin acts as the EMI address line 13.
12	EMI_A14	O	EMI Address Line 14. these pin acts as the EMI address line 14.
13	EMI_A15	O	EMI Address Line 15. these pin acts as the EMI address line 15.
14	VDD	I	Digital power supply
15	GND	I	Ground
16	EMI_A16	O	EMI Address Line 16. these pin acts as the EMI address line 16.
17	EMI_A17	O	EMI Address Line 17. these pin acts as the EMI address line 17.
18	EMI_A18	O	EMI Address Line 18. these pin acts as the EMI address line 18.
19	EMI_A19	O	EMI Address Line 19. these pin acts as the EMI address line 19.
20	EMI_A20	O	EMI Address Line 20. these pin acts as the EMI address line 20.
21	EMI_A21	O	EMI Address Line 21. these pin acts as the EMI address line 21.
22	DWRN	O	EMI Write Enable. This pin serves as the write enable for the EMI
23	TEST1	I	Test 1. Used for test: set to LOW for normal operation
24	TEST2	I	Test 2. Used for test: set to HIGH for normal operation
25	MISO	I/O	SPI Master Output Slave Input Serial Data. Serial Data Output for SPI type serial Port when in SPI master Mode and Serial Data Input when in SPI Slave Mode
26	MOSI	I/O	SPI Master Input Slave Output Serial Data. Serial Data Input for SPI type serial Port when in SPI master Mode and Serial Data Output when in SPI Slave Mode
27	VDD	I	Digital Power Supply
28	GND	I	Ground
29	TEST3	I	Test 3. Used for test: set to LOW for normal operation
30	SDI	I	SAI Data Input
31	SCK	I/O	SAI Bit Clock
32	LRCK	I/O	SAI Left/Right Clock
33	VDD	I	Digital power supply
34	GND	I	Ground
35	SDO	O	SAI Data Output

PIN FUNCTIONS (continued)

N.	Name	Type	Description
36	GPIO1	I/O	General Purpose I/O
37	GPIO0	I/O	General Purpose I/O
38	GPIO5	I/O	General Purpose I/O
39	DBCK	I/O	Debug port Bit Clock/Chip Status 1. The serial clock for the Debug Port is provided. May also be used as GPIO9.
40	DBIN	I/O	Debug port Serial Input/Chip Status 0. The serial data input for the Debug Port is provided. May also be used as GPIO11.
41	DBOUT	I/O	Debug Port Serial Output. This pin is the serial Data output for the Debug port. May also be used as GPIO10.
42	DBRQN	I	Debug Port Request Input. This pin is used to request Debug Mode operation to Euterpe
43	NRESET	I	System Reset. A low level applied to RESET input initializes the IC.
44	INTN	I	External interrupt line. When this line is asserted low the DSP may be interrupted.
45	SCL/SCK	I/O	I^2C Serial Clock Line. Clock line for I^2C bus. Schmitt trigger input.
		I/O	SPI Bit Clock. If SPI interface is enabled, it behaves as SPI bit clock.
46	SDA/SS	I/O	I^2C Serial Data Line. Data line for I^2C bus. Schmitt trigger input.
		I	SPI Slave Select. If SPI interface is enabled, it behaves as Slave select line for SPI bus.
47	VDD	I	Digital Power Supply
48	GND	I	Ground
49	GPIO2	I/O	General Purpose I/O
50	GPIO6	I/O	General Purpose I/O
51	GPIO3	I/O	General Purpose I/O
52	CGND	I	Ground for the internal CODEC cell
53	CVDD	I	Power Supply for the internal CODEC cell
54	VOUTR	O	Single-ended right channel analogue output from DAC
55	VOUTL	O	Single-ended left channel analogue output from DAC
56	VDD	I	Digital power supply
57	GND	I	Ground
58	VINR	I	Single-ended right channel analogue input to ADC
59	VINL	I	Single-ended left channel analogue input to ADC
60	CGNDA	I	Ground for the internal CODEC cell
61	TEST4	O	Connect a 22K pull-down resistor
62	CVDDA	I	Power Supply for the internal CODEC cell
63	VREF	O	Voltage Reference from the CODEC cell
64	REFCAP	O	Voltage Reference Capacitor Bypass
65	GPIO7	I/O	General Purpose I/O
66	GPIO4	I/O	General Purpose I/O
67	VDD	I	Digital power supply
68	CLKOUT	O	Clock Output. Output Clock divided down from PLL

PIN FUNCTIONS (continued)

N.	Name	Type	Description
69	XTI	I	Crystal Oscillator Input. Crystal Oscillator Input drive
70	PGND	O	PLL Ground Input. Ground connection for Oscillator circuit
71	PVCC	I	PLL Power Supply Positive. Supply for PLL Clock Oscillator
72	XTO	O	Crystal Oscillator Output. Crystal Oscillator Output drive
73	ALE	O	EMI Address Latch Enable. This pin acts as the EMI Address Latch Enable for the External Memory Interface
74	GND	I	Ground
75	DRDN	O	EMI Read Enable. This pin serves as the read enable for the EMI
76	EMI_AD0	I/O	EMI Multiplexed Address/Data Line 0. these pin acts as the EMI multiplexed address and data line 0
77	EMI_AD1	I/O	EMI Multiplexed Address/Data Line 1. these pin acts as the EMI multiplexed address and data line 1
78	EMI_AD2	I/O	EMI Multiplexed Address/Data Line 2. these pin acts as the EMI multiplexed address and data line 2
79	EMI_AD3	I/O	EMI Multiplexed Address/Data Line 3. these pin acts as the EMI multiplexed address and data line 3
80	EMI_AD4	I/O	EMI Multiplexed Address/Data Line 4. these pin acts as the EMI multiplexed address and data line 4

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Volrage Range		3	3.3	3.6	V
T_J	Operating Junction Temp.		–40		125	°C

24 BIT DSP CORE

The DSP Core is a general purpose 24-bit DSP. The main feature of the DSP Core are listed below:

- 50Mhz Operating Frequency (50 MIPS)
- Single cycle multiply and accumulate
- 2x56-bit Accumulators
- Double precision multiply
- Convergent rounding
- Scaling and saturation arithmetic
- 48-bit or 2x24-bit parallel moves
- 64 interrupt vector locations
- Fast or long interrupts possible
- Programmable interrupt priorities and masking
- 8 each Address Registers, Address Offset Registers and Address Modulo Registers
- Linear, Reverse Carry, Multiple Buffer Modulo, Multiple Wrap-around Modulo address arithmetic
- Post-increment or decrement by 1 or by offset, Index by offset, predecrement address
- Repeat instruction and zero overhead DO loops
- Hardware stackcapable of nesting 7 DO loops or 15 interrupts/subroutines
- Bit manipulation instructions possible on all registers and memory locations. Also Jump on bit test.
- Data Arithmetic Logic Unit (DALU)
- Address Generation Unit (AGU)
- Program Control Unit (PCU)
- Three Data Buses
- Three Address Buses
- Internal Data Bus Switch
- bit Manipulation Unit
- Debug Logic

Memories

16384x24-bit Program ROM used for storing the program code.

16384x24-bit Data RAM used for storing Data.

DSP peripherals

- **Serial Audio Interface (SAI)**
  The SAI is used to deliver digital audio to the DSP from an external source and to deliver digital audio from the DSP to an external DAC. It allows using an external CODEC. The main features of this block are listed below:
  – One Data Transmission Line
  – One Data Reception Line
  – Master and Slave Operating Modes
  – Reference clock for transmission supplied
  – Transmit and Receive Interrupt Logic modified to trigger on Left/Right data pairs
  – Receive and Transmit Data Registers have two locations to hold left and right data

- **I^2C interface/SPI**
  The inter integrated-circuit bus is a simple bi-directional two-wire bus used for efficient inter IC control. All I^2C bus compatible devices incorporate an on-chip interface which allows them communicate directly with each via the I^2C bus.
  Every component hoocked up to the I^2C bus has it's own unique address whether it is a CPU, memory or some other complex function chip. Each of these chips can act as a receiver and/or transmitter depending on it's functionality.
  The Serial Peripheral Interface (SPI) can be enabled instead of the I^2C interface. During an SPI transfer, data is trasmitted and received simulaneously. A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows individual selection of a slve SPI device. When an SPI transfer occurs an 8-bit word is shifted out one data pin while another 8-bit character is simultaneously shifted in a second data pin. The central element in the SPI system is the shift register and the read data buffer. The system is single buffered in the trasmit direction and double buffered in the receive direction.

EMI

- The External Memory Interface is viewed as a memory mapped peripheral. Data transfers are performed by moving data into/from data registers and the control is exercised by polling status flags in the control/status register or by servicing interrupts. An external memory write is executed by writing data into the Data Write register. An external memory read operation is executed by either writing to the Offset register or reading the Data read register, depending on the configuration.
  The main features of the EMI are listed below:
  – Data bus width fixed at 4 bits for DRAM and 8 bits for SRAM
  – 22 bit address bus multiplexed with an 8 bit data bus
  – Three choices of data word lenghths, 8, 16 or 24 bits in SRAM mode
  – Two choices of data word lenght, 16 or 24 bits in DRAM mode
  – Thirteen address lines 2^{26}= 256Mbits

addressable DRAM
– Refresh rate for DRAM can be chosen among sixteen divide factors
– SRAM or DRAM relative addressing modes
– 2^{22}=4MBytes addressable SRAM
– Four SRAM Timing choices
– Two Read Offset Register

- **PLL**

The Euterpe clock system generates the following clocks:
– DCLK the DSP core clock
– MCLK CODEC master clock
– LRCLK left/right clock for the SAI and the CODEC
– SCLK shift serial clock for the SAI and the CODEC

The output of the PLL operates from 70 to 140 MHz. The DSP core can operate with a clock up to 50 MHz.

From the VCO output the audio clock are derived.

- **CODEC**

The main features of the CODEC are listed below:
– one 16-bit Delta Sigma Stereo ADC
– 80 dB Dynamic Range
– Oversampling Ratio: 128
– one 16-bit Delta Sigma Stereo DAC
– 80 dB Dynamic Range
– Interpolating Ratio: 128
– Sampling rates of 4kHz to 48kHz
– Signal Noise Ratio: 80 dB Typ.

The analog interface is in the form of differential signals for each channel. The interface on the digital side has the form of an SAI interface and can interface directly to an SAI channel and then to the DSP core.

DEVICE versions

Part No.	Internal Program Memory	Function	Serial I/F	External Memory	Audio Input	Audio Output	Software
TDA7550R	RAM	One of the below	Master or Slave I^2C	FLASH or RAM	YES (by appl.)	YES (by appl.)	Custom Specs.
TDA7550	ROM	Speech Recognition	Slave I^2C	FLASH	YES, 1 (voice in)	YES (prompts)	ASR-311 Engine by Lernout & Hauspie
TDA7551		Speaker Verification	Slave I^2C	Optional FLASH	YES, 1 (voice in)	YES (prompts)	SV208 Engine by Lernout & Hauspie
TDA7552		Text-To-Speech	Slave I^2C	–	NO	YES (voice out)	TTS3000 Engine by Lernout & Hauspie
TDA7553		SF/FDE	Master I^2C or SPI	(RAM)	YES, 1 (voice in)	YES (filtered)	Engine by NCTI

Note: TDA7550 requires word databases on FLASH (cfr. Document words)

TDA7550

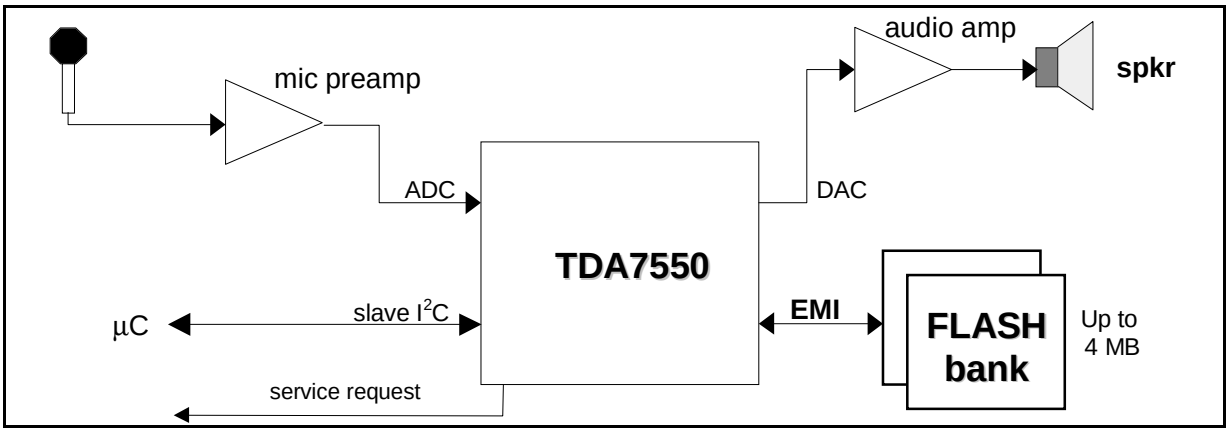
ASR311 Automatic Speech Recognition solution

The TDA-7550 is a single-chip solution for isolated word speech recognition, featuring the Lernout & Hauspie ASR311 Automatic Speech Recognition engine.

Word base recognition Isolated word recognition	The words database is created from an extensive set of recordings, with an equal distribution of speakers; the recordings are partially taken in automotive conditions at low, medium and high speed.
Quasi-connected digit recognition	Minimum pause between two numbers 150ms.
Noise-robust recognition	The recognition is still very robust even in high noisy environment (as automotive or industrial environments)
Speaker-independent recognition	Recognition is affected by selected language, no training is required
Speaker-dependent recognition	User words can be stored and mixed with speaker-independent words
Training phase	User words can be trained by repeating three times the selected word. Recognition is guaranteed when the same speaker is talking.
Prompts	Voice prompts can be stored on FLASH for creating a voice-based user interface
Control through I^2C	Management of the recognition engine, user words and voice prompts is accomplished through an I^2C protocol: the TDA7550 appears as a slave I^2C device.
Many languages available	Vocabularies in the following languages are available: US English, French, German, Italian, Spanish, Japanese. All the vocabularies have a common subset of about 150 words. Other words and languages are available on request.
The external FLASH is used to store:	♦ Speaker Independent vocabulary (4 KB/word) ♦ User Words (4 KB/word) ♦ Voice prompts (11 KB/sec)

Sample rate:	11.025 kHz
Recognition rate:	> 95%
Maximum number of active words:	30
Maximum number of words:	450
Word memory requirements:	4 KB (speaker-independent) 4 KB (speaker-dependent)
Prompt memory requirements:	11 KB/s

Figure 1.



TDA7551

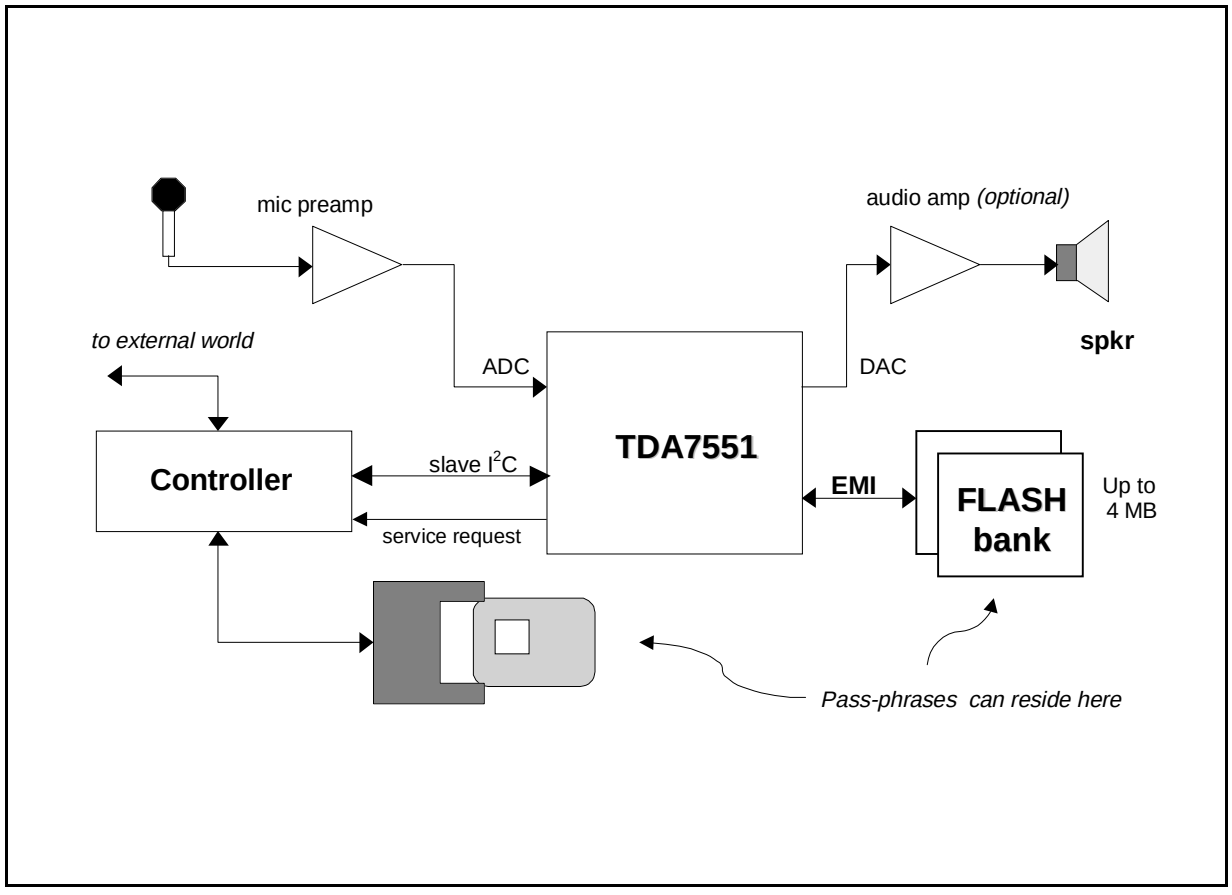
SV208 Speaker Verification solution

The TDA7551 is a single-chip solution for speaker verification, featuring the Lernout & Hauspie SV208 verification engine. Pass-phrases can be stored by performing an enrollment (the pass-phrase must be repeated three times), then the incoming prompt can be compared with the pre-stored pass-phrase to verify the speaker identity.

Known password speaker recognition	Noise-robust recognition of isolated words
Enrollment phase	The speaker associates his identity to an utterance, which must last from 1 to 2 seconds, and reapeat it three times; the algorithm performs an analysis and accepts or rejects the enrollment phase.
Verification phase	The claimed identity of the speaker is compared with the result of the verification phase, in which the input prompt is compared with the selected pass-phrase.
Control through I^2C	Management of the verification engine is accomplished through an I^2C protocol: the TDA7551 appears as a slave I^2C device.

Sample rate:	8 kHz
Equal error rate:	> 94%

Figure 2.



TDA7552

TTS3000 Text-To-Speech solution

The TDA7551 is part of a two-chip solution for Text-To-Speech, featuring the Lernout & Hauspie TTS3000 engine. Two devices are needed:

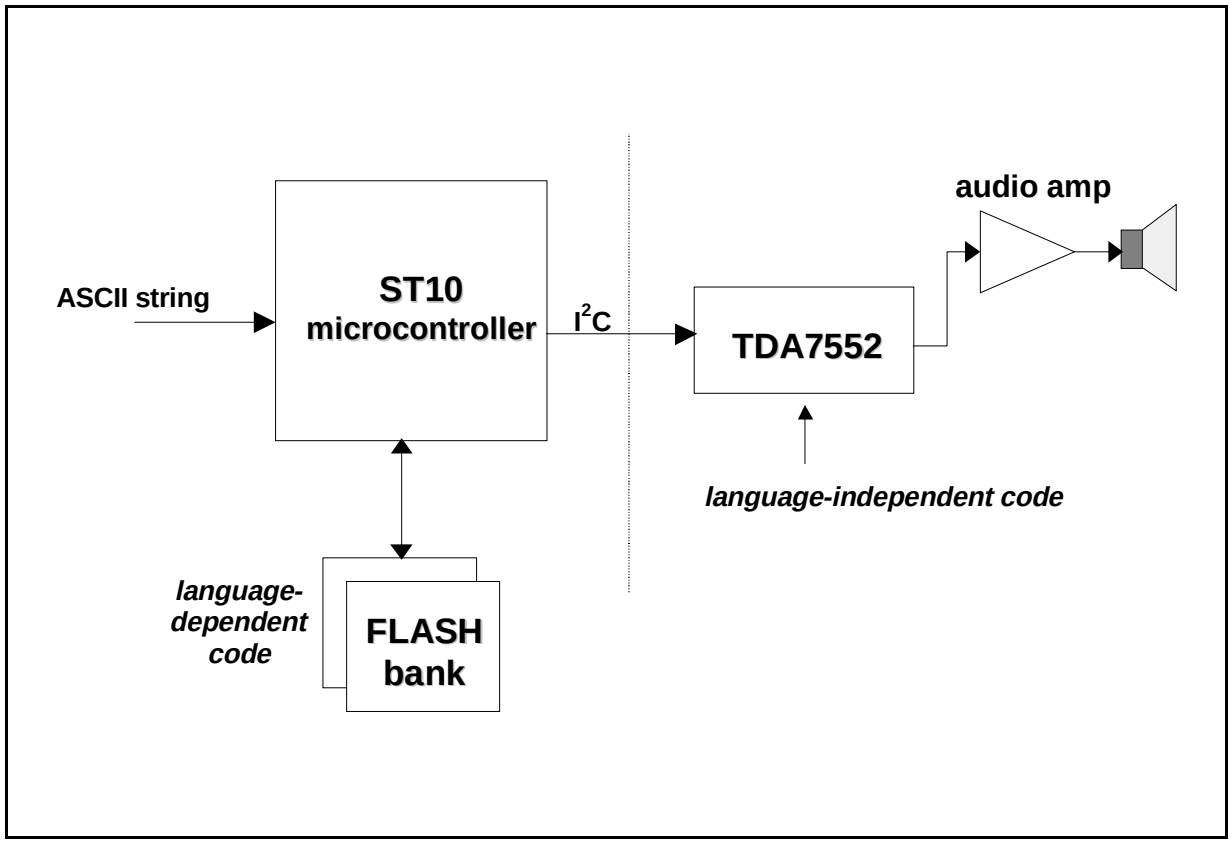
- A 16-bit microcontroller (ST10) for string analysis and conversion
- The TDA7552 DSP for voice synthesis.

An external application sends ASCII strings to the microcontroller, which perform an analysis of the entire sentence; language-dependent data is needed on the FLASH accessed by the ST10. As a result of the analysis, a data stream is sent through I^2C to the TDS7552 DSP. No external memory is required by the DSP. The software running on the TDA7552 DSP is independent from languages.

Control through I^2C	Management of the DSP is accomplished through an I^2C protocol: the TDA7552 appears as a slave i^2c device.
Many languages available	The following languages are available: US English, French, German, Italian, Spanish, Japanese. Other languages available on request.

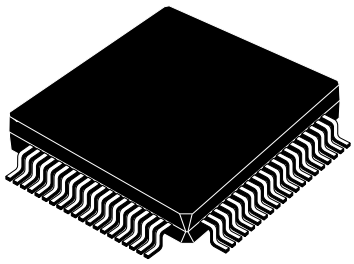
Sample rate: 11.025 kHz

Figure 3.

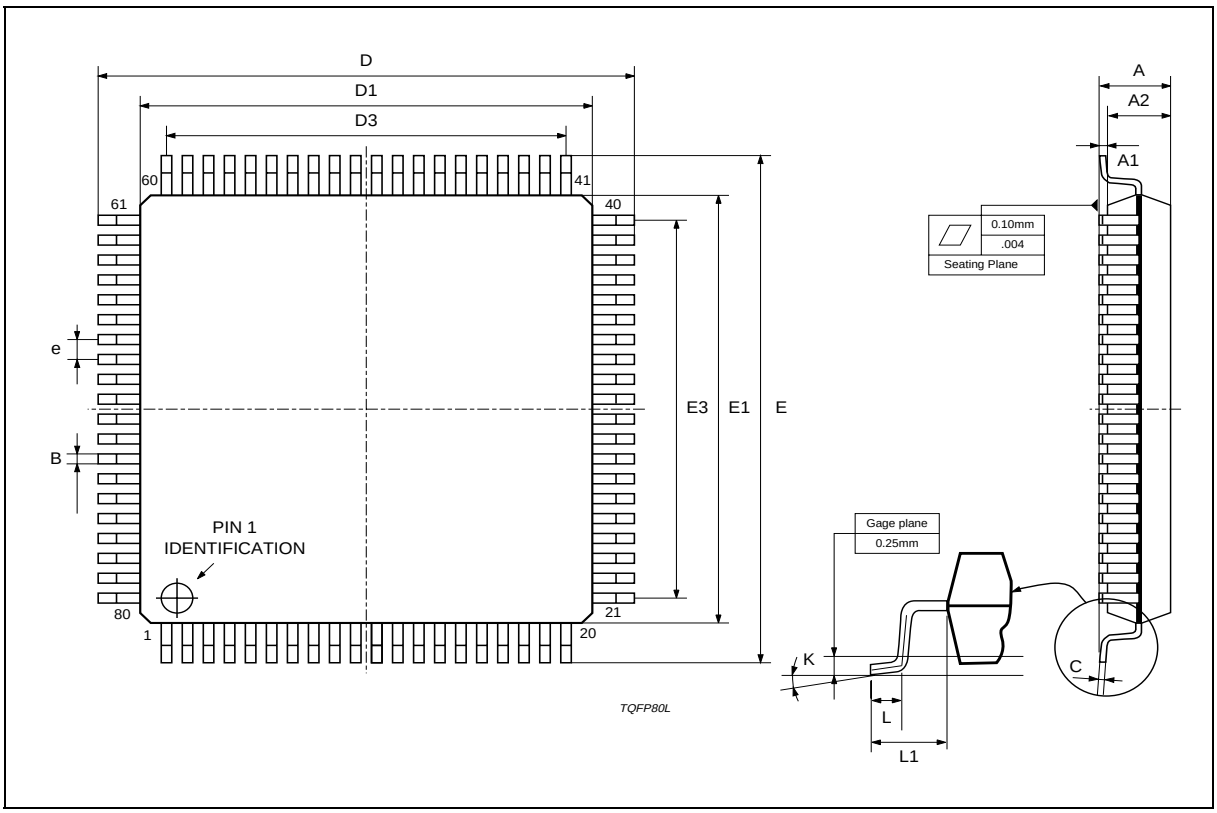


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.22	0.32	0.38	0.009	0.013	0.015
C	0.09		0.20	0.003		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.35			0.295	
e		0.65			0.0256	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.35			0.486	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.0393	
K	3.5°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP80 (14x14x1.40mm)



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