0.37 Ω, Low Capacitance, Dual DPDT / Quad SPDT Analog Switch

DESCRIPTION

The DG2788A, is a four-channel single-pole double-throw (SPDT) analog switch with two control inputs. It is also known as a two-channel double-pole double-throw (DPDT) configuration. The part is designed to operate from 1.8 V to 5.5 V single power rail. All switches conduct equally well in both directions, offering rail to rail signal witching and can be used both as multiplexers as well as de-multiplexers.

The DG2788A offers low parasitic capacitance and highly matched low and flat switch resistance over the full signal range. It features break-before-make switching and low control logic threshold. The part supports rail to rail fast edge pulsing signals and have 0.1 ns/typ. propagation delay. It is ideal for both analog and digital signal switching in space constrain applications requiring high performance and efficient use of board space.

The DG2788A comes in a small miniQFN-16 lead package of 2.6 mm x 1.8 mm x 0.55 mm.

FEATURES

Pb-free

RoHS COMPLIANT

- 1.8 V to 5.5 V single supply operation
- Low resistance: 0.37 Ω/typ. at 2.7 V
- Highly flat and matched R_{ON}
- Low parasitic capacitance, C_{ON} = 26 pF, C_{OFF} = 14.5 pF
- High bandwidth: 338 MHz
- 0.1 ns/typ. propagation delay for rail to rail fast edge pulsing signal
- Guaranteed logic high 1.2 V, logic low 0.3 V
- Break before make switching
- Signal swing over V+ capable
- Power down protection
- Latch up current: 300 mA (JESD78)
- ESD / HBM: > 2 kV
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

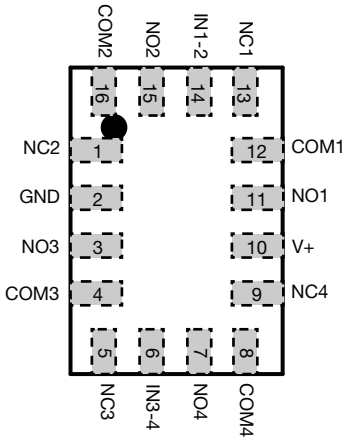
BENEFITS

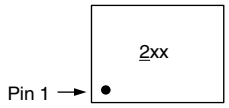
- Low and flat resistance
- Excellent total harmonic distortion
- Low parasitic capacitance
- Low voltage control interface

APPLICATIONS

- Analog and digital signal switching
- SMA optical image stabilization
- Relay replacement
- Portable instrumentation
- Smart phones and tablets
- Modems and peripherals
- Data storage

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION





Device marking: 2xx

xx = date / lot traceability code
Note: pin 1 has long lead

TRUTH TABLE		
LOGIC	NC1, 2, 3 and 4	NO1, 2, 3 and 4
0	On	Off
1	Off	On

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ORDERING INFORMATION			
TEMPERATURE RANGE	**PACKAGE**	**PART NUMBER**	**MIN. ORDER / PACK. QUANTITY**
-40 °C to +85 °C lead (Pb)-free	miniQFN-16	DG2788ADN-T1-GE4	Tape and reel, 3000 units

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Reference to GND	V+		-0.3 to +6	V
	IN, COM, NC, NO [a]		-0.3 to (V+ + 0.3)	
Current (any terminal except NO, NC, or COM)			30	mA
Continuous current (NO, NC, or COM)			± 300	
Peak current (pulsed at 1 ms, 10 % duty cycle)			± 500	
Storage temperature (D suffix)			-65 to +150	°C
Package solder reflow conditions [d]	miniQFN-16		250	
Power dissipation (packages) [b]	miniQFN-16 [c]		525	mW

Notes

a. Signals on NC, NO, or COM, or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6.6 mW/°C above 70 °C.
d. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

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SPECIFICATIONS (V+ = 3 V)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS** unless otherwise specified V+ = 3 V, ± 10 %, V_{IN} = 0.5 or 1.4 V [e]	**TEMP.** [a]	**LIMITS** -40 °C to +85 °C			**UNIT**
				MIN. [b]	**TYP.** [c]	**MAX.** [b]	
Analog Switch							
Analog signal range [d]	V_{NO}, V_{NC}, V_{COM}		Full	0	-	V+	V
On-resistance	R_{ON}	V+ = 2.7 V, V_{COM} = 0 to 2.7 V, I_{NO}, I_{NC} = 100 mA	Room	-	0.37	0.5	Ω
			Full	-	-	0.6	
R_{ON} flatness [d]	R_{ON} flatness	V+ = 2.7 V, V_{COM} = 0 to V+, I_{NO}, I_{NC} = 100 mA	Room	-	0.01	0.05	
R_{ON} match [d]	ΔR_{ON}		Room	-	0.05	-	
Switch off leakage current	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 5.5 V, V_{NO}, V_{NC} = 0.5 V / 4 V, V_{COM} = 4 V / 0.5 V	Room	-0.1	-	0.1	µA
			Full	-0.5	-	0.5	
	$I_{COM(off)}$		Room	-1.2	-	1.2	
			Full	-2	-	2	
Channel-on leakage current	$I_{COM(on)}$	V+ = 5.5 V, V_{NO}, V_{NC} = V_{COM} = 0.5 V / 4 V	Room	-1.2	-	1.2	
			Full	-2	-	2	
Digital Control							
Input high voltage	V_{INH}		Full	1.2	-	-	V
Input low voltage	V_{INL}		Full	-	-	0.3	
Input capacitance	C_{IN}		Full	-	5	-	pF
Input current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	-1	-	1	µA
Dynamic Characteristics							
Turn-on time	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room	-	30	50	µs
			Full	-	-	150	
Turn-off time	t_{OFF}		Room	-	0.35	1	
			Full	-	-	3	
Break-before-make time	t_d		Full	1	-	-	
Charge injection [d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 1.5 V, R_{GEN} = 0 Ω	Room	-	-245	-	pC
-3 dB bandwidth	BW	R_L = 50 Ω, C_L = 5 pF	Room	-	338	-	MHz
Off-isolation [d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz	Room	-	-82	-	dB
		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		-	-56	-	
Crosstalk [d, f]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz		-	-87	-	
		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		-	-61	-	
NO, NC off capacitance [d]	$C_{NO(off)}$	f = 1 MHz	Room	-	14.5	-	pF
	$C_{NC(off)}$		Room	-	14.5	-	
Channel-on capacitance [d]	$C_{NO(on)}$		Room	-	26	-	
	$C_{NC(on)}$		Room	-	26	-	
Power Supply							
Power supply range	V+			1.8	-	5.5	V
Power supply current	I+	V_{IN} = 0 or V+	Full	-	24	60	µA

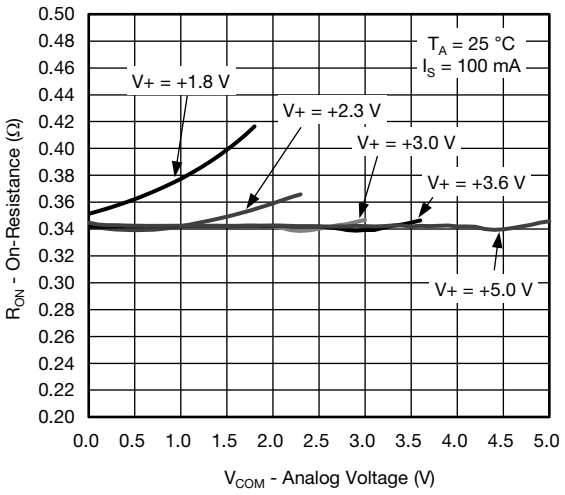
Notes

a. Room = 25 °C, full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, not subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Crosstalk measured between channels.

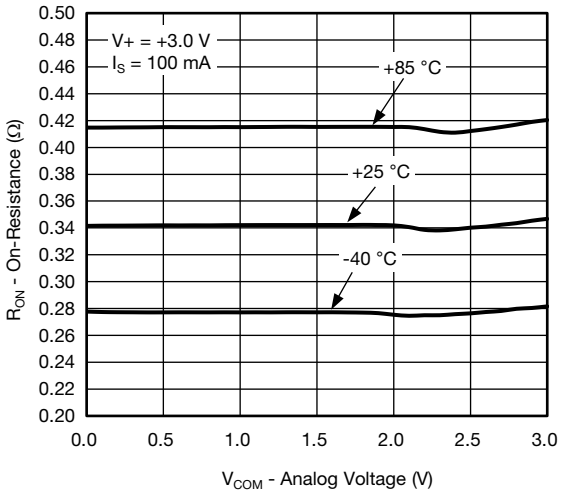
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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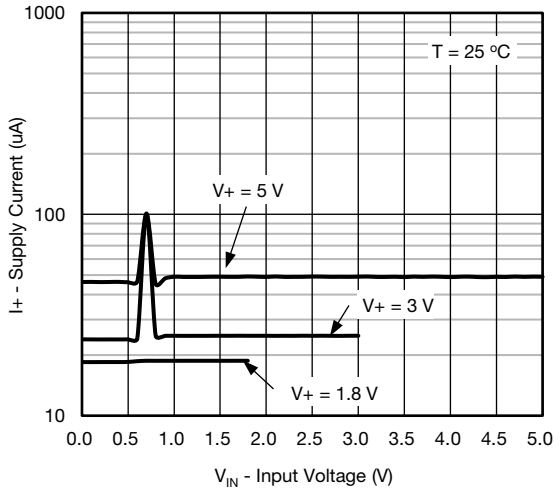
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



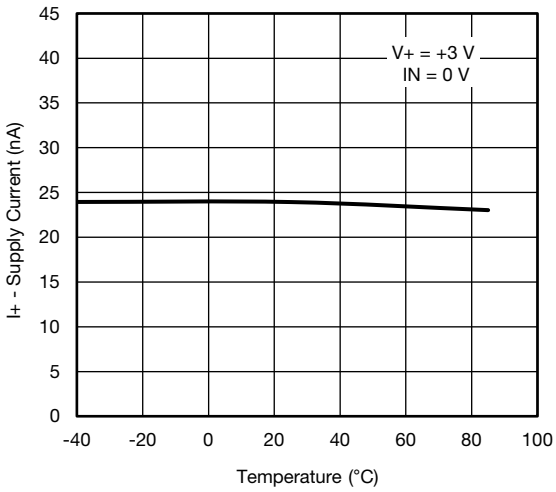
R_{ON} vs. V_{COM} and Supply Voltage



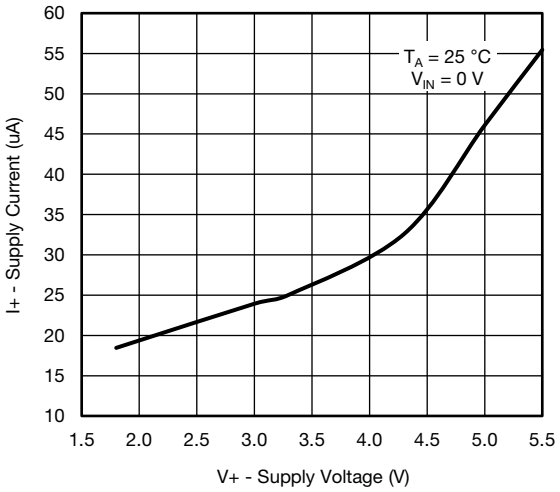
R_{ON} vs. Analog Voltage and Temperature



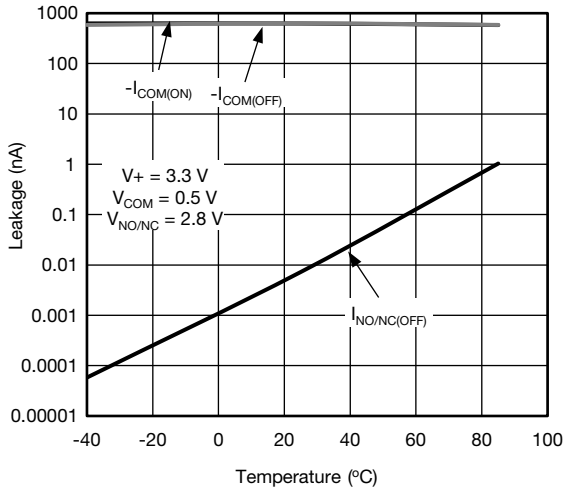
Supply Current vs. Input Voltage



Supply Current vs. Temperature



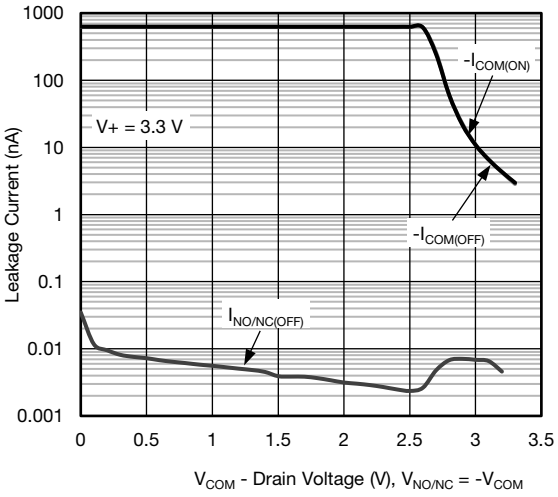
Supply Current vs. Supply Voltage



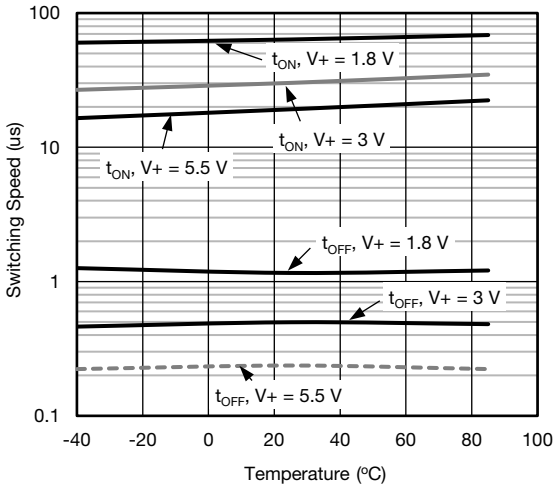
Leakage Current vs. Temperature

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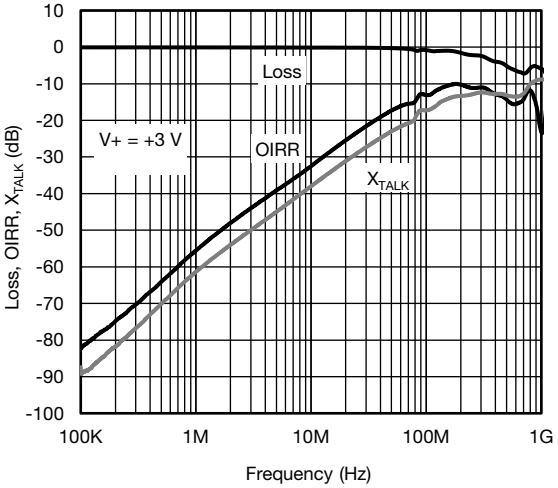
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



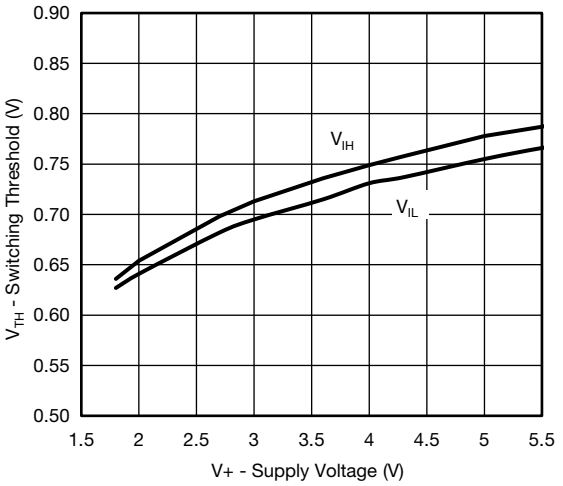
Leakage Current vs. Drain Voltage



Switching Time vs. Temperature



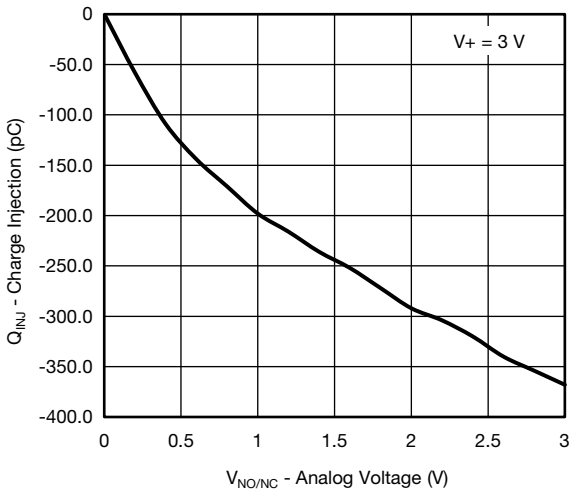
Insertion Loss, Off-Isolation Crosstalk vs. Frequency



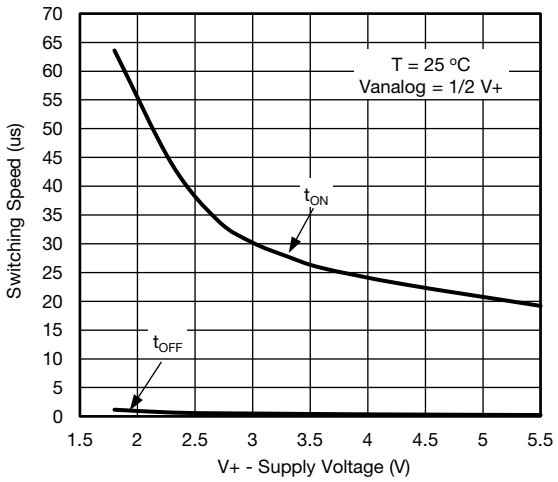
Switching Threshold vs. Supply Voltage

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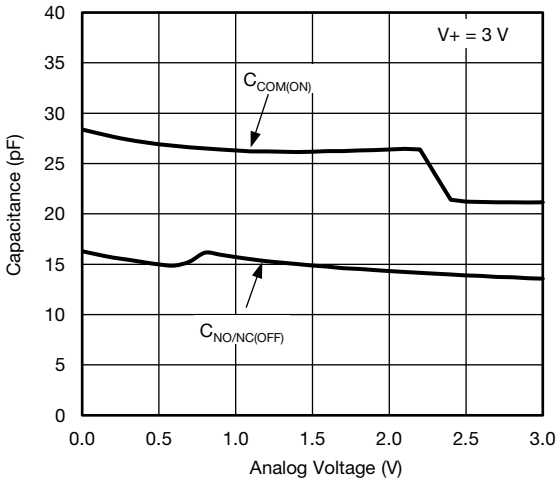
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Charge Injection vs. Analog Voltage



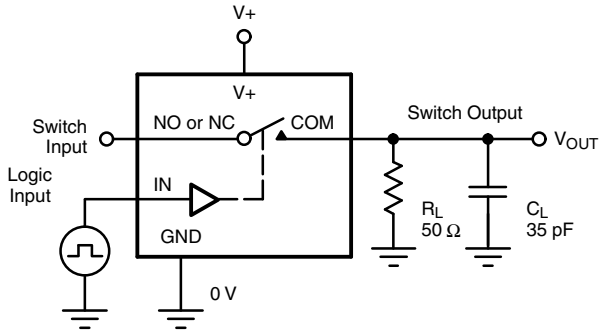
Switching Time vs. Supply Voltage



Capacitance vs. Analog Voltage

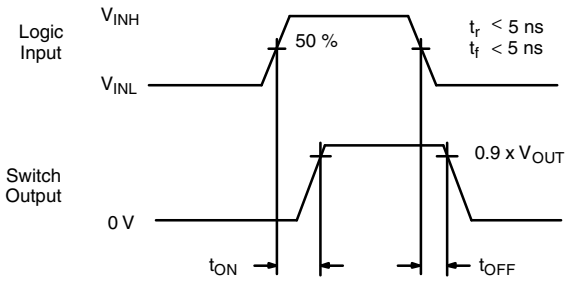
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TEST CIRCUITS



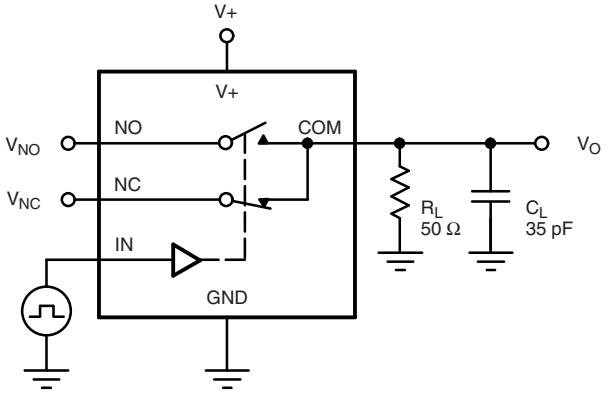
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Fig. 1 - Switching Time



C_L (includes fixture and stray capacitance)

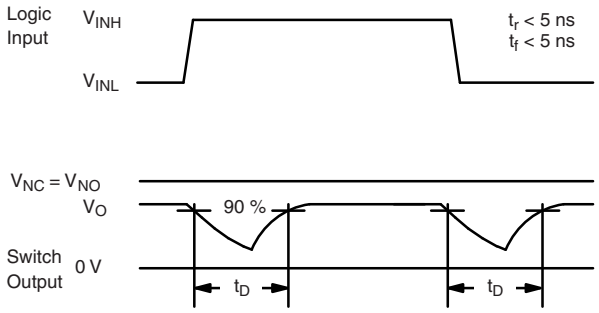
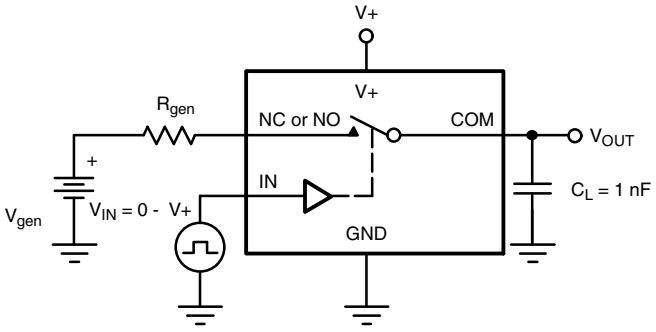
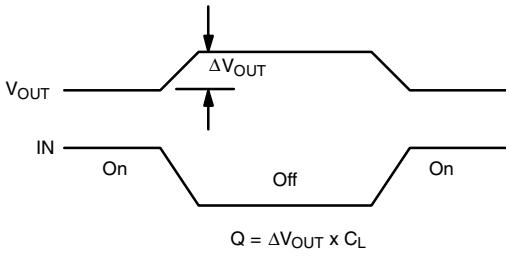


Fig. 2 - Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Fig. 3 - Charge Injection

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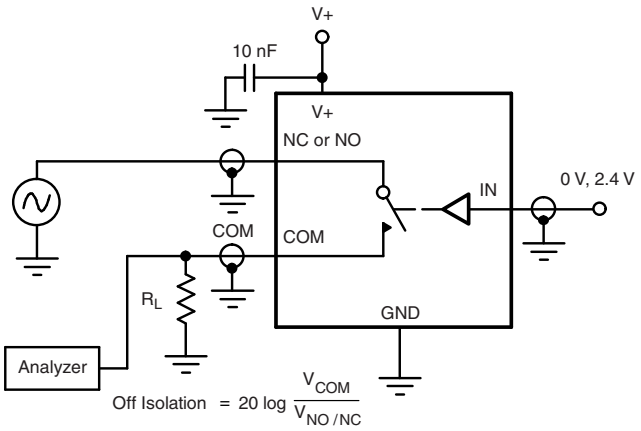


Fig. 4 - Off-Isolation

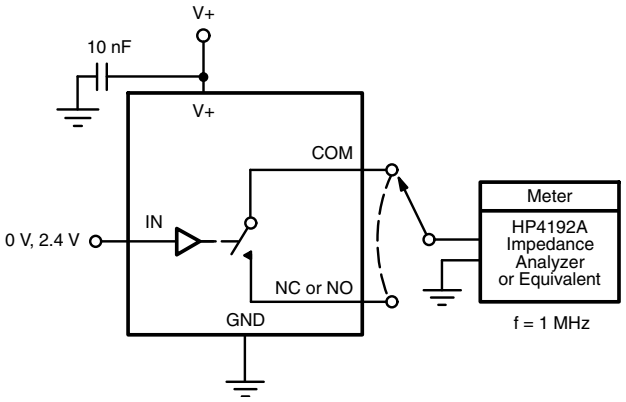
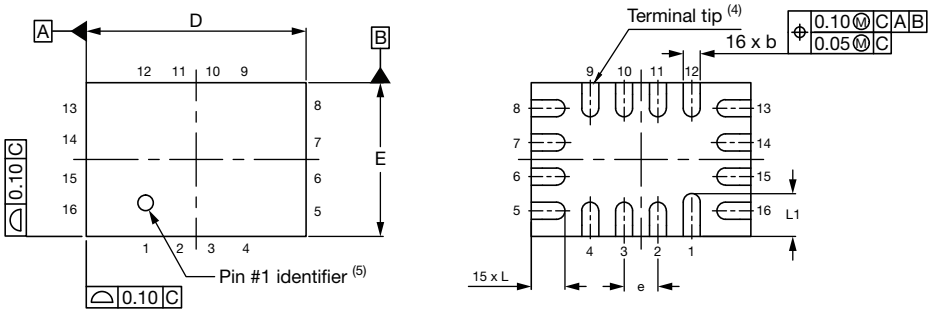


Fig. 5 - Channel Off / On Capacitance

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Thin miniQFN16 Case Outline



DIMENSIONS	MILLIMETERS (1)			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0	-	0.05	0	-	0.002
A3	0.15 ref.			0.006 ref.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	2.50	2.60	2.70	0.098	0.102	0.106
e	0.40 BSC			0.016 BSC		
E	1.70	1.80	1.90	0.067	0.071	0.075
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.018	0.020	0.022
N (3)	16			16		
Nd (3)	4			4		
Ne (3)	4			4		

Notes

(1) Use millimeters as the primary measurement.

(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.

(3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.

(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.

(5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.

(6) Package warpage max. 0.05 mm.

ECN: T16-0226-Rev. B, 09-May-16
DWG: 6023

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