TC1307

Four-Channel CMOS LDO with Select Mode, Shutdown and Independent Reset

Features

- Four Independent 150 mA LDOs
- Low Supply Current (220 µA typical)
- High Output Voltage Accuracy (0.5% typical)
- Low Dropout Voltage (100 mV typical with 150 mA load)
- Four Independent Shutdown Inputs
- Select Mode™: Selectable Output Voltages for High Design Flexibility
- Integrated Independent Microprocessor Reset
- Low Noise Outputs
- Fast Response from Shutdown (10 µs typical)
- $\overline{\text{RESET}}$ Output for Low Battery Detection or Reset Generator
- Over Current and Over-Temperature Protection
- Small 16-Pin QSOP Package
- Specified Junction Temperature Range:
  - -40°C to +125°C

Applications

- Battery Operated Systems
- Potable Computers
- Set Top Boxes
- Load Partitioning
- Medical Instruments
- Cellular / GSM / PHS Phones
- Instrumentation
- Linear Post Regulator for SMPS
- Pagers

Description

The TC1307 combines four CMOS Low Dropout Linear Regulators with a Microcontroller Monitor in a space-saving 16-Pin QSOP package. Developed specifically for battery powered portable applications, all four outputs of the TC1307 typically consume a total of 220 µA supply current, hold the output voltage to a tolerance of 0.5% and require 100 mV of headroom for regulation at the maximum output current of 150 mA. In addition to the four high performance LDOs, the TC1307 also includes a voltage detector with a delayed $\overline{\text{RESET}}$ output that can be configured for low battery detection or Microcontroller Reset Generator.

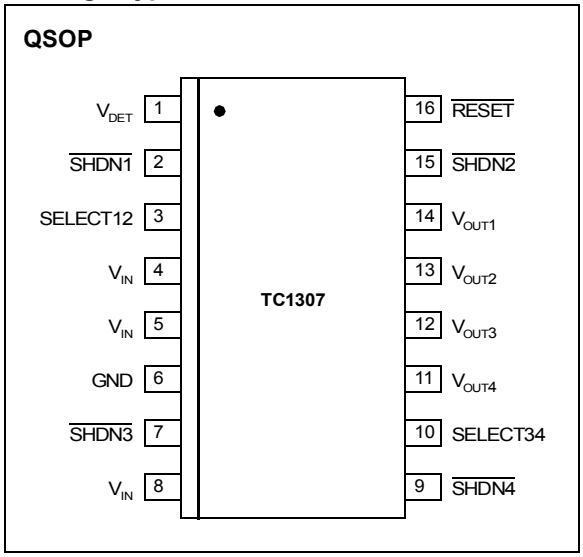
All four LDOs have independent shutdown inputs and can be programmed using two select inputs making the TC1307 adaptable for a wide range of multiple output applications. The tri-state SELECT12 input pin allows the designer to select the output voltages on V_{OUT1}, and V_{OUT2} from three different values (2.5V, 2.8V or 3.0V). The tri-state SELECT34 input pin allows the designer to select the output voltages on V_{OUT3}, and V_{OUT4} from three different values (1.8V, 2.5V or 2.8V). All four LDO's require only a 1 µF output capacitor for stability that can be ceramic, tantalum or aluminum over the entire input voltage operating range and 0 mA to 150 mA rated load range. All four LDOs have low output noise and excellent dynamic response when faced with sudden line and load changes.

The voltage detect pin is set for a threshold of 2.63V (typical) and operates down to a minimum input voltage of 1.0V. When the voltage on the detect pin rises above the 2.63V threshold, the $\overline{\text{RESET}}$ output is held low for 300 ms (typical).

Additional integrated features include over-current protection and over-temperature protection providing full protection from external load faults.

Package Types

QSOP



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{DD}.....6.5V

All inputs and outputs w.r.t. ....V_{IN} + 0.3V to -0.3V

Output Short Circuit Current ....continuous

Storage temperature..... .... -65°C to +150°C

Operating Junction Temperature, T_J.....-40°C < T_J < +150°C

Maximum Junction Temperature, T_J.....150°C

ESD protection on all pins.....≥ 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
V_{DET}	Voltage Detect Input
$\overline{SHDN1}$	Shutdown for V_{OUT1}
SELECT12	Input for setting V_{OUT1} and V_{OUT2}.
V_{IN}	Input Voltage Connection
V_{IN}	Input Voltage Connection
GND	Ground connection
$\overline{SHDN3}$	Shutdown for V_{OUT3}
V_{IN}	Input Voltage Connection
$\overline{SHDN4}$	Shutdown for V_{OUT4}
SELECT34	Input for setting V_{OUT3} and V_{OUT4}.
V_{OUT4}	LDO4 Output
V_{OUT3}	LDO3 Output
V_{OUT2}	LDO2 Output
V_{OUT1}	LDO1 Output
$\overline{SHDN2}$	Shutdown for V_{OUT2}
$\overline{RESET}$	Reset Output

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits are established for V_{IN} = V_R+1, I_L = 100 µA, C_L = 3.3 µF, $\overline{SHDN}$ > V_{IH}, T_A = 25°C.
Boldface type specifications apply for junction temperatures, T_J (**Note 9**) of -40°C to +125°C.

Parameter	Sym	Min	Typ	Max	Units	Conditions
Input Characteristics:						
Input Operating Voltage	V_{IN}	**2.7**	—	**6.0**	V	**Note 1**
Input Quiescent Current	I_{IN}	—	220	**370**	µA	$\overline{SHDN}$ = V_{IH}, I_L = 0
Input Shutdown Current	$I_{IN_\overline{SHDN}}$	—	0.1	0.5	µA	$\overline{SHDN}$ = 0V
Output Characteristics:						
Maximum Output Current	I_{OUT_MAX}	**150**		—	mA	
Output Short Circuit Current (Average)	I_{OUT_SC}	—	360	—	mA	V_{OUT} = 0V
Voltage Regulation LDO1/LDO2/LDO3/LDO4	V_{OUT}	**V_R-2.5%**	V_R±0.5	**V_R+2.5%**	V	**Note 2**

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 2.7V$ and $V_{IN} \geq (V_R + 2.5\%) + V_{DROPOUT}$.

2: V_R is the nominal regulator output voltage. For example: V_R = 1.8V, 2.5V, 2.8V or 3.0V.

3: $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) * 10^6 / (V_R * \Delta Temperature)$, $V_{OUT-HIGH}$ = Highest voltage measured over the temperature range. $V_{OUT-LOW}$ = Lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 1mA to the maximum specified output current. Changes in output voltage due to heating effects are determined using thermal regulation specification TCV_{OUT}.

5: Thermal regulation is defined as the change in output voltage at a time t after a change in power dissipation is applied. Specifications are for a current pulse equal to I_{LMAX} at V_{IN} = 6.0V for t = 10 msec.

6: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value with a 1V differential applied.

7: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e. T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

8: V_{TH-MIN} = 2.55V and V_{TH-MAX} = 2.70V.

9: The Junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.

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Unless otherwise specified, all limits are established for $V_{IN} = V_R+1$, I_L = 100 µA, C_L = 3.3 µF, $\overline{SHDN} > V_{IH}$, T_A = 25°C.
Boldface type specifications apply for junction temperatures, T_J (**Note 9**) of -40°C to +125°C.

Parameter	Sym	Min	Typ	Max	Units	Conditions
VOUT Temperature Coefficient LDO1/LDO2/LDO3/LDO4	TCV_{OUT}	—	20 **40**	—	ppm/°C	**Note 3**
Line Regulation LDO1/LDO2/ LDO3/LDO4	$\Delta V_{OUT}/(V_{OUT} x \Delta V_{IN})$	—	0.05	0.2	%/V	$(V_R+1) \le V_{IN} \le 6.0V$
Load Regulation LDO1/LDO2/LDO3/LDO4	$\Delta V_{OUT}/V_{OUT}$	—	—	**2.0**	%	I_L = 0.1 mA to I_{OUT_MAX} **Note 4**
Thermal Regulation LDO1/LDO2/LDO3/LDO4	$\Delta V_{OUT}/\Delta P_D$	—	0.04	—	V/W	**Note 5**
Dropout Voltage LDO1/LDO2/LDO3/LDO4	$V_{IN}-V_{OUT}$	—	2	—	mV	I_L = 100 µA, **Note 6**
		—	15	—		I_L = 20 mA, **Note 6**
		—	35	**90**		I_L = 50 mA, **Note 6**
		—	100	**280**		I_L = 150 mA, **Note 6**
Output Noise LDO1/LDO2/LDO3/LDO4	e_N	—	1.2	—	µV/(Hz)$^{1/2}$	I_{OUT} = 100 mA, f = 10 kHz C_{OUT} = 1 µF to noise
Over Temperature Protection Characteristics:						
Thermal Shutdown Protection	T_{SD}	—	150	—	°C	**Note 7**
Thermal Shutdown Hysteresis	ΔTSD	—	10	—	°C	
$\overline{SHDN}$ Input Characteristics:						
$\overline{SHDN}$ Input High Threshold	V_{IH}	**60**	—	—	% of V_{IN}	V_{IN} = 2.7V to 6.0V
$\overline{SHDN}$ Input Low Threshold	V_{IL}	—	—	**15**	% of V_{IN}	V_{IN} = 2.7V to 6.0V
Wake-up Time (from $\overline{SHDN}$ mode)	t_{WK}	—	10	—	µsec	V_{IN} = 5V, I_L = 100 mA, C_{OUT} = 1 µF, C_{IN} = 1 µF, see Figure 4-1
Settling Time (from $\overline{SHDN}$ mode)	t_S	—	40	—	µsec	V_{IN} = 5V, I_L = 100 mA, C_{OUT} = 1 µF, C_{IN} = 1 µF, See Figure 4-1
Shutdown Leakage Current	$I_{\overline{SHDN}}$	—	±0.01	—	nA	$V_{\overline{SHDN}} = V_{IN}$ or GND
SELECT Input Characteristics:						
SELECT Input High Threshold	V_{SELH}	**V_{IN}-0.2**	—	—	V	V_{IN} = 2.7V to 6.0V
SELECT Input Low Threshold	V_{SELL}	—	—	**0.2**	V	V_{IN} = 2.7V to 6.0V
SELECT Input Leakage Current	I_{SELECT}	— —	±0.11 ±0.06	— **—**	µA	$V_{SELECT} = V_{IN}$ V_{SELECT} = GND
RESET Output Characteristics:						
Detect Operating Voltage Range	V_{DET}	1.0 **1.2**	— —	6.0 **6.0**	V	T_A = 0°C to +70°C T_A = -40°C to +125°C

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \ge 2.7V$ and $V_{IN} \ge (V_R + 2.5\%) + V_{DROPOUT}$.

2: V_R is the nominal regulator output voltage. For example: V_R = 1.8V, 2.5V, 2.8V or 3.0V.

3: $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) * 10^6 / (V_R * \Delta Temperature)$, $V_{OUT-HIGH}$ = Highest voltage measured over the temperature range. $V_{OUT-LOW}$ = Lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 1mA to the maximum specified output current. Changes in output voltage due to heating effects are determined using thermal regulation specification TCV_{OUT}.

5: Thermal regulation is defined as the change in output voltage at a time t after a change in power dissipation is applied. Specifications are for a current pulse equal to I_{LMAX} at V_{IN} = 6.0V for t = 10 msec.

6: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value with a 1V differential applied.

7: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e. T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 150°C rating. Sustained junction temperatures above 150°C can impact the device reliability.

8: V_{TH-MIN} = 2.55V and V_{TH-MAX} = 2.70V.

9: The Junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.

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Unless otherwise specified, all limits are established for $V_{IN} = V_R+1$, I_L = 100 µA, C_L = 3.3 µF, $\overline{SHDN} > V_{IH}$, T_A = 25°C.
Boldface type specifications apply for junction temperatures, T_J (**Note 9**) of -40°C to +125°C.

Parameter	Sym	Min	Typ	Max	Units	Conditions
Reset Threshold Voltage	V_{TH}	2.59 **2.55**	2.63 —	2.66 **2.70**	V V	T_A = +25°C T_A = -40°C to +125°C See Figure 4-2
Reset Circuit Supply Current	I_{VDET}	—	20	40	µA	$\overline{RESET}$ = Open
Reset Threshold Voltage Temperature Coefficient	$V_{TH-TEMP}$	—	30	—	ppm/°C	
Detect Threshold to $\overline{RESET}$ Active Time Delay	$T_{VDET-\overline{RESET}}$	—	135	—	µsec	$V_{DET} = V_{TH}$ to V_{TH} - 100 mV, See Figure 4-2
Reset Time-out Period	$T_{\overline{RESET}}$	**140**	300	**560**	msec	See Figure 4-2
$\overline{RESET}$ Output Voltage Low	$V_{OL-\overline{RES}}$	—	—	**0.3**	V	$V_{DET} = V_{TH-min}$ I_{SINK} = 1.2 mA
		—	—	**0.4**		$V_{DET} = V_{TH-min}$ I_{SINK} = 3.2 mA
		—	—	**0.3**		V_{DET} > 1.0V I_{SINK} = 50 µA **Note 8**, See Figure 4-2
$\overline{RESET}$ Output Voltage High	$V_{OH-\overline{RES}}$	0.8*V_{DET} V_{DET}-1.5V	—	—	V	I_{SOURCE} = 500 µA Isource = 800 µA $V_{DET}>V_{TH-max}$ (Both cases), See Figure 4-2
Temperature Ranges:						
Maximum Junction Temperature Range	T_J	-40	—	+150	°C	
Maximum Junction Temperature Range	T_J	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances:						
Thermal Resistance, 16L-QSOP	θ_{JA}	—	112.4	—	°C/W	EIA/JEDEC JESD51-751-7 4 Layer Board

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 2.7V$ and $V_{IN} \geq (V_R + 2.5\%) + V_{DROPOUT}$.

2: V_R is the nominal regulator output voltage. For example: V_R = 1.8V, 2.5V, 2.8V or 3.0V.

3: $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) * 10^6 / (V_R * \Delta Temperature)$, $V_{OUT-HIGH}$ = Highest voltage measured over the temperature range. $V_{OUT-LOW}$ = Lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 1mA to the maximum specified output current. Changes in output voltage due to heating effects are determined using thermal regulation specification TCV_{OUT}.

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8: V_{TH-MIN} = 2.55V and V_{TH-MAX} = 2.70V.

9: The Junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.

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2.0 TYPICAL PERFORMANCE CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{IN} = 3.8V, C_{IN} = 10 µF ceramic (X5R), C_{OUT} = 1 µF ceramic (X5R), I_{LOAD} = 100 µA, SELECT12 = NC, SELECT34 = V_{IN}, $\overline{SHDN1/2/3/4}$ = V_{IN}, T_A = 25°C.

Junction temperature (T_J) is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.

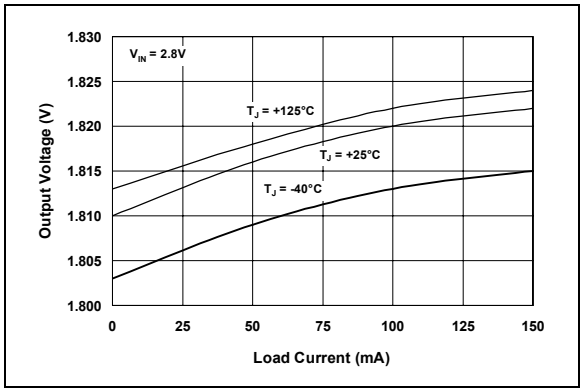


FIGURE 2-1: *V_{OUT} vs. Load Current.*

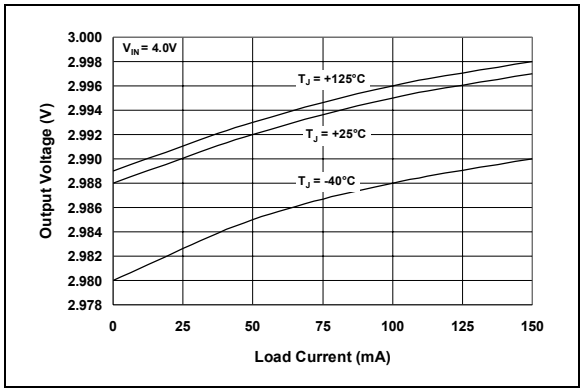


FIGURE 2-4: *V_{OUT} vs. Load Current.*

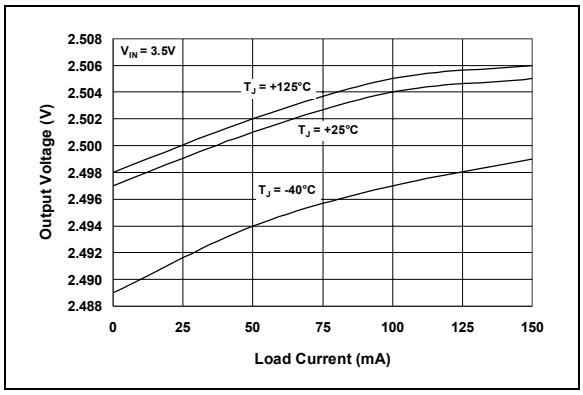


FIGURE 2-2: *V_{OUT} vs. Load Current.*

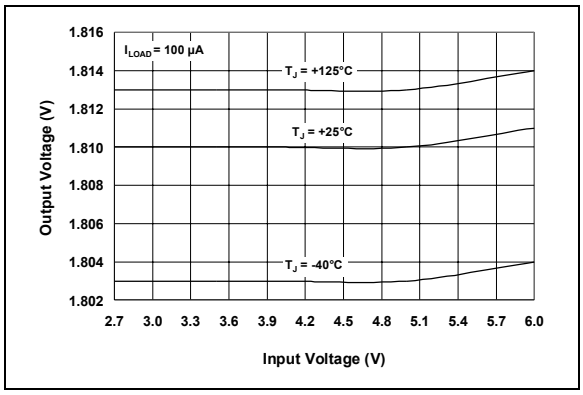


FIGURE 2-5: *V_{OUT} vs. Input Voltage.*

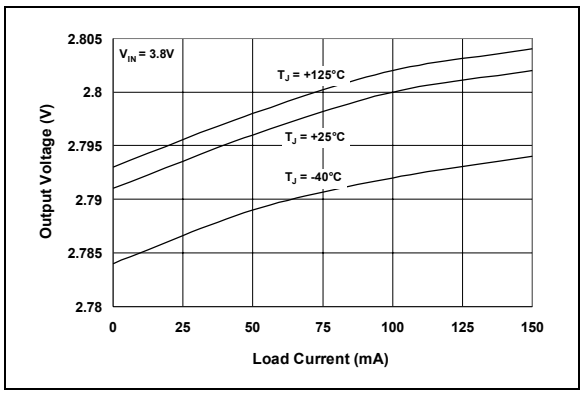


FIGURE 2-3: *V_{OUT} vs. Load Current.*

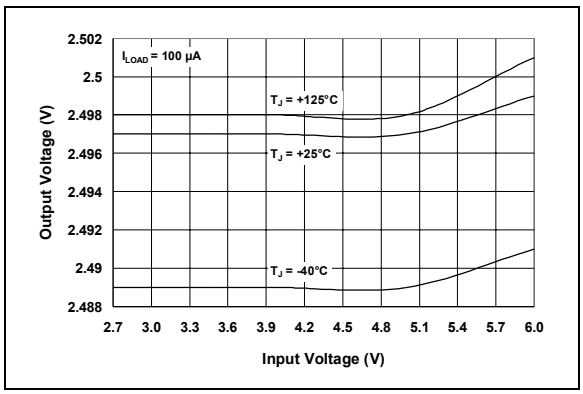


FIGURE 2-6: *V_{OUT} vs. Input Voltage.*

Note: Unless otherwise indicated, V_{IN} = 3.8V, C_{IN} = 10 µF ceramic (X5R), C_{OUT} = 1 µF ceramic (X5R), I_{LOAD} = 100 µA, SELECT12 = NC, SELECT34 = V_{IN}, $\overline{SHDN1/2/3/4}$ = V_{IN}, T_A = 25°C.

Junction temperature (T_J) is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.

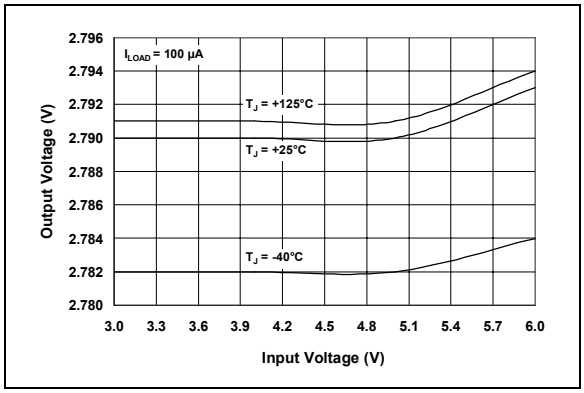


FIGURE 2-7: *V_{OUT} vs. Input Voltage.*

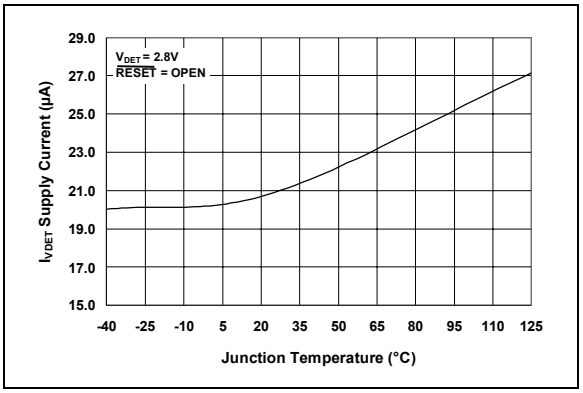


FIGURE 2-10: *V_{DET} Supply Current vs. Junction Temperature.*

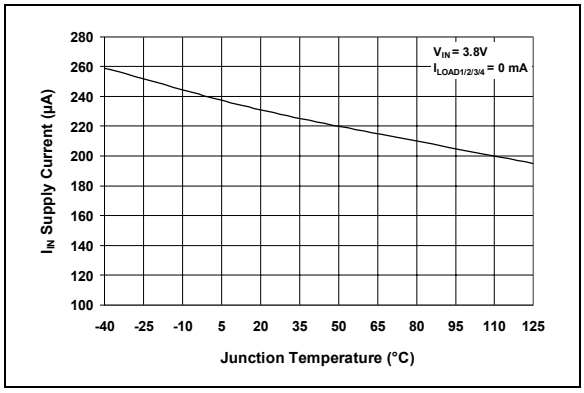


FIGURE 2-8: *V_{IN} Supply Current vs. Junction Temperature.*

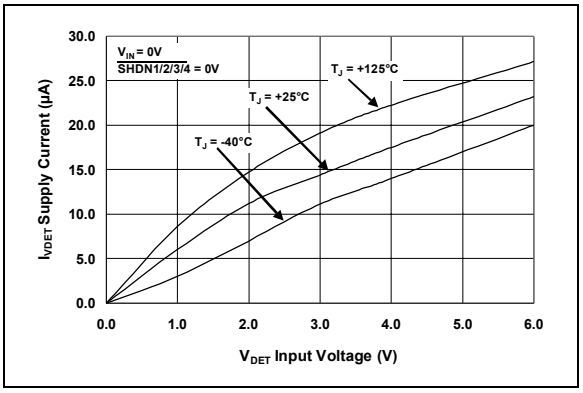


FIGURE 2-11: *V_{DET} Supply Current vs. V_{DET} Input Voltage.*

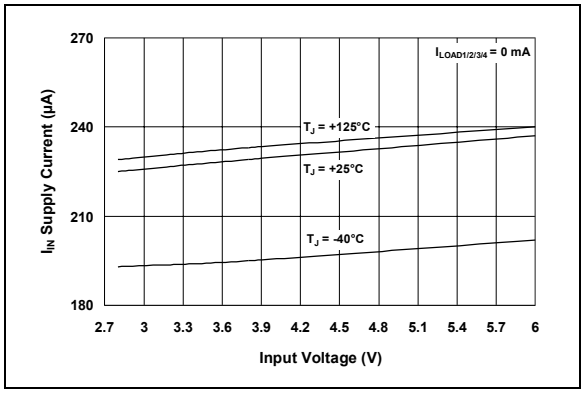


FIGURE 2-9: *Supply Current vs. Input Voltage, V_{IN}.*

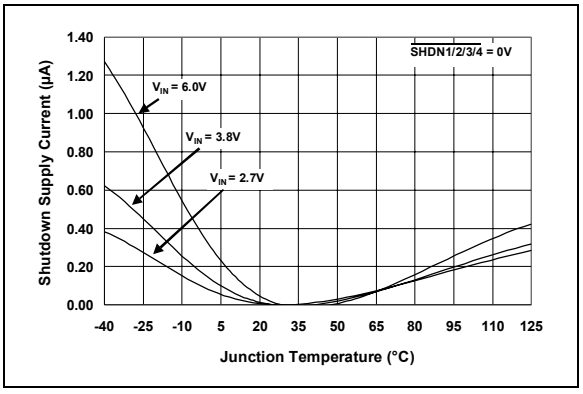


FIGURE 2-12: *Supply Current vs. Junction Temperature.*

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Note: Unless otherwise indicated, V_{IN} = 3.8V, C_{IN} = 10 µF ceramic (X5R), C_{OUT} = 1 µF ceramic (X5R), I_{LOAD} = 100 µA, SELECT12 = NC, SELECT34 = V_{IN}, $\overline{SHDN1/2/3/4}$ = V_{IN}, T_A = 25°C.

Junction temperature (T_J) is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.

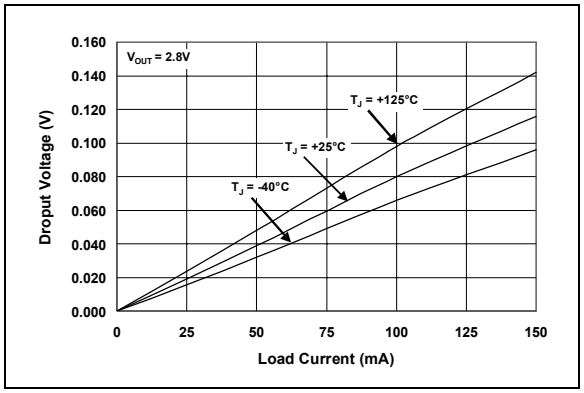


FIGURE 2-13: *Dropout Voltage vs. Load Current.*

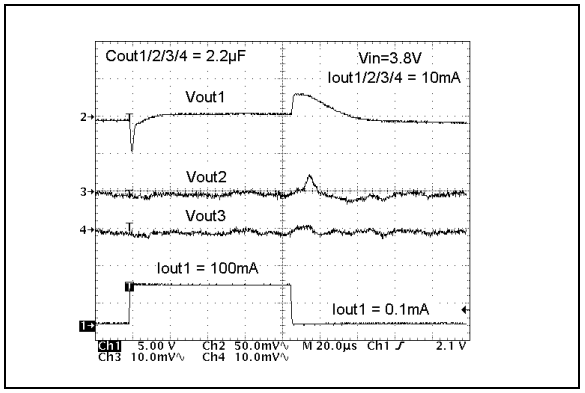


FIGURE 2-16: *Crosstalk Characteristics V_{OUT1}, V_{OUT2}, and V_{OUT3}.*

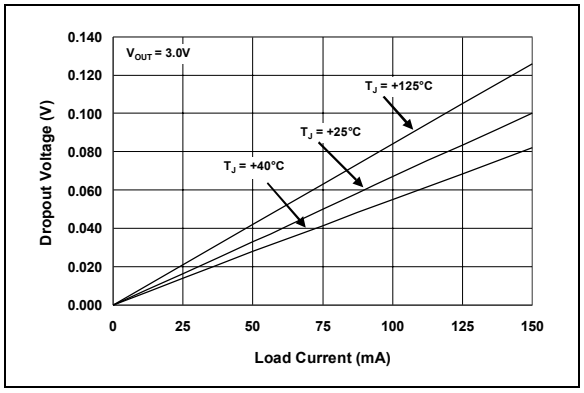


FIGURE 2-14: *Dropout Voltage vs. Load Current.*

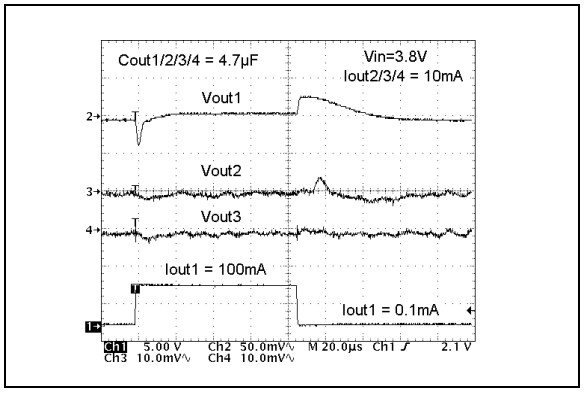


FIGURE 2-17: *Crosstalk Characteristics V_{OUT1}, V_{OUT2}, and V_{OUT3}.*

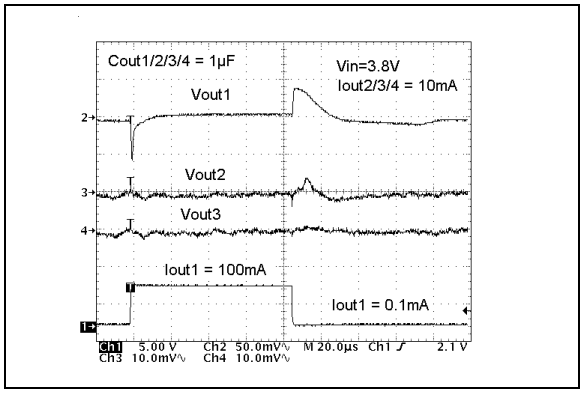


FIGURE 2-15: *Crosstalk Characteristics V_{OUT1}, V_{OUT2} and V_{OUT3}.*

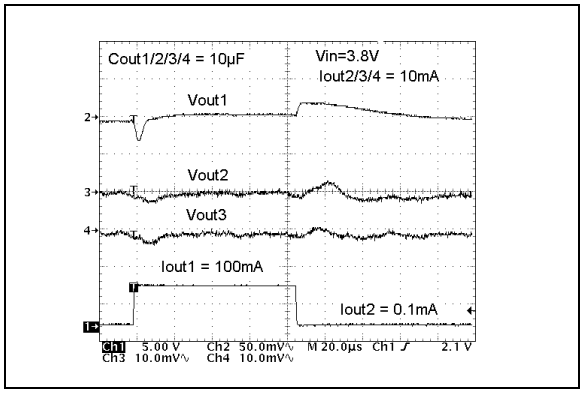


FIGURE 2-18: *Crosstalk Characteristics V_{OUT1}, V_{OUT2}, and V_{OUT3}.*

Note: Unless otherwise indicated, V_{IN} = 3.8V, C_{IN} = 10 µF ceramic (X5R), C_{OUT} = 1 µF ceramic (X5R), I_{LOAD} = 100 µA, SELECT12 = NC, SELECT34 = V_{IN}, $\overline{SHDN1/2/3/4}$ = V_{IN}, T_A = 25°C.

Junction temperature (T_J) is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.

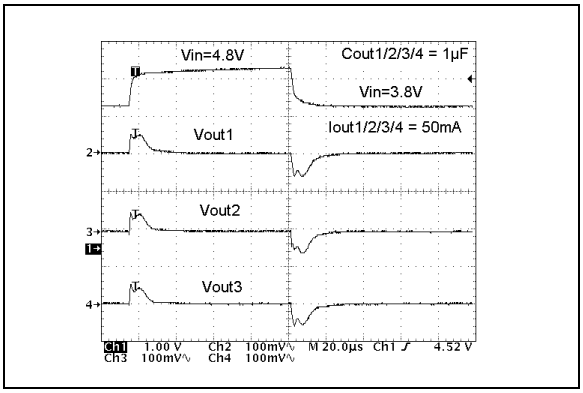


FIGURE 2-19: *Line Step Response.*

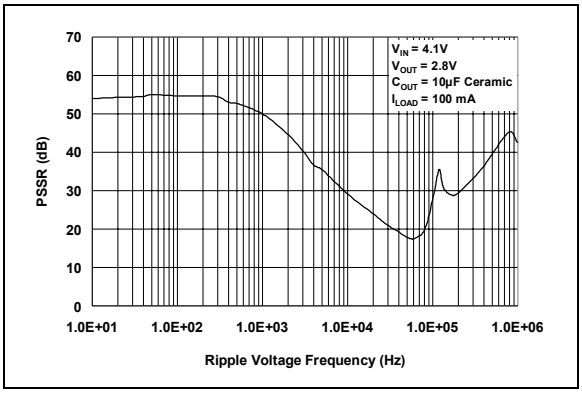


FIGURE 2-22: *Power Supply Rejection Ratio vs. Ripple Voltage Frequency.*

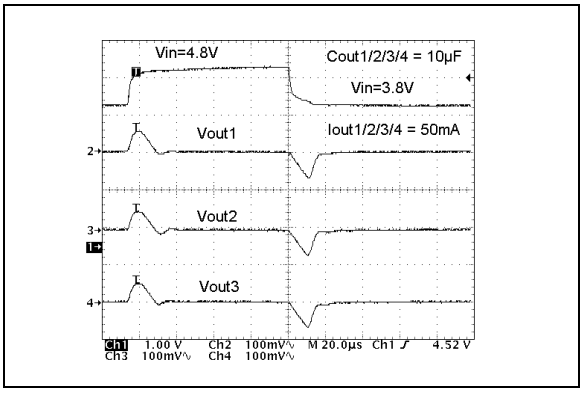


FIGURE 2-20: *Line Step Response.*

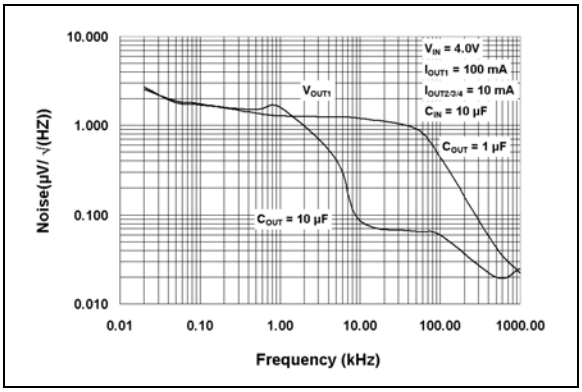


FIGURE 2-23: *Output Noise.*

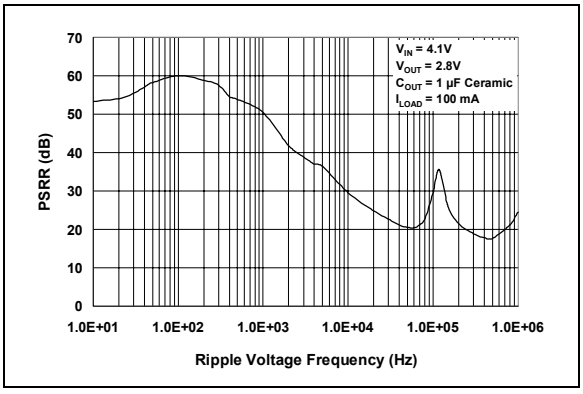


FIGURE 2-21: *Power Supply Rejection Ratio vs. Ripple Voltage Frequency.*

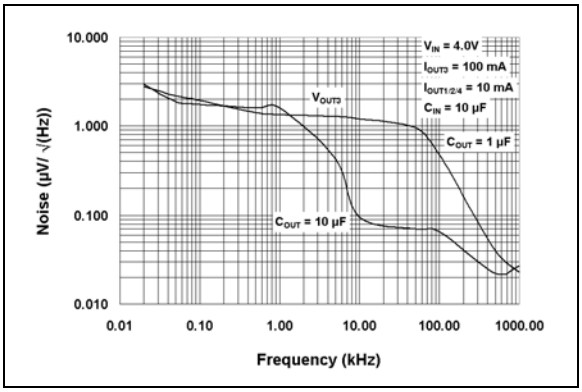


FIGURE 2-24: *Output Noise.*

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Note: Unless otherwise indicated, V_{IN} = 3.8V, C_{IN} = 10 µF ceramic (X5R), C_{OUT} = 1 µF ceramic (X5R), I_{LOAD} = 100 µA, SELECT12 = NC, SELECT34 = V_{IN}, $\overline{SHDN1/2/3/4}$ = V_{IN}, T_A = 25°C.

Junction temperature (T_J) is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.

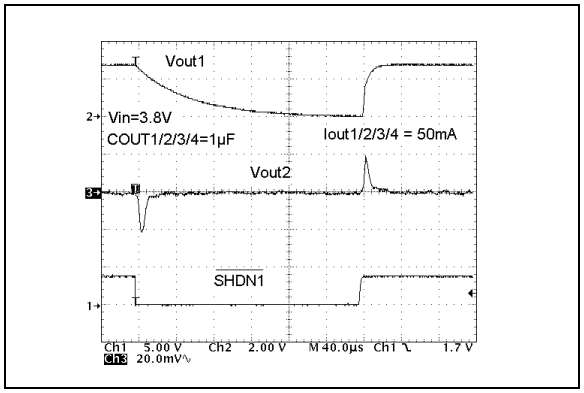


FIGURE 2-25: *Response From $\overline{SHDN}$.*

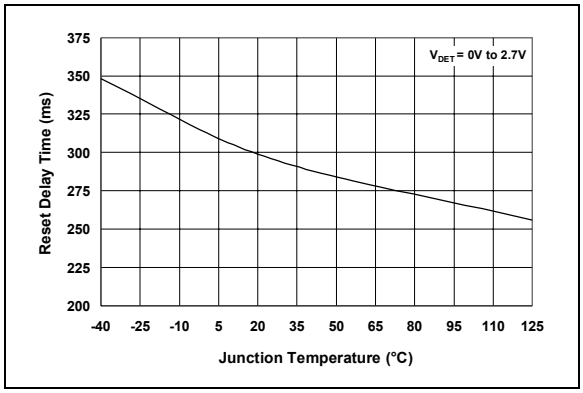


FIGURE 2-28: *Power-Up Reset Time-out Period vs. Junction Temperature.*

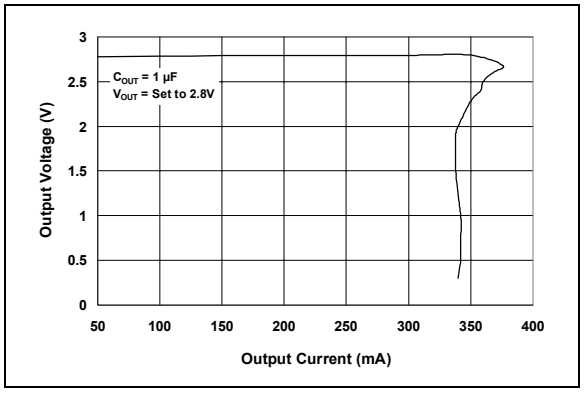


FIGURE 2-26: *Output Voltage vs. Current.*

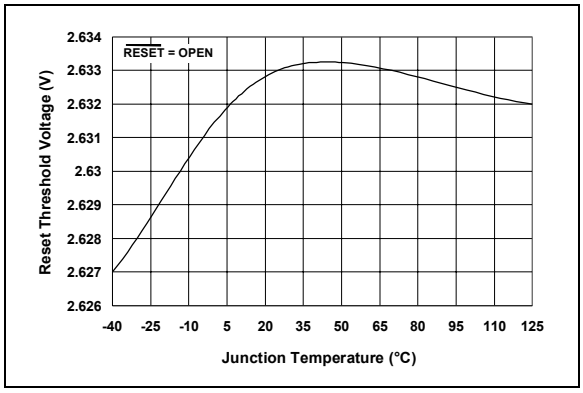


FIGURE 2-29: *Reset Threshold Voltage vs. Junction Temperature.*

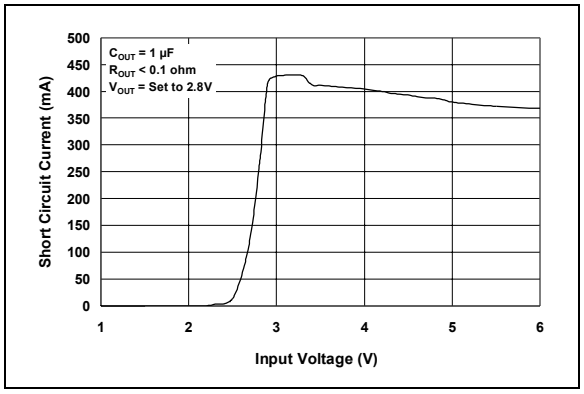


FIGURE 2-27: *Short Circuit Current vs. Input Voltage.*

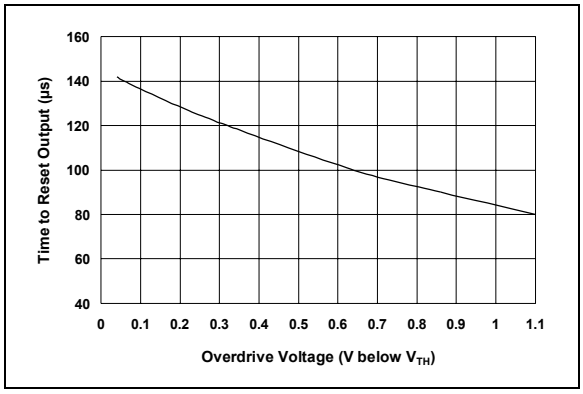


FIGURE 2-30: *Reset Delay vs. Overdrive Voltage.*

Note: Unless otherwise indicated, V_{IN} = 3.8V, C_{IN} = 10 µF ceramic (X5R), C_{OUT} = 1 µF ceramic (X5R), I_{LOAD} = 100 µA, SELECT12 = NC, SELECT34 = V_{IN}, $\overline{SHDN1/2/3/4}$ = V_{IN}, T_A = 25°C.

Junction temperature (T_J) is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the Ambient temperature is not significant.

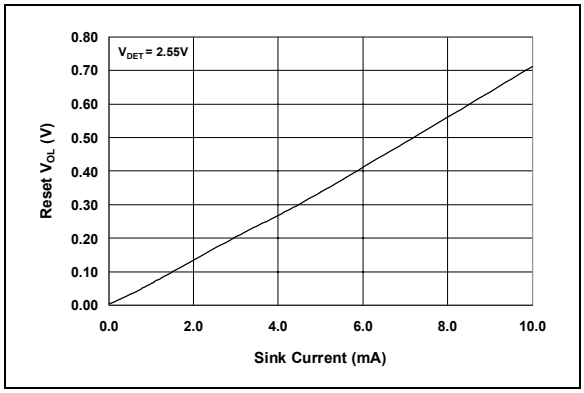


FIGURE 2-31: *Reset $V_{OL\text{-}\overline{RES}}$ vs. I_{SINK}.*

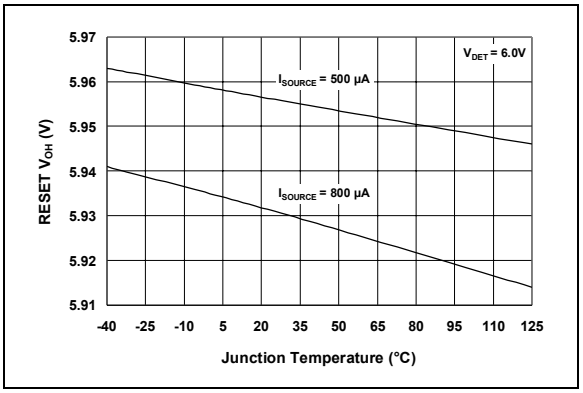


FIGURE 2-34: *Reset $V_{OH\text{-}\overline{RES}}$ vs.Junction Temperature.*

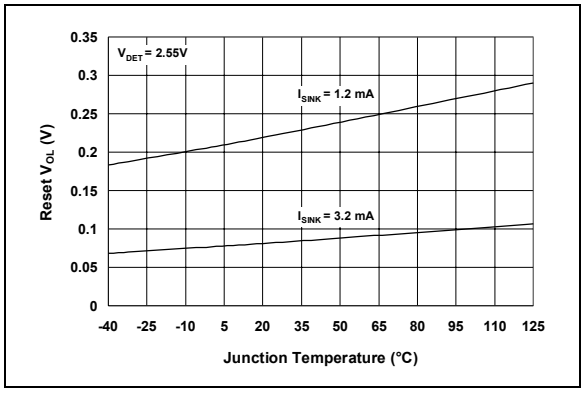


FIGURE 2-32: *Reset $V_{OL\text{-}\overline{RES}}$ vs. Junction Temperature.*

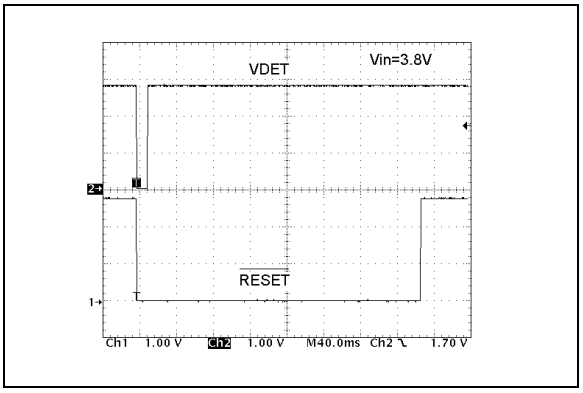


FIGURE 2-35: *Power-Up $\overline{RESET}$ Timing.*

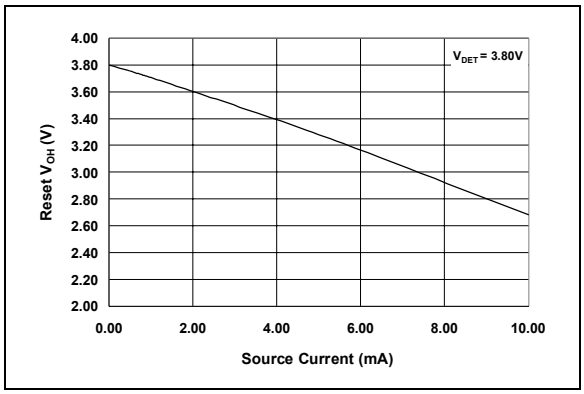


FIGURE 2-33: *Reset $V_{OH\text{-}\overline{RES}}$ vs. I_{SOURCE}.*

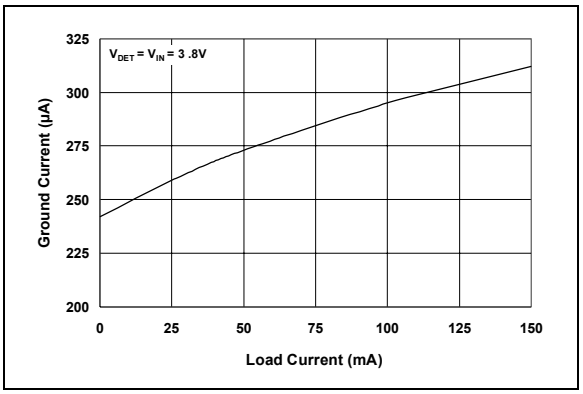


FIGURE 2-36: *Ground Current vs. Load Current.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

Name	Function
V_{DET}	Voltage Detect Input
$\overline{SHDN1}$	Shutdown for V_{OUT1}
SELECT12	Input for setting V_{OUT1} and V_{OUT2}.
V_{IN}	Input Voltage Connection
V_{IN}	Input Voltage Connection
GND	Ground connection
$\overline{SHDN3}$	Shutdown for V_{OUT3}
V_{IN}	Input Voltage Connection
$\overline{SHDN4}$	Shutdown for V_{OUT4}
SELECT34	Input for setting V_{OUT3} and V_{OUT4}.
V_{OUT4}	LDO4 Output
V_{OUT3}	LDO3 Output
V_{OUT2}	LDO2 Output
V_{OUT1}	LDO1 Output
$\overline{SHDN2}$	Shutdown for V_{OUT2}
$\overline{RESET}$	Reset Output

TABLE 3-1: *Pin Description Table.*

3.1 Voltage Detect Input (V_{DET})

Input pin that is compared to internal threshold voltage (typically 2.63V). When the V_{DET} input is below the 2.63V threshold, the $\overline{RESET}$ output is held in its normal low state. When the input voltage on the V_{DET} pin rises above the threshold voltage, the $\overline{RESET}$ output pin remains low for 300 mS (Typical). After the delay, the $\overline{RESET}$ pin changes to a logic high state.

3.2 Shutdown Control Input for V_{OUT1} ($\overline{SHDN1}$)

LDO#1 output is enabled when a logic high is applied to the $\overline{SHDN1}$ input. LDO#1 output is disabled with a logic low tied to the $\overline{SHDN1}$ pin. When shutdown, LDO#1 enters a low quiescent current state and the linear pass P-Channel MOSFET is off. The $\overline{RESET}$ output remains valid and is independent of $\overline{SHDN1}$.

3.3 SELECT Control Input for Setting V_{OUT1} and V_{OUT2} (SELECT12)

Input pin used to select the output voltage of LDO#1 and LDO#2. When SELECT is tied to V_{IN}, V_{OUT1} = V_{OUT2} = 3.0V. When SELECT is tied to GND, V_{OUT1} = V_{OUT2} = 2.5V. If the SELECT input is not connected, V_{OUT1} = V_{OUT2} = 2.8V.

3.4 Input Voltage V_{IN}

Connect input source to this pin. All V_{IN} pins must be tied together.

3.5 Ground (GND)

Connect this pin to the circuit ground. NOTE: This pin does not carry high current and should be connected to quiet circuit ground.

3.6 Shutdown Control Input for V_{OUT3} ($\overline{SHDN3}$)

LDO#3 output is enabled when a logic high is applied to the $\overline{SHDN3}$ input. LDO#3 output is disabled with a logic low tied to the $\overline{SHDN3}$ pin. When shutdown, LDO#3 enters a low quiescent current state and the linear pass P-Channel MOSFET is off. The $\overline{RESET}$ output remains valid and is independent of $\overline{SHDN3}$.

3.7 Shutdown Control Input for V_{OUT4} ($\overline{SHDN4}$)

LDO#4 output is enabled when a logic high is applied to the $\overline{SHDN4}$ input. LDO#4 output is disabled with a logic low tied to the $\overline{SHDN4}$ pin. When shutdown, LDO#4 enters a low quiescent current state and the linear pass P-Channel MOSFET is off. The $\overline{RESET}$ output remains valid and is independent of $\overline{SHDN4}$.

3.8 SELECT Control Input for Setting V_{OUT3} and V_{OUT4} (SELECT34)

Input pin used to select the output voltage of LDO#3 and LDO#4. When SELECT is tied to V_{IN}, V_{OUT3} = V_{OUT4} = 2.8V. When SELECT is tied to GND, V_{OUT3} = V_{OUT4} = 1.8V. If the SELECT input is not connected, V_{OUT3} = V_{OUT4} = 2.5V.

3.9 Regulated Output Voltage #4 (V_{OUT4})

Output voltage selected by tri-state input SELECT34. Output can be set to 1.80V, 2.50V or 2.80V

3.10 Regulated Output Voltage #3 (V_{OUT3})

Output voltage selected by tri-state input SELECT34. Output can be set to 1.80V, 2.50V or 2.80V

3.11 Regulated Output Voltage #2 (V_{OUT2})

Output voltage selected by tri-state input SELECT12. Output can be set to 2.50V, 2.80V or 3.00V

3.12 Regulated Output Voltage #1 (V_{OUT1})

Output voltage selected by tri-state input SELECT12. Output can be set to 2.50V, 2.80V or 3.00V.

3.13 Shutdown Control Input for V_{OUT2} (SHDN2)

LDO#2 output is enabled when a logic high is applied to the SHDN2 input. LDO#2 output is disabled with a logic low tied to the SHDN2 pin. When shutdown, LDO#2 enters a low quiescent current state and the linear pass P-Channel MOSFET is off. The RESET output remains valid and is independent of SHDN2.

3.14 RESET Output (RESET)

Logic low output when voltage on V_{DET} pin is below the RESET Threshold Voltage. When the voltage on the V_{DET} pin rises above the RESET Threshold Voltage, the RESET output will remain low for the RESET Time-out Period and then transition to a logic high.

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4.0 DEVICE OVERVIEW

The TC1307 integrates four high performance linear Low Dropout Regulators and a microcontroller reset function.

As shown in the block diagram (Figure 4-3) using dashed lines, each LDO has an independent shutdown, error amplifier, P-MOS pass transistor and feedback divider resistors. All four LDOs share a common voltage reference. LDO output numbers one and two share a tri-state select input while LDO numbers three and four share a tri-state select input. The select input is used to program the LDO output voltage.

Also shown in the block diagram is the microcontroller reset monitor. The reset monitor voltage detect input is independent of the LDO input or output voltages.

4.1 Low Dropout Out Linear Regulators

4.1.1 OUTPUT

The TC1307 integrates four low drop out linear regulators. Each regulator has 150 mA output current capability. A minimum of 1 µF output capacitance is required on each of the LDOs for circuit stability. The output capacitor type can be ceramic, tantalum or aluminum. The esr range required for the output capacitor is 0 Ω to 2 Ω. To improve the dynamic performance of the LDO in cases where sudden input voltage changes or load current changes are present, larger capacitors can be used.

The output voltage of the LDO can be selected using the SELECT input pins. Table 4-1 summarizes how to select the desired LDO output voltage for V_{OUT1} and V_{OUT2}. Table 4-2 summarizes how to select the desired LDO output voltage for V_{OUT3} and V_{OUT4}.

SELECT12	V_{OUT1}	V_{OUT2}
GND	2.50V	2.50V
No Connect	2.80V	2.80V
V_{IN}	3.00V	3.00V

TABLE 4-1: *SELECT12 MODE settings.*

SELECT34	V_{OUT3}	V_{OUT4}
GND	1.80V	1.80V
No Connect	2.50V	2.50V
V_{IN}	2.80V	2.80V

TABLE 4-2: *SELECT34 MODE Settings.*

4.1.2 INPUT

The TC1307, like all low drop out linear regulators, requires a relatively low source impedance (< 10 Ω) tied to the V_{IN} pin of the device to ensure circuit stability. For battery applications or in applications that have long lead length from the input voltage source to the LDO V_{IN} pin, a minimum capacitance of 2.2 µF is recommended to lower the source impedance. For applications that have more than 1 µF of capacitance on the LDO outputs, higher input capacitance (4.7 µF) may be needed to ensure stability.

4.1.3 SHUTDOWN OPERATION

Each LDO output can be enabled and disabled using its respective shutdown input pin. For example, when the level on $\overline{SHDN1}$ is below the logic low level threshold (V_{IL}), LDO#1 output is disabled (P-Channel MOSFET is turned OFF). If all four shutdown inputs are below V_{IL}, the bandgap reference is turned off and the shutdown current is typically less than 0.1 µA. The LDO output will typically wake-up in 10 µs and the output will settle in approximately 40 µs when brought out of shutdown mode. See Figure 4-1 for timing definition. The microcontroller $\overline{RESET}$ output function is independent of all $\overline{SHDN}$ input pins.

4.2 Voltage Reset Monitor

The independent voltage reset output of the TC1307 can be used for low battery input voltage detect or microcontroller power on reset function. The voltage reset function monitors the voltage on the V_{DET} pin. The active low $\overline{RESET}$ output is capable of sourcing and sinking current (Push-Pull). When the voltage on the V_{DET} pin is below the 2.63V typical threshold, the $\overline{RESET}$ output pin is active low and capable of sinking 3.2 mA while holding the $\overline{RESET}$ output voltage below 0.4V. When the voltage on the V_{DET} pin rises above the 2.63V typical threshold, the $\overline{RESET}$ output will remain low for the $T_{\overline{RESET}}$ time period. After the $\overline{RESET}$ time out period, the $\overline{RESET}$ output voltage will transition to the high output state (> V_{DET}-1.5V when sourcing 800 µA), if the V_{DET} pin remains above the threshold voltage. The $\overline{RESET}$ output is current limited. The maximum source or sink current recommended for normal operation is 10 mA.

The $\overline{RESET}$ output will be driven low within 100 µsec of V_{DET} pin going below the $\overline{RESET}$ voltage threshold of 2.63V typical. The $\overline{RESET}$ output will remain valid for V_{DET} voltages greater than 1.0V. See Figure 4-2 for V_{DET} and $\overline{RESET}$ output timing diagram.

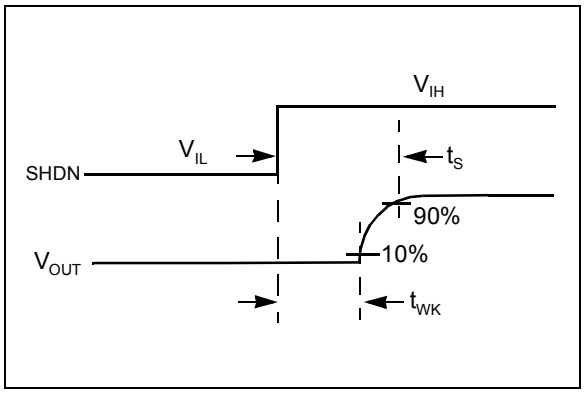


FIGURE 4-1: *Wake-up From $\overline{SHDN}$.*

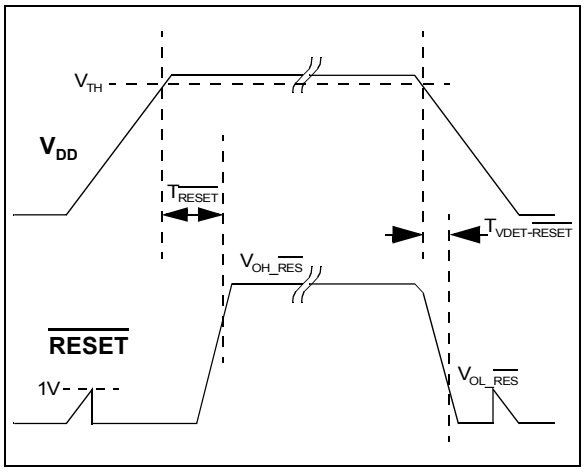


FIGURE 4-2: *$\overline{RESET}$ Timing Diagram.*

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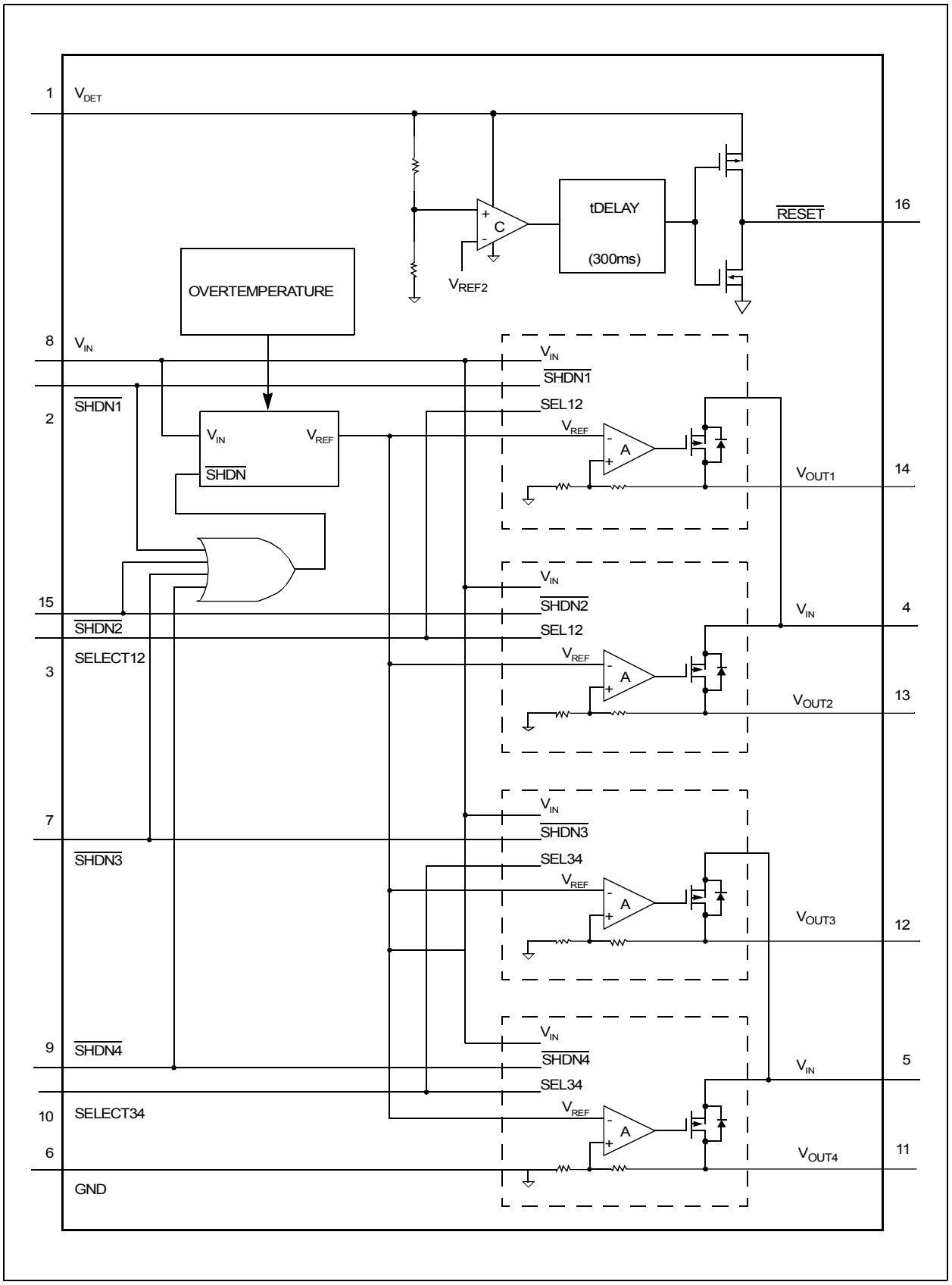


FIGURE 4-3: *TC1307 Block Diagram.*

5.0 APPLICATIONS

5.1 Load Partitioning

The TC1307 can be used to power two separate channels for a wide range of applications. Each channel can be turned ON and OFF independently of the other. In this example, the SELECT12 pin is tied to V_{IN} and the SELECT34 pin is tied to GND. The output voltages of V_{OUT1} and V_{OUT2} are 3.0V and the output voltage of V_{OUT3} and V_{OUT4} are 1.8V. If V_{OUT1} and V_{OUT3} were powering 1 Channel and V_{OUT2} and V_{OUT4} were powering an identical Channel, either Channel could be powered independent of the other Channel. The output voltage of V_{OUT1} is being monitored by the internal voltage detection circuit. When the output of V_{OUT1} is below the typical 2.63V threshold voltage, the $\overline{\text{RESET}}$ output will transition low.

5.2 Input Capacitor

Low input source impedance is necessary for the LDO to operate properly. When operating off of batteries or in applications with long lead length (>10”) between the input source and the LDO, some input capacitance is required. A minimum of 2.2 µF is recommended for most applications and the capacitor should be placed as close to the input of the LDO as practical (>0.2”). Larger input capacitors will help reduce the input impedance and further reduce any high frequency noise on the input and output of the LDO. If more than 1 µF of capacitance is used on the LDO outputs, a 4.7 µF input capacitor is recommended.

5.3 Output Capacitor

A minimum output capacitance of 1 µF for the TC1307 is required for stability. The esr requirements on the output capacitor are between 0 and 2 ohms. The output capacitor should be located as close to the LDO output as practical. Ceramic materials X7R and X5R have low temperature coefficients and are well within the acceptable esr range required. A typical 1 µF X5R 0805 capacitor has an esr of 50 milli-ohms. Larger output capacitors can be used with the TC1307 to improve dynamic behavior, noise and ripple rejection performance.

5.4 Power Dissipation

The internal power loading within the TC1307 is a function of input voltage, output voltage, output current, quiescent current and $\overline{\text{RESET}}$ output dissipation. For many applications the power dissipation within the linear P-Channel device can be used as a good approximation of total power dissipation. This is due to the low quiescent current consumed even when the LDO output is providing full load current (150 mA).

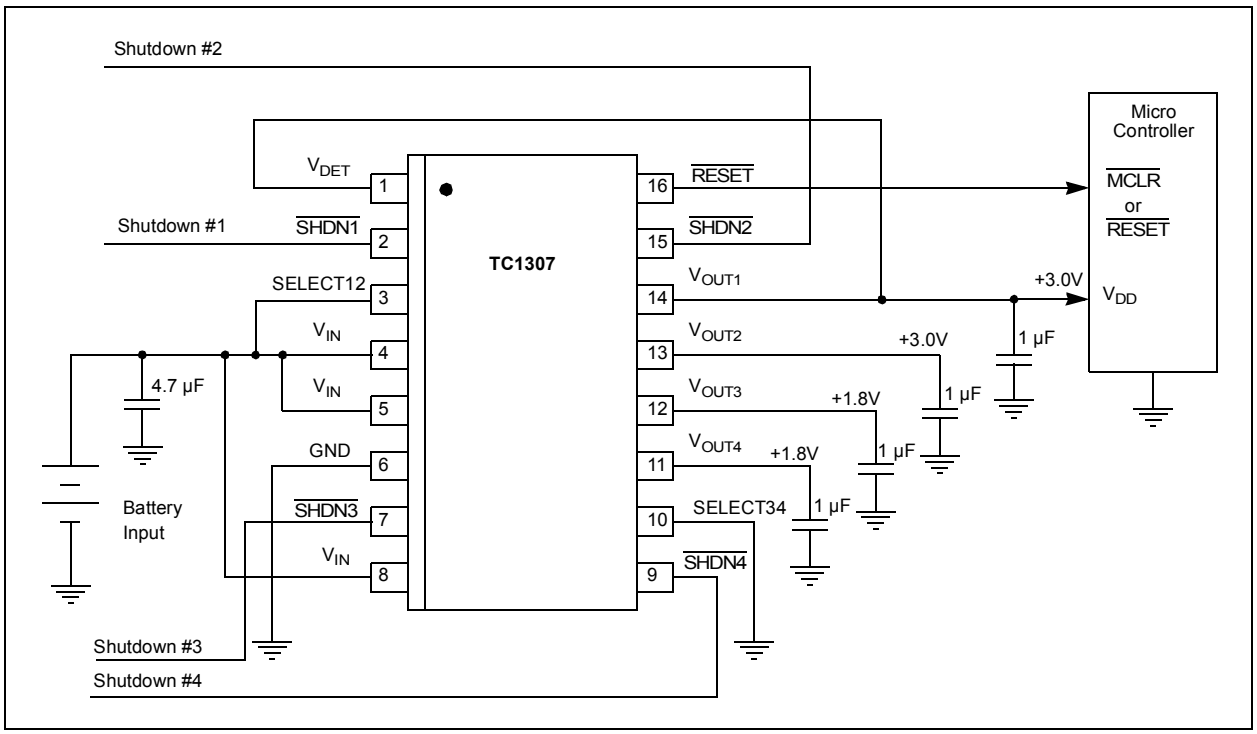


FIGURE 5-1: *Typical 4 Output with $\overline{\text{RESET}}$ Application.*

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5.4.1 P-CHANNEL LINEAR PASS DEVICE

$$P_{Linear} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$$

Where:

P_{Linear} = Power dissipated in the LDO P-Channel linear pass element.

$V_{IN(MAX)}$ = Maximum input voltage (V_{IN})

$V_{OUT(MAX)}$ = Minimum LDO output Voltage (V_{OUT})

$I_{OUT(MAX)}$ = Maximum LDO output current

5.4.2 QUIESCENT CURRENT

The quiescent current consumed by the TC1307 has two components. The quiescent current required to bias the LDO regulators and the quiescent current required to bias the voltage detection circuitry. To determine the power dissipation as a result of the total device quiescent current both the maximum input voltage on the V_{IN} and V_{DET} inputs should be used.

$$P_Q = V_{IN} \times I_{IN} + V_{DET} \times I_{DET}$$

Where:

P_Q = Power internal to the LDO as a result of internal biasing

V_{IN} = Input voltage

I_{IN} = Input current when all load currents = 0 mA

V_{DET} = Detect Input Voltage

I_{VDET} = Voltage detect input pin current

5.4.3 $\overline{\text{RESET}}$ OUTPUT

The power dissipation for the $\overline{\text{RESET}}$ output driver can be a result of the sinking current or sourcing current depending on the state of the output.

$$P_{RESET} = V_{OL} \times I_{SINK}$$

Where:

P_{RESET} = Power dissipated as a result of the RESET output.

V_{OL} = $\overline{\text{RESET}}$ low output voltage

I_{SINK} = $\overline{\text{RESET}}$ sink current

The power dissipation internal to the $\overline{\text{RESET}}$ output due to sourcing current can be calculated by using the following equation.

$$P_{RESET} = (V_{DET} - V_{SOURCE}) \times I_{SOURCE}$$

Where:

P_{RESET} = Power dissipation as a result of $\overline{\text{RESET}}$ output while in the high state

V_{DET} = Detect Voltage

V_{SOURCE} = $\overline{\text{RESET}}$ output pin voltage while in the high state

I_{SOURCE} = Output current being sourced

5.4.4 TOTAL INTERNAL POWER DISSIPATION

The total power dissipated within the TC1307 is the sum of the power dissipated in each of the four LDOs, the P_Q term and the P_{RESET} term (either sinking or sourcing). Because of the CMOS construction, the typical I_{IN} for the TC1307 is 220 µA. When operating at a maximum of 5V this results is a power dissipation of 1.2 milli-Watts. For most applications this is small compared to the LDO pass device power dissipation and can be neglected. The $P_{\overline{\text{RESET}}}$ term for a typical 3.2 mA sinking application will dissipate a maximum of 3.2 mA x 0.4V or 1.28 milli-Watts. A typical sourcing application of 800 µA will have a maximum 1.5V drop from the VDET voltage will dissipate a maximum of 800 µA x 1.5V or 1.2 milli-Watts. Again for most applications this is small compared to the LDO pass device power dissipation and can be neglected.

$$P_{TOTAL} = P_{Linear} + P_Q + P_{RESET}$$

5.4.5 MAXIMUM JUNCTION TEMPERATURE

The operating junction temperature (T_J) specified for the TC1307 is 125°C. To estimate the internal junction temperature of the TC1307, the total internal power dissipation (P_{TOTAL}) is multiplied by the thermal resistance from junction to ambient (θ_{JA}) of the device. The thermal resistance from junction to ambient for the QSOP 16-pin package is estimated at 112.4°C/W. The actual thermal resistance from junction to air can vary from application to application for the QSOP16 depending on board copper area, copper thickness, airflow and other external environmental factors.

$$T_{J(MAX)} = P_{TOTAL} \times \theta_{JA}$$

The maximum power dissipation capability for a package ($P_{D(MAX)}$) can be calculated given the junction to air thermal resistance and the maximum ambient temperature ($T_{A(MAX)}$) for the application. The following equation can be used to determine the package maximum internal power dissipation.

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{\theta_{JA}}$$

5.5 Typical Application

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation as a result of quiescent current and $\overline{\text{RESET}}$ output are small enough to be neglected.

Input Voltage:

V_{IN} = 3.1V to 4.1V

LDO Output Voltages and Currents:

V_{OUT1} = 3.0V

I_{IOUT1} = 100 mA

V_{OUT2} = 3.0V

I_{IOUT2} = 100 mA

V_{OUT3} = 1.8V

I_{IOUT3} = 60 mA

V_{OUT4} = 1.8V

I_{IOUT4} = 60 mA

Maximum Ambient Temperature:

$T_{A(MAX)}$= 50°C

Internal Power Dissipation:

Internal Power dissipation is the sum of the power dissipation for each LDO pass device.

$P_{LDO1} = (V_{IN(MAX)}-V_{OUT1(MIN)}) \times I_{OUT1(MAX)}$

P_{LDO1} = (4.1V - (0.975 x 3.0V)) x 100 mA

P_{LDO1} = 117.5 milli-Watts

P_{LDO2} = (4.1V - (0.975 x 3.0V)) x 100 mA

P_{LDO2} = 117.5 milli-Watts

P_{LDO3} = (4.1V - (0.975 x 1.8V)) x 60 mA

P_{LDO3} = (2.35V x 60 mA)

P_{LDO3} = 140.7 milli-Watts

P_{LDO4} = (4.1V - (0.975 x 1.8V)) x 60 mA

P_{LDO4} = 140.7 milli-Watts

$P_{TOTAL} = P_{LDO1} + P_{LDO2} + P_{LDO3} + P_{LDO4}$

P_{TOTAL} = 516.4 milli-Watts

Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to air (θ_{JA}) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface mount packages. The EIA/JEDEC specification is JESD51-7 “High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages”. The standard describes the test method and board specifications for measuring the thermal resistance from junction to case. The actual thermal resistance for a particular application can vary depending on many factors such as copper area and thickness. Refer to AN792 for more information regarding this subject.

$T_{JRISE} = P_{TOTAL} \times \theta_{JA}$

T_{JRISE} = 516.4 milli-Watts x 112.4°C/Watt

T_{JRISE} = 58.1°C

Junction Temperature Estimate

To estimate the internal junction temperature (T_J), the calculated junction temperature rise (T_{JRISE}) is added to the ambient or offset temperature ($T_{AMBIENT}$). For this example the worst case junction temperature is estimated below.

$T_J = T_{JRISE} + T_{AMBIENT}$

T_J =108.1°C

Maximum Package Power Dissipation

The maximum power dissipation capability for the TC1307 can be approximated by finding the maximum allowable temperature rise from junction to case and dividing that by the estimated thermal resistance of the application. For this example, the maximum allowable junction temperature rise is 125°C - 50°C or 75°C. By dividing 75°C by the estimated thermal resistance (112.4°C/Watt), the maximum allowable power dissipation is calculated to be 667.3 milli-Watts.

5.6 Device Protection

5.6.1 OVER CURRENT LIMIT

In the event of a faulted output load, the maximum current the LDO will permit to flow is limited internally. For each of the four LDO’s internal to the TC1307, the limit in the event of a short circuit will be 360 mA typical. This limit can be used to prevent damage to the circuit board or connectors. The over current protection for each LDO output is independent. For example, if LDO1 output is shorted to ground, the over current protection will limit the output current for LDO1. If the junction temperature does not rise above the typical 150°C thermal shutdown point the other three LDO outputs (LDO2, LDO3, LDO4) will remain within regulation.

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5.6.2 OVER TEMPERATURE PROTECTION

If the internal power dissipation within the TC1307 is excessive due to a faulted load or higher than specified line voltage, an internal temperature sensing element will prevent the junction temperature from exceeding approximately 150°C. If the junction temperature does exceed approximately 150°C, all LDO outputs will be disabled until the junction temperature cools to approximately 140°C, at which point the device will resume normal operation. The $\overline{\text{RESET}}$ output will continue to operate normally in the event of a thermal shutdown.

5.7 Recommended Physical Layout

Figure 5-2 represents a typical layout using the TC1307 16-pin QSOP package. C_1, C_2, C_3 and C_4 are 1 µF X5R 0603 ceramic output capacitors and C_{IN} is a 2.2 µF X5R 0805 ceramic capacitor. No other components are required for this quad output LDO with microcontroller reset function. Utilizing the highly integrated TC1307, the total board area required is less than 0.300 square inches.

For CMOS LDOs, the GND or quiescent current is small when compared to the maximum output current capability. The GND pins connected to the TC1307 do not carry high current and it is not necessary for them to be wide. It is more important for the GND pins to be connected to a quiet circuit ground. Noise on the GND pins may result in noise at the output of the LDO. In Figure 5-2, a ground plane is used to connect the TC1307 Pins to the GND plane that has the V_{OUT} capacitor return tied to it. For applications that have ripple voltage on the input, the C_{IN} capacitor return can be separated from the ground plane by running a trace from the capacitor to the ground plane. This impedance will help to reduce the noise on the output of the LDO.

The output voltage regulation uses the GND pins of the TC1307 as the return path for the internal bandgap reference. Any voltage drops between the load and the respective V_{OUT} pin and GND pin will show up as regulation losses. It is important to size the V_{OUT} and GND conductors for minimum voltage drops. The maximum application load current will determine how large these traces should be. As shown in Figure 5-2, a ground plane can be used minimize the trace resistance from the load to the TC1307 GND pin.

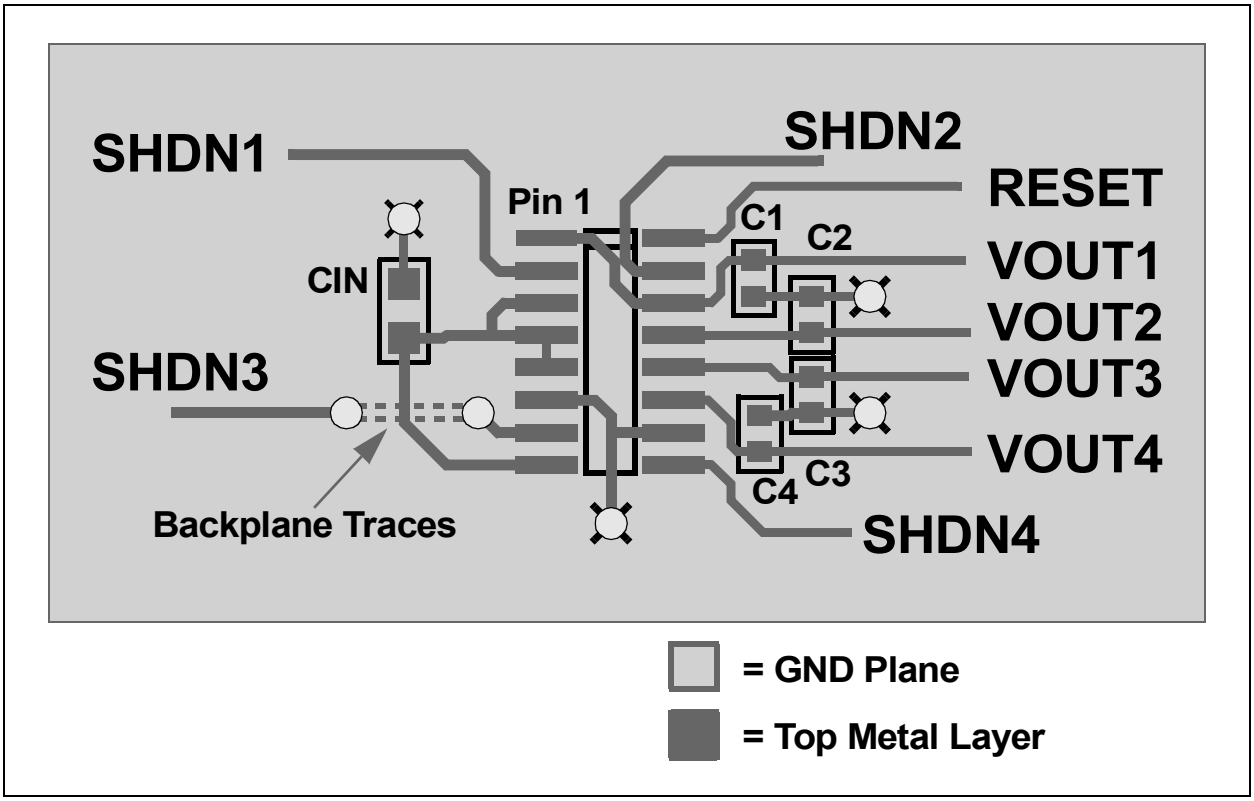
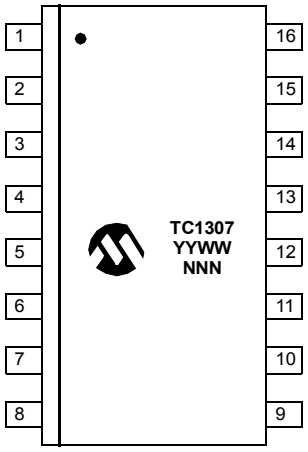


FIGURE 5-2: *TC1307 Typical Layout.*

6.0 PACKAGING INFORMATION

6.1 Package Marking Information



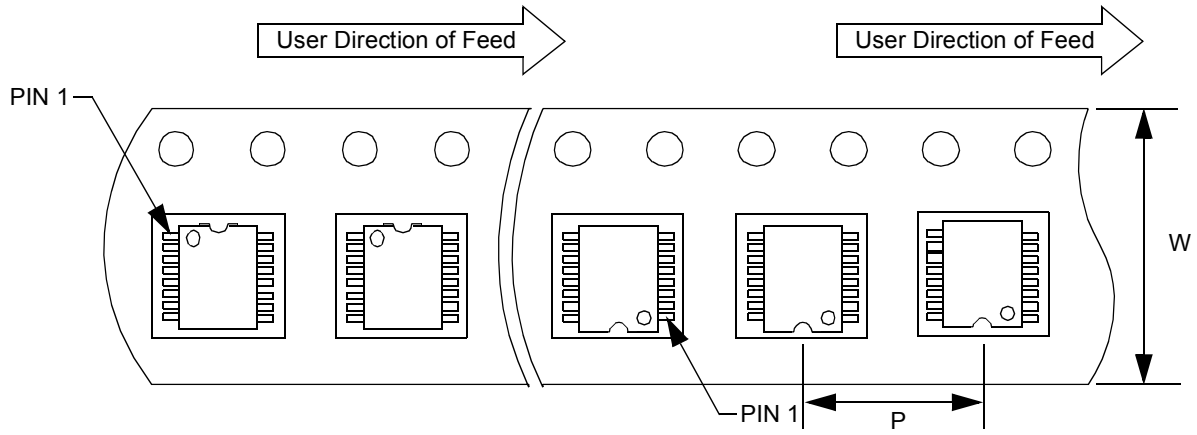
Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

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6.2 Taping Form

Component Taping Orientation for 16-Pin QSOP (Narrow) Devices



Standard Reel Component Orientation
for TR Suffix Device

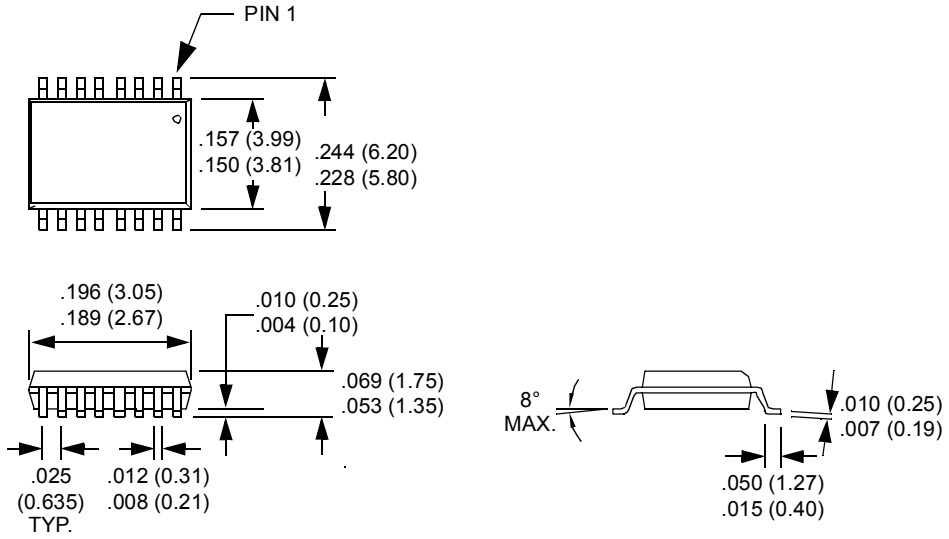
Reverse Reel Component Orientation
for RT Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size:

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
16-Pin QSOP (N)	12 mm	8 mm	2500	13 in.

6.3 Packaging Information

16-Pin QSOP (Narrow)



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PART NO.	X	-XX	X	X	X	XX
Device	Threshold Voltage	LDO Output Voltages	Temp. Range	Packaging Type	# Leads	Tape & Reel

Device:	TC1307:	4-Channel LDO w/Select Mode, Shutdown and Independent Reset
Threshold Voltage:	R =	2.63V
LDO Output Voltages:	XY =	1.8V
	XY =	2.5V
	XY =	2.8V
	XY =	3.0V
Temperature Range:	V =	-40°C to +125°C (Extended)
Package:	QR =	QSOP Package, 16-lead
Tape and Reel:	TR =	Tape and Reel

Examples:

a) TC1307R-XYVQRTR

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