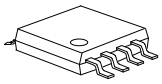
LION BATTERY PROTECTION IC FOR 2-SERIAL, 3-SERIAL, OR 4-SERIAL-CELL PACK (SECONDARY PROTECTION)



TSSOP-8

■ DESCRIPTION

The UTC **UB264B** Series is secondary protection IC for 2-, 3-, or 4-Cell lithium-ion rechargeable battery packs, and incorporates a high-accuracy voltage detection circuit.

The UTC **UB264B** Series also includes a high accuracy delay circuit for over voltage detection time without external capacitors.

■ FEATURES

* High-accuracy voltage detection circuit for each cell
* Overcharge detection voltage n (n=1 to 4): 4.30V to 4.80V (in 50mV steps)
* Overcharge hysteresis voltage n (n=1 to 4): -0.52V±0.21V, −0.39V±0.16V, −0.26V±0.11V, −0.13V±0.06V, None
* Delay times for overcharge detection can be set by an internal circuit without external capacitors
* Output latch function after overcharge detection
* CMOS output active “H”
* Wide operating voltage range 3.6V to 24V
* Wide operating temperature range −40°C to +85°C
* Low current consumption: 2.5μA typ. (+25° C) at 3.5V for each cell

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UB264BL-P08-R	UB264BG-P08-R	TSSOP-8	Tape Reel

Note: xx: SERIAL CODE, refer SERIAL CODE LIST.

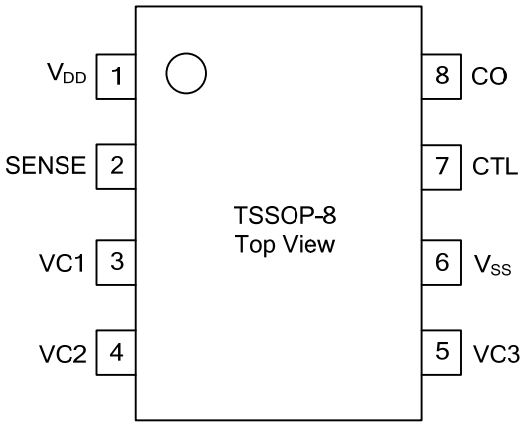
UB264BG-xx-P08-R

(1)Packing Type
(2)Package Type
(3)SERIAL CODE
(4)Halogen Free

(1) R: Tape Reel
(2) P08: TSSOP-8
(3) xx: Refer to SERIAL CODE LIST
(4) G: Halogen Free, L: Lead Free

Copyright © 2012 Unisonic Technologies Co., Ltd

■ PIN CONFIGURATION



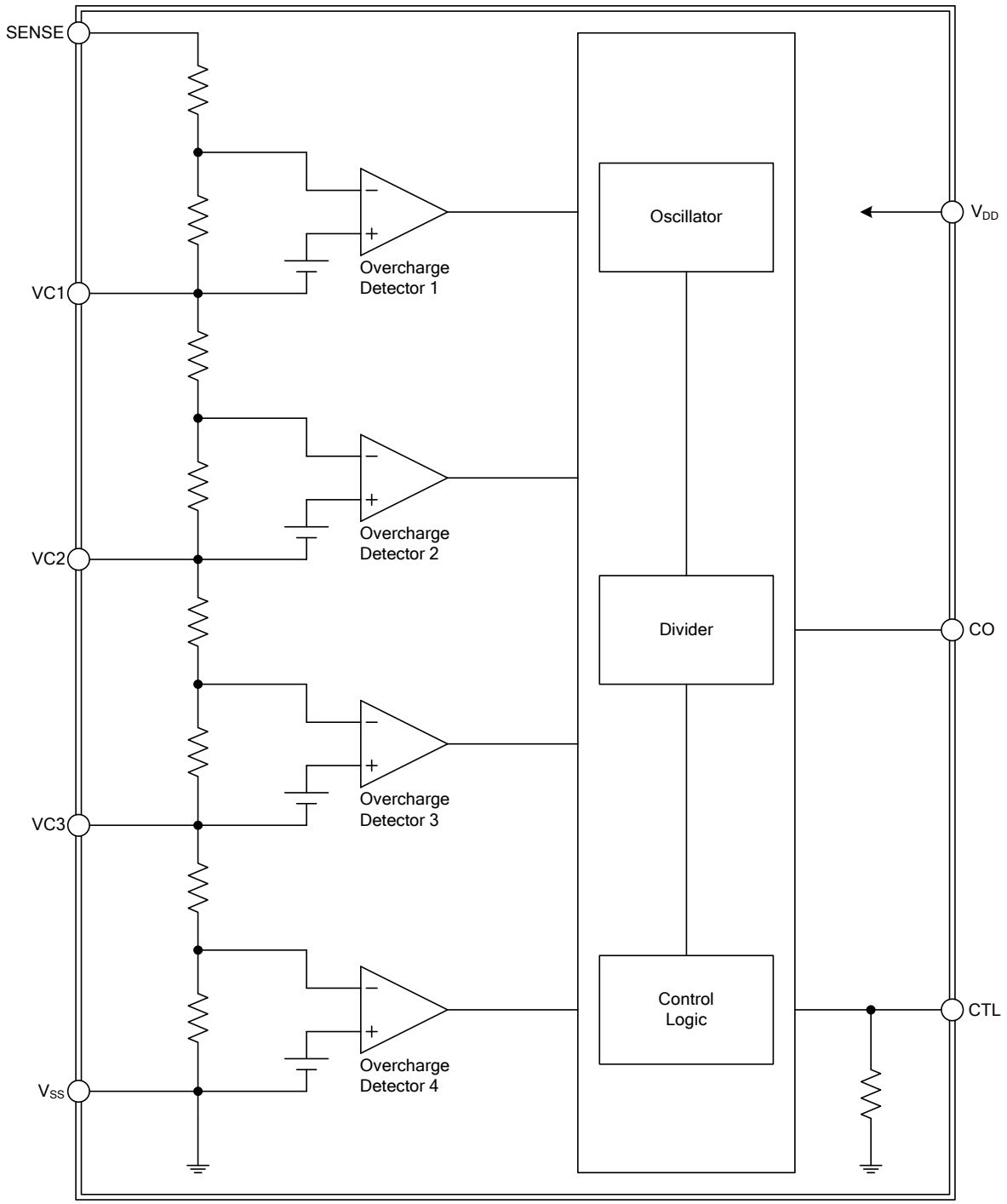
■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{DD}	Positive power input pin
2	SENSE	Positive voltage connection pin of battery 1
3	VC1	Negative voltage connection pin of battery 1 Positive voltage connection pin of battery 2
4	VC2	Negative voltage connection pin of battery 2 Positive voltage connection pin of battery 3
5	VC3	Negative voltage connection pin of battery 3 Positive voltage connection pin of battery 4
6	V_{SS}	Negative power input pin Negative voltage connection pin of battery 4
7	CTL	Overcharge detection latch reset pin
8	CO	FET gate connection pin for charge

■ SERIAL CODE LIST

MODEL	CODE	OVERCHARGE DETECTION VOLTAGE [V_{CU}](V)	OVERCHARGE HYSTERSIS VOLTAGE [V_{HC}](V)	OVERCHARGE DETECTION DELAY TIME [t_{CU}](S)	OVERCHARGE RELEASE DELAY TIME [t_{CL}](mS)	OUTPUT FORM
UB264B	AA	4.45±0.050	−0.39±0.16	4.0±1.0	60.0±20.0	CMOS output active “H”
	AB	4.35±0.050	−0.39±0.16	4.0±1.0	60.0±20.0	CMOS output active “H”
	AC	4.50±0.050	−0.39±0.16	4.0±1.0	60.0±20.0	CMOS output active “H”
	AD	4.35±0.050	−0.39±0.16	2.0±0.5	30.0±10.0	CMOS output active “H”
	AE	4.30±0.050	−0.39±0.16	4.0±1.0	60.0±20.0	CMOS output active “H”
	AF	4.45±0.050	−0.39±0.16	2.0±0.5	30.0±10.0	CMOS output active “H”
	AG	4.30±0.050	−0.39±0.16	2.0±0.5	30.0±10.0	CMOS output active “H”
	AH	4.40±0.050	−0.39±0.16	4.0±1.0	60.0±20.0	CMOS output active “H”

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage Between V_{DD} And V_{SS}	V_{DS}	V_{SS} −0.3 ~ V_{SS}+26	V
Input Pin Voltage	V_{IN}	V_{SS} −0.3 ~ V_{DD}+0.3	V
CO Output Pin Voltage	V_{CO}	V_{SS} −0.3 ~ V_{DD}+0.3	V
Power Dissipation (Note 2)	P_D	650	mW
Operation Ambient Temperature	T_{opr}	−40 ~ +85	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. When mounted on printed circuit board

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DETECTION VOLTAGE						
Overcharge Detection Voltage n (n = 1, 2, 3, 4)	V_{CUn}	4.30 ~ 4.80 V, adjustable	V_{CUn}− 0.050	V_{CUn}	V_{CUn}+ 0.050	V
Overcharge Hysteresis Voltage n (n = 1, 2, 3, 4)	V_{HCn}	V_{HCn}=−0.52 ±0.21V, −0.39 ±0.16V, −0.26 ±0.11V, −0.13 ±0.06V, None		V_{HCn}		V
DELAY TIME						
Overcharge Detection Delay Time	t_{CU}		3.0	4.0	5.0	s
		For AD, AF and AG products	1.5	2.0	2.5	
Overcharge Release Delay Time	t_{CL}		40	60	80	ms
		For AD, AF and AG products	20	30	40	
Overcharge Timer Reset Delay Time	t_{TR}		10	15	20	ms
		For AD, AF and AG products	5	7.5	10	
Transition Time To Test Mode(Note1)	t_{TST}		40	60	80	ms
		For AD, AF and AG products	20	30	40	
CTL Pin Response Time	t_{CTL}				3.0	ms
INPUT VOLTAGE						
Operating Voltage Between V_{DD} And V_{SS}	V_{DSOP}		3.6		24	V
CTL Input “H” Voltage	V_{CTLH}		V_{DD}× 0.95			V
CTL Input “L” Voltage	V_{CTLL}				V_{DD}× 0.4	V
INPUT CURRENT						
Current Consumption During Operation	I_{OPE}	V1=V2=V3=V4=3.5V		2.5	10	μA
Current Consumption During Overdischarge	I_{OPED}	V1=V2=V3=V4=2.3V		2.0	10	μA
SENSE Pin Current	I_{SENSE}	V1=V2=V3=V4=3.5V		1.5	6.0	μA
VC1 Pin Current	I_{VC1}	V1=V2=V3=V4=3.5V	-0.5	0	0.5	μA
VC2 Pin Current	I_{VC2}	V1=V2=V3=V4= 3.5 V	-0.5	0	0.5	μA
VC3 Pin Current	I_{VC3}	V1=V2=V3=V4=3.5 V	-0.5	0	0.5	μA
CTL Pin “H” Current	I_{CTLH}	V1=V2=V3=V4=3.5 V, V_{CTL}=V_{DD}	1.0	1.5	2.0	μA
CTL Pin “L” Current	I_{CTLL}	V1=V2=V3=V4=3.5 V, V_{CTL}=0 V	-0.1			μA
OUTPUT CURRENT						
CO Pin Sink Current	I_{COL}	V_{COP}=V_{SS}+0.5V	0.4			mA
CO Pin Source Current	I_{COH}	V_{COP}=V_{DD}−0.5V	20			μA

Note: 1. Test conditions: V1=V2= V3=V4=3.5 V, V_{DD} ≥ V_{SENSE} + 8.5V.

■ OPERATING

1. Overcharge Detection

Under normal conditions, when the voltage of any one cell battery exceeds the overcharge detection voltage (V_{CU}) during charging, and after the state is retained for the overcharge detection delay time (t_{CU}), CO will become “H”. This state is called overcharge. Attaching FET to the CO pin provides charge control and a second protection.

Only the voltage of all the batteries decreases below the total of the overcharge detection voltage (V_{CU}) and the overcharge hysteresis voltage (V_{HC}) and the state is retained for the overcharge release delay time (t_{CL}) or longer, the overcharge status is released; however, CO stays at “H”. When the CTL pin is switched from “L” to “H”, CO becomes “L”.

2. Overcharge Timer Reset

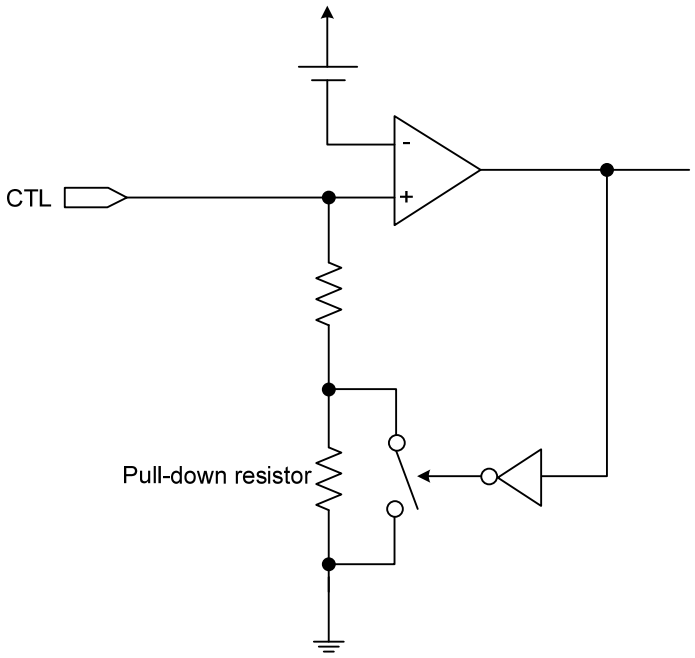
When an overcharge release noise that forces the voltage of the battery temporarily below the overcharge detection voltage (V_{CU}) is input during the overcharge detection delay time (t_{CU}) from when V_{CU} is exceeded to when charging is stopped, t_{CU} is continuously counted if the time the overcharge release noise persists is shorter than the overcharge timer reset delay time (t_{TR}). Under the same conditions, if the time the overcharge release noise persists is t_{TR} or longer, counting of t_{CU} is reset once. After that, when V_{CU} has been exceeded, counting t_{CU} resumes.

3. CTL Pin

The CTL pin is used to control the output voltage of the CO pin. In the UTC **UB264B** Series, when the CTL pin is switched from “L” to “H”, a reset signal is output to the overcharge detection latch and CO becomes “L”.

CTL PIN	CO PIN
“H”	Without latch
Open	Normal state (Note 1)
“L”	Normal state (Note 1)
“L”→ “H”	Latch reset (Note 2)
“H” →“L”	-

Notes: 1. The state is controlled by the overcharge detection circuit.
2. Latch reset becomes effective when the voltages of all the batteries are lower than the total of the overcharge detection voltage (V_{CU}) and the overcharge hysteresis voltage (V_{HC}) and the overcharge release delay time (t_{CL}) has elapsed.

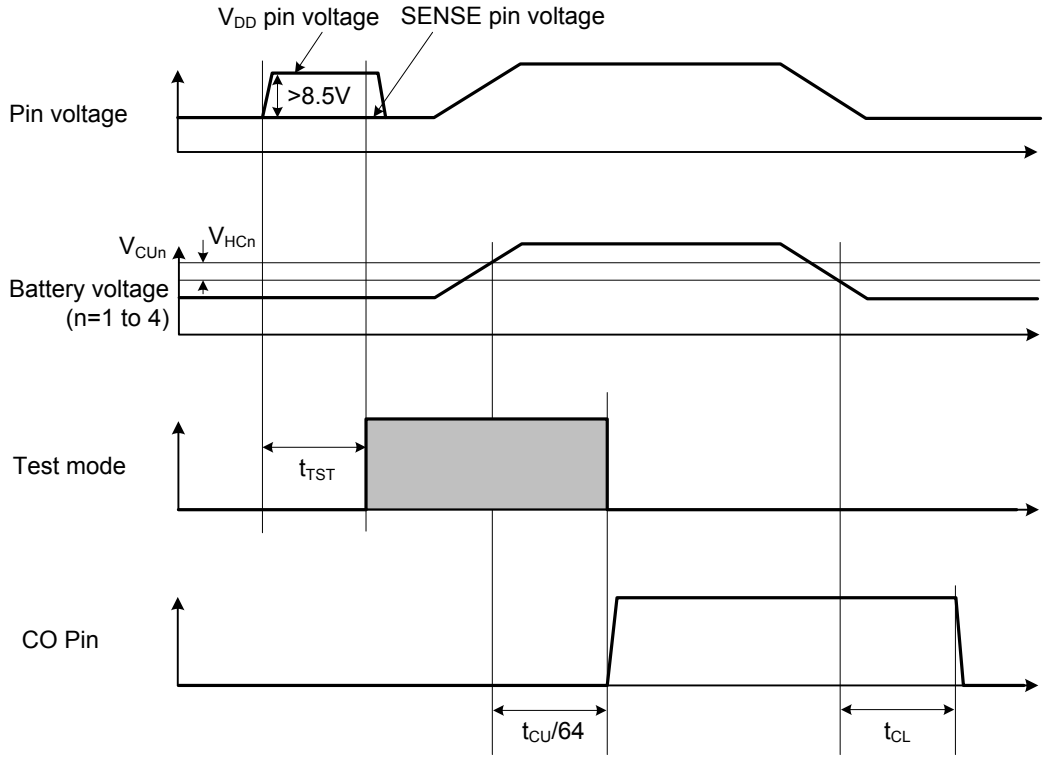


■ OPERATING(Cont.)

Notes: 1. The reverse voltage “H” to “L” or “L” to “H” of CTL pin is V_{DD} pin voltage −2.8 V (Typ.), does not have the hysteresis.
2. Since the CTL pin implements high resistance of 8MΩ to 12MΩ for pull down, be careful of external noise application. If an external noise is applied, CO may become “H”. Perform thorough evaluation using the actual application.
3. In the UTC UB264B Series, when the CTL pin is open or “L”, CO latches “H”. When the V_{DD} pin voltage is decreased to the UVLO voltage of 2 V (Typ.) or lower, the latch is reset.

4. Test Mode

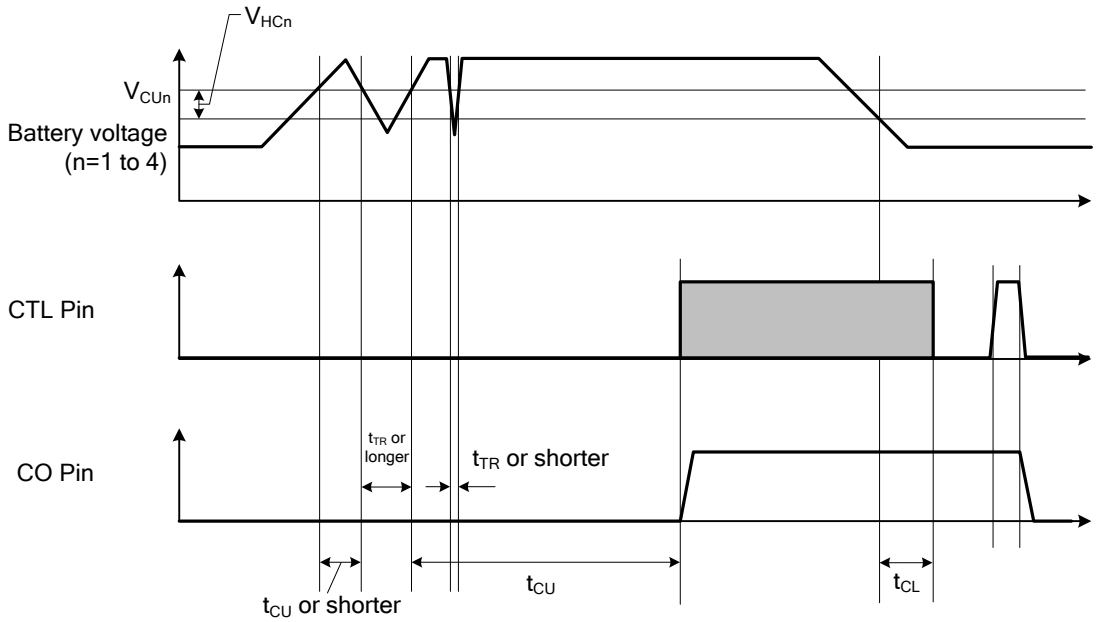
In the UTC **UB264B** Series, the overcharge detection delay time (t_{CU}) can be shortened by entering the test mode. The test mode can be set by retaining the V_{DD} pin voltage 8.5 V or more higher than the SENSE pin voltage for at least 80ms (V1=V2=V3=V4=3.5 V, Ta=25°C). The status is retained by the internal latch and the test mode is retained even if the V_{DD} pin voltage is decreased to the same voltage as that of the SENSE pin. When CO becomes “H” when the delay time has elapsed after overcharge detection, the latch for retaining the test mode is reset and the UTC **UB264B** Series exits from the test mode.



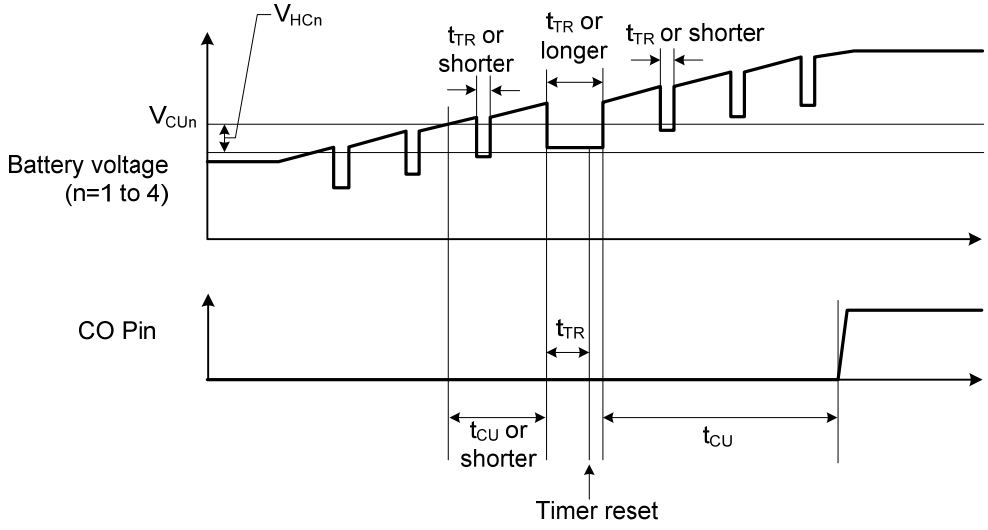
Notes: 1. When the V_{DD} pin voltage is decreased to lower than the UVLO voltage of 2 V (Typ.), the UTC UB264B Series returns to the normal mode.
2. Set the test mode when no batteries are overcharged.
3. The overcharge release delay time (t_{CL}) is not shortened in the test mode.
4. The overcharge timer reset delay time (t_{TR}) is not shortened in the test mode.

■ TIMING CHARTS

1. Overcharge Detection Operation

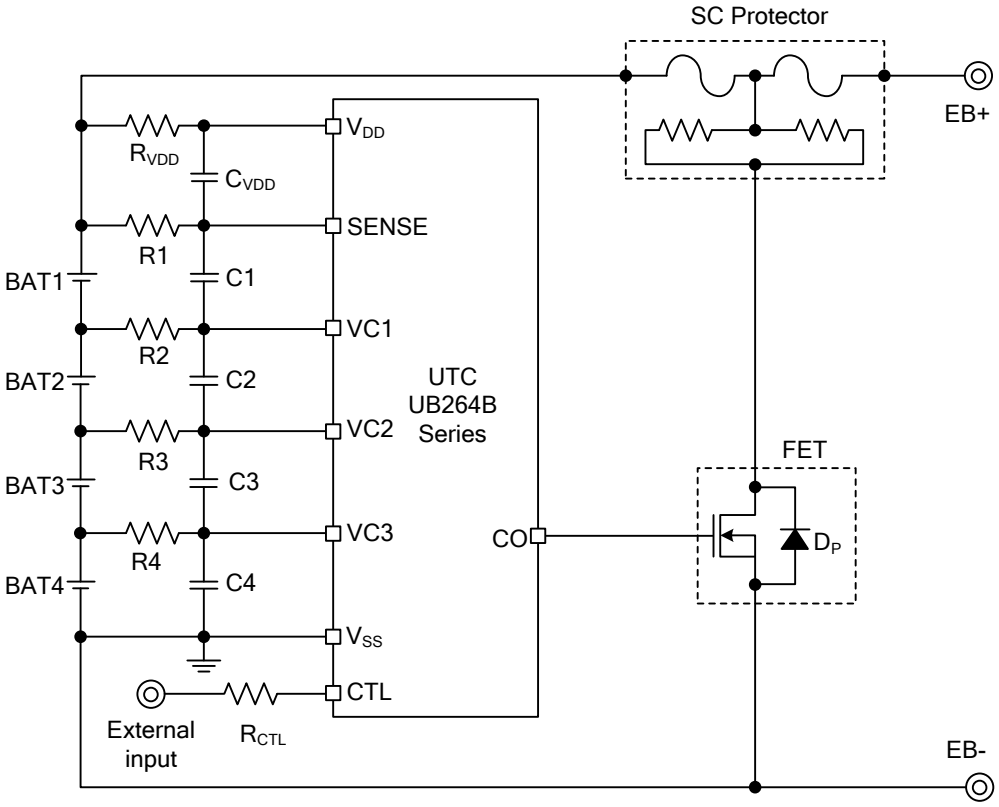


2. Overcharge Timer Reset Operation

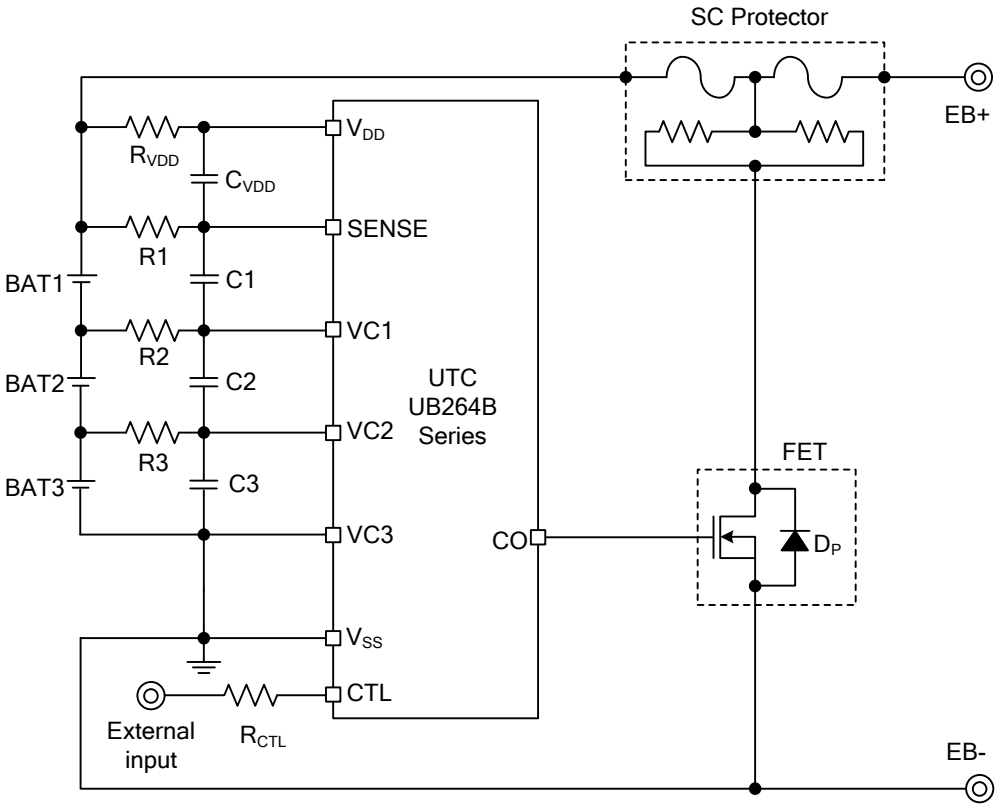


■ TYPICAL APPLICATION CIRCUIT

1. 4-serial cell

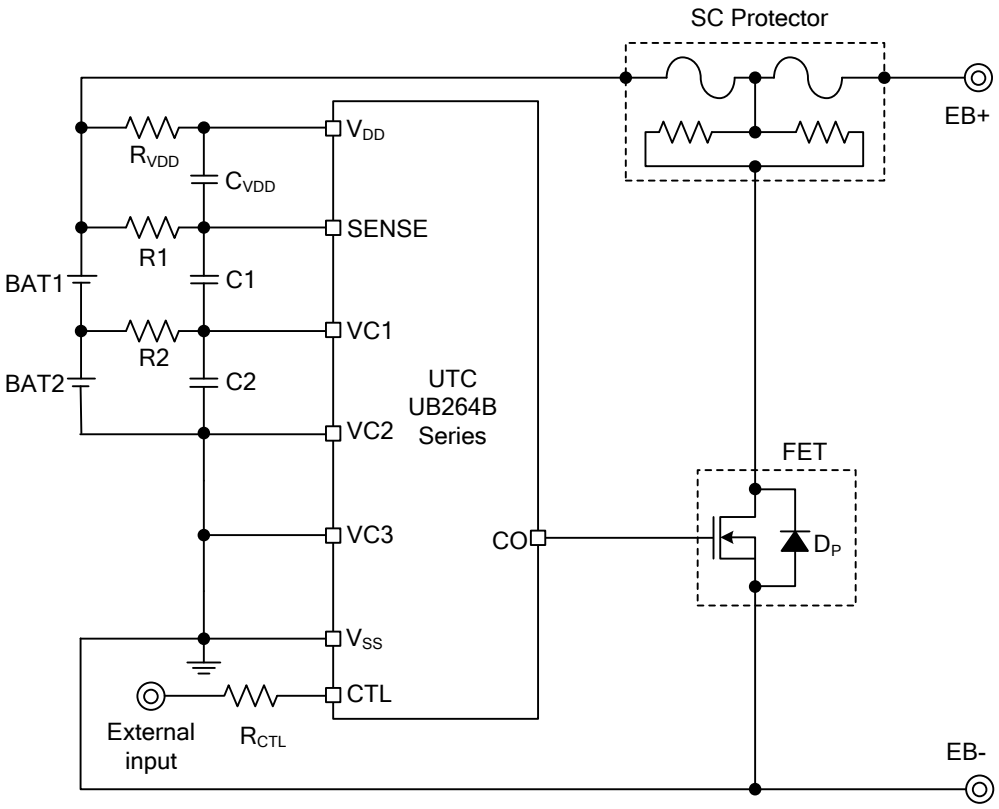


2. 3-serial cell



■ TYPICAL APPLICATION CIRCUIT(Cont.)

3. 2-serial cell



Constants for External Components

NO.	PART	MIN	TYP	MAX	UNIT
1	R1 to R4	0.1	1	10	KΩ
2	C1 to C4, C_{VDD}	0.01	0.1	1	μF
3	R_{VDD}	50	100	500	Ω
4	R_{CTL}	0	100	500	Ω

Notes:
1. the examples of connection shown above and the constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
2. Set the same constants to R1 to R4 and to C1 to C4 and C_{VDD}.
3. Set R_{VDD}, C1 to C4 and C_{VDD} so that the condition (R_{VDD}) × (C1 to C4, C_{VDD}) ≥ 5×10^{-6} is satisfied.
4. T Set R1 to R4, C1 to C4, and C_{VDD} so that the condition (R1 to R4) × (C1 to C4, C_{VDD}) ≥ 1×10^{-4} is satisfied.
5. In some application circuits, even if an overcharged battery is not included, the order of connecting batteries may be restricted to prevent transient output of CO detection pulses when the batteries are connected. Perform thorough evaluation with the actual application circuit.
6. Since “H” may be output at CO transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.
7. Before the battery connection, short-circuit the battery side pins R_{VDD} and R1.
8. In the UTC UB264B Series, normally input “L” to the external input, and input “H” when releasing the latch that maintains CO at “H” after overcharge detection.

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.