Discontinued Product

This version: Feb. 23. 1999

OKI Semiconductor

MSC23136D/DL-xxBS10/DS10

1,048,576-word x 36-bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

DESCRIPTION

The MSC23136D/DL-xxBS10/DS10 is a fully decoded, 1,048,576-word x 36-bit CMOS dynamic random access memory module composed of eight 4Mb DRAMs in SOJ packages and two 2Mb DRAMs in SOJ packages mounted with ten decoupling capacitors on a 72-pin glass epoxy single-inline package. This module supports any application where high density and large capacity of storage memory are required. The MSC23136DL (the low-power version) is specially designed for lower-power applications.

FEATURES

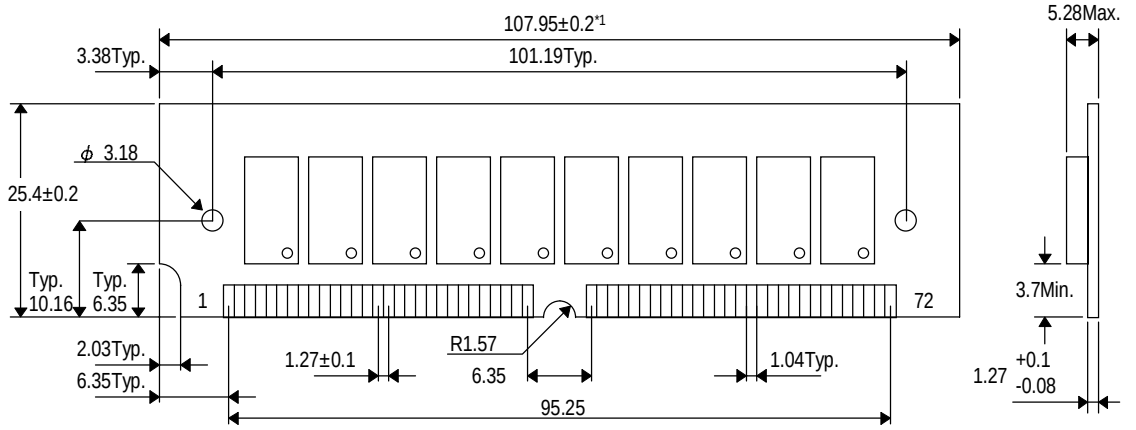
· 1,048,576-word x 36-bit organization
· 72-pin socket insertable module
  MSC23136D/DL-xxBS10 : Gold tab
  MSC23136D/DL-xxDS10 : Solder tab
· Single +5V supply ± 10% tolerance
· Input : TTL compatible
· Output : TTL compatible, 3-state
· Refresh : 1024cycles/16ms (1024cycles/128ms: L-version)
· /CAS before /RAS refresh, hidden refresh, /RAS only refresh capability
· Fast page mode capability
· Multi-bit test mode capability

PRODUCT FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Operating(Max.)	Standby(Max.)
MSC23136D/DL-60BS10/DS10	60ns	30ns	15ns	110ns	4840mW	55mW/ 9.9mW(L-version)
MSC23136D/DL-70BS10/DS10	70ns	35ns	20ns	130ns	4290mW	

MODULE OUTLINE

MSC23136D/DL-xxBS10/DS10 (Unit : mm)



*1 The common size difference of the board width 12.5mm of its height is specified as ±0.2.
The value above 12.5mm is specified as ±0.5.

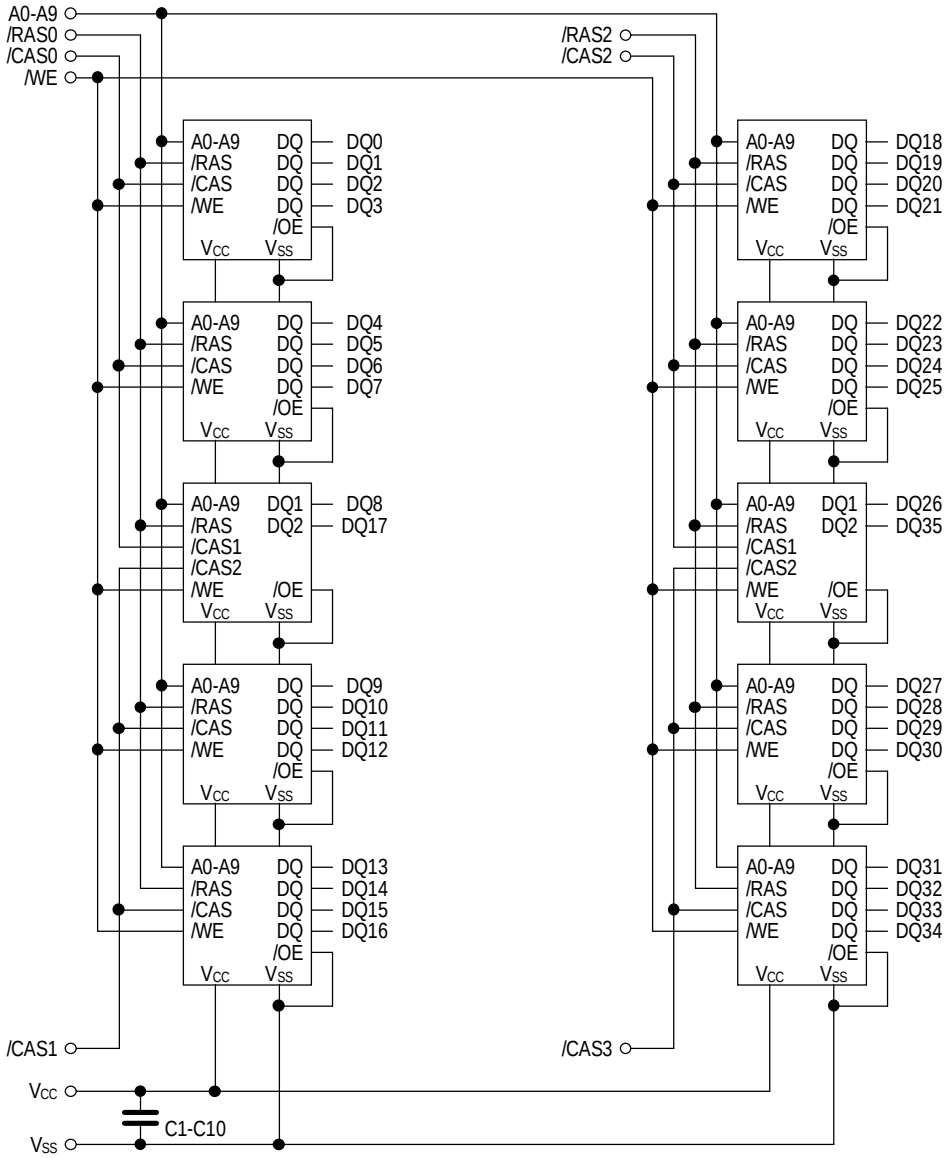
PIN CONFIGURATION

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V_{SS}	57	DQ13
4	DQ1	22	DQ5	40	/CAS0	58	DQ31
5	DQ19	23	DQ23	41	/CAS2	59	V_{CC}
6	DQ2	24	DQ6	42	/CAS3	60	DQ32
7	DQ20	25	DQ24	43	/CAS1	61	DQ14
8	DQ3	26	DQ7	44	/RAS0	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	V_{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	/WE	65	DQ16
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	/RAS2	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V_{SS}

Presence Detect Pins

Pin No.	Pin Name	MSC23136D/DL -60BS10/DS10	MSC23136D/DL -70BS10/DS10
67	PD1	V_{SS}	V_{SS}
68	PD2	V_{SS}	V_{SS}
69	PD3	NC	V_{SS}
70	PD4	NC	NC

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(Ta = 25°C)

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	10	W
Operating Temperature	T_{OPR}	0 to +70	°C
Storage Temperature	T_{STG}	-40 to +125	°C

Recommended Operating Conditions

(Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	6.5	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

Capacitance

(V_{CC} = 5V ± 10%, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	C_{IN1}	-	70	pF
Input Capacitance (/WE)	C_{IN2}	-	80	pF
Input Capacitance (/RAS0, /RAS2)	C_{IN3}	-	43	pF
Input Capacitance (/CAS0- /CAS3)	C_{IN4}	-	24	pF
I/O Capacitance (DQ0 - DQ35)	C_{DQ}	-	13	pF

Note: Capacitance measured with Boonton Meter.

DC Characteristics

(V_{CC} = 5V ± 10%, Ta = 0°C to +70°C)

Parameter	Symbol	Condition		MSC23136D/DL -60BS10/DS10		MSC23136D/DL -70BS10/DS10		Unit	Note
				Min.	Max.	Min.	Max.		
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 6.5V: All other pins not under test = 0V		-100	100	-100	100	µA	
Output Leakage Current	I_{LO}	Data out is disable 0V ≤ V_{OUT} ≤ 5.5V		-10	10	-10	10	µA	
Output High Voltage	V_{OH}	I_{OH} = -5.0mA		2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2mA		0	0.4	0	0.4	V	
Average Power Supply Current (Operating)	I_{CC1}	/RAS cycling, /CAS cycling, t_{RC} = min.		-	880	-	780	mA	1, 2
Power supply current (Standby)	I_{CC2}	/RAS = V_{IH} /CAS = V_{IH}	TTL	-	20	-	20	mA	1
			MOS	-	10	-	10	mA	1
				-	1.8	-	1.8	mA	1, 5
Average Power Supply Current (/RAS only refresh)	I_{CC3}	/RAS cycling, /CAS = V_{IH}, t_{RC} = min.		-	880	-	780	mA	1, 2
Average Power Supply Current (/CAS before /RAS refresh)	I_{CC6}	t_{RC} = min.		-	880	-	780	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	/RAS = V_{IL}, /CAS cycling, t_{PC} = min.		-	680	-	590	mA	1, 3
Average Power Supply Current (Battery Backup)	I_{CC10}	t_{RC} = 125µs, /CAS before /RAS cycling		-	2.8	-	2.8	mA	1, 4, 5

Notes: 1. I_{CC} is dependent on output loading and cycles rates. Specified values are obtained with the output open.
2. Address can be changed once or less while /RAS = V_{IL}.
3. Address can be changed once or less while /CAS = V_{IH}.
4. V_{CC} - 0.2V ≤ V_{IH} ≤ 6.5V, - 1.0V ≤ V_{IL} ≤ 0.2V.
5. L-version.

AC Characteristics (1/2)

(V_{CC} = 5V ± 10%, Ta = 0°C to +70°C) Note: 1, 2, 3, 9, 10

Parameter	Symbol	MSC23136D/DL -60BS10/DS10		MSC23136D/DL -70BS10/DS10		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	-	130	-	ns	
Fast Page Mode Cycle Time	t_{PC}	40	-	45	-	ns	
Access Time from /RAS	t_{RAC}	-	60	-	70	ns	4, 5, 6
Access Time from /CAS	t_{CAC}	-	15	-	20	ns	4, 5
Access Time from Column Address	t_{AA}	-	30	-	35	ns	4, 6
Access Time from /CAS Precharge	t_{CPA}	-	35	-	40	ns	4
Output Low Impedance Time from /CAS	t_{CLZ}	0	-	0	-	ns	4
/CAS to Data Output Buffer Turn-off Delay Time	t_{OFF}	0	15	0	20	ns	7
Transition Time	t_T	3	50	3	50	ns	3
Refresh Period	t_{REF}	-	16	-	16	ms	
Refresh Period (L-version)	t_{REF}	-	128	-	128	ms	
/RAS Precharge Time	t_{RP}	40	-	50	-	ns	
/RAS Pulse Width	t_{RAS}	60	10K	70	10K	ns	
/RAS Pulse Width (Fast Page Mode)	t_{RASP}	60	100K	70	100K	ns	
/RAS Hold Time	t_{RSH}	15	-	20	-	ns	
/CAS Precharge Time (Fast Page Mode)	t_{CP}	10	-	10	-	ns	
/CAS Pulse Width	t_{CAS}	15	10K	20	10K	ns	
/CAS Hold Time	t_{CSH}	60	-	70	-	ns	
/CAS to /RAS Precharge Time	t_{CRP}	5	-	5	-	ns	
/RAS Hold Time from /CAS Precharge	t_{RHCP}	35	-	40	-	ns	
/RAS to /CAS Delay Time	t_{RCD}	20	45	20	50	ns	5
/RAS to Column Address Delay Time	t_{RAD}	15	30	15	35	ns	6
Row Address Set-up Time	t_{ASR}	0	-	0	-	ns	
Row Address Hold Time	t_{RAH}	10	-	10	-	ns	
Column Address Set-up Time	t_{ASC}	0	-	0	-	ns	
Column Address Hold Time	t_{CAH}	15	-	15	-	ns	
Column Address Hold Time from /RAS	t_{AR}	50	-	55	-	ns	
Column Address to /RAS Lead Time	t_{RAL}	30	-	35	-	ns	
Read Command Set-up Time	t_{RCS}	0	-	0	-	ns	
Read Command Hold Time	t_{RCH}	0	-	0	-	ns	8
Read Command Hold Time referenced to /RAS	t_{RRH}	0	-	0	-	ns	8

AC Characteristics (2/2)

(V_{CC} = 5V ± 10%, Ta = 0°C to +70°C) Note: 1, 2, 3, 9, 10

Parameter	Symbol	MSC23136D/DL -60BS10/DS10		MSC23136D/DL -70BS10/DS10		Unit	Note
		Min.	Max.	Min.	Max.		
Write Command Set-up Time	t_{WCS}	0	-	0	-	ns	
Write Command Hold Time	t_{WCH}	10	-	10	-	ns	
Write Command Hold Time from /RAS	t_{WCR}	45	-	50	-	ns	
Write Command Pulse Width	t_{WP}	10	-	10	-	ns	
Write Command to /RAS Lead Time	t_{RWL}	15	-	20	-	ns	
Write Command to /CAS Lead Time	t_{CWL}	15	-	20	-	ns	
Data-in Set-up Time	t_{DS}	0	-	0	-	ns	
Data-in Hold Time	t_{DH}	15	-	15	-	ns	
Data-in Hold Time from /RAS	t_{DHR}	50	-	55	-	ns	
/CAS Active Delay Time from /RAS Precharge	t_{RPC}	10	-	10	-	ns	
/RAS to /CAS Set-up Time (/CAS before /RAS)	t_{CSR}	5	-	5	-	ns	
/RAS to /CAS Hold Time (/CAS before /RAS)	t_{CHR}	10	-	10	-	ns	
/WE to /RAS Precharge Time (/CAS before /RAS)	t_{WRP}	10	-	10	-	ns	
/WE Hold Time from /RAS (/CAS before /RAS)	t_{WRH}	10	-	10	-	ns	
/RAS to /WE Set-up Time (Test Mode)	t_{WTS}	10	-	10	-	ns	
/RAS to /WE Hold Time (Test Mode)	t_{WTH}	10	-	10	-	ns	

Notes: 1. A start-up delay of 200µs is required after power-up, followed by a minimum of eight initialization cycles (/RAS only refresh or /CAS before /RAS refresh) before proper device operation is achieved.

2. The AC characteristics assumes t_T = 5ns.

3. V_{IH}(Min.) and V_{IL}(Max.) are reference levels for measuring input timing signals. Transition time (t_T) are measured between V_{IH} and V_{IL}.

4. This parameter is measured with a load circuit equivalent to 2TTL loads and 100pF.

5. Operation within the t_{RCD}(Max.) limit ensures that t_{RAC}(Max.) can be met.
t_{RCD}(Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(Max.) limit, then the access time is controlled by t_{CAC}.

6. Operation within the t_{RAD}(Max.) limit ensures that t_{RAC}(Max.) can be met.
t_{RAD}(Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(Max.) limit, then the access time is controlled by t_{AA}.

7. t_{OFF}(Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. The test mode is initiated by performing a /WE and /CAS before /RAS refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is a 2-bit parallel test function. CA0 is not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level.
The test mode is cleared and the memory device returned to its normal operating state by a /RAS only refresh or /CAS before /RAS refresh cycle.

10. In a test mode read cycle, the value of access time parameters is delayed for 5ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.