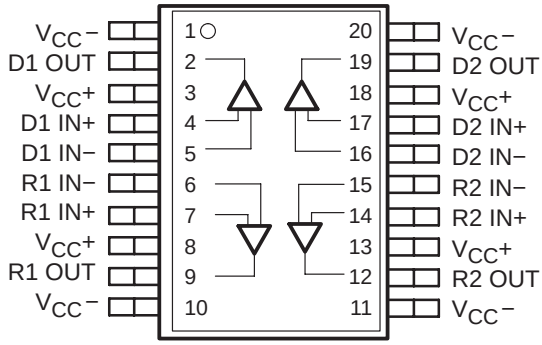
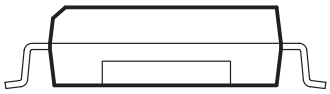
- **ADSL Differential Line Driver and Receiver**
- **Driver Features**
  - **140 MHz Bandwidth (−3dB) With 25-Ω Load**
  - **315 MHz Bandwidth (−3dB) With 100-Ω Load**
  - **1000 V/μs Slew Rate, G = 2**
  - **400 mA Output Current Minimum Into 25-Ω Load**
  - **−72 dB 3rd Order Harmonic Distortion at f = 1 MHz, 25-Ω Load, and 20 $V_{O(PP)}$**
- **Receiver Features**
  - **330 MHz Bandwidth (−3dB)**
  - **900 V/μs Slew Rate at G = 2**
  - **−76 dB 3rd Order Harmonic Distortion at f = 1 MHz, 150-Ω Load, and 20 $V_{O(PP)}$**
- **Wide Supply Range ±4.5 V to ±16 V**
- **Available in the PowerPAD™ Package**
- **Improved Replacement for AD816 or EL1501**
- **Evaluation Module Available**

**DWP PACKAGE**
**(TOP VIEW)**



Cross Section View Showing PowerPAD

## description

The THS6002 contains two high-current, high-speed drivers and two high-speed receivers. These drivers and receivers can be configured differentially for driving and receiving signals over low-impedance lines. The THS6002 is ideally suited for asymmetrical digital subscriber line (ADSL) applications where it supports the high-peak voltage and current requirements of that application. Both the drivers and the receivers are current feedback amplifiers designed for the high slew rates necessary to support low total harmonic distortion (THD) in ADSL applications. Separate power supply connections for each driver are provided to minimize crosstalk.

**HIGH-SPEED xDSL LINE DRIVER/RECEIVER FAMILY**

| DEVICE | DRIVER | RECEIVER | 5 V | ±5 V | ±15 V | BW (MHz) | SR (V/μs) | THD f = 1 MHz (dB) | $I_O$ (mA) | $V_n$ (nV/√Hz) |
|---|---|---|---|---|---|---|---|---|---|---|
| THS6002 | • | • | | • | • | 140 | 1000 | −62 | 500 | 1.7 |
| THS6012 | • | | | • | • | 140 | 1300 | −65 | 500 | 1.7 |
| THS6022 | • | | | • | • | 210 | 1900 | −66 | 250 | 1.7 |
| THS6062 | | • | • | • | • | 100 | 100 | −72 | 90 | 1.6 |
| THS7002 | | • | | • | • | 70 | 100 | −84 | 25 | 2.0 |



CAUTION: The THS6002 provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.**

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## description (continued)

The THS6002 is packaged in the patented PowerPAD package. This package provides outstanding thermal characteristics in a small footprint package, which is fully compatible with automated surface mount assembly procedures. The exposed thermal pad on the underside of the package is in direct contact with the die. By simply soldering the pad to the PWB copper and using other thermal outlets, the heat is conducted away from the junction.

**AVAILABLE OPTIONS**

| $T_A$ | PACKAGED DEVICE | |
|---|---|---|
| | PowerPAD PLASTIC SMALL OUTLINE† (DWP) | EVALUATION MODULE |
| 0°C to 70°C | THS6002CDWP | THS6002EVM |
| −40°C to 85°C | THS6002IDWP | |

† The DWP packages are available taped and reeled. Add an R suffix to the device type (i.e., THS6002CDWPR)

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, $V_{CC+}$ to $V_{CC-}$ . . . . . 33 V
Input voltage, $V_I$ (driver and receiver) . . . . . $\pm V_{CC}$
Output current, $I_O$ (driver) (see Note 1) . . . . . 800 mA
Output current, $I_O$ (receiver) (see Note 1) . . . . . 150 mA
Differential input voltage, $V_{ID}$ (driver and receiver) . . . . . 6 V
Continuous total power dissipation at (or below) $T_A$ = 25°C (see Note 1) . . . . . 5.8 W
Operating free air temperature, $T_A$ . . . . . −40°C to 85°C
Storage temperature, $T_{stg}$ . . . . . −65°C to 125°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

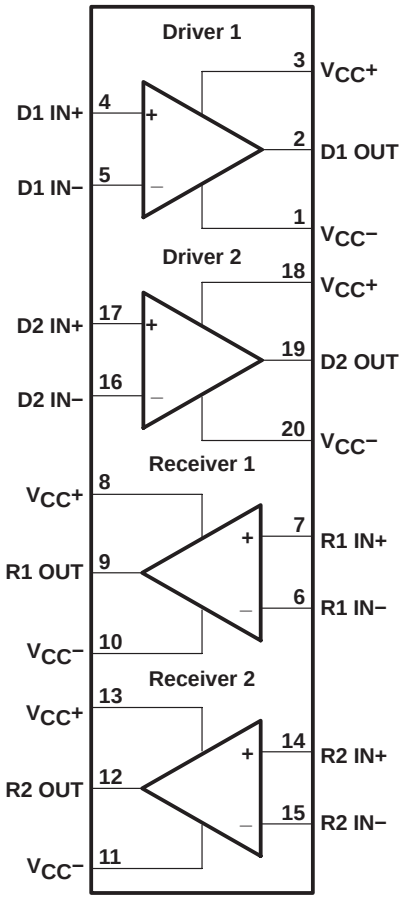
† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS6002 incorporates a PowerPad on the underside of the chip. This acts as a heatsink and must be connected to a thermal dissipation plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature, which could permanently damage the device. See the *Thermal Information* section of this document for more information about PowerPad technology.

## recommended operating conditions

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC+}$ and $V_{CC-}$ | Split supply | ±4.5 | | ±16 | V |
| | Single supply | 9 | | 32 | |
| Operating free-air temperature, $T_A$ | C suffix | 0 | | 70 | °C |
| | I suffix | −40 | | 85 | |

## functional block diagram



## DRIVER

### electrical characteristics, $V_{CC}$ = ±15 V, $R_L$ = 25 Ω, $R_F$ = 1 kΩ, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS† | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Power supply operating range | | Split supply | | ±4.5 | | ±16.5 | V |
| | | | Single supply | | 9 | | 33 | |
| $V_O$ | Output voltage swing | Single ended | $R_L$ = 25 Ω | $V_{CC}$ = ±5 V | 3 to −2.8 | 3.2 to −3 | | V |
| | | | | $V_{CC}$ = ±15 V | 11.8 to −11.5 | 12.5 to −12.2 | | |
| | | Differential | $R_L$ = 50 Ω | $V_{CC}$ = ±5 V | 6 to −5.6 | 6.4 to −6 | | V |
| | | | | $V_{CC}$ = ±15 V | 23.6 to −23 | 25 to −24.4 | | |
| $V_{ICR}$ | Common-mode input voltage range | | $V_{CC}$ = ±5 V | | ±3.6 | ±3.7 | | V |
| | | | $V_{CC}$ = ±15 V | | ±13.4 | ±13.5 | | |
| $V_{IO}$ | Input offset voltage | | $V_{CC}$ = ±5 V or ±15 V | $T_A$ = 25°C | | 2 | 5 | mV |
| | | | | $T_A$ = full range | | | 7 | |
| | Input offset voltage drift | | $V_{CC}$ = ±5 V or ±15 V, | $T_A$ = full range | | | 20 | µV/°C |
| | Differential input offset voltage | | $V_{CC}$ = ±5 V or ±15 V | $T_A$ = 25°C | | 1.5 | 4 | mV |
| | | | | $T_A$ = full range | | | 5 | |
| | Differential input offset voltage drift | | $V_{CC}$ = ±5 V or ±15 V, | $T_A$ = full range | | | 10 | µV/°C |
| $I_{IB}$ | Input bias current | Negative | $V_{CC}$ = ±5 V or ±15 V | $T_A$ = 25°C | | 3 | 9 | µA |
| | | | | $T_A$ = full range | | | 12 | |
| | | Positive | | $T_A$ = 25°C | | 4 | 10 | µA |
| | | | | $T_A$ = full range | | | 12 | |
| | | Differential | | $T_A$ = 25°C | | 1.5 | 8 | µA |
| | | | | $T_A$ = full range | | | 11 | |
| $I_O$ | Output current (see Note 2) | | $V_{CC}$ = ±5 V, | $R_L$ = 5 Ω | | 500 | | mA |
| | | | $V_{CC}$ = ±15 V, | $R_L$ = 25 Ω | 400 | 500 | | |
| $I_{OS}$ | Short-circuit output current (see Note 2) | | | | | 800 | | mA |
| | Open loop transresistance | | $V_{CC}$ = ±5 V | | | 1.5 | | MΩ |
| | | | $V_{CC}$ = ±15 V | | | 5 | | |
| CMRR | Common-mode rejection ratio | | $V_{CC}$ = ±5 V or ±15 V, | $T_A$ = full range | 62 | 70 | | dB |
| | Differential common-mode rejection ratio | | | | | 100 | | |
| | Crosstalk | Driver to driver | $V_I$ = 200 mV, | f = 1 MHz | | −62 | | dB |

† Full range is 0°C to 70°C for the THS6002C and −40°C to 85°C for the THS6002I.

NOTE 2: A heat sink is required to keep the junction temperature below absolute maximum when an output is heavily loaded or shorted. See absolute maximum ratings and Thermal Information section.

## DRIVER

### electrical characteristics, $V_{CC}$ = ±15 V, $R_L$ = 25 Ω, $R_F$ = 1 kΩ, $T_A$ = 25°C (unless otherwise noted) (continued)

| PARAMETER | | TEST CONDITIONS† | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| PSRR | Power supply rejection ratio | $V_{CC}$ = ±5 V | $T_A$ = 25°C | −68 | −74 | | dB |
| | | | $T_A$ = full range | −65 | | | |
| | | $V_{CC}$ = ±15 V | $T_A$ = 25°C | −64 | −72 | | dB |
| | | | $T_A$ = full range | −62 | | | |
| $C_I$ | Differential input capacitance | | | | 1.4 | | pF |
| $R_I$ | Input resistance | | | | 300 | | kΩ |
| $R_O$ | Output resistance | Open loop | | | 13 | | Ω |
| $I_{CC}$ | Quiescent current | $V_{CC}$ = ±5 V | $T_A$ = 25°C | | 8.5 | 10 | mA |
| | | | $T_A$ = full range | | | 12 | |
| | | $V_{CC}$ = ±15 V | $T_A$ = 25°C | | 11.5 | 13 | |
| | | | $T_A$ = full range | | | 15 | |

† Full range is 0°C to 70°C for the THS6002C and −40°C to 85°C for the THS6002I.

### operating characteristics, $V_{CC}$ = ±15 V, $R_L$ = 25 Ω, $R_F$ = 1 kΩ, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| SR | Differential slew rate | | $V_O$ = 20 $V_{(PP)}$, G = 2 | | | 1000 | | V/μs |
| $t_s$ | Settling time to 0.1% | | 0 V to 10 V Step, G = 2 | | | 70 | | ns |
| THD | Total harmonic distortion | | $V_{O(PP)}$ = 20 V, $R_F$ = 4 kΩ, G = 5, f = 1 MHz | | | −62 | | dBc |
| $V_n$ | Input voltage noise | | $V_{CC}$ = ±5 V or ±15 V, G = 2, f = 10 kHz, Single-ended | | | 1.7 | | nV/√Hz |
| $I_n$ | Input noise current | Positive (IN+) | $V_{CC}$ = ±5 V or ±15 V, G = 2 f = 10 kHz, | | | 11.5 | | pA/√Hz |
| | | Negative (IN−) | | | | 16 | | |
| BW | Small-signal bandwidth (−3 dB) | | $V_I$ = 200 mV, G = 1, $R_F$ = 680 Ω | $V_{CC}$ = ±5 V | 90 | 110 | | MHz |
| | | | | $V_{CC}$ = ±15 V | 110 | 140 | | MHz |
| | | | $V_I$ = 200 mV, G = 2, $R_F$ = 620 Ω | $V_{CC}$ = ±15 V | | 120 | | MHz |
| | | | $V_I$ = 200 mV, G = 1, $R_F$ = 820 Ω, $R_L$ = 100 Ω | $V_{CC}$ = ±15 V | | 315 | | MHz |
| | | | $V_I$ = 200 mV, G = 2, $R_F$ = 560 Ω, $R_L$ = 100 Ω | $V_{CC}$ = ±15 V | | 265 | | MHz |
| | Bandwidth for 0.1 dB flatness | | $V_I$ = 200 mV, G = 1, $R_F$ = 680 Ω | $V_{CC}$ = ±5 V | | 30 | | MHz |
| | | | | $V_{CC}$ = ±15 V | | 40 | | |
| | Full power bandwidth (see Note 3) | | $V_O$ = 20 $V_{(PP)}$ | | | 16 | | MHz |
| $A_D$ | Differential gain error | | G = 2, NTSC, $R_L$ = 150 Ω, 40 IRE | $V_{CC}$ = ±5 V | | 0.04% | | |
| | | | | $V_{CC}$ = ±15 V | | 0.05% | | |
| $\phi_D$ | Differential phase error | | G = 2, NTSC, $R_L$ = 150 Ω, 40 IRE | $V_{CC}$ = ±5 V | | 0.07° | | |
| | | | | $V_{CC}$ = ±15 V | | 0.08° | | |

NOTE 3: Full power bandwidth = slew rate/$2\pi V_{peak}$

## RECEIVER

### electrical characteristics, $V_{CC}$ = ±15 V, $R_L$ = 150 Ω, $R_F$ = 1 kΩ, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS† | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Power supply operating range | | Split supply | | ±4.5 | | ±16.5 | V |
| | | | Single supply | | 9 | | 33 | |
| $V_O$ | Output voltage swing | Single ended | $V_{CC}$ = ±5 V | | ±3 | ±3.3 | | V |
| | | | $V_{CC}$ = ±15 V | | ±12.4 | ±12.8 | | |
| $V_{ICR}$ | Common-mode input voltage range | | $V_{CC}$ = ±5 V | | ±3.6 | ±3.7 | | V |
| | | | $V_{CC}$ = ±15 V | | ±13.4 | ±13.5 | | |
| $V_{IO}$ | Input offset voltage | Single ended | $V_{CC}$ = ±5 V or ±15 V | $T_A$ = 25°C | | 1 | 4 | mV |
| | | | | $T_A$ = full range | | | 6 | |
| | | Differential | | $T_A$ = 25°C | | 1.5 | 4 | |
| | | | | $T_A$ = full range | | | 5 | |
| | Input offset voltage drift | Single ended | $V_{CC}$ = ±5 V or ±15 V | | | | 20 | µV/°C |
| | | Differential | | | | | 10 | |
| $I_{IB}$ | Input bias current | Negative | $V_{CC}$ = ±5 V or ±15 , | $T_A$ = 25°C | | 2 | 8 | µA |
| | | | | $T_A$ = full range | | | 10 | |
| | | Positive | $V_{CC}$ = ±5 V or ±15 V | $T_A$ = 25°C | | 3.5 | 9 | |
| | | | | $T_A$ = full range | | | 11 | |
| | | Differential | $V_{CC}$ = ±5 V or ±15 V | $T_A$ = 25°C | | 1.5 | 8 | |
| | | | | $T_A$ = full range | | | 10 | |
| $I_O$ | Output current (see Note 2) | | $V_{CC}$ = ±5 V | $R_L$ = 25 Ω | | 95 | | mA |
| | | | $V_{CC}$ = ±15 V | $R_L$ = 150 Ω | 80 | 85 | | |
| $I_{OS}$ | Short-circuit output current (see Note 2) | | $R_L$ = 25 Ω | | | 110 | | mA |
| | Open loop transresistance | | $V_{CC}$ = ±5 V | | | 1.5 | | MΩ |
| | | | $V_{CC}$ = ±15 V | | | 5 | | |
| CMRR | Common-mode rejection ratio | Single ended | $V_{CC}$ = ±5 V or ±15 V, | $T_A$ = full range | 60 | 70 | | dB |
| | | Differential | | | | 100 | | |
| | Crosstalk (receiver to receiver) | | $V_I$ = 200 mV, | f = 1 MHz | | −67 | | dB |
| PSRR | Power supply rejection ratio | | $V_{CC}$ = ±5 V | $T_A$ = 25°C | −66 | −74 | | dB |
| | | | | $T_A$ = full range | −63 | | | |
| | | | $V_{CC}$ = ±15 V | $T_A$ = 25°C | −65 | −72 | | |
| | | | | $T_A$ = full range | −62 | | | |
| $R_I$ | Input resistance | | | | | 300 | | kΩ |
| $C_I$ | Differential input capacitance | | | | | 1.4 | | pF |
| $R_O$ | Output resistance | | Open loop | | | 10 | | Ω |

† Full range is 0°C to 70°C for the THS6002C and −40°C to 85°C for the THS6002I.

NOTE 2: A heat sink is required to keep junction temperature below absolute maximum when an output is heavily loaded or shorted. See absolute maximum ratings and Thermal Information section.

## RECEIVER

### electrical characteristics, $V_{CC}$ = ±15 V, $R_L$ = 150 Ω, $R_F$ = 1 kΩ, $T_A$ = 25°C (unless otherwise noted) (continued)

| PARAMETER | | TEST CONDITIONS† | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent current | $V_{CC}$ = ±5 V | $T_A$ = 25°C | | 4.2 | 5.5 | mA |
| | | | $T_A$ = full range | | | 7.5 | |
| | | $V_{CC}$ = ±15 V | $T_A$ = 25°C | | 5 | 7 | |
| | | | $T_A$ = full range | | | 9 | |

† Full range is 0°C to 70°C for the THS6002C and −40°C to 85°C for the THS6002I.

### operating characteristics, $V_{CC}$ = ±15 V, $R_L$ = 150 Ω, $R_F$ = 1 kΩ, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| SR | Differential slew rate | | $V_O$ = 10 $V_{(PP)}$, G = 2 | | | 900 | | V/µs |
| $t_s$ | Settling time to 0.1% | | 10 V Step, G = 2 | | | 50 | | ns |
| THD | Total harmonic distortion | | $V_{O(PP)}$ = 20 V, G = 5, | $R_F$ = 510 Ω, f =1 MHz | | −68 | | dBc |
| $V_n$ | Input voltage noise | | $V_{CC}$ = ±5 V or ±15 V G = 2 | f = 10 kHz, | | 1.7 | | nV/√Hz |
| $I_n$ | Input current noise | Positive (IN+) | $V_{CC}$ = ±5 V or ±15 V, G = 2 | f = 10 kHz, | | 11.5 | | pA/√Hz |
| | | Negative (IN−) | | | | 16 | | |
| BW | Small-signal bandwidth (−3 dB) | | $V_I$ = 200 mV, G = 1, $R_F$ = 560 Ω | $V_{CC}$ = ±5 V | 270 | 300 | | MHz |
| | | | | $V_{CC}$ = ±15 V | 300 | 330 | | |
| | | | $V_I$ = 200 mV, G = 2, $R_F$ = 430 Ω | $V_{CC}$ = ±15 V | | 285 | | MHz |
| | Bandwidth for 0.1 dB flatness | | $V_I$ = 200 mV, G = 1, $R_F$ = 560 Ω | $V_{CC}$ = ±5 V | | 20 | | MHz |
| | | | | $V_{CC}$ = ±15 V | | 25 | | |
| | Full power bandwidth (see Note 3) | | $V_O$ = 20 $V_{(PP)}$ | | | 14 | | MHz |
| $A_D$ | Differential gain error | | 40 IRE, G = 2, $R_L$ = 150 Ω, NTSC | $V_{CC}$ = ±5 V | | 0.09% | | |
| | | | | $V_{CC}$ = ±15 V | | 0.1% | | |
| $\phi_D$ | Differential phase error | | 40 IRE, G = 2, $R_L$ = 150 Ω, NTSC | $V_{CC}$ = ±5 V | | 0.13° | | |
| | | | | $V_{CC}$ = ±15 V | | 0.16° | | |

NOTE 3: Full power bandwidth = slew rate/2π$V_{peak}$

## PARAMETER MEASUREMENT INFORMATION




**Figure 1. Driver Input-to-Output Crosstalk Test Circuit**

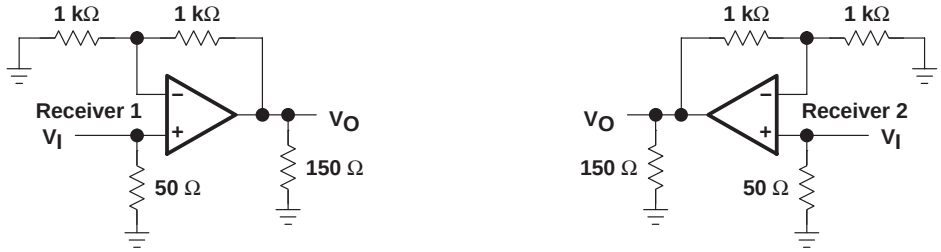



**Figure 2. Receiver Input-to-Output Crosstalk Test Circuit**

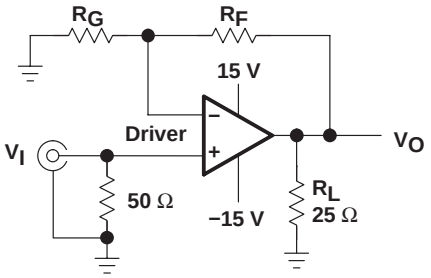



**Figure 3. Driver Test Circuit, Gain = 1 + ($R_F$/$R_G$)**

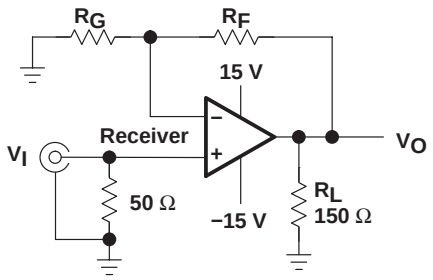



**Figure 4. Receiver Test Circuit, Gain = 1 + ($R_F$/$R_G$)**

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | | | FIGURE |
|---|---|---|---|---|
| | Supply current | Driver and Receiver | vs Supply voltage | 5 |
| | Input voltage noise | Driver and Receiver | vs Frequency | 6 |
| | Input current noise | Driver and Receiver | vs Frequency | 6 |
| | Closed-loop output impedance | Driver and Receiver | vs Frequency | 7 |
| | Peak-to-peak output voltage swing | Driver | vs Supply voltage | 8 |
| | | Receiver | vs Supply voltage | 31 |
| | Peak-to-peak output voltage | Driver | vs Load resistance | 9 |
| | | Receiver | vs Load resistance | 32 |
| $V_{IO}$ | Input offset voltage | Driver | vs Free-air temperature | 10 |
| | | Receiver | vs Free-air temperature | 33 |
| $I_{IB}$ | Input bias current | Driver | vs Free-air temperature | 11 |
| | | Receiver | vs Free-air temperature | 34 |
| CMMR | Common-mode rejection ratio | Driver | vs Free-air temperature | 12 |
| | | Receiver | vs Free-air temperature | 35 |
| | Input-to-output crosstalk | Driver | vs Frequency | 13 |
| | | Receiver | vs Frequency | 36 |
| | Driver-to-receiver crosstalk | | vs Frequency | 14 |
| | Receiver-to-driver crosstalk | | vs Frequency | 37 |
| PSSR | Power supply rejection ratio | Driver | vs Free-air temperature | 15 |
| | | Receiver | vs Free-air temperature | 38 |
| $I_{CC}$ | Supply current | Driver | vs Free-air temperature | 16 |
| | | Receiver | vs Free-air temperature | 39 |
| | Normalized frequency response | Driver | vs Frequency | 17, 18 |
| | | Receiver | vs Frequency | 40, 41 |
| | Normalized output response | Driver | vs Frequency | 19 – 22 |
| | Single-ended output distortion | Driver | vs Output voltage | 23 |
| | Output distortion | Receiver | vs Output voltage | 42 |
| | Small and large signal frequency response | Receiver | | 43, 44 |
| | Differential gain | Driver | DC input offset voltage | 24, 25 |
| | | | Number of 150-Ω loads | 26, 27 |
| | | Receiver | DC input offset voltage | 45, 46 |
| | | | Number of 150-Ω loads | 47, 48 |
| | Differential phase | Driver | DC input offset voltage | 24, 25 |
| | | | Number of 150-Ω loads | 26, 27 |
| | | Receiver | DC input offset voltage | 45, 46 |
| | | | Number of 150-Ω loads | 47, 48 |
| | Output step response | Driver | | 28 – 30 |
| | | Receiver | | 49 – 51 |

## TYPICAL CHARACTERISTICS

DRIVER AND RECEIVER
SUPPLY CURRENT
vs
SUPPLY VOLTAGE

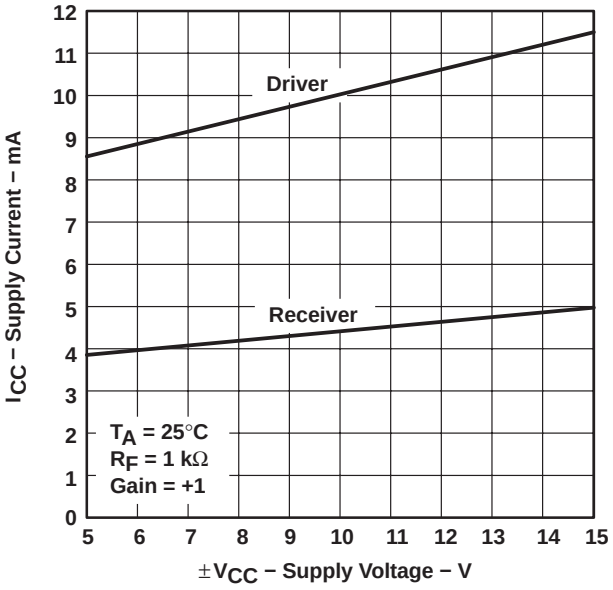



Figure 5

DRIVER AND RECEIVER
INPUT VOLTAGE AND CURRENT NOISE
vs
FREQUENCY

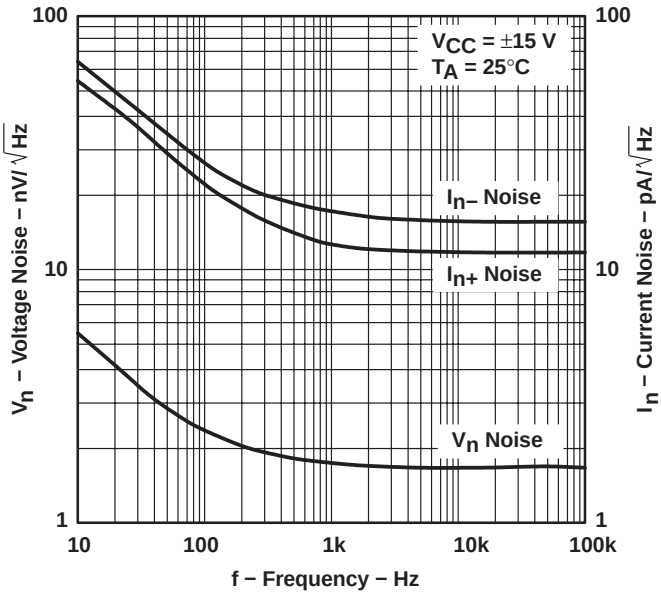



Figure 6

DRIVER AND RECEIVER
CLOSED-LOOP OUTPUT IMPEDANCE
vs
FREQUENCY

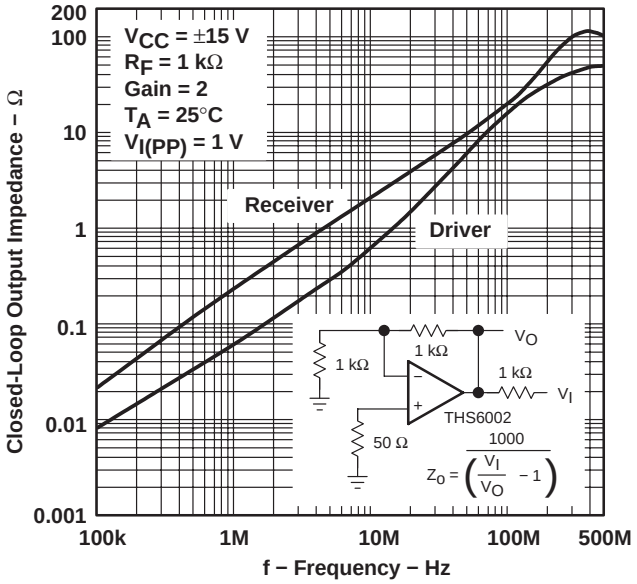



Figure 7

## TYPICAL CHARACTERISTICS

**DRIVER**
**PEAK-TO-PEAK OUTPUT VOLTAGE SWING**
**vs**
**SUPPLY VOLTAGE**

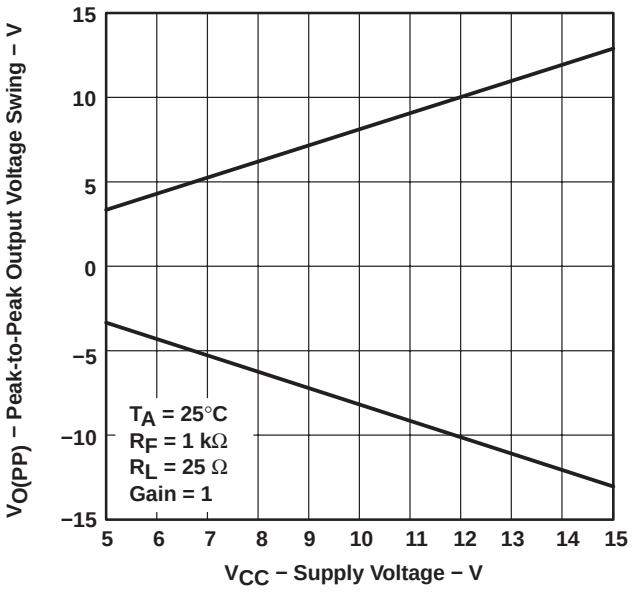



**Figure 8**

**DRIVER**
**PEAK-TO-PEAK OUTPUT VOLTAGE**
**vs**
**LOAD RESISTANCE**

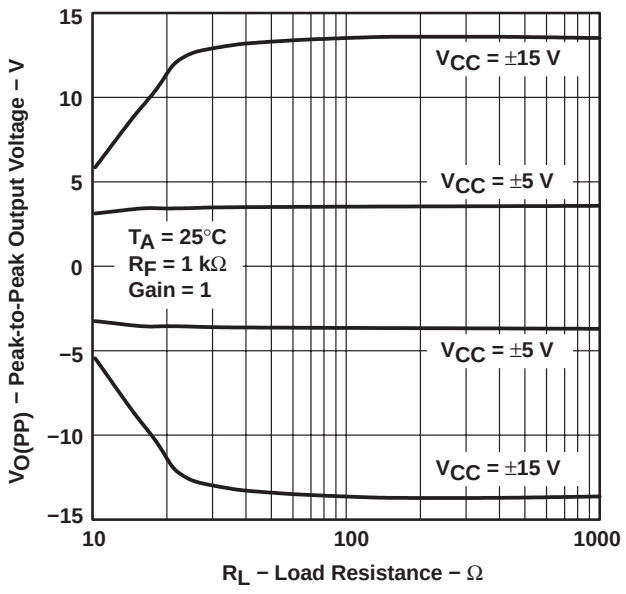



**Figure 9**

**DRIVER**
**INPUT OFFSET VOLTAGE**
**vs**
**FREE-AIR TEMPERATURE**

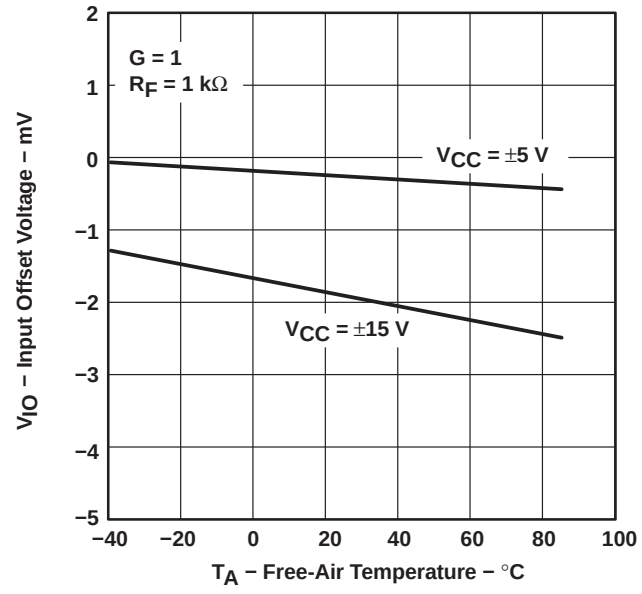



**Figure 10**

**DRIVER**
**INPUT BIAS CURRENT**
**vs**
**FREE-AIR TEMPERATURE**

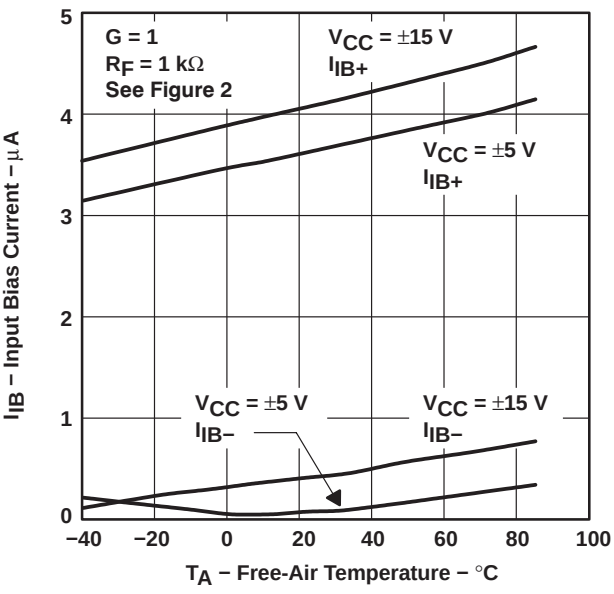



**Figure 11**

## TYPICAL CHARACTERISTICS

**DRIVER**
**COMMON-MODE REJECTION RATIO**
**vs**
**FREE-AIR TEMPERATURE**

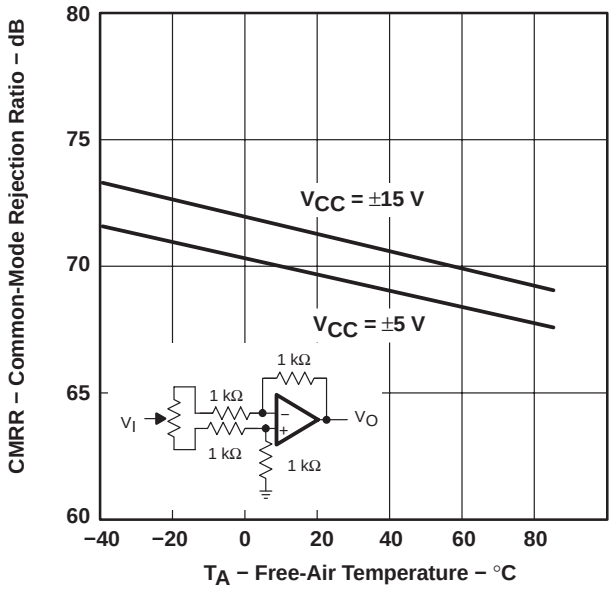



Figure 12

**DRIVER**
**INPUT-TO-OUTPUT CROSSTALK**
**vs**
**FREQUENCY**

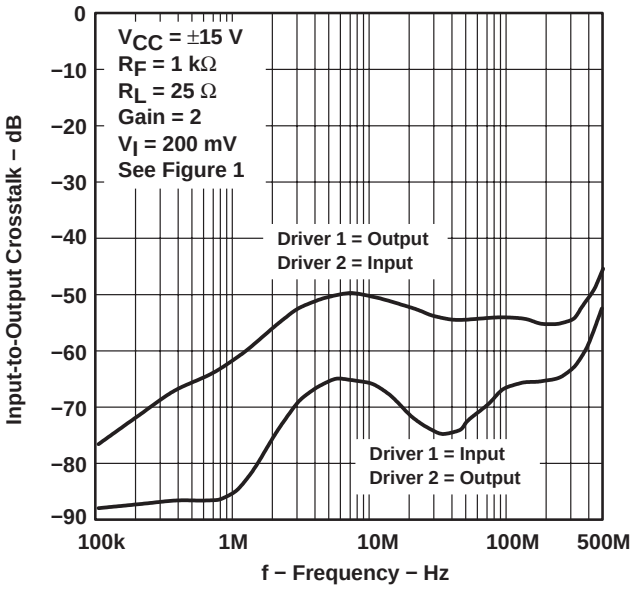



Figure 13

**DRIVER-TO-RECEIVER CROSSTALK**
**vs**
**FREQUENCY**

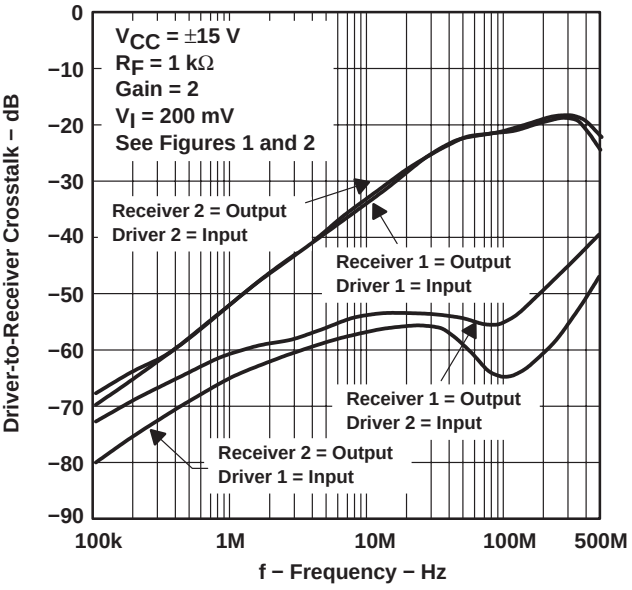



Figure 14

**DRIVER**
**POWER SUPPLY REJECTION RATIO**
**vs**
**FREE-AIR TEMPERATURE**

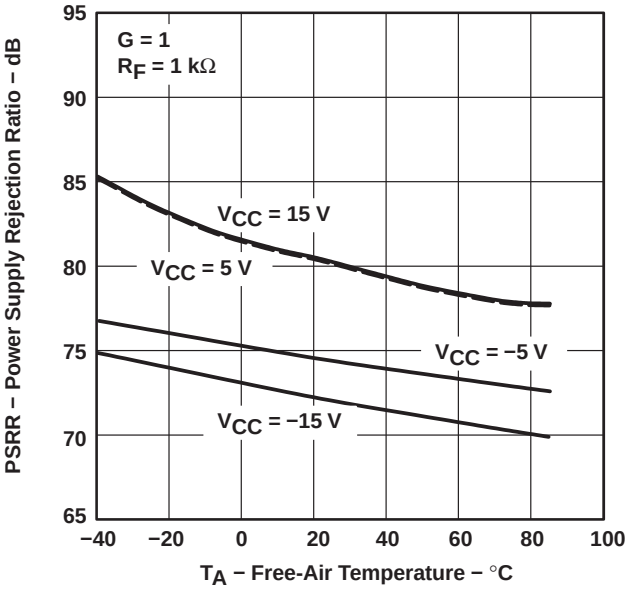



Figure 15

## TYPICAL CHARACTERISTICS

**DRIVER**
**SUPPLY CURRENT**
**vs**
**FREE-AIR TEMPERATURE**

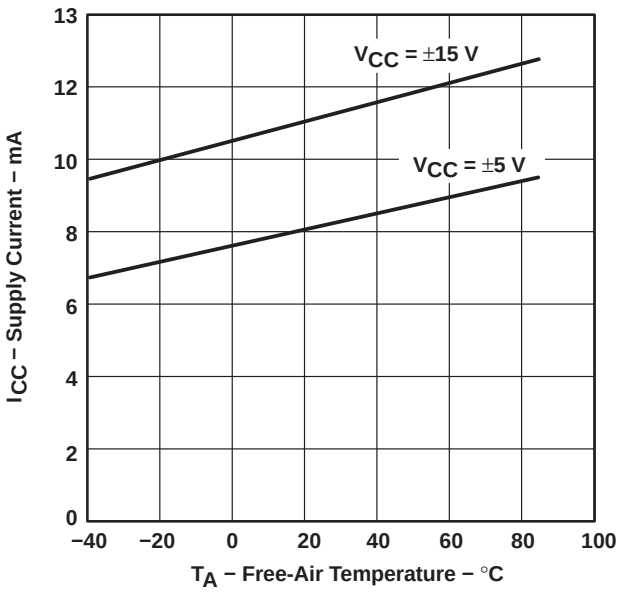



**Figure 16**

**DRIVER**
**NORMALIZED FREQUENCY RESPONSE**
**vs**
**FREQUENCY**

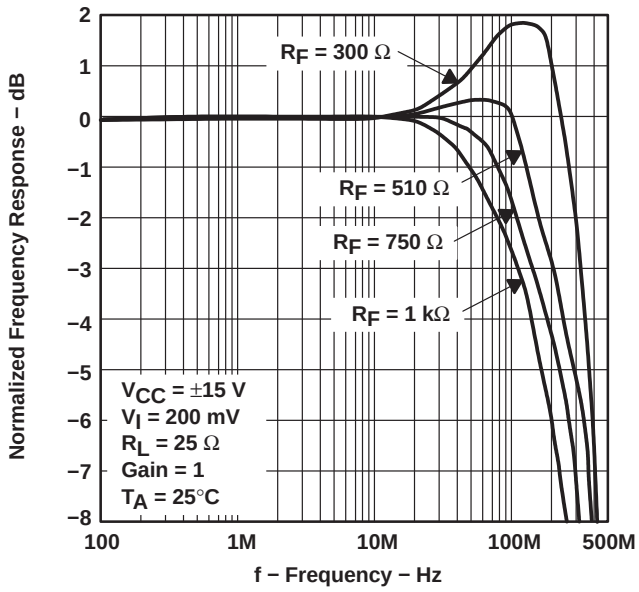



**Figure 17**

**DRIVER**
**NORMALIZED FREQUENCY RESPONSE**
**vs**
**FREQUENCY**

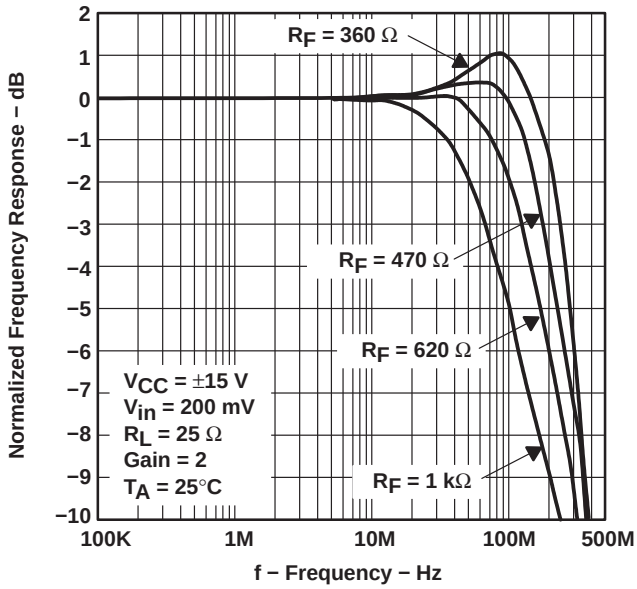



**Figure 18**

**DRIVER**
**NORMALIZED OUTPUT RESPONSE**
**vs**
**FREQUENCY**

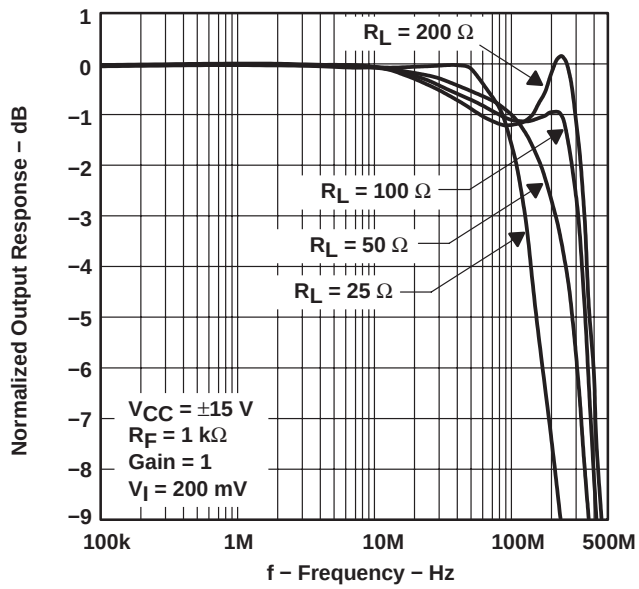



**Figure 19**

## TYPICAL CHARACTERISTICS

DRIVER
NORMALIZED OUTPUT RESPONSE
vs
FREQUENCY

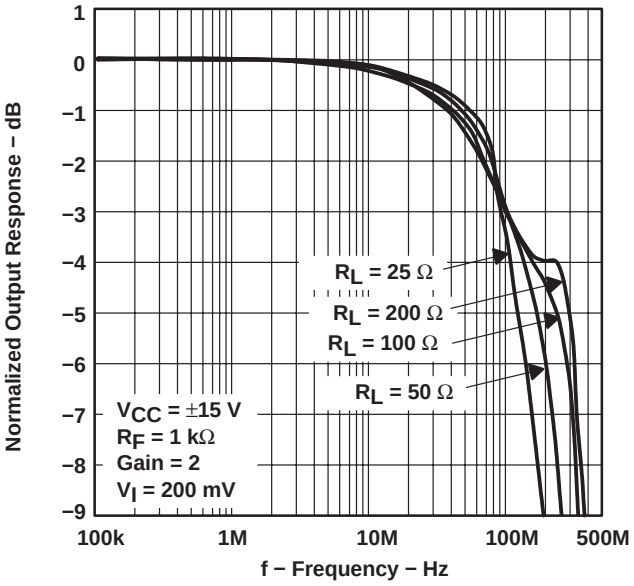



Figure 20

DRIVER
NORMALIZED OUTPUT RESPONSE
vs
FREQUENCY

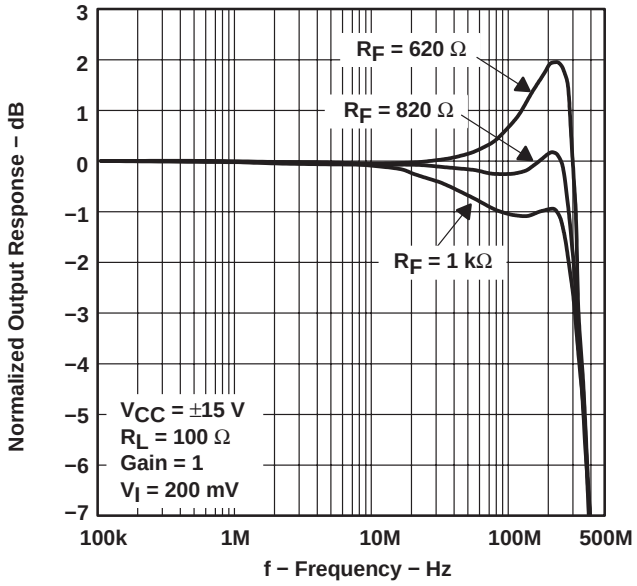



Figure 21

DRIVER
NORMALIZED OUTPUT RESPONSE
vs
FREQUENCY

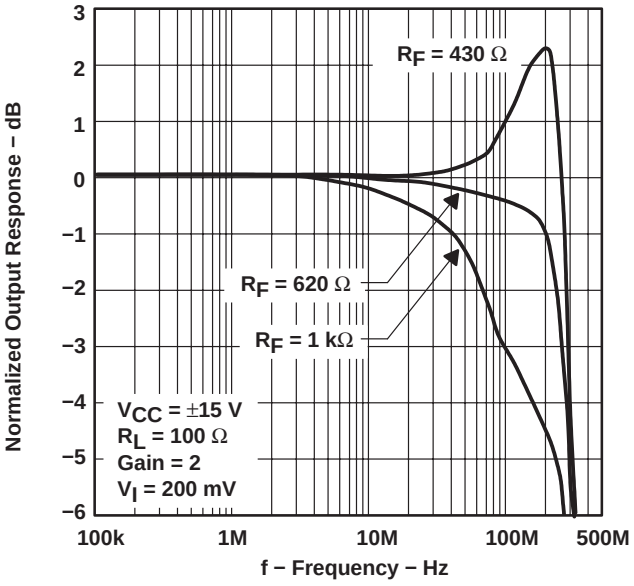



Figure 22

DRIVER
SINGLE-ENDED OUTPUT DISTORTION
vs
OUTPUT VOLTAGE

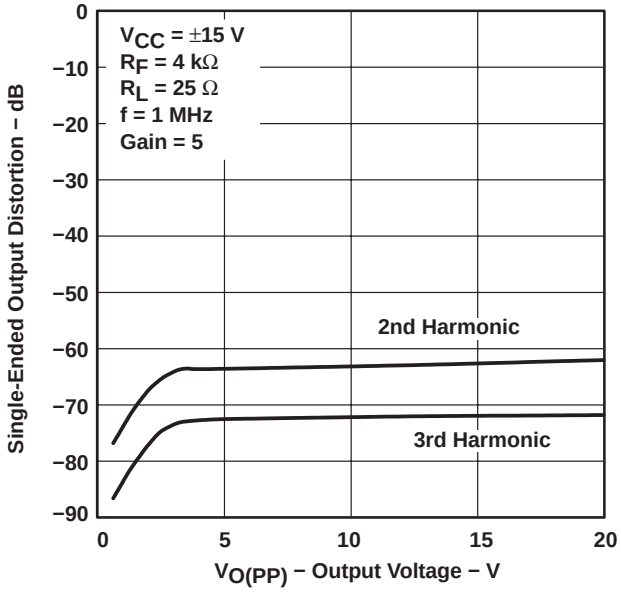



Figure 23

## TYPICAL CHARACTERISTICS

**DRIVER**
**DIFFERENTIAL GAIN AND PHASE**
**vs**
**DC INPUT OFFSET VOLTAGE**

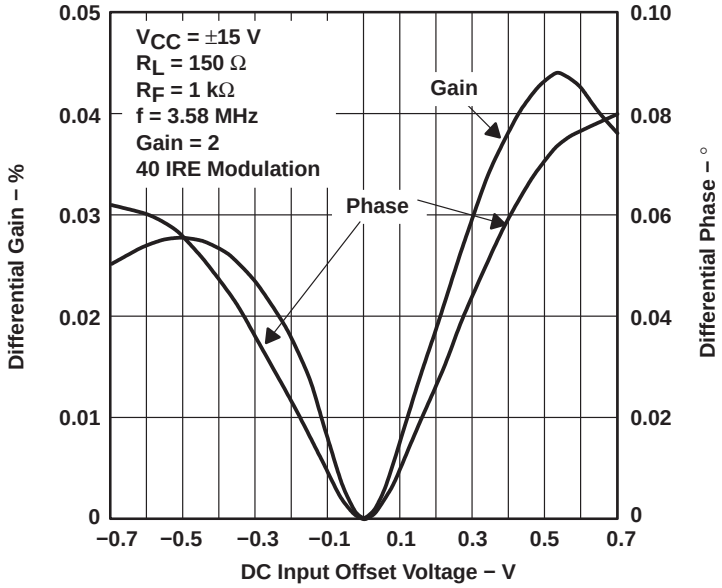



**Figure 24**

**DRIVER**
**DIFFERENTIAL GAIN AND PHASE**
**vs**
**DC INPUT OFFSET VOLTAGE**

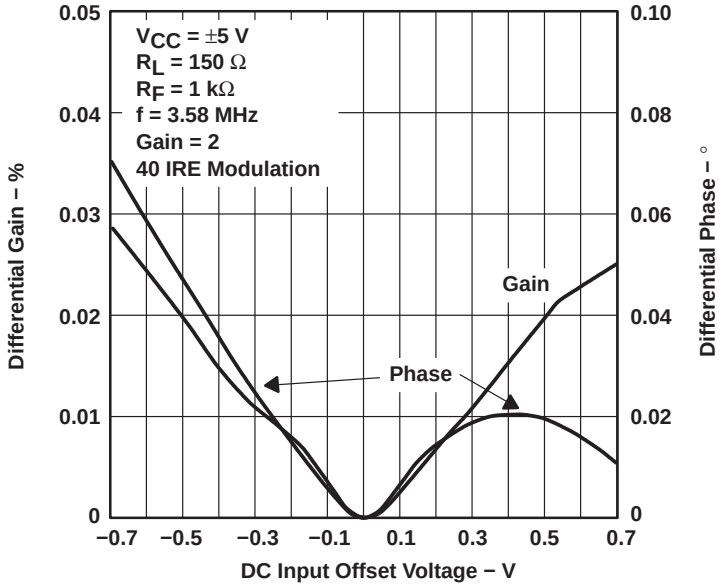



**Figure 25**

## TYPICAL CHARACTERISTICS

**DRIVER**
**DIFFERENTIAL GAIN AND PHASE**
**vs**
**NUMBER OF 150-Ω LOADS**

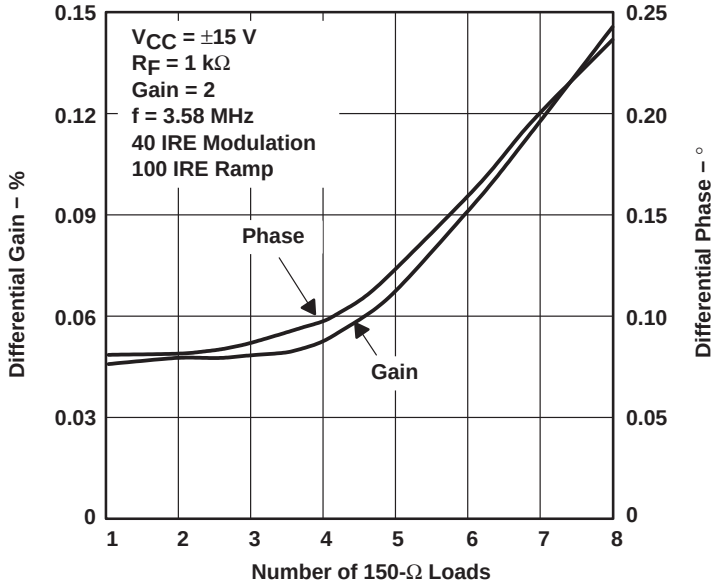



**Figure 26**

**DRIVER**
**DIFFERENTIAL GAIN AND PHASE**
**vs**
**NUMBER OF 150-Ω LOADS**

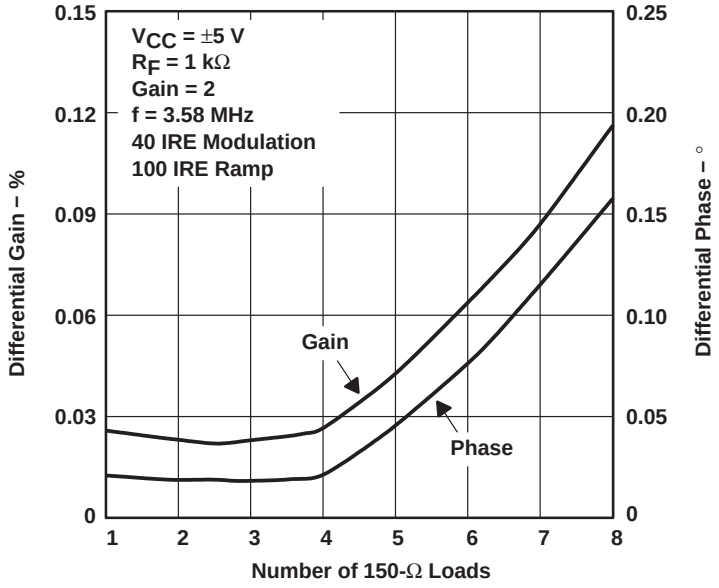



**Figure 27**

## TYPICAL CHARACTERISTICS

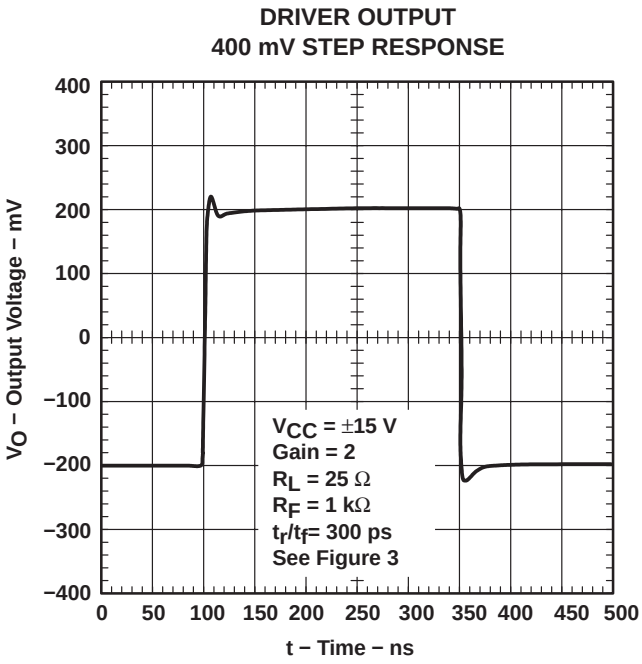



Figure 28

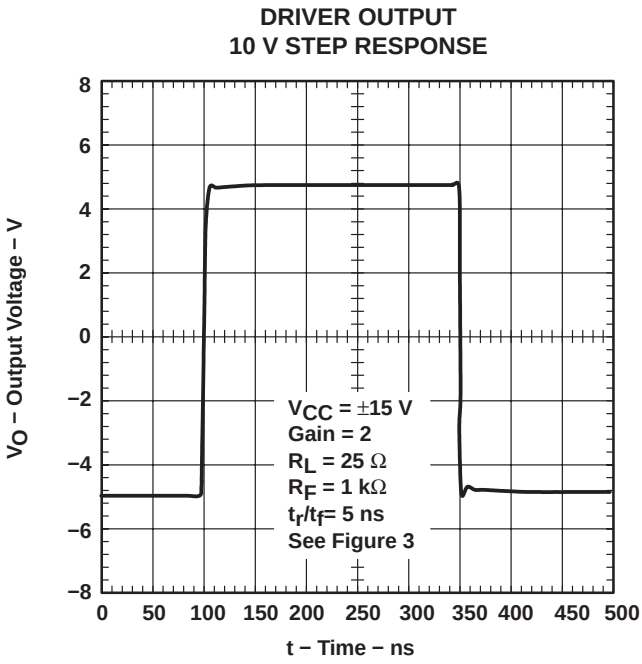



Figure 29

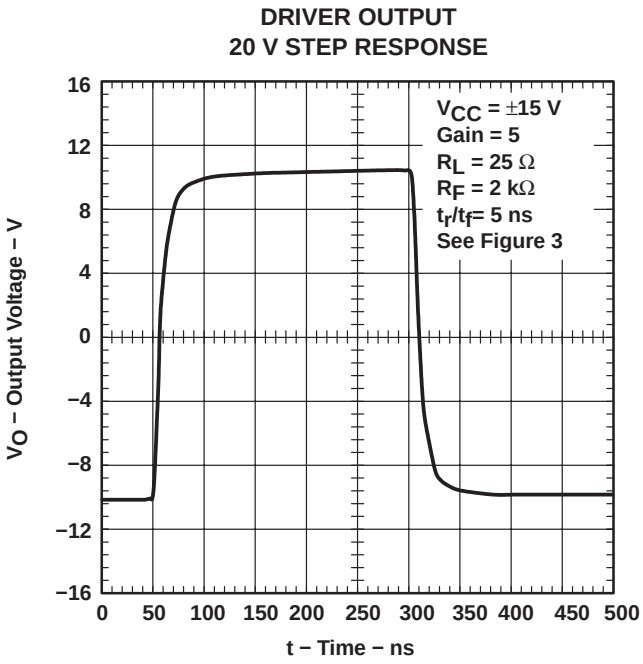



Figure 30

## TYPICAL CHARACTERISTICS

**RECEIVER**
**PEAK-TO-PEAK OUTPUT VOLTAGE SWING**
**vs**
**SUPPLY VOLTAGE**

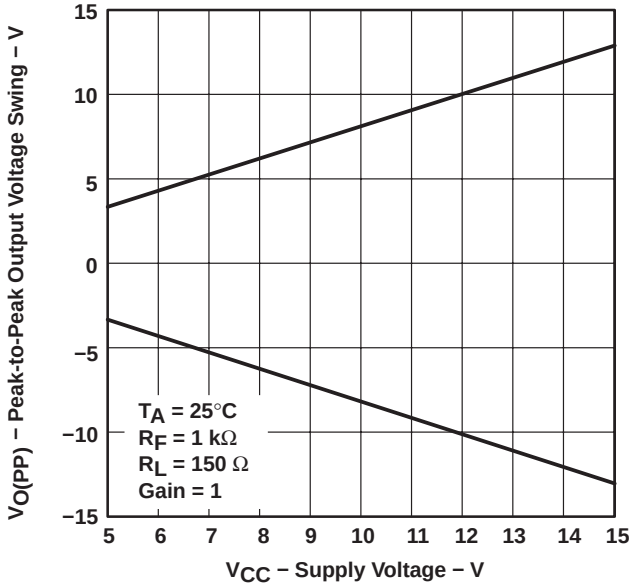



**Figure 31**

**RECEIVER**
**PEAK-TO-PEAK OUTPUT VOLTAGE**
**vs**
**LOAD RESISTANCE**

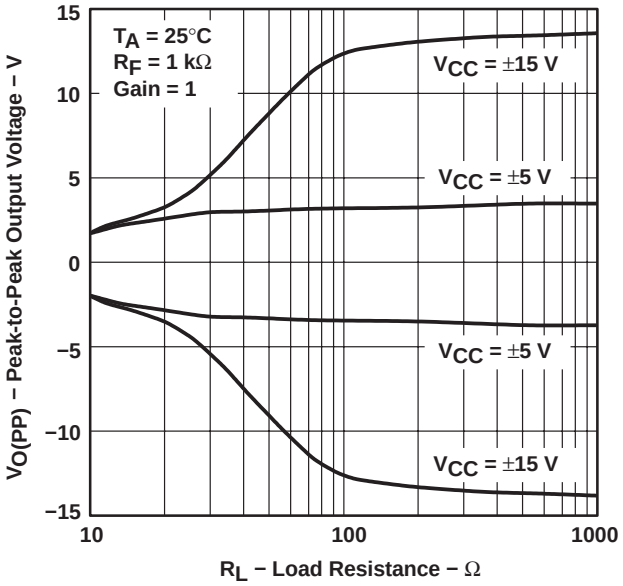



**Figure 32**

**RECEIVER**
**INPUT OFFSET VOLTAGE**
**vs**
**FREE-AIR TEMPERATURE**

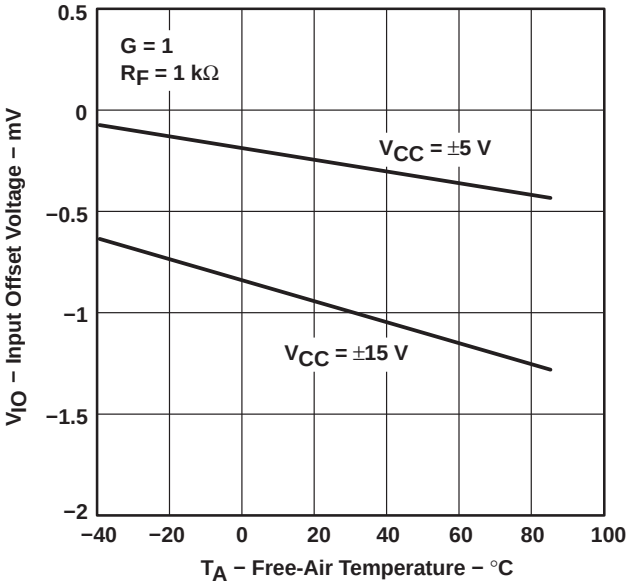



**Figure 33**

**RECEIVER**
**INPUT BIAS CURRENT**
**vs**
**FREE-AIR TEMPERATURE**

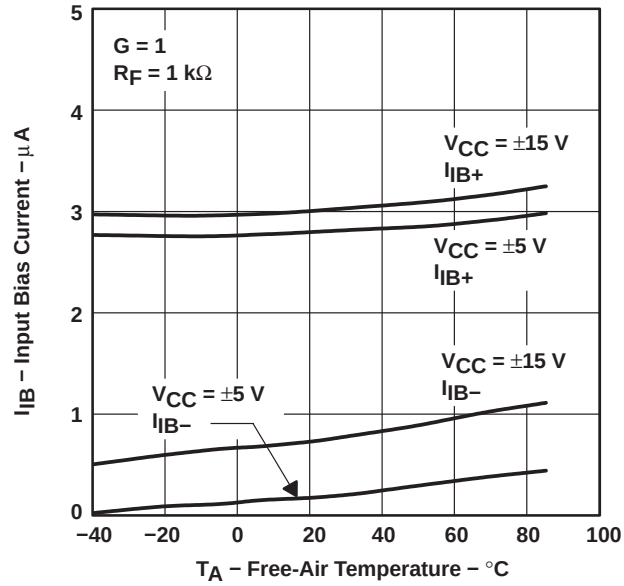



**Figure 34**

## TYPICAL CHARACTERISTICS

**RECEIVER**
**COMMON-MODE REJECTION RATIO**
**vs**
**FREE-AIR TEMPERATURE**

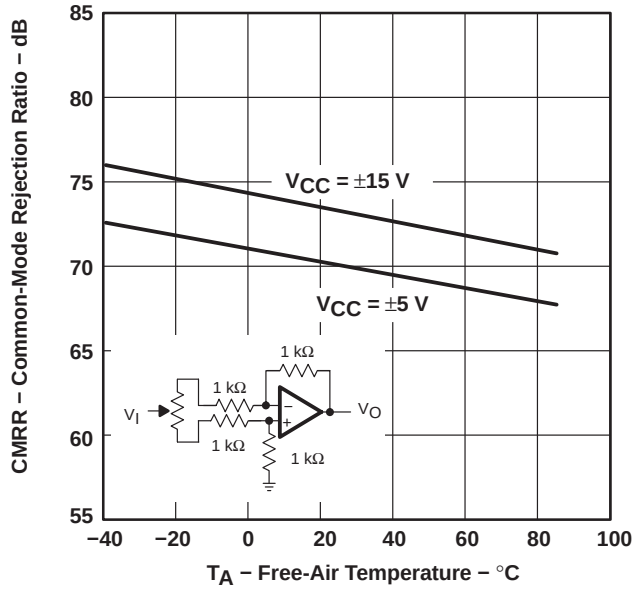



**Figure 35**

**RECEIVER**
**INPUT-TO-OUTPUT CROSSTALK**
**vs**
**FREQUENCY**

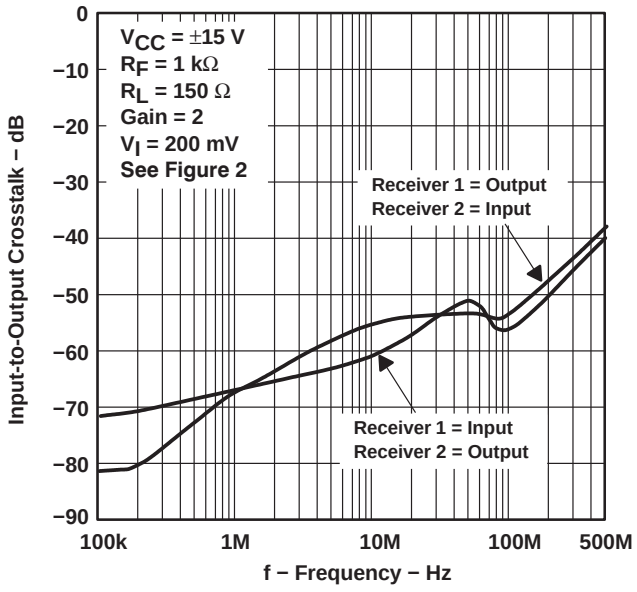



**Figure 36**

**RECEIVER-TO-DRIVER CROSSTALK**
**vs**
**FREQUENCY**

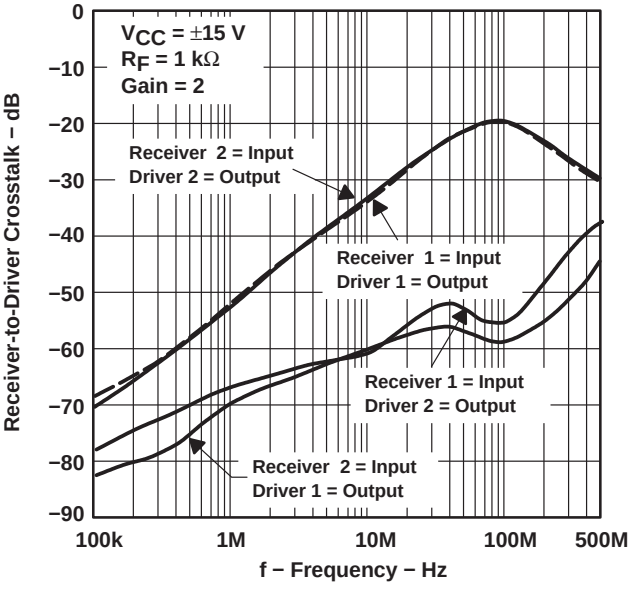



**Figure 37**

**RECEIVER**
**POWER SUPPLY REJECTION RATIO**
**vs**
**FREE-AIR TEMPERATURE**

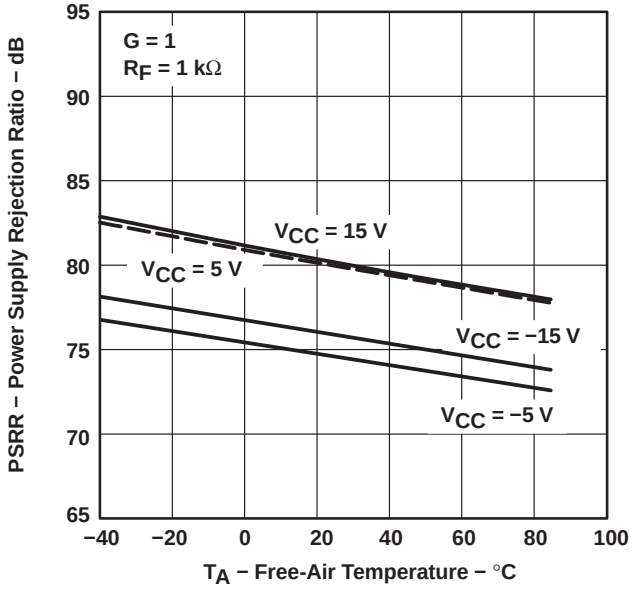



**Figure 38**

## TYPICAL CHARACTERISTICS

**RECEIVER**
**SUPPLY CURRENT**
**vs**
**FREE-AIR TEMPERATURE**

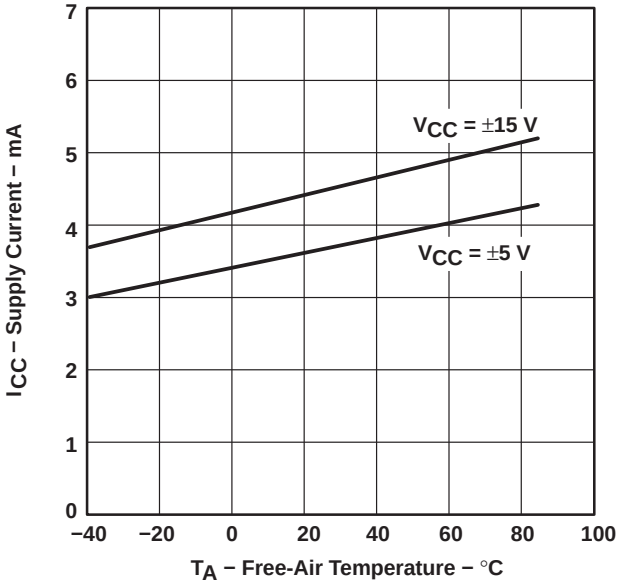



Figure 39

**RECEIVER**
**NORMALIZED OUTPUT RESPONSE**
**vs**
**FREQUENCY**

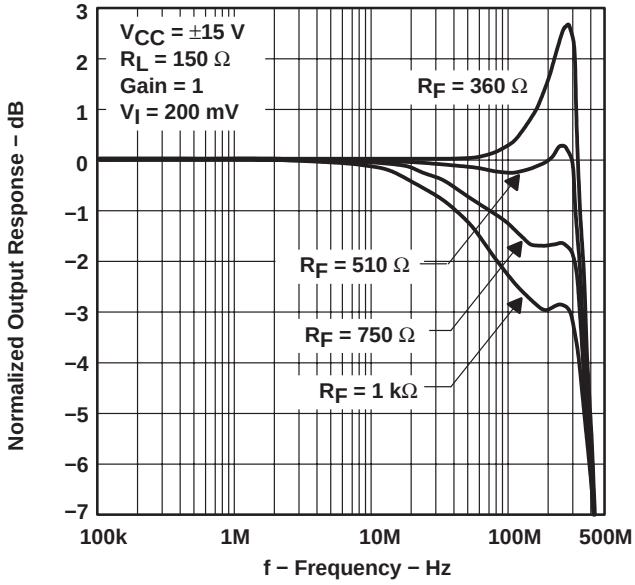



Figure 40

**RECEIVER**
**NORMALIZED OUTPUT RESPONSE**
**vs**
**FREQUENCY**

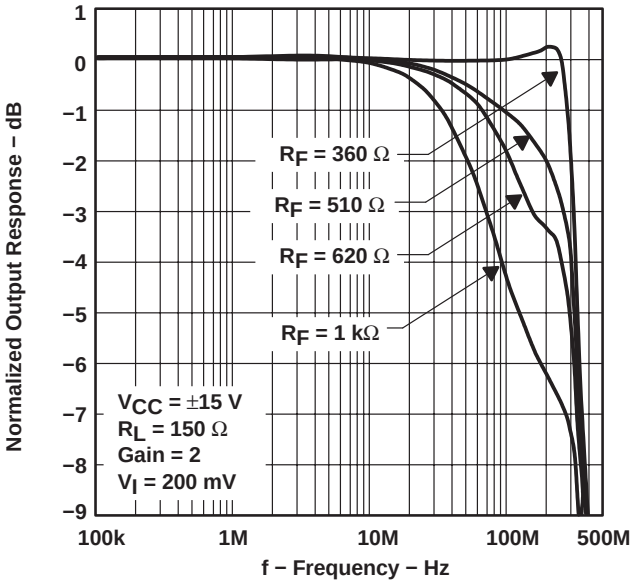



Figure 41

**RECEIVER**
**OUTPUT DISTORTION**
**vs**
**OUTPUT VOLTAGE**

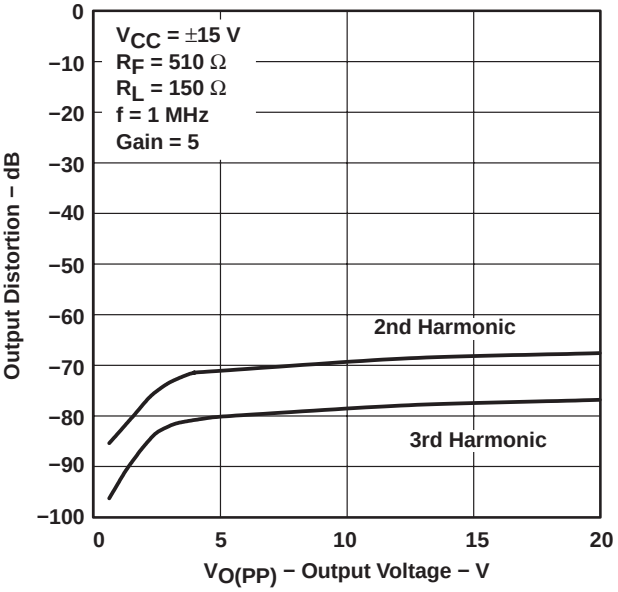



Figure 42

## TYPICAL CHARACTERISTICS

RECEIVER
SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

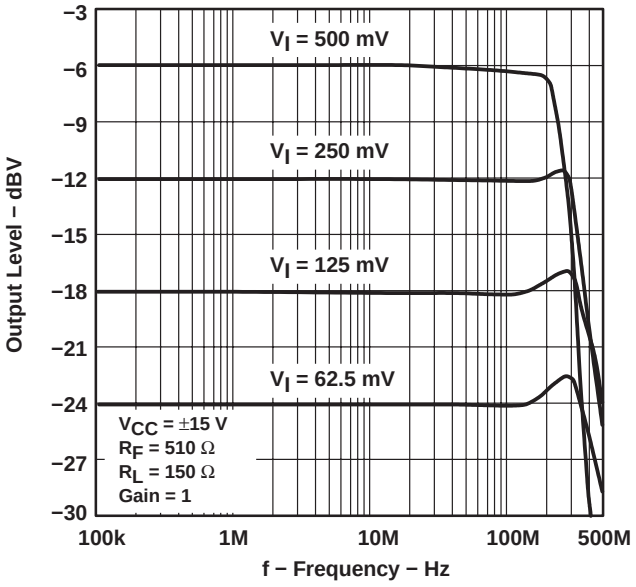



Figure 43

RECEIVER
SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

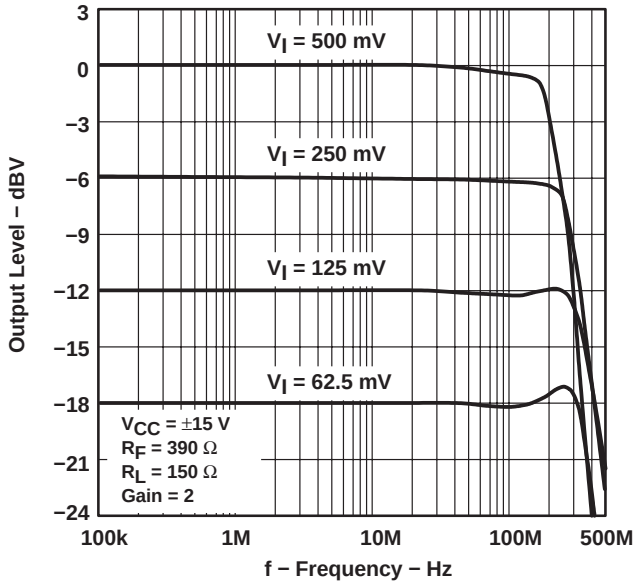



Figure 44

RECEIVER
DIFFERENTIAL GAIN AND PHASE
vs
DC INPUT OFFSET VOLTAGE

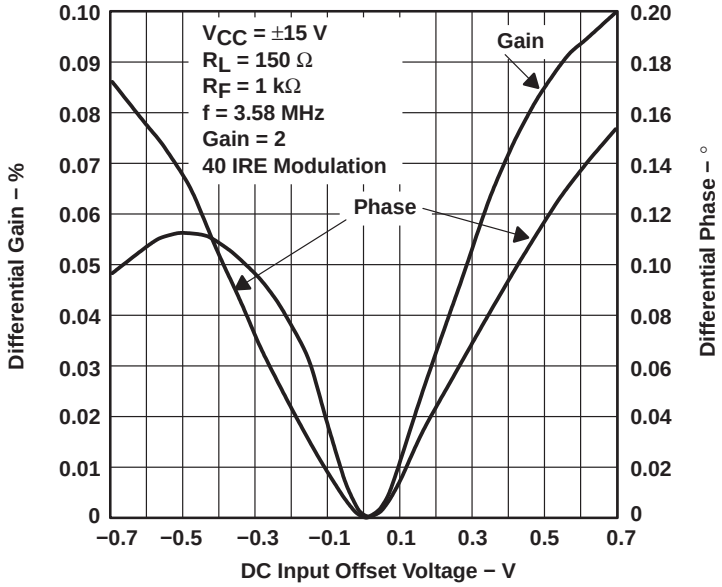



Figure 45

## TYPICAL CHARACTERISTICS

**RECEIVER**
**DIFFERENTIAL GAIN AND PHASE**
**vs**
**DC INPUT OFFSET VOLTAGE**

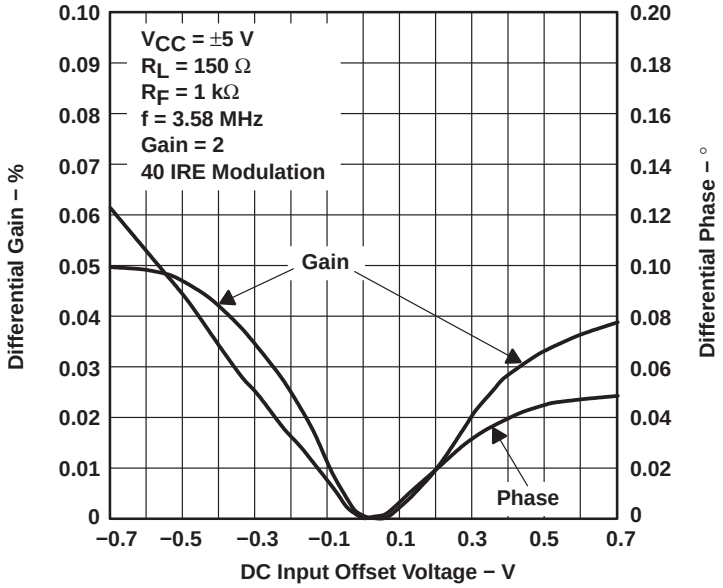



**Figure 46**

**RECEIVER**
**DIFFERENTIAL GAIN AND PHASE**
**vs**
**NUMBER OF 150-Ω LOADS**

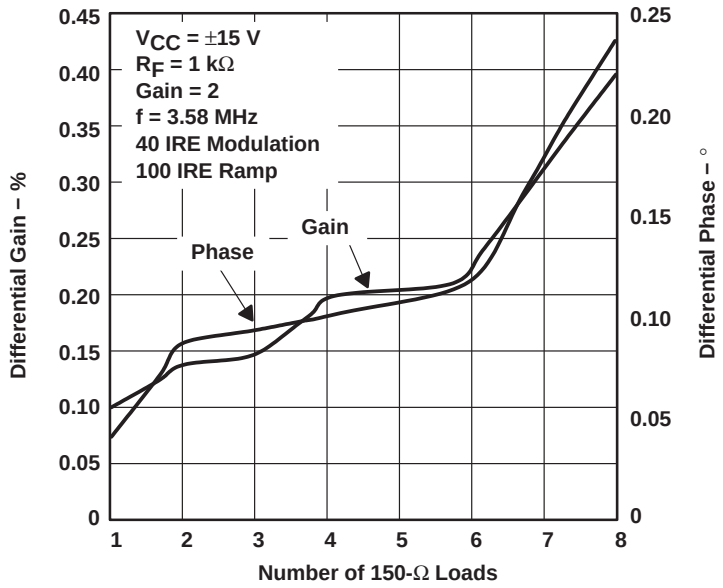



**Figure 47**

## TYPICAL CHARACTERISTICS

**RECEIVER**
**DIFFERENTIAL GAIN AND PHASE**
**vs**
**NUMBER OF 150-Ω LOADS**

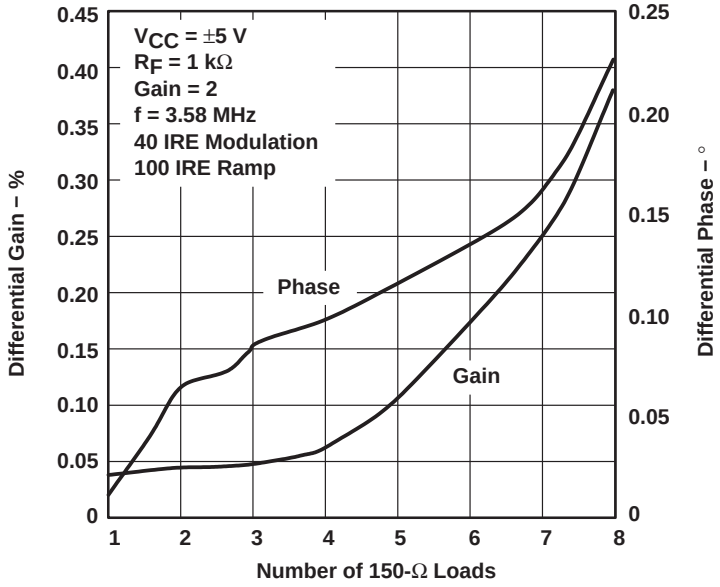



**Figure 48**

**RECEIVER OUTPUT**
**400-mV STEP RESPONSE**

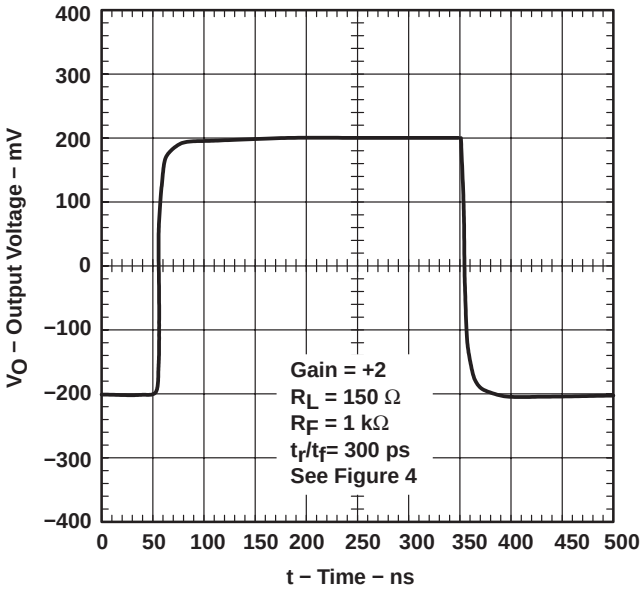



**Figure 49**

**RECEIVER OUTPUT**
**10-V STEP RESPONSE**

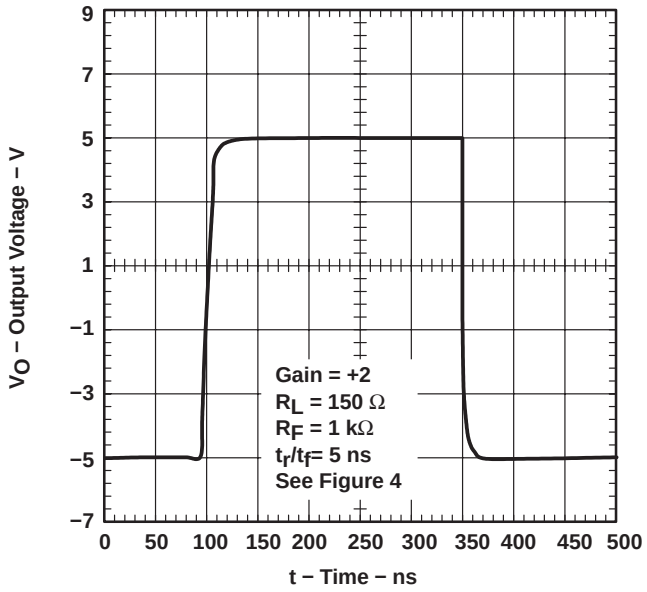



**Figure 50**

## TYPICAL CHARACTERISTICS

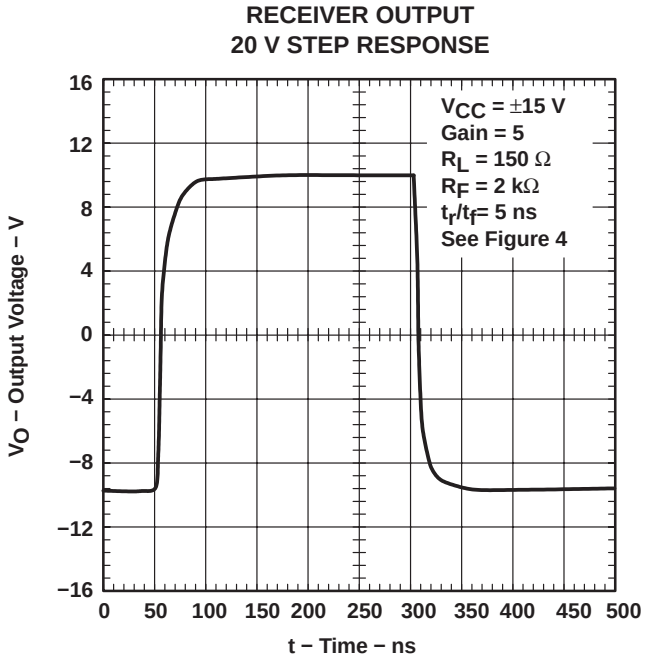



**Figure 51**

## APPLICATION INFORMATION

The THS6002 contains four independent operational amplifiers. Two are designated as drivers because of their high output current capability, and two are designated as receivers. The receiver amplifiers are current feedback topology amplifiers made for high-speed operation and are capable of driving output loads of at least 80 mA. The drivers are also current feedback topology amplifiers. However, the drivers have been specifically designed to deliver the full power requirements of ADSL and therefore can deliver output currents of at least 400 mA at full output voltage.

The THS6002 is fabricated using Texas Instruments 30-V complementary bipolar process, HVBiCOM. This process provides excellent isolation and high slew rates that result in the device's excellent crosstalk and extremely low distortion.

### independent power supplies

Each amplifier of the THS6002 has its own power supply pins. This was specifically done to solve a problem that often occurs when multiple devices in the same package share common power pins. This problem is crosstalk between the individual devices caused by currents flowing in common connections. Whenever the current required by one device flows through a common connection shared with another device, this current, in conjunction with the impedance in the shared line, produces an unwanted voltage on the power supply. Proper power supply decoupling and good device power supply rejection helps to reduce this unwanted signal. What is left is crosstalk.

However, with independent power supply pins for each device, the effects of crosstalk through common impedance in the power supplies is more easily managed. This is because it is much easier to achieve low common impedance on the PCB with copper etch than it is to achieve low impedance within the package with either bond wires or metal traces on silicon.

## APPLICATION INFORMATION

### power supply restrictions

Although the THS6002 is specified for operation from power supplies of ±5 V to ±15 V (or singled-ended power supply operation from 10 V to 30 V), and each amplifier has its own power supply pins, several precautions must be taken to assure proper operation.

1. The power supplies for each amplifier must be the same value. For example, if the drivers use ±15 volts, then the receivers must also use ±15 volts. Using ±15 volts for one amplifier and ±5 volts for another amplifier is not allowed.
2. To save power by powering down some of the amplifiers in the package, the following rules must be followed.
   - The amplifier designated Receiver 1 must always receive power whenever any other amplifier(s) within the package is used. This is because the internal startup circuitry uses the power from the Receiver 1 device.
   - The $-V_{CC}$ pins from all four devices must always be at the same potential.
   - Individual amplifiers are powered down by simply opening the $+V_{CC}$ connection.

As an example, if only the two drivers within the THS6002 are used, then the package power is reduced by removing the $+V_{CC}$ connection to Receiver 2. This reduces the power consumption by an amount equal to the quiescent power of a single receiver amplifier. The $+V_{CC}$ connections to Receiver 1 and both drivers are required. Also, all four amplifiers must be connected to $-V_{CC}$, including Receiver 2.

The THS6002 incorporates a standard Class A-B output stage. This means that some of the quiescent current is directed to the load as the load current increases. So under heavy load conditions, accurate power dissipation calculations are best achieved through actual measurements. For small loads, however, internal power dissipation for each amplifier in the THS6002 can be approximated by the following formula:

$$P_D \cong \left(2\, V_{CC}\, I_{CC}\right) + \left(V_{CC} - V_O\right) \times \left(\frac{V_O}{R_L}\right)$$

Where:

$P_D$ = power dissipation for one amplifier
$V_{CC}$ = split supply voltage
$I_{CC}$ = supply current for that particular amplifier
$V_O$ = output voltage of amplifier
$R_L$ = load resistance

To find the total THS6002 power dissipation, we simply sum up all four amplifier power dissipation results. Generally, the worst case power dissipation occurs when the output voltage is one-half the $V_{CC}$ voltage. One last note, which is often overlooked: the feedback resistor ($R_F$) is also a load to the output of the amplifier and should be taken into account for low value feedback resistors.

## APPLICATION INFORMATION

### device protection features

The THS6002 has two built-in protection features that protect the device against improper operation. The first protection mechanism is output current limiting. Should the output become shorted to ground the output current is automatically limited to the value given in the data sheet. While this protects the output against excessive current, the device internal power dissipation increases due to the high current and large voltage drop across the output transistors. Continuous output shorts are not recommended and could damage the device. Additionally, connection of the amplifier output to one of the supply rails ($\pm V_{CC}$) can cause failure of the device and is not recommended.

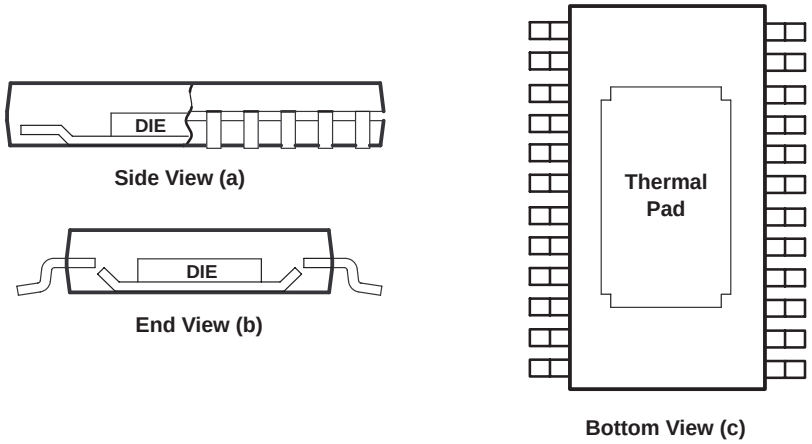
The second built-in protection feature is thermal shutdown. Should the internal junction temperature rise above approximately 180°C, the device automatically shuts down. Such a condition could exist with improper heat sinking or if the output is shorted to ground. When the abnormal condition is fixed, the internal thermal shutdown circuit automatically turns the device back on.

### thermal information

The THS6002 is packaged in a thermally-enhanced DWP package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 52(a) and Figure 52(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 52(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. This is discussed in more detail in the *PCB design considerations* section of this document.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.




NOTE A: The thermal pad is electrically isolated from all terminals in the package.

**Figure 52. Views of Thermally Enhanced DWP Package**

## APPLICATION INFORMATION

### recommended feedback and gain resistor values

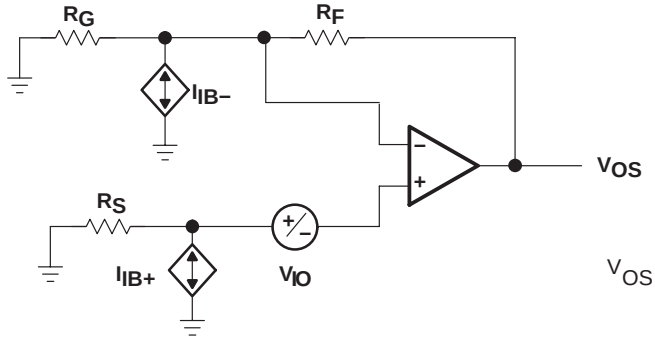
As with all current feedback amplifiers, the bandwidth of the THS6002 is an inversely proportional function of the value of the feedback resistor. This can be seen from Figures 17 and 18. For the driver, the recommended resistors for the optimum frequency response for a 25-Ω load system are 680-Ω for a gain = 1 and 620-Ω for a gain = 2 or −1. For the receivers, the recommended resistors for the optimum frequency response are 560 Ω for a gain = 1 and 390 Ω for a gain = 2 or −1. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics. Because there is a finite amount of output resistance of the operational amplifier, load resistance can play a major part in frequency response. This is especially true with the drivers, which tend to drive low-impedance loads. This can be seen in Figure 7, Figure 19, and Figure 20. As the load resistance increases, the output resistance of the amplifier becomes less dominant at high frequencies. To compensate for this, the feedback resistor should change. For 100-Ω loads, it is recommended that the feedback resistor be changed to 820 Ω for a gain of 1 and 560 Ω for a gain of 2 or −1. Although, for most applications, a feedback resistor value of 1 kΩ is recommended, which is a good compromise between bandwidth and phase margin that yields a very stable amplifier.

Consistent with current feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and internal dominant-pole capacitor. The ability to control the amplifier gain independently of the bandwidth constitutes a major advantage of current feedback amplifiers over conventional voltage feedback amplifiers. Therefore, once a frequency response is found suitable to a particular application, adjust the value of the gain resistor to increase or decrease the overall amplifier gain.

Finally, it is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third order harmonic distortion increases more than the second order harmonic distortion.

### offset voltage

The output offset voltage, ($V_{OO}$) is the sum of the input offset voltage ($V_{IO}$) and both input bias currents ($I_{IB}$) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:




$$V_{OS} = \left(\pm V_{IO} \pm I_{IB+} R_S\right)\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-} R_F$$

**Figure 53. Output Offset Voltage Model**

## APPLICATION INFORMATION

### noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true for the receiver amplifiers which are generally used for amplifying small signals coming over a transmission line. The noise model for current feedback amplifiers (CFB) is the same as voltage feedback amplifiers (VFB). The only difference between the two is that the CFB amplifiers generally specify different current noise parameters for each input while VFB amplifiers usually only specify one noise current parameter. The noise model is shown in Figure 54. This model includes all of the noise sources as follows:

- $e_n$ = amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = noninverting current noise (pA/$\sqrt{Hz}$)
- IN− = inverting current noise (pA/$\sqrt{Hz}$)
- $e_{Rx}$ = thermal voltage noise associated with each resistor ($e_{Rx} = 4\ kTR_x$)

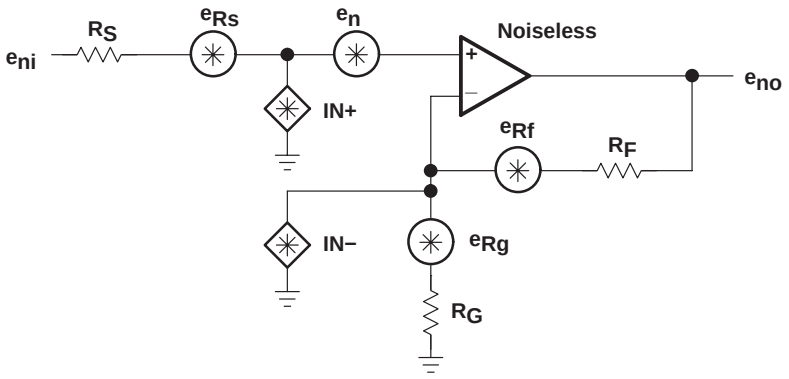



**Figure 54. Noise Model**

The total equivalent input noise density ($e_{ni}$) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_S + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = $1.380658 \times 10^{-23}$
T = temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = parallel resistance of $R_F$ and $R_G$

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density ($e_{ni}$) by the overall amplifier gain ($A_V$).

$$e_{no} = e_{ni}\,A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

## APPLICATION INFORMATION

### noise calculations and noise figure (continued)

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing $R_G$), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor ($R_S$) and the internal amplifier noise voltage ($e_n$). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{e_{Rs}}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\,kTR_S}\right]$$

The Figure 55 shows the noise figure graph for the THS6002.

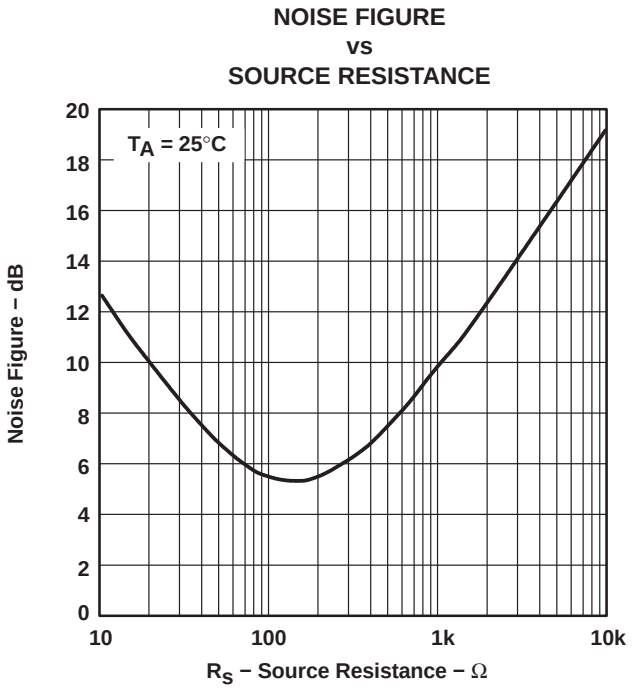



**Figure 55. Noise Figure vs. Source Resistance**

## APPLICATION INFORMATION

### PCB design considerations

Proper PCB design techniques in two areas are important to assure proper operation of the THS6002. These areas are high-speed layout techniques and thermal-management techniques. Because the THS6002 is a high-speed part, the following guidelines are recommended.

- Ground plane − It is essential that a ground plane be used on the board to provide all components with a low inductive ground connection. Although a ground connection directly to a terminal of the THS6002 is not necessarily required, it is recommended that the thermal pad of the package be tied to ground. This serves two functions. It provides a low inductive ground to the device substrate to minimize internal crosstalk and it provides the path for heat removal.
- Input stray capacitance − To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane must be removed under any etch runs connected to the inverting input, and external components should be placed as close as possible to the inverting input. This is especially true in the noninverting configuration. An example of this can be seen in Figure 56, which shows what happens when 1.8 pF is added to the inverting input terminal in the noninverting configuration. The bandwidth increases dramatically at the expense of peaking. This is because some of the error current is flowing through the stray capacitor instead of the inverting node of the amplifier. Although, in the inverting mode, stray capacitance at the inverting input has little effect. This is because the inverting node is at a *virtual ground* and the voltage does not fluctuate nearly as much as in the noninverting configuration.

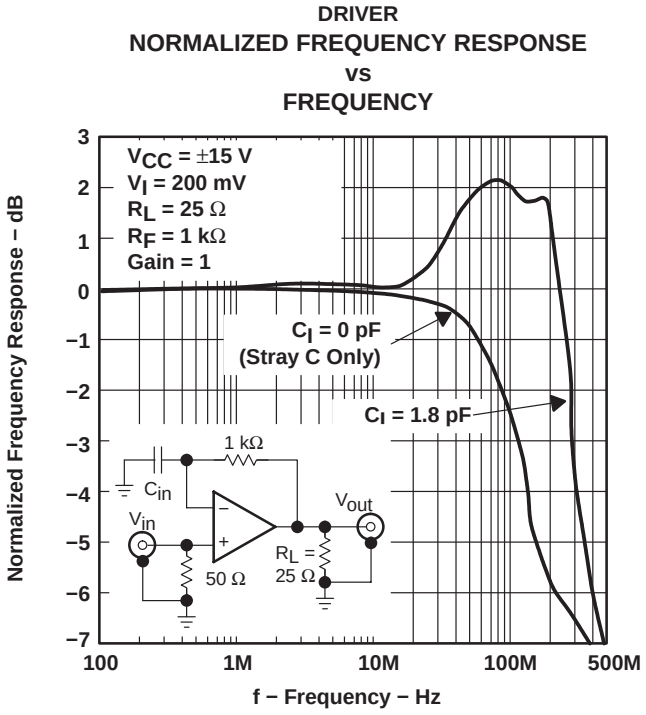



**Figure 56. Driver Normalized Frequency Response vs. Frequency**



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## APPLICATION INFORMATION

### PCB design considerations (continued)

- Proper power supply decoupling − Use a minimum of a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches (2,54 mm) between the device power terminal and the ceramic capacitors.

Because of its power dissipation, proper thermal management of the THS6002 is required. Although there are many ways to properly heatsink this device, the following steps illustrate one recommended approach for a multilayer PCB with an internal ground plane.

1. Prepare the PCB with a top side etch pattern as shown in Figure 57. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils (0,33 mm) in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
3. Place four more holes under the package, but outside the thermal pad area. These holes are 25 mils (0,635 mm) in diameter. They may be larger because they are not in the area to be soldered so that wicking is not a problem.
4. Connect all nine holes, the five within the thermal pad area and the four outside the pad area, to the internal ground plane.
5. When connecting these holes to the ground plane, do **not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6002 package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole.
6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area with its five holes. The four larger holes outside the thermal pad area, but still under the package, should be covered with solder mask.
7. Apply solder paste to the exposed thermal pad area and all of the operational amplifier terminals.
8. With these preparatory steps in place, the THS6002 is simply placed in position and run through the solder reflow operation as any standard surface mount component. This results in a part that is properly installed.

## APPLICATION INFORMATION

### PCB design considerations (continued)

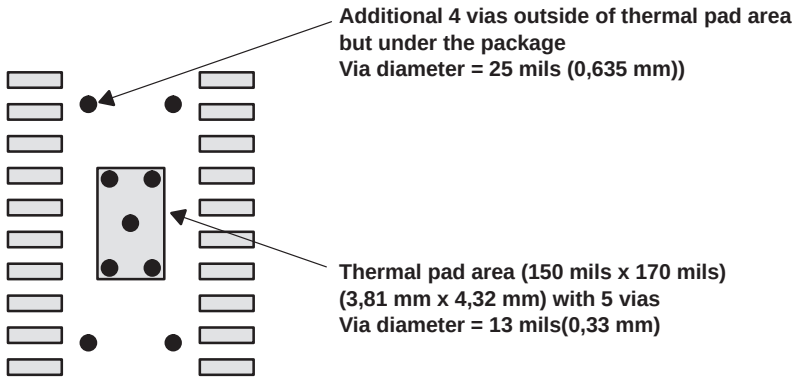



**Figure 57. PowerPad PCB Etch and Via Pattern**

The actual thermal performance achieved with the THS6002 in its PowerPAD package depends on the application. In the previous example, if the size of the internal ground plane is approximately 3 inches × 3 inches (76,2 mm x 76,2 mm), then the expected thermal coefficient, $\theta_{JA}$, is about 21.5°C/W. For a given $\theta_{JA}$, the maximum power dissipation is shown in Figure 58 and is calculated by the following formula:

$$P_D = \left( \frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

$P_D$ = Maximum power dissipation of THS6002 (watts)
$T_{MAX}$ = Absolute maximum junction temperature (150°C)
$T_A$ = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
$\theta_{JC}$ = Thermal coefficient from junction to case (0.37°C/W)
$\theta_{CA}$ = Thermal coefficient from case to ambient

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

## APPLICATION INFORMATION

### PCB design considerations (continued)

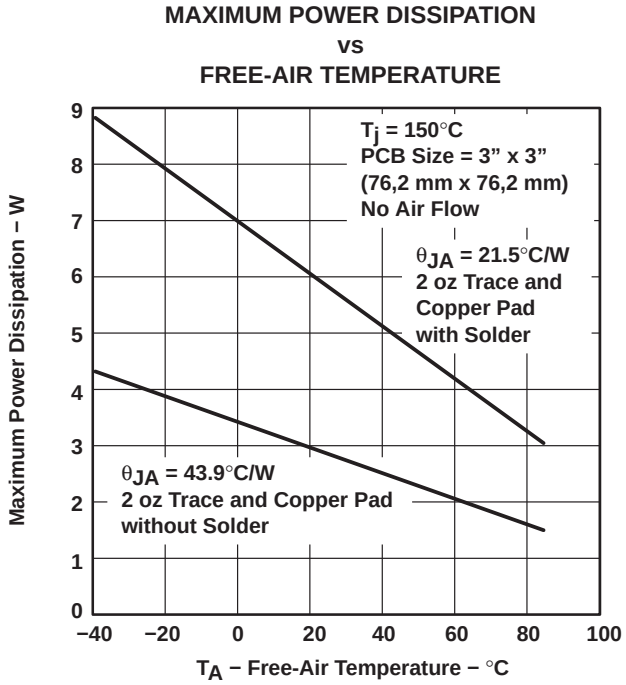



**Figure 58. Maximum Power Dissipation vs Free-Air Temperature**

## APPLICATION INFORMATION

### ADSL

The THS6002 was primarily designed as a line driver and line receiver for ADSL (asymmetrical digital subscriber line). The driver output stage has been sized to provide full ADSL power levels of 20 dBm onto the telephone lines. Although actual driver output peak voltages and currents vary with each particular ADSL application, the THS6002 is specified for a minimum full output current of 400 mA at its full output voltage of approximately 12 V. This performance meets the demanding needs of ADSL at the central office end of the telephone line. A typical ADSL schematic is shown in Figure 59.

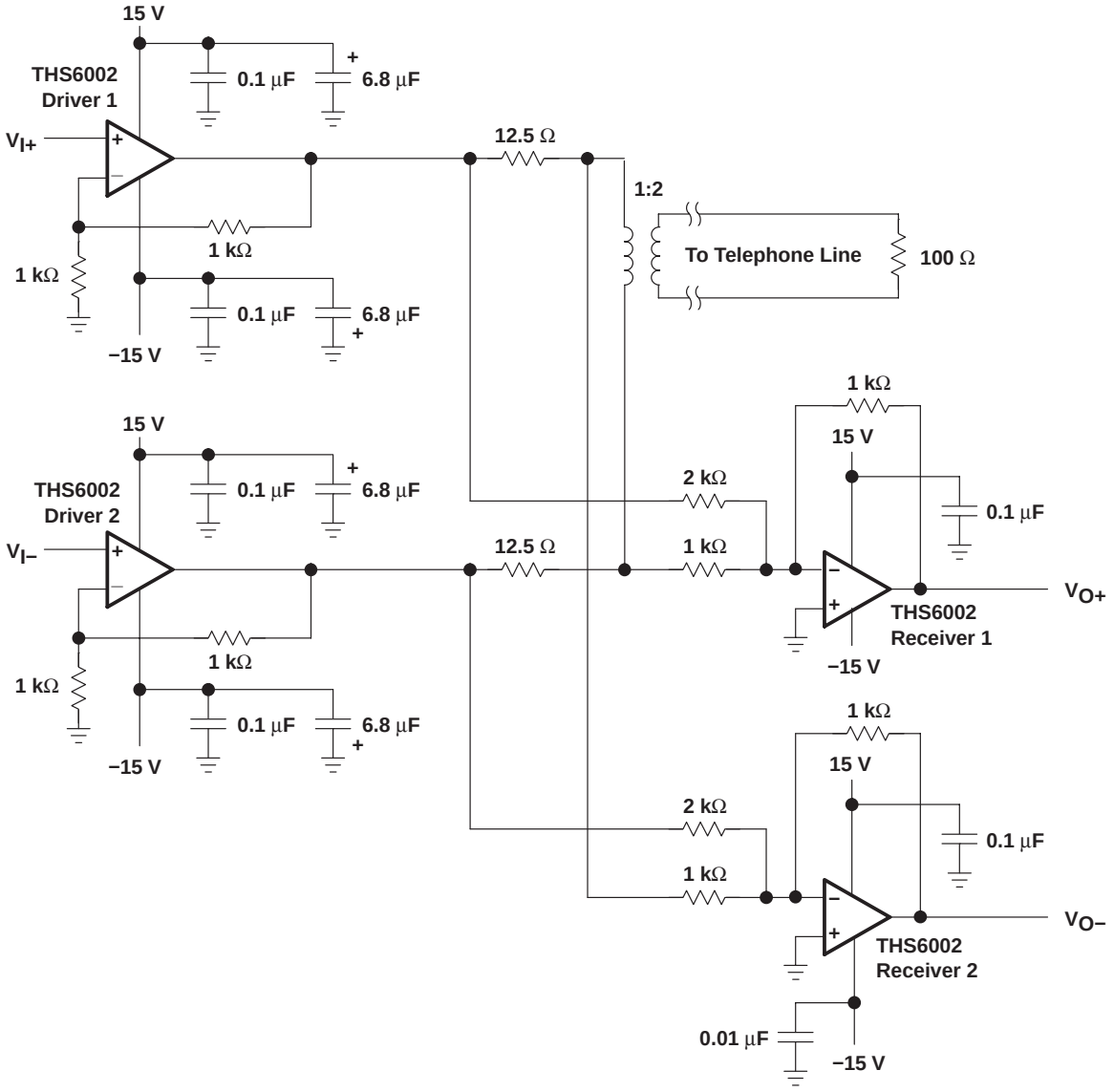



**Figure 59. THS6002 ADSL Application**

## APPLICATION INFORMATION

### ADSL (continued)

The ADSL transmit band consists of 255 separate carrier frequencies each with its own modulation and amplitude level. With such an implementation, it is imperative that signals put onto the telephone line have as low a distortion as possible. This is because any distortion either interferes directly with other ADSL carrier frequencies or it creates intermodulation products that interfere with ADSL carrier frequencies.

The THS6002 has been specifically designed for ultra low distortion by careful circuit implementation and by taking advantage of the superb characteristics of the complementary bipolar process. Driver single-ended distortion measurements are shown in Figure 23. It is commonly known that in the differential driver configuration, the second order harmonics tend to cancel out. Thus, the dominant total harmonic distortion (THD) will be primarily due to the third order harmonics. For this test, the load was 25 Ω and the output signal produced a 20 $V_{O(PP)}$ signal. Thus, the test was run at full signal and full load conditions. Because the feedback resistor used for the test was 4 kΩ, the distortion numbers are actually in a worst-case scenario. Distortion should be reduced as the feedback resistance drops. This is because the bandwidth of the amplifier increases dramatically, which allows the amplifier to react faster to any nonlinearities in the closed-loop system.

Another significant point is the fact that distortion decreases as the impedance load increases. This is because the output resistance of the amplifier becomes less significant as compared to the output load resistance.

## APPLICATION INFORMATION

### HDSL

Shown in Figure 60 is an example of the THS6002 being used for HDSL-2 applications. The receiver amplifiers within the THS6002 have been configured as predrivers for the driver amplifiers. This dual composite amplifier setup has the effect of raising the open loop gain for the combination of both amplifiers, thereby giving improved distortion performance.

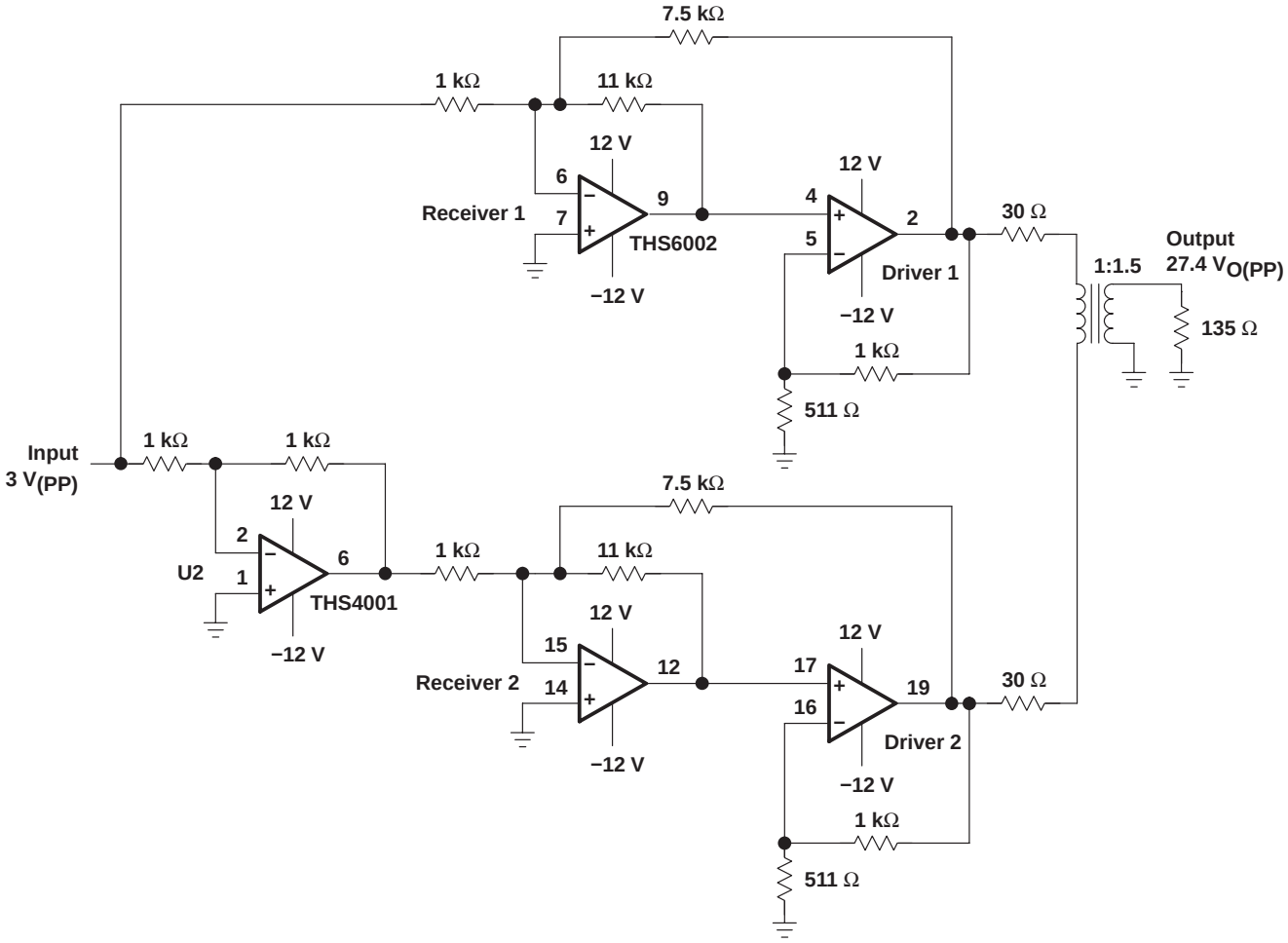


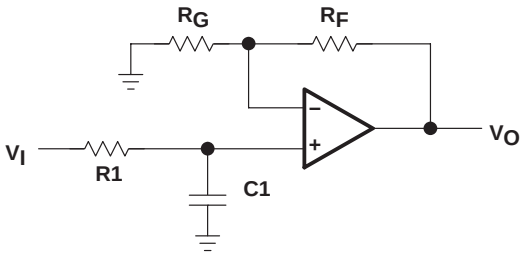

**Figure 60. HDSL-2 Line Driver**

### general configurations

A common error for the first-time CFB user is to create a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration is now commonly referred to as an oscillator. The THS6002, like all CFB amplifiers, **must** have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 61).

## APPLICATION INFORMATION

### general configurations (continued)

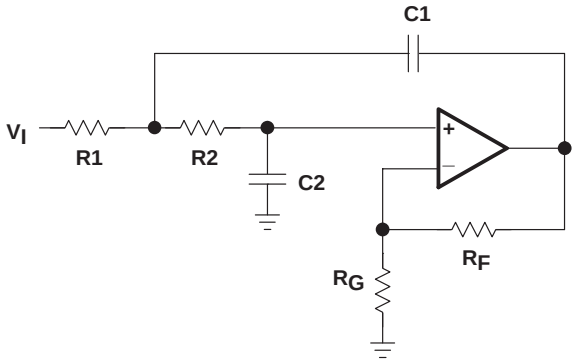



$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

**Figure 61. Single-Pole Low-Pass Filter**

If a multiple pole filter is required, the use of a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. An example is shown in Figure 62.



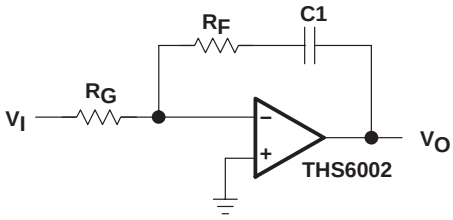

R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

**Figure 62. 2-Pole Low-Pass Sallen-Key Filter**

There are two simple ways to create an integrator with a CFB amplifier. The first one shown in Figure 63 adds a resistor in series with the capacitor. This is acceptable because at high frequencies, the resistor is dominant and the feedback impedance never drops below the resistor value. The second one shown in Figure 64 uses positive feedback to create the integration. Caution is advised because oscillations can occur because of the positive feedback.

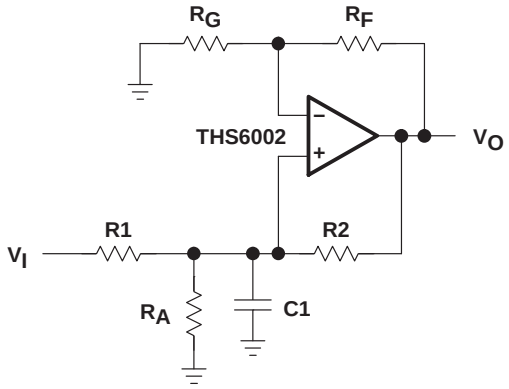



$$\frac{V_O}{V_I} = \left(\frac{R_F}{R_G}\right)\left(\frac{S + \frac{1}{R_F C1}}{S}\right)$$

**Figure 63. Inverting CFB Integrator**

## APPLICATION INFORMATION

### general configurations (continued)




**For Stable Operation:**

$$\frac{R2}{R1 \parallel R_A} \geq \frac{R_F}{R_G}$$

$$V_O \cong V_I \left( \frac{1 + \frac{R_F}{R_G}}{sR1C1} \right)$$

**Figure 64. Non-Inverting CFB Integrator**

Another good use for the THS6002 driver amplifiers are as very good video distribution amplifiers. One characteristic of distribution amplifiers is the fact that the differential phase (DP) and the differential gain (DG) are compromised as the number of lines increases and the closed-loop gain increases. Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| THS6002CDWP | ACTIVE | SO PowerPAD | DWP | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | THS6002C | Samples |
| THS6002CDWPG4 | ACTIVE | SO PowerPAD | DWP | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | THS6002C | Samples |
| THS6002IDWP | ACTIVE | SO PowerPAD | DWP | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | THS6002I | Samples |
| THS6002IDWPR | ACTIVE | SO PowerPAD | DWP | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | THS6002I | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

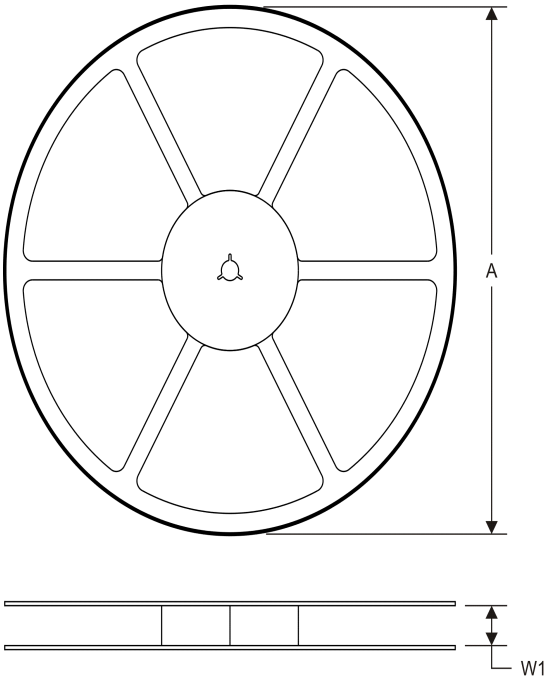
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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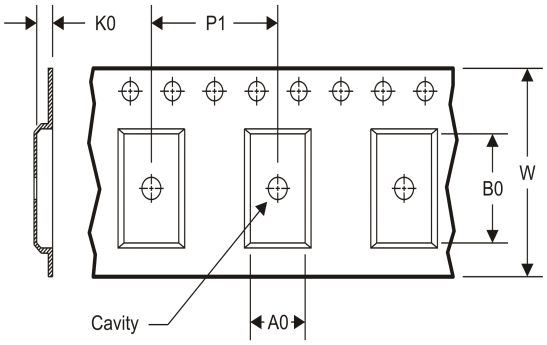
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



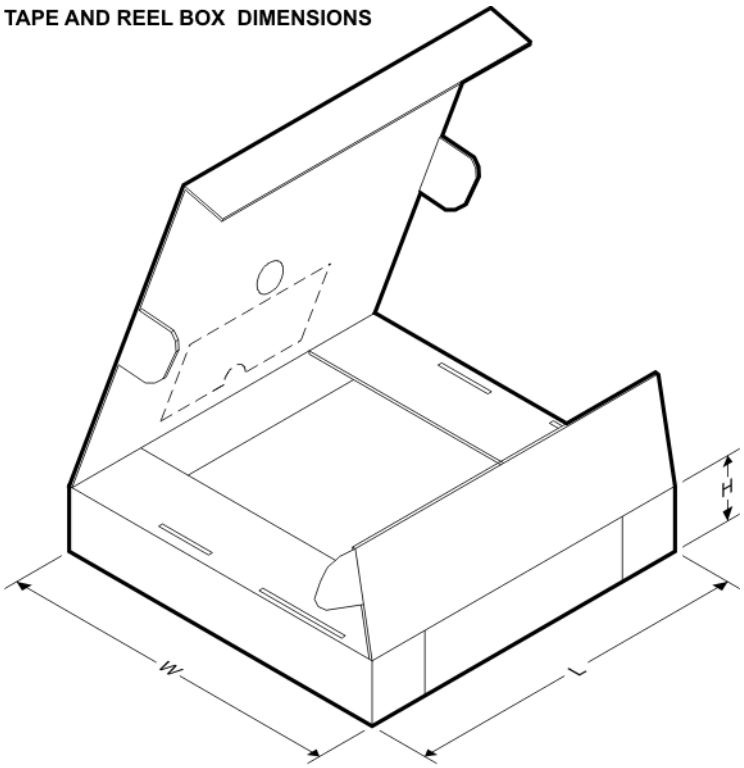

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| THS6002IDWPR | SO Power PAD | DWP | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

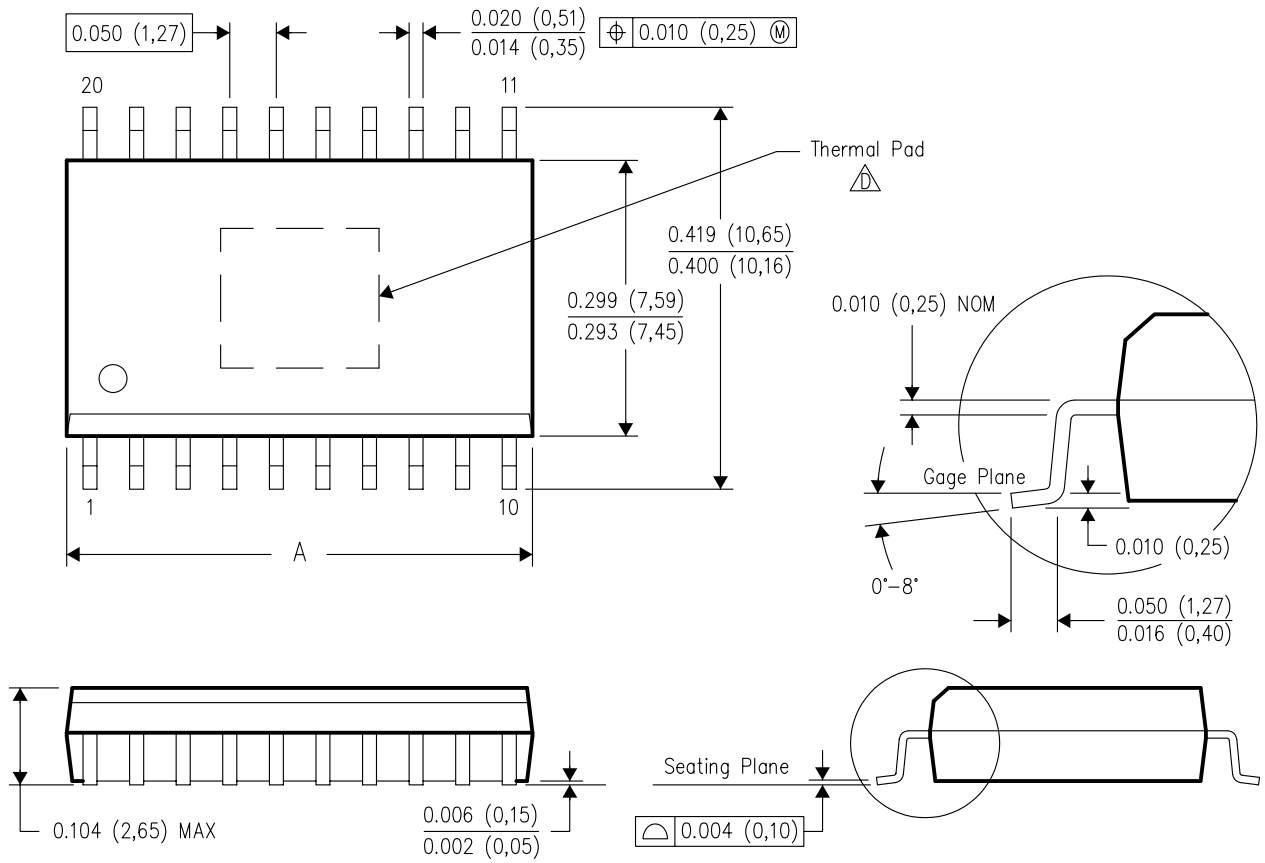



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| THS6002IDWPR | SO PowerPAD | DWP | 20 | 2000 | 367.0 | 367.0 | 45.0 |

## DWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PINS SHOWN




| DIM \ PINS ** | 16 | 20 | 24 | 28 |
|---|---|---|---|---|
| A MAX | 0.410 (10,41) | 0.510 (12,95) | 0.610 (15,49) | 0.710 (18,03) |
| A MIN | 0.400 (10,16) | 0.500 (12,70) | 0.600 (15,24) | 0.700 (17,78) |

4147575/C 02/05

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

**PowerPAD is a trademark of Texas Instruments.**

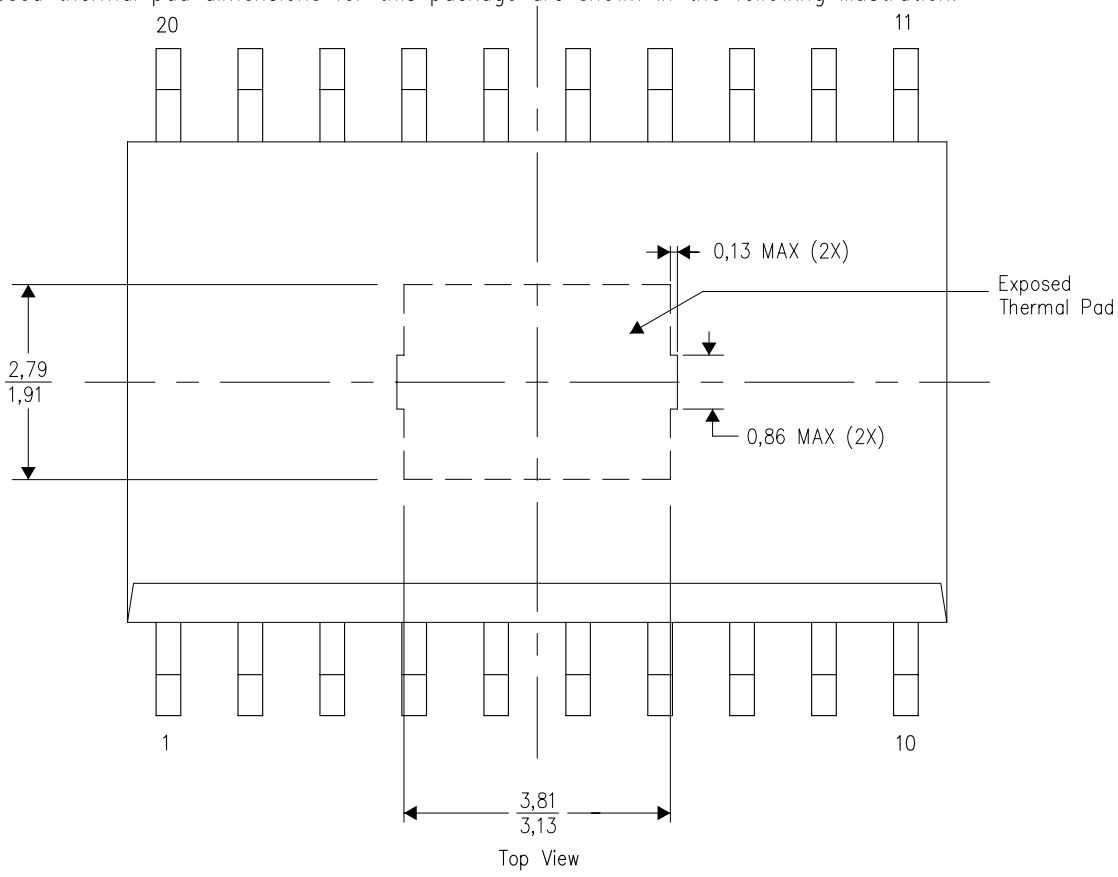
DWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

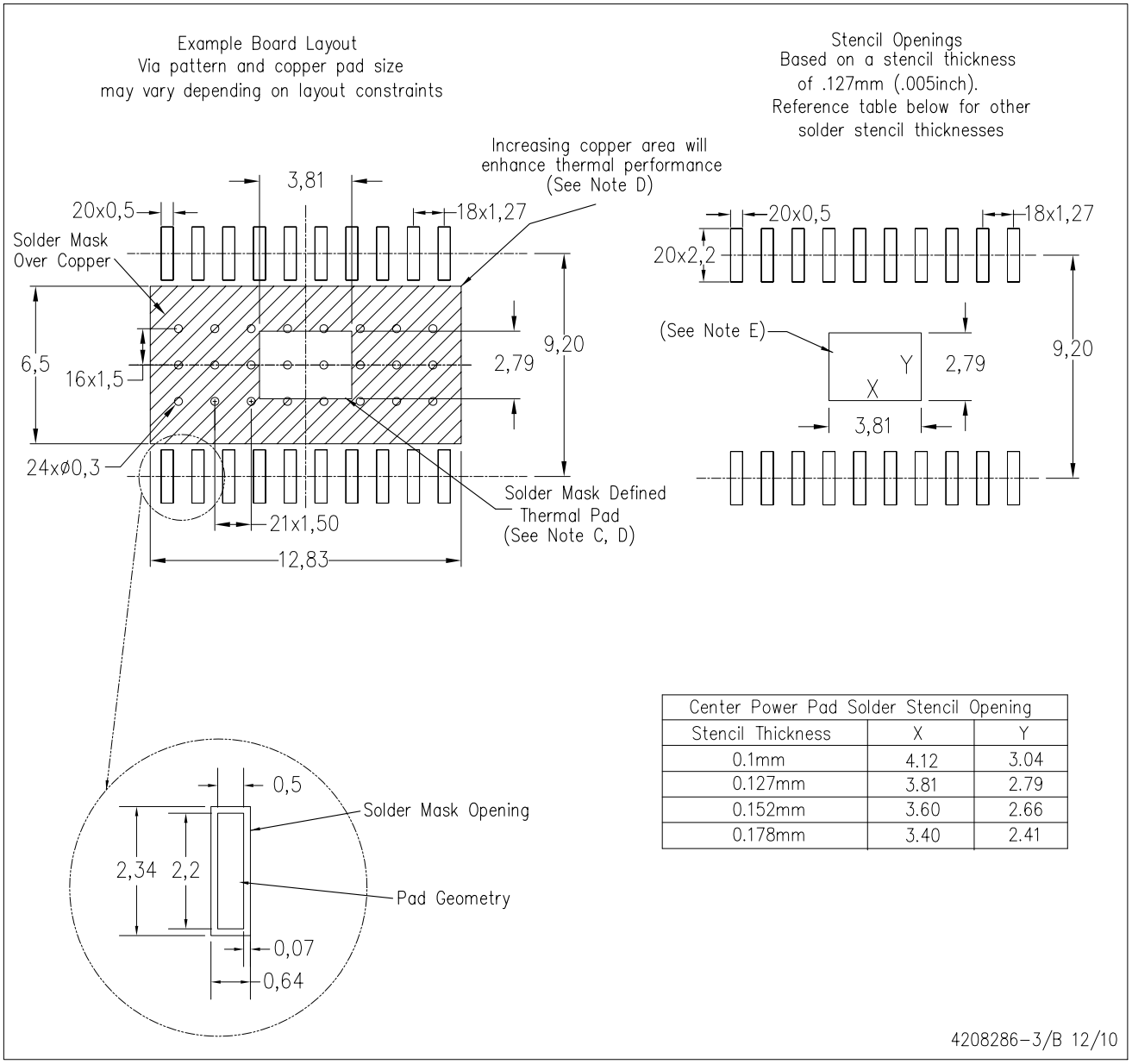



Exposed Thermal Pad Dimensions

4206325–4/E 12/10

NOTE: A. All linear dimensions are in millimeters

DWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 4.12 | 3.04 |
| 0.127mm | 3.81 | 2.79 |
| 0.152mm | 3.60 | 2.66 |
| 0.178mm | 3.40 | 2.41 |

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste.

PowerPAD is a trademark of Texas Instruments.

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