PI90SD1636A

SERDES Gigabit Ethernet Transceiver

Features

- IEEE 802.3z Gigabit Ethernet Compliant
- Supports 1.25 Gbps Using NRZ Coding over uncompensated twin coax cable
- Fully integrated CMOS IC
- Low Power Consumption
- ESD rating >2000V (Human Body Model) or > 200V (Machine Model)
- 5-Volt Input Tolerance
- Pin-Compatible with Agilent HDMP1636A/HDMP- 1646A and Vitesse VSC7123 transceivers (see Appendix A)
- Packaging (Pb-free & Green available):
  - 64-pin LQFP (FC)
  - 64-pin LQFP (FD)

Applications

- Gigabit Ethernet
- Serial Backplane
- Proprietary point-to-point applicaitons

Description

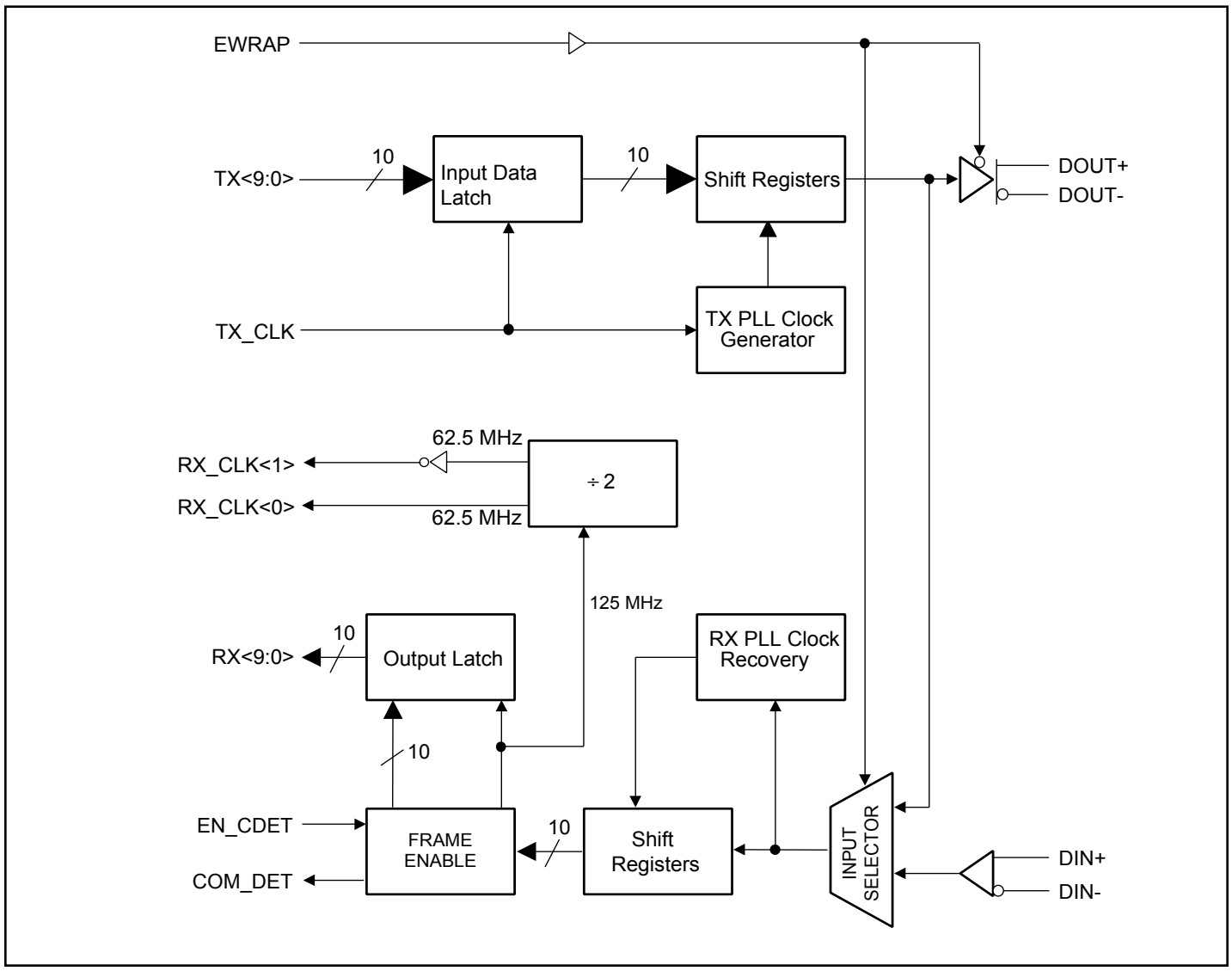
The PI90SD1636A is a single chip, Gigabit Ethernet transceiver. It performs all the functions of the Physical Medium Attachment (PMA) portion of the Physical layer, as specified by the IEEE 802.3z Gigabit Ethernet standard. These functions include parallel-to-serial and serial-to-parallel conversion, clock generation, clock data recovery, and word synchronization. In addition, an internal loopback function is provided for system debugging.

The PI90SD1636A is ideal for Gigabit Ethernet, serial backplane and proprietary point-to-point applications. The device supports 1000BASE-LX and 1000BASE-SX fiber-optic media, and 1000BASE-CX copper media.

The transmitter section of the PI90SD1636A accepts 10-bit wide parallel TTL data and converts it to a high speed serial data stream. The parallel data is encoded in 8b/10b format. This incoming parallel data is latched into an input register, and synchronized on the rising edge of the 125 MHz reference clock supplied by the user. A phase locked loop (PLL) locks to the 125 MHz clock. The clock is then multiplied by 10 to produce a 1.25 GHz serial clock that is used to provide the high speed serial data output. The output is sent through a Pseudo Emitter Coupled Logic (PECL) driver. This output connects directly to a copper cable in the case of 1000BASE-CX medium, or to a fiber optic module in the case of 1000BASE-LX or 1000BASE SX fiber optic medium.

The receiver section of the PI90SD1636A accepts a serial PECL-compatible data stream at a 1.25 Gbps rate, recovers the original 10-bit wide parallel data format, and retimes the data. A PLL locks onto the incoming serial data stream, and recovers the 1.25 GHz high speed serial clock and data. This is accomplished by continually frequency locking onto the 125 MHz reference clock, and by phase locking onto the incoming data stream. The serial data is converted back to parallel data format. The ‘comma’ character is used to establish byte alignment. Two 62.5 MHz clocks, 180 degrees out of phase, are recovered. These clocks are alternately used to clock out the parallel data on the rising edge. This parallel data is sent to the user in TTL-compatible form.

Functional Block Diagram



Pin Configuration

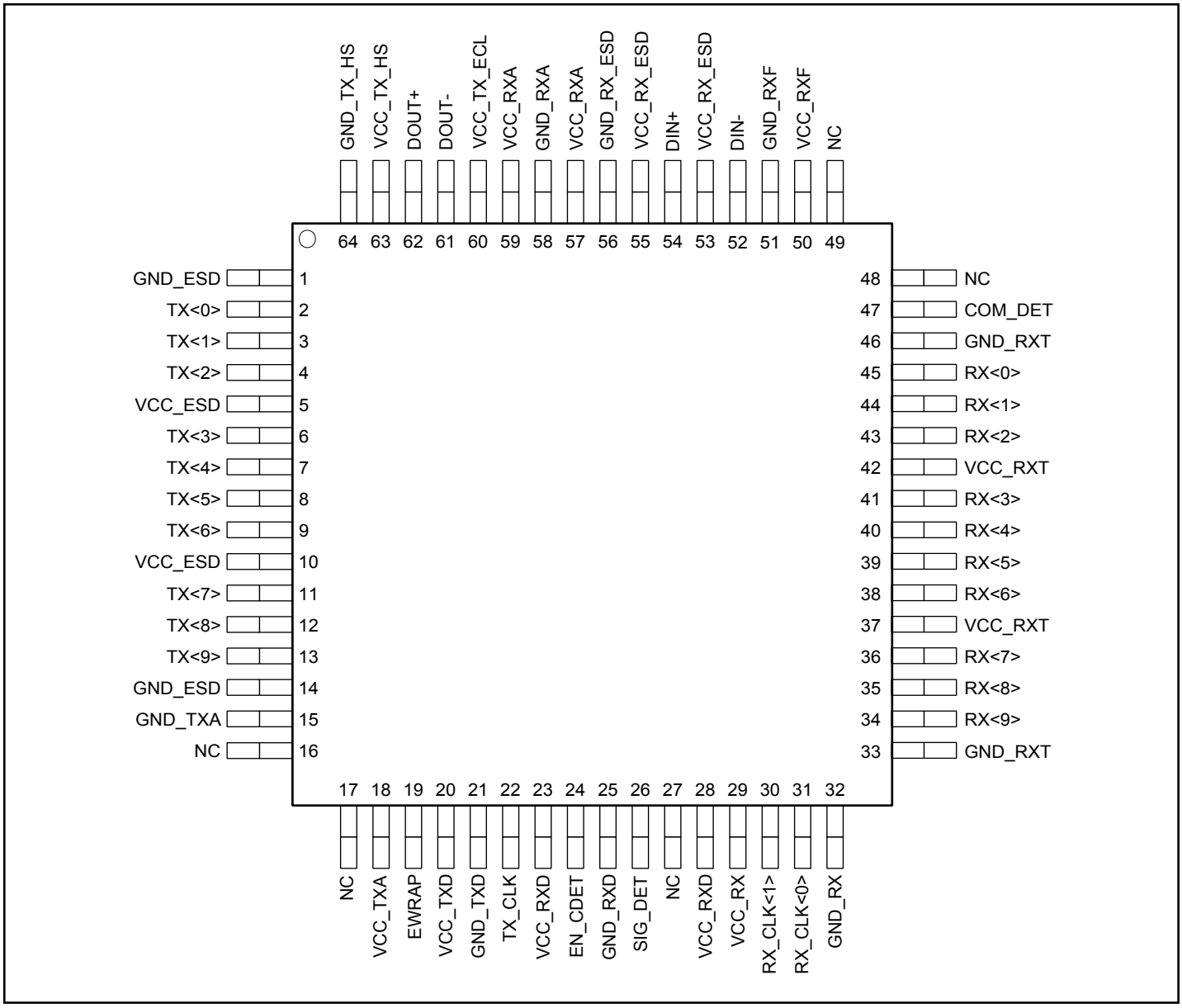


Table 1. I/O Type Definitions

Type	Definition
TTL_IN	TTL Input
TTL_OUT	TTL Output
HS_IN	Hight-Speed Input
HS_OUT	High-Speed Output
P	Power Ground

Table 2. Pin Description

Name	Pin #	Type	Description
GND_ESD VCC_ESD	1, 14 5, 10	P	Power and ground pairs for pad ESD structure.
TX<0> TX<1> TX<2> TX<3> TX<4> TX<5> TX<6> TX<7> TX<8> TX<9>	2 3 4 6 7 8 9 11 12 13	TTL_IN	**0-bit parallel data input pins**. This data should be 10b/8b encoded. The least significant bit is TX<0> and is transmitted first.
GND_TXA VCC_TXA	15 18	P	Power and ground pair for TX PLL analog circuits.
NC	16, 17,27, 48, 49	NC	No Connect
EWRAP	19	TTL_IN	**Wrap Enable**. This pin is active HIGH. When asserted, the high-speed serial data are internally wrapped from the transmitter serial data output back to the receiver data input. Also, when asserted, DOUT± are held static at logic 1. When deasserted, DOUT± and .DIN± are active.
VCC_TXD GND_TXD	20 21	P	Power and ground pair for TX digital circuits.
TX_CLK	22	TTL_IN	**Reference clock and transmit byte clock**. This is a 125 MHz system clock supplied by the host system. On the positive edge of the clock, the input data, TX<9:0>, are latched into the register. This clock is multiplied by 10 internally, to generate the transmit serial bit clock.
VCC_RXD GND_RXD	23 28, 25	P	Power and ground pair for digital circuits in the receiver portion.
EN_CDET	24	TTL_IN	**Comma Detect Enable**. This pin is active HIGH. When asserted, the internal byte alignment function is turned on, to allow the clock to synchronize with the comma character (0011111XXX). When de-asserted, the function is disabled and will not align the clock and data. In this mode COM_DET is set to LOW.
SIG_DET	26	TTL_ OUT	**Signal Detect**. This pin is active HIGH. It indicates the loss of input signal on the high-speed serial inputs, DIN±. SIG_DET is set to LOW when differential inputs are less than 50 mV.
VCC_RX GND_RX	29 32	P	Power and ground pair for the clock signal of the receiver portion.
RX_CLK<1> RX_CLK<0>	30 31	TTL_ OUT	**Receiver Byte Clocks**. Two 180 degrees out-of-phase 62.5 MHz clock signals that are recovered by the receiver section. The received bytes are alternately clocked by the rising edges of these signals. The rising edge of RX_CLK<1> aligns with a comma character when detected.

Table 2. Pin Description (Continued.)

Name	Pin#	Type	Description
GND_RXT VCC_RXT	33 46, 37, 42	P	Power and ground pairs for ESD structure.
RX<9> RX<8> RX<7> RX<6> RX<5> RX<4> RX<3> RX<2> RX<1> RX<0>	34 35 36 37 38 39 40 41 43 44 45	TTL_OUT	**Received Parallel Data Output**. RX<0> is the least significant bit and is received first. When DIN± lose input data, all RX pins will be held HIGH.
COM_DET	47	TTL_OUT	**Comma detect**. This pin is active HIGH. When asserted, it indicates the detection of comma character (0011111XXX). It is active only when EN_CEDT is enabled.
VCC_RXF GND_RXF	50 51	P	Power and ground pair for the front-end of the receiver section.
DIN-	52	HS_IN	**High-speed serial data input**. Serial data input is received when
DIN+	54		EWRAP is disabled.
VCC_RXESD GND_RXESD	53,55 56	P	Power and ground pair for ESD structure.
VCC_RXA GND_RXA	57, 59 58	P	Power and ground pair for analog circuits of the receiver section.
VCC_TX_ECL	60	P	Power supply to line driver circuits. Ground supply is from pin 64.
DOUT- DOUT+	61 62	HS_OUT	**High-speed serial data output**. These pins are active when EWRAP is disabled and are held static at logic 1 when EWRAP is enable.
VCC_TX_HS GND_TX_HS	63 64	P	Power and ground pair for high-speed transmit logic in the parallel-to-serial section.

Functional Block Description

Input Data Latch

The input data latch block latches the 10-bit TTL input parallel byte, TX<9:0>, on the rising edge of the 125 MHz user-provided TX_CLK into the holding registers.

Parallel-to-Serial Converter

The received 10-bit TTL parallel input byte is converted to serial PECL level data stream by the parallel-to-serial block, and is transmitted differentially to the line driver block at 1.25 Gbps. The 8b/10b encoded data is transmitted sequentially with bit 0 being sent first.

Clock Generator

The 125 MHz signal used for clocking the serial outputs is generated by the TX PLL block based on the user-provided TX_CLK. This clock should have a ±100 ppm tolerance.

Internal Loopback

When EWRAP is set to a logic HIGH, the serial data stream generated by the transmitter is looped back to the receiver path, instead of going out to the DOUT± pins. When in loopback mode, a static logic 1 is transmitted at the line driver (DOUT+ is HIGH and DOUT- is LOW).

Signal Detect

Signal detect block is used to sense the serial input data stream at pins DIN±. If the serial input is lower than 50mV differentially, this block deasserts SIG_DET and sets the output, RX<9:0>, to all logic ones. When the serial input at pins DIN± is greater than 50mV, the signal is directed to the receive path.

Equalizer and Slicer

The signal received from the line (DIN± pins) is distorted by the cable bandwidth. In order to maintain a low bit-error rate, an equalizer is used to compensate for the signal loss. The slicer recovers the differential low-level signal to a CMOS-level single-ended signal, for clock recovery and data re-timing.

Clock Recovery

The serial input data stream contains both data and clock. The clock recovery block is used to extract both data and clocks from this input. In addition to data, two clocks of 62.5 MHz are recovered.

Table 3. Absolute Maximun Ratings

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply voltage	-0.5	5.0	V
$V_{IN,TTL}$	TTL Input Voltage	-0.7	V_{CC} + 2.8	
V_{IN,HS_IN}	High-Speed Input Voltage	2.0	V_{CC}	
$I_{OUT,TTL}$	TTL Output Source Current		13	mA
T_{stg}	Storage Temperature	-65	+150	°C
T_j	Junction Operating Temperature	0	+150	

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4. Guaranteed Operating Rates $T_A = 0^oC$ to $+70^oC$, $V_{CC} = 3.15V$ to $3.45V$

Parallel Clock Rate (MHz)		SerialBaud Rate (Mbaud)	
Min.	Max.	Min.	Max.
124.0	126.0	1240	1260

Table 5. AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 3.15V$ to $3.45V$

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{r,REFCLK}$	REFCLK Rise Time, 0.8 to 2.0 Volts			2.4	ns
$t_{f,REFCLK}$	REFCLK Fall Time, 2.0 to 0.8 Volts			2.4	
t_{r,TTL_IN}	Input TTL Rise Time, 0.8 to 2.0 Volts		2		
t_{f,TTL_IN}	Input TTL Fall Time, 2.0 to 0.8 Volts		2		
t_{r,TTL_OUT}	Output TTL Rise Time, 0.8 to 2.0 Volts, 10 pF Load		1.5	2.4	
t_{f,TTL_OUT}	Output TTL Fall Time, 2.0 to 0.8 Volts, 10 pF Load		1.1	2.4	
t_{rs,HS_OUT}	HS_OUT Single-Ended (DOUT+) Rise Time	85	225	327	ps
t_{fs,HS_OUT}	HS_OUT Single-Ended (DOUT+) Fall Time	85	200	327	
t_{rd,HS_OUT}	HS_OUT Differential Rise Time	85		327	
t_{fd,HS_OUT}	HS_OUT Differential Fall Time	85		327	
V_{IP,HS_IN}	HS_IN Input Peak-to-Peak Differential Voltage	200	1200	2000	mV
V_{OP,HS_OUT}(1)	HS_OUT Output Peak-to-Peak Differential Voltage	1200	1600	2000	

Note:
1. Output Peak-to-Peak Differential Voltage specified as DOUT+ minus DOUT-

Table 6. DC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{IH,TTL}$	TTL Input High Voltage Level, Guaranteed High Signal for All Inputs	2		5.5	V
$V_{IL,TTL}$	TTL Input Low Voltage Level, Guaranteed Low Signal for All Inputs	0		0.8	
$V_{OH,TTL}$	TTL Output High Voltage Level, I_{OH} = -400 mA	2.2		V_{CC}	
$V_{OL,TTL}$	TTL Output Low Voltage Level, I_{OL} = 1 mA	0		0.6	
$I_{IH,TTL}$	Input High Current, V_{IN} = 2.4 V, V_{CC} = 3.45 V			40	µA
$I_{IL,TTL}$	Input Low Current, V_{IN} = 0.4 V, V_{CC} = 3.45 V			-600	
$I_{CC,TRX}$[1,2]	Transceiver V_{CC} Supply Current, TA = 25°C		220		mA

Notes:
1. Measurement Conditions: Tested sending 1250 MBd PRBS 2^7-1 sequence from a serial Bit Error Rate Tester (BERT) with DOUT± outputs terminated with 150Ω resistors to GND.
2. Typical values are at V_{CC} = 3.3 volts.

Table 7. Transceiver Reference Clock Requirements T_A = 0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Min.	Typ.	Max.	Unit
f	Nominal Frequency (for gigabit Ethernet Compliance)		125		MHz
F_{tol}	Frequency Tolerance	-100		+100	ppm
Symm	Symmetry (Duty Cycle)	40		60	%
Tj	Peak-to-Peak Jitter		80		ps

Table 8. Transmitter Timing Characteristics T_A = 0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{setup}	Setup Time to Rising Edge of TX_CLK	1.5			ns
t_{hold}	Hold Time to Rising Edge of TX_CLK	1.0			
t_txlat[1]	Transmitter Latency		3.5		
			4.4		bits

Note:
1. The transmitter latency, as shown in Figure 4, is defined as the time between the latching in of the parallel data word (as triggered by the rising edge of the transmit by clock, REFCLK) and the transmission of the first serial bit of that parallel word (defined by the rising edge of the first bit transmitted).

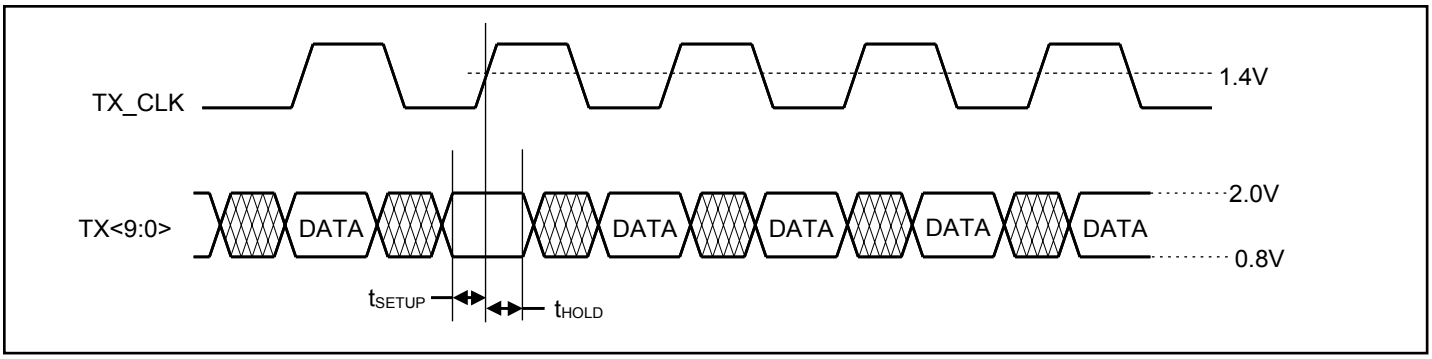


Figure 3. Transmitter Section Timing

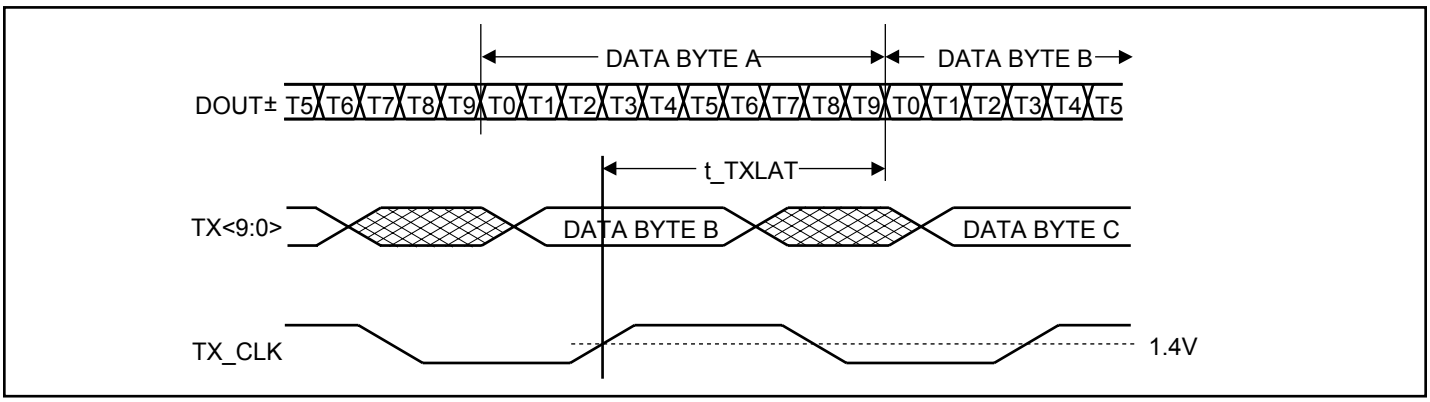


Figure 4. Transmitter Latency

Table 9. Receiver Timing Characteristics T_A = 0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Min.	Typ.	Max.	Unit
b_sync[1]	Bit Sync Time			2500	bits
f_lock	Frequency Lock at Powerup			500	µs
t_{SETUP}	Data Setup Before Rising Edge of RX_CLK	2.5			ns
t_{HOLD}	Data Hold After Rising Edge of RX_CLK	1.5			
t_{DUTY}	RX_CLK Duty Cycle	40		60	%
t_{A-B}	RX_CLK Skew	7.5		8.5	ns
T_rxlat[2]	Receiver Latency		22.4		ns
			28.0		bits

Notes:
1. This is the recovery for input phase jumps.
2. The receiver latency as shown in Figure 6, is defined as the time between receiving the first serial bit of a parallel data word (defined as the first edge of the first serial bit) and the clocking out of that parallel word (defined by the rising edge of the receive byte clock, either RBC1 or RBC0).

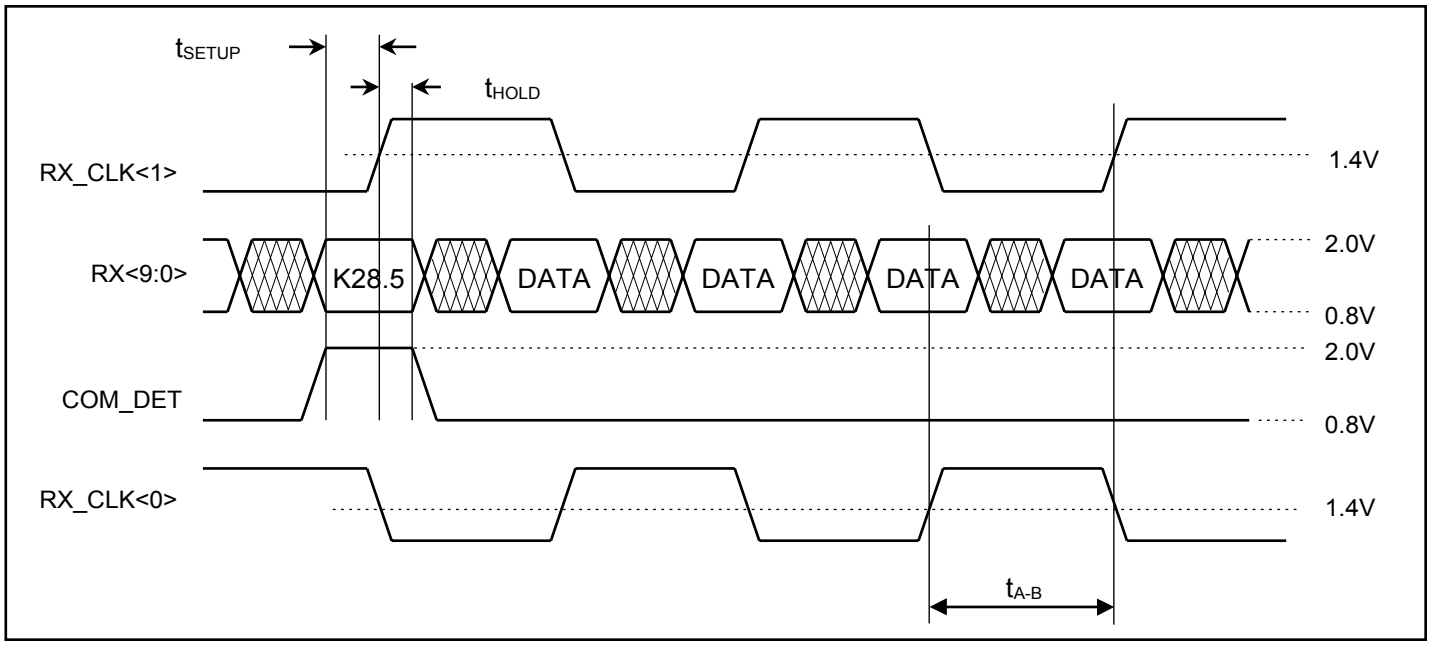


Figure 5. Receiver Section Timing

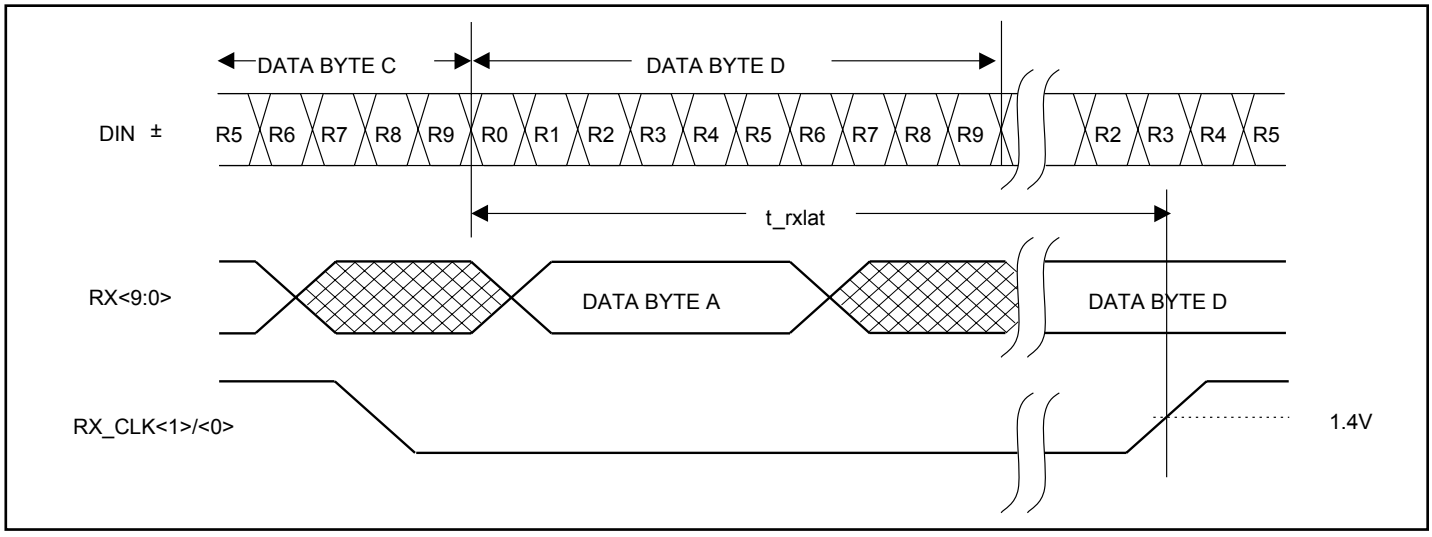
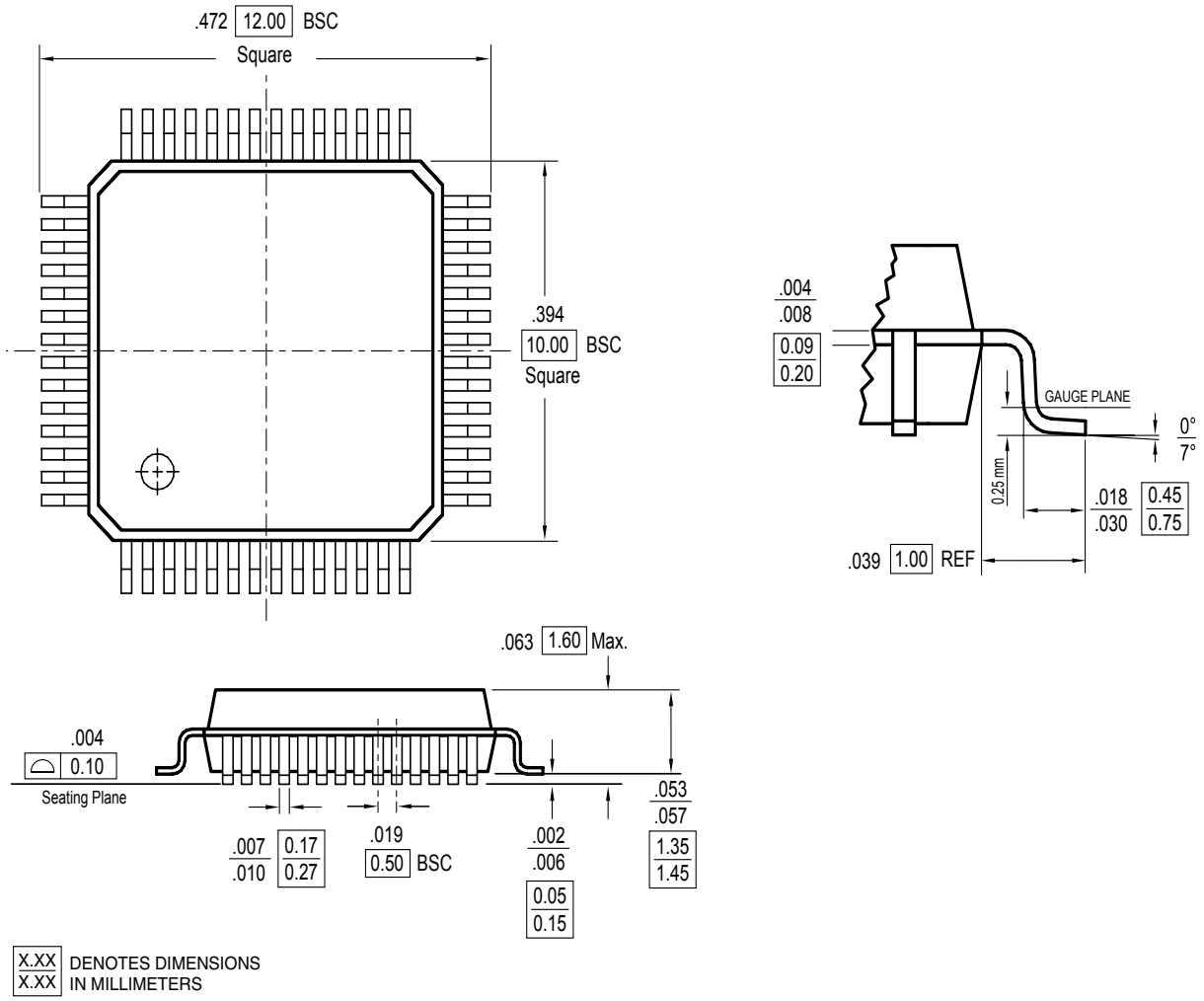
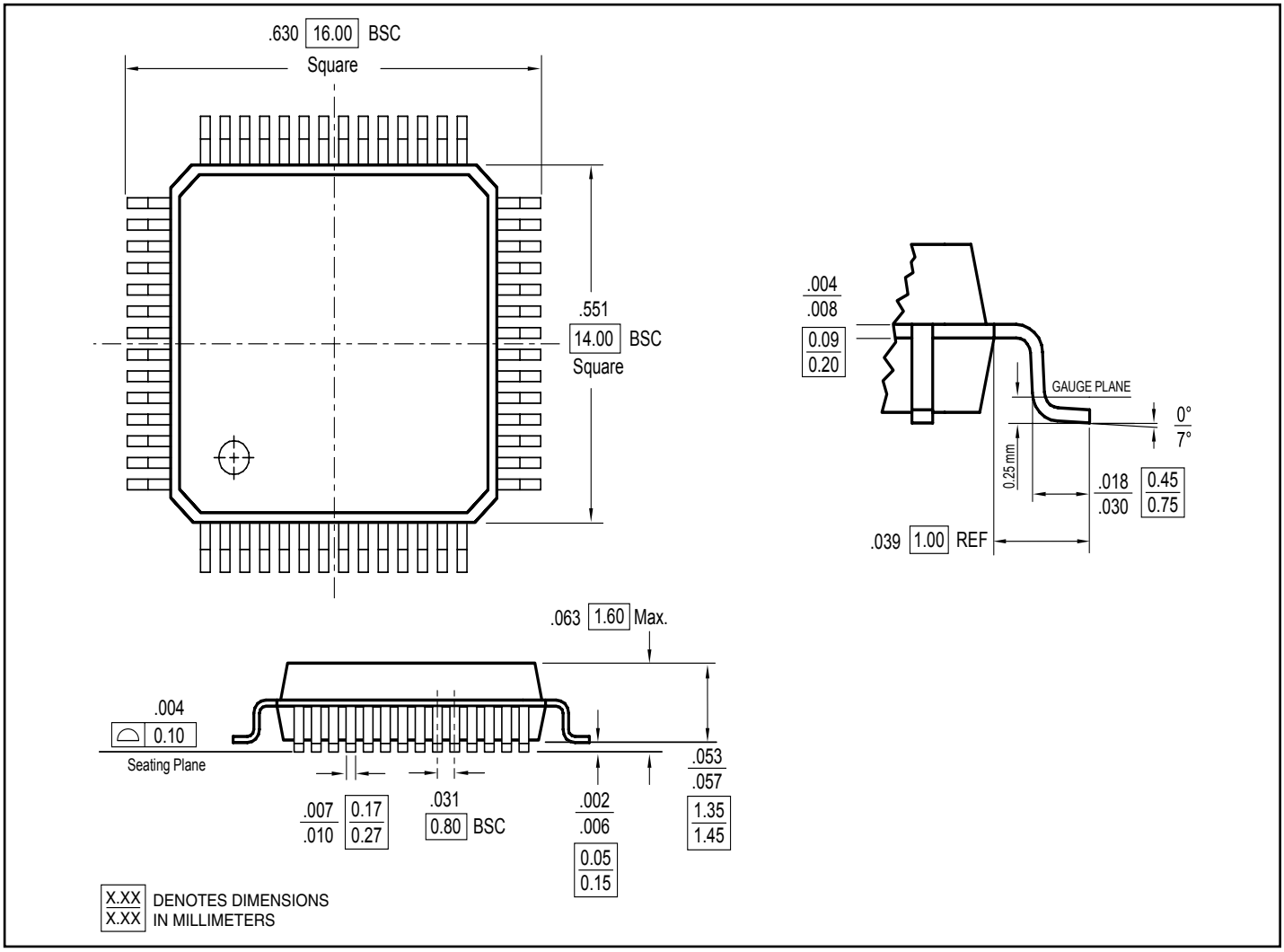


Figure 6. Receiver Latency

Packaging Mechanical: 64-pin LQFP (FC)



Packaging Mechanical: 64-pin LQFP (FD)



Ordering Information

Ordering Code	Package Code	Package Description
PI90SD1636AFC	FC	64-pin 10mm x10mm LQFP
PI90SD1636AFCE	FC	Pb-free & Green, 64-pin 10mm x10mm LQFP
PI90SD1636AFD	FD	64-pin 14mm x14mm LQFP
PI90SD1636AFDE	FD	Pb-free & Green, 64-pin 14mm x14mm LQFP

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

Appendix A

Gigabit Ethernet Transceiver

Pin Cross Reference Guide
PI90SD1636A, VSC7123 and HDMP1636A/1646A

Summary:

Pericom Semiconductor's PI90SD1636A is functionally pin compatible with Vitesse's VSC7123 and Agilent's HDMP-1636A/46A. Minor differences exist amongst the parts regarding the use of certain pins that are used by the manufacturer for internal tests, as is further clarified below. These differences will not affect plug compatibility during normal operations.

	Pericom	Vitesse	Agilent	
Pin #	PI90SD1636A	VSC7123	HDMP1636A/46A	Comments
1	GND_ESD	VSSD	GND	Connect to the ground plane.
2	TX<0>	T0	TX[0]	10-bit parallel data input pins.
3	TX<1>	T1	TX[1]	
4	TX<2>	T2	TX[2]	
6	TX<3>	T3	TX[3]	
7	TX<4>	T4	TX[4]	
8	TX<5>	T5	TX[5]	
9	TX<6>	T6	TX[6]	
11	TX<7>	T7	TX[7]	
12	TX<8>	T8	TX[8]	
13	TX<9>	T9	TX[9]	
5	VDD_ESD	VDDD	VCC	Connect to 3.3V
10	VDD_ESD	VDDD	VCC	Connect to 3.3V
14	GND_ESD	VSSD	GND	Connect to the ground plane.
15	GND_TXA	VSSA	GND_TXA	Connect to the ground plane.
16	NC	CAP0	TXCAP1	Pericom requires no external caps. External capacitor will not affect performance
17	NC	CAP1	TX_CAP0	Pericom requires no external caps. External capacitor will not affect performance
18	VDD_TXA	VDDA	VCC_TXA	Connect to 3.3V
19	EWRAP	EWRAP	LOOPEN	Loop-back Enable when HIGH. Set LOW for normal operation
20	VDD_TXD	VDDD	VCC	Connect to 3.3V
21	GND_TXD	VSSD	GND	Connect to the ground plane
22	TX_CLK	REFCLK	REFCLK	125MHz reference clock.
23	VDD_RXD	VDDD	VCC	Connect to 3.3V
24	EN_CDET	ENCDET	ENBYTSYNC	Comma Detect Enable (Active HIGH)
25	GND_RXD	VSSD	GND	Connect to the ground plane.
26	SIG_DET	SIGDET	SIG_DET	Signal Detect (Active HIGH)
27	NC	(Note 1)	NC	NCTD0, No connect for normal operation.
28	VDD_RXD	VDDD	VCC	Connect to 3.3V
29	VDD_RX	VDDT	VCC_RXTTL	Connect to 3.3V
30	RX_CLK<1>	RCLKN	RBC1	Receiver Byte Clock
31	RX_CLK<0>	RCLK	RBC0	Receiver Byte Clock
32	GND_RX	VSST	GND_RXTTL	Connect to the ground plane
33	GND_RXT	VSST	GND_RXTTL	Connect to the ground plane

	Pericom	Vitesse	Agilent	
Pin #	PI90SD1636A	VSC7123	HDMP1636A/ 46A	Comments
34	RX<9>	R9	RX[9]	Received Parallel Data Output
35	RX<8>	R8	RX[8]	
36	RX<7>	R7	RX[7]	
38	RX<6>	R6	RX[6]	
39	RX<5>	R5	RX[5]	
40	RX<4>	R4	RX[4]	
41	RX<3>	R3	RX[3]	
43	RX<2>	R2	RX[2]	
44	RX<1>	R1	RX[1]	
45	RX<0>	R0	RX[0]	
37	VDD_RXT	VDDT	VCC_RXTTL	Connect to 3.3V
42	VDD_RXT	VDDT	VCC_RXTTL	Connect to 3.3V
46	GND_RXT	VSST	GND_RXTTL	Connect to the ground plane
47	COM_DET	COMDET	BYTSYNC	Comma Detect (Byte Sync)
48	NC	TDI	RXCAP0	Pericom requires no external caps. External capacitor will not affect performance
49	NC	TCK	RXCAP1	Pericom requires no external caps. External capacitor will not affect performance
50	VDD_RXF	VDDD	VCC_RXA	Connect to 3.3V
51	GND_RXF	VSSD	GND_RXA	Connect to the ground plane
52	DIN-	RX-	-DIN	High-speed serial data input
53	VDD_RXESD	N/C	VCC	
		(Note 2)		Connect to 3.3V
54	DIN+	RX+	+DIN	High-speed serial data input
55	VDD_RXESD	TMS	VCC	Connect to 3.3V
56	GND_RXESD	TRSTN	GND	Connect to the ground plane
57	VDD_RXA	VDDD	VCC	Connect to 3.3V
58	GND_RXA	VSSD	GND	Connect to the ground plane
59	VDD_RXA	VDDD	VCC	Connect to 3.3V
60	VDD_TX_ECL	VDDP	VCC_TXECL	Connect to 3.3V
61	DOUT-	TX-	-DOUT	High-speed serial data output
62	DOUT+	TX+	+DOUT	High-speed serial data output
63	VDD_TX_HS	VDDP	VCC_TXHS	Connect to 3.3V
64	GND_TX_HS	VSSD	GND_TXHS	Connect to the ground plane

Notes:
1. For VSC7123, this pin is in high-impedance state in normal operation.
2. For VSC7123, this pin has no internal connection.