



Integrated Device Technology, Inc.

LOW POWER 3V CMOS SRAM 1 MEG (128K x 8-BIT)

**ADVANCE
INFORMATION
IDT71L024**

FEATURES:

- 128K x 8 Organization
- Wide Operating Voltage Range: 2.7V to 3.6V
- Speed Grades: 70ns, 100ns
- Low Operating Power: 25mA (max)
- Low Standby Power: 5 μ A (max)
- Low-Voltage Data Retention: 1.5V (min)
- Available in 32-pin, 13.4mm x 8mm Type I TSOP package

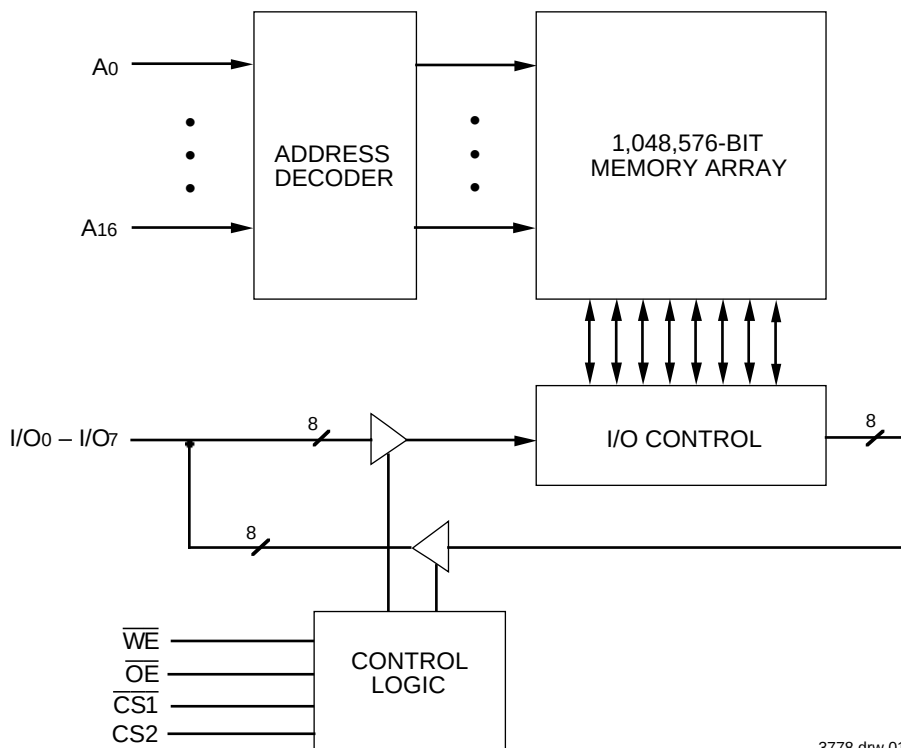
DESCRIPTION:

The IDT71L024 is a 1,048,576-bit very low-power Static RAM organized as 128K x 8. It is fabricated using IDT's high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for low-power memory needs. It uses a 6-transistor memory cell.

All input and output signals of the IDT71L024 are LVTTTL-compatible and operation is from a single extended-range 3.3V supply. This extended supply range makes the device ideally suited for unregulated battery-powered applications. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71L024 is packaged in a JEDEC standard 32-pin TSOP Type I.

FUNCTIONAL BLOCK DIAGRAM



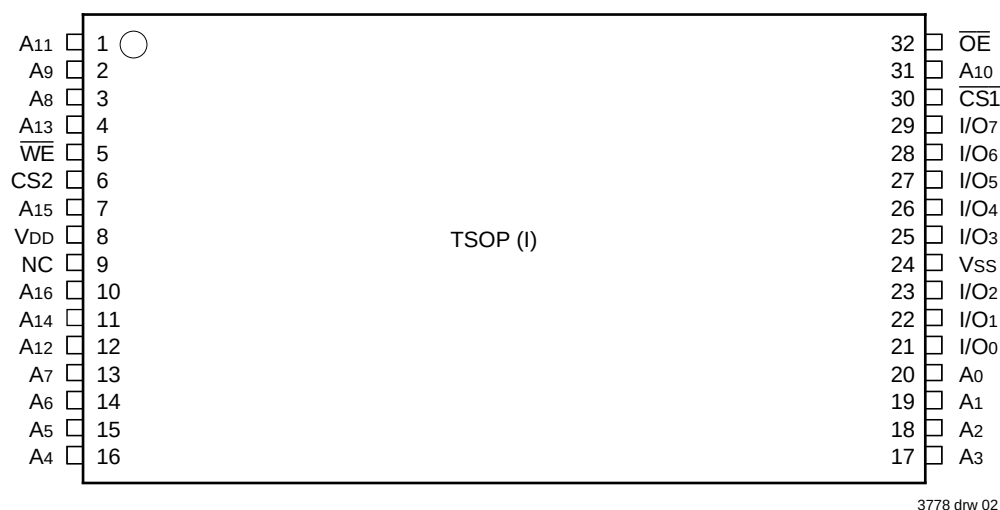
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INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

MAY 1997

PIN CONFIGURATIONS



**TSOP
TOP VIEW**

TRUTH TABLE⁽¹⁾

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	I/O ₀ -I/O ₇	Function
H	X	X	X	High-Z	Deselected - Standby
X	L	X	X	High-Z	Deselected - Standby
L	H	L	H	DATA _{OUT}	Read
L	H	X	L	DATA _{IN}	Write
L	H	H	H	High-Z	Outputs Disabled

NOTE:

1. H = V_{IH}, L = V_{IL}, X = Don't care.

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PIN DESCRIPTIONS

A0 – A16	Address Inputs	Input
$\overline{CS1}$	Chip Select	Input
CS2	Chip Select	Input
$\overline{WE}$	Write Enable	Input
$\overline{OE}$	Output Enable	Input
I/O ₀ - I/O ₇	Data Input/Output	I/O
VDD	Power	Pwr
VSS	Ground	Gnd

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CAPACITANCE

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	6	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 3dV	7	pF

NOTE:

1. This parameter is guaranteed by device characterization, but not production tested.

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l. and Ind'l.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to V _{SS}	-0.5 to +4.6	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to V _{SS}	-0.5 to V _{DD} +0.5V	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	20	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{DD} terminals only.
- Input, Output, and I/O terminals; 4.6V maximum.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	V _{SS}	V _{DD}
Commercial	0°C to +70°C	0V	2.7V to 3.6V
Industrial	-40°C to +85°C	0V	2.7V to 3.6V

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RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	2.7	3.0	3.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.0	—	V _{DD} +0.3 ⁽¹⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽²⁾	—	0.8	V

NOTE:

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- V_{IH} (max.) = V_{DD} + 1.5V for pulse width less than 5ns, once per cycle.
- V_{IL} (min.) = -1.5V for pulse width less than 5ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7V to 3.6V, Commercial and Industrial Temperature Ranges

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I _{LI}	Input Leakage Current	V _{DD} = Max., V _{IN} = V _{SS} to V _{DD}	—	1	μA
I _{LO}	Output Leakage Current	V _{DD} = Max., $\overline{CS}$ = V _{IH} , V _{OUT} = V _{SS} to V _{DD}	—	1	μA
V _{OH}	Output High Voltage	I _{OH} = -1mA, V _{DD} = Min.	2.4	—	V
V _{OL}	Output Low Voltage	I _{OL} = 2mA, V _{DD} = Min.	—	0.4	V

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DC ELECTRICAL CHARACTERISTICS^(1, 2)

V_{DD} = 2.7 to 3.6V, V_{LC} = 0.2V, V_{HC} = V_{DD}-0.2V, Commercial and Industrial Temperature Ranges

Symbol	Parameter	Test Conditions		Typ. ⁽⁵⁾	Max.	Unit
I _{CC2}	Dynamic Operating Current	$\overline{CS1} = V_{LC}$, $CS2 = V_{HC}$, Outputs Open, $V_{DD} = 3.6V$, $f = f_{MAX}^{(3)}$	-70 ns	—	25	mA
			-100 ns	—	18	
I _{CC}	Static Operating Current	$\overline{CS1} = V_{LC}$, $CS2 = V_{HC}$, Outputs Open, $\overline{WE} = V_{HC}$, $V_{DD} = 3.6V$, $f = 0^{(4)}$		—	5	mA
I _{SB1}	Standby Supply Current	$\overline{CS1}$ and $CS2 = V_{HC}$, or $CS2 = V_{LC}$, Outputs Open, $V_{DD} = 3.6V$	-40 to 85°C	—	10	μA
			0 to 70°C	—	5	
			40°C	—	2	
			25°C	—	1	

NOTES:

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- All values are maximum guaranteed values.
- Input low and high voltage levels are 0.2V and V_{DD}-0.2V respectively for all tests.
- f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}).
- f = 0 means no address input lines are changing.
- Typical conditions are V_{DD} = 3.0V and specified temperature.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

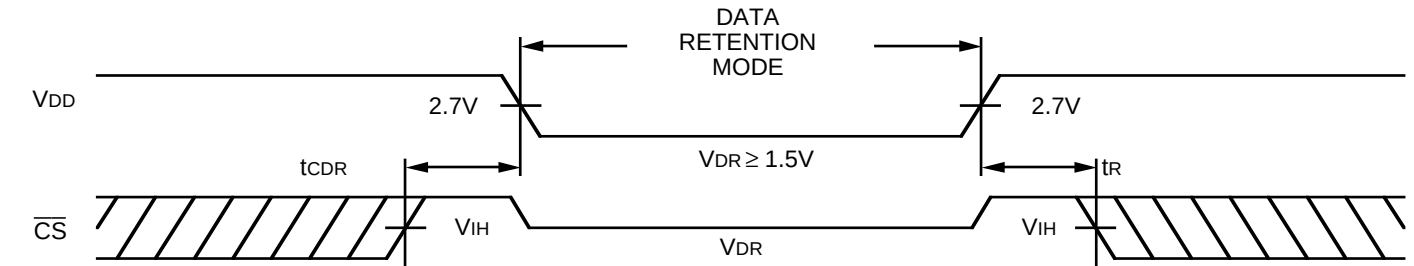
(VLC = 0.2V, VHC = VDD - 0.2V)

Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾	Max.	Unit
VDR	VCC for Data Retention	—	1.5	—	—	V
ICCDR	Data Retention Current	1) $\overline{CS1} \geq V_{HC}$ and $CS2 \geq V_{HC}$ or 2) $CS2 \leq V_{LC}$	—	<1	5	μA
tCDR ⁽³⁾	Chip Deselect to Data Retention Time		0	—	—	ns
tr ⁽³⁾	Operation Recovery Time		trc ⁽²⁾	—	—	ns

- NOTES:
- TA = +25°C.
 - trc = Read Cycle Time.
 - This parameter is guaranteed by device characterization, but is not production tested.

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LOW VDD DATA RETENTION WAVEFORM



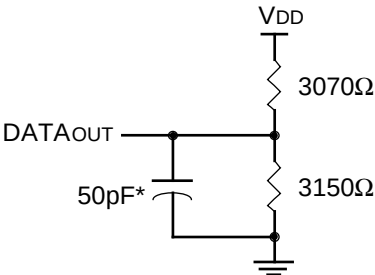
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AC TEST CONDITIONS

Input Pulse Levels	GND to 2.5V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1

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AC TEST LOAD



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*Including jig and scope capacitance.

Figure 1. AC Test Load

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 2.7 to 3.6V, All Temperature Ranges)

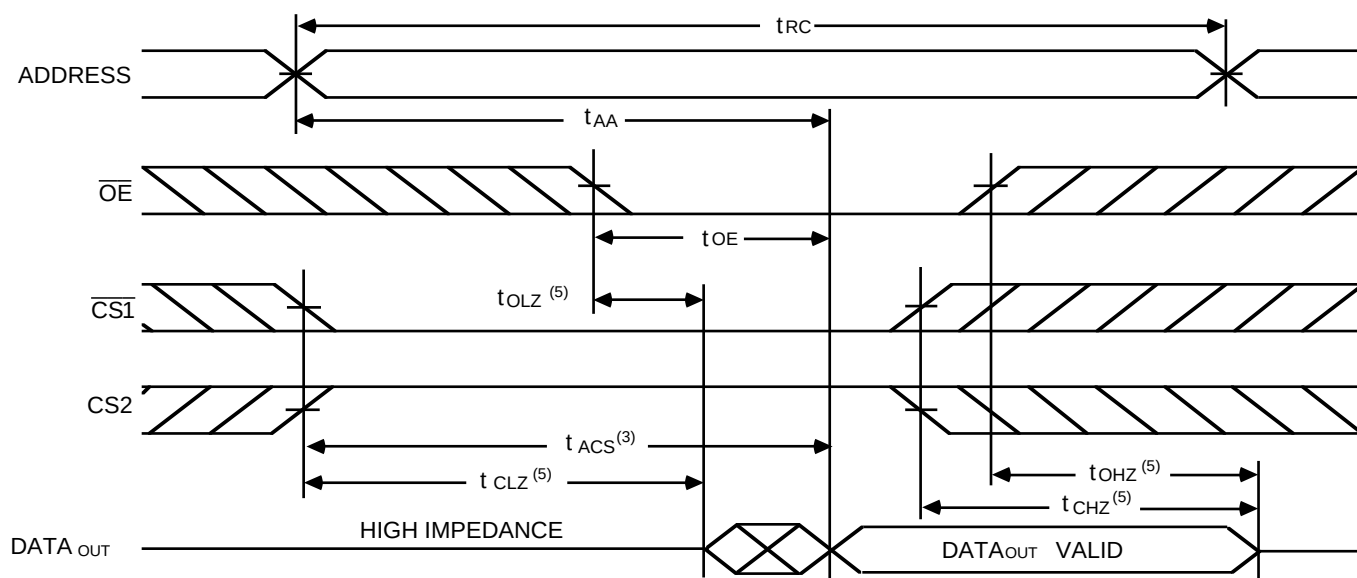
Symbol	Parameter	71L024L70		71L024L100		Units
		Min.	Max.	Min.	Max.	
Read Cycle						
tRC	Read Cycle Time	70	—	100	—	ns
tAA	Address Access Time	—	70	—	100	ns
tACS	Chip Select Access Time	—	70	—	100	ns
tCLZ ⁽¹⁾	Chip Select Low to Output in Low-Z	10	—	10	—	ns
tCHZ ⁽¹⁾	Chip Select High to Output in High-Z	—	25	—	30	ns
tOE	Output Enable Low to Output Valid	—	35	—	50	ns
tOLZ ⁽¹⁾	Output Enable Low to Output in Low-Z	5	—	5	—	ns
tOHZ ⁽¹⁾	Output Enable High to Output in High-Z	—	25	—	30	ns
tOH	Output Hold from Address Change	10	—	15	—	ns
Write Cycle						
tWC	Write Cycle Time	70	—	100	—	ns
tAW	Address Valid to End of Write	65	—	80	—	ns
tCW	Chip Select Low to End of Write	65	—	80	—	ns
tAS	Address Set-up Time	0	—	0	—	ns
tWR	Address Hold from End of Write	0	—	0	—	ns
tWP	Write Pulse Width	55	—	70	—	ns
tdW	Data Valid to End of Write	30	—	40	—	ns
tdH	Data Hold Time	0	—	0	—	ns
tOW ⁽¹⁾	Write Enable High to Output in Low-Z	5	—	5	—	ns
tWHZ ⁽¹⁾	Write Enable Low to Output in High-Z	—	25	—	30	ns

NOTE:

1. This parameter is guaranteed by device characterization, but is not production tested.

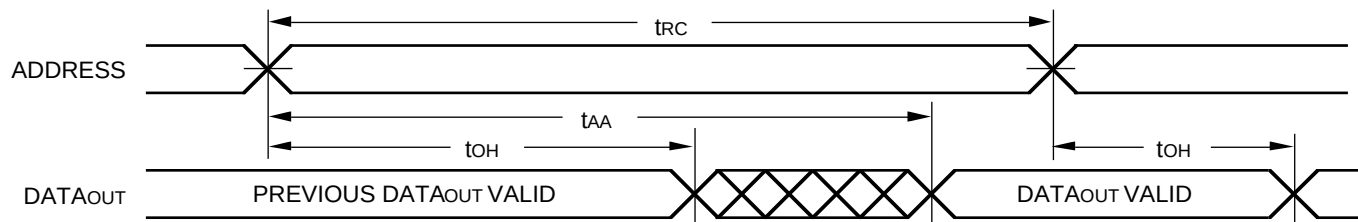
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TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



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TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)

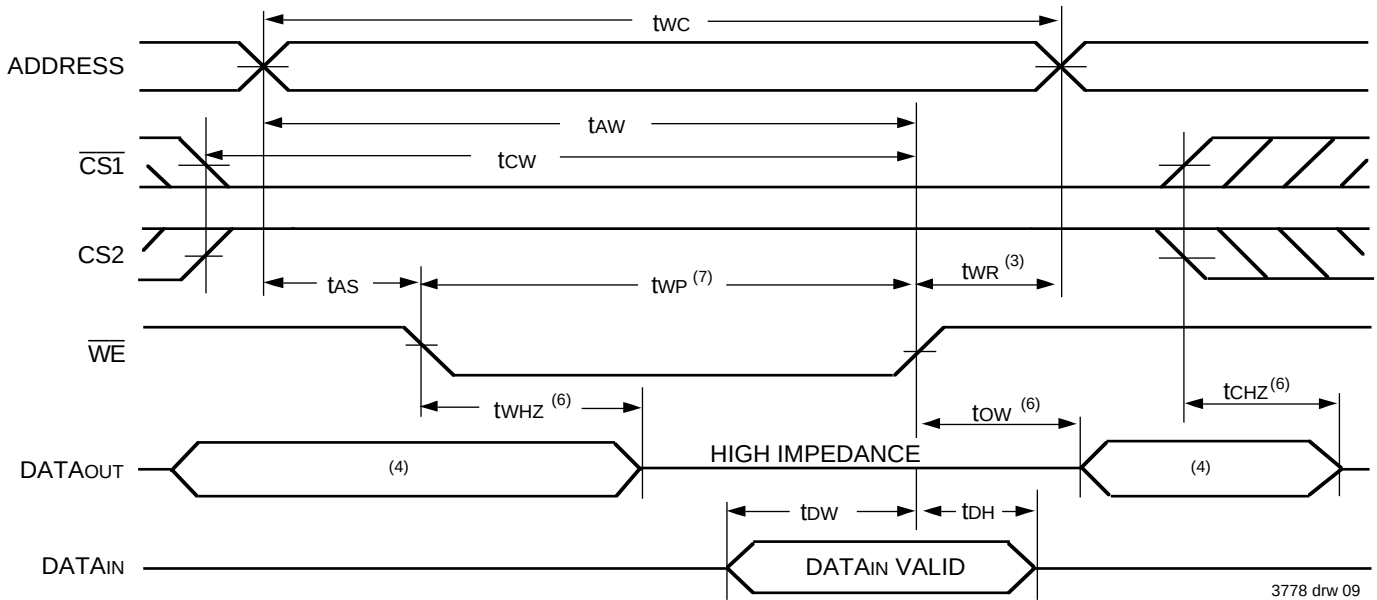


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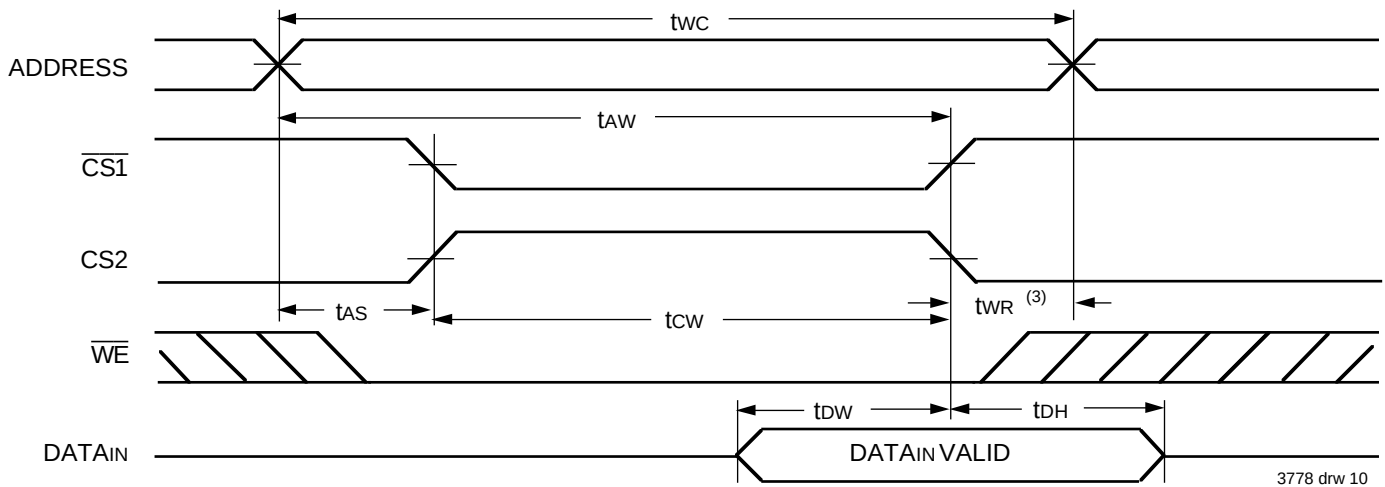
NOTES:

1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected; $\overline{CS1}$ is LOW and CS2 is HIGH.
3. Address must be valid prior to or coincident with the later of $\overline{CS1}$ transition LOW and CS2 transition HIGH; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)^(1, 2, 5)



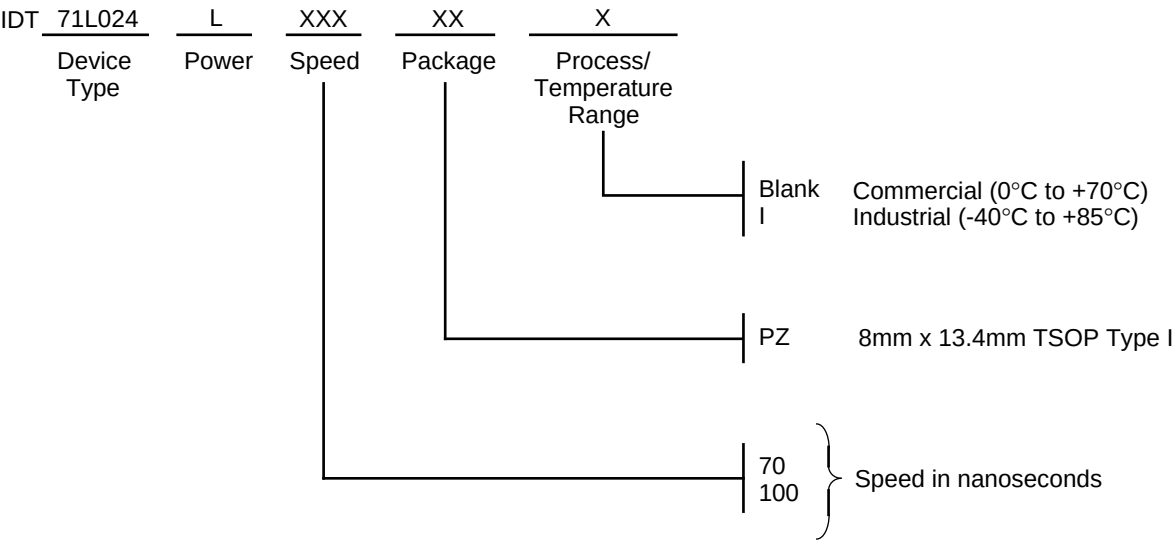
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS1}$ AND CS2 CONTROLLED TIMING)^(1,2,5)



NOTES:

1. $\overline{WE}$ or $\overline{CS1}$ must be HIGH, or CS2 must be LOW during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS1}$, HIGH CS2, and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of either $\overline{CS1}$ or $\overline{WE}$ going HIGH or CS2 going LOW to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS1}$ LOW transition or CS2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state.
7. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, tWP must be greater than or equal to tWHZ + tOW to allow the I/O drivers to turn off and data to be placed on the bus for the required tOW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified tWP.

ORDERING INFORMATION



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