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RF3196

QUAD-BAND GSM850/GSM900/DCS/PCS POWER AMP MODULE

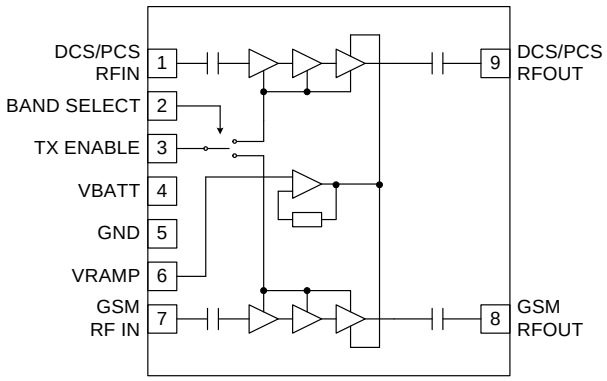
RoHS Compliant and Pb-Free Product
Package Style: Module, 6mm x 6mm

Features

- Reduced Current into Mismatch
- Ultra-Small 6mm x 6mm Package Size
- Integrated V_{REG}
- Complete Power Control Solution
- Automatic V_{BATT} Tracking Circuit
- No External Components or Routing

Applications

- 3V Quad-Band GSM Handsets
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment
- GSM850/EGSM900/DCS/PCS Products
- GPRS Class 8
- Power Star™ Module



Functional Block Diagram

Product Description

The RF3196 is a high-power, high-efficiency power amplifier module with integrated power control that provides over 50dB of control range. The device is a self-contained 6mm x 6mm module with 50Ω input and output terminals. The device is designed for use as the final RF amplifier in GSM850, EGSM900, DCS and PCS handheld digital cellular equipment and other applications in the 824MHz to 849MHz, 880MHz to 915MHz, 1710MHz to 1785MHz and 1850MHz to 1910MHz bands. The RF3196 incorporates RFMD's latest V_{BATT} tracking circuit, which monitors battery voltage and prevents the power control loop from reaching saturation. The RF3196 also has a power flattening circuit that reduces power variation and max current draw into mismatch. The RF3196 requires no external routing or external components, simplifying layout and reducing board space.

Ordering Information

RF3196	Quad-Band GSM850/GSM900/DCS/PCS Power Amp Module
RF3196 SB	Power Amp Module 5-Piece Sample Pack
RF3196PCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.3 to +6.0	V_{DC}
Power Control Voltage (V_{RAMP})	-0.3 to +2.2	V
Input RF Power	+10	dBm
Max Duty Cycle	50	%
Output Load VSWR	10:1	
Operating Case Temperature	-20 to +85	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

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Operating Conditions

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall Power Control V_{RAMP}					
Power Control "ON"			2.1	V	Max. P_{OUT}
Power Control "OFF"		0.26		V	Min. P_{OUT}
V_{RAMP} Input Capacitance		2	20	pF	DC to 2MHz
V_{RAMP} Input Current			30	µA	V_{RAMP}=2.1V
TX Enable "ON"	1.5			V	
TX Enable "OFF"			0.5	V	
GSM Band Enable			0.5	V	
DCS/PCS Band Enable	1.5			V	
Overall Power Supply					
Power Supply Voltage	3.0	3.5	4.5	V	Operating limits
Power Supply Current		1		µA	P_{IN}<-30dBm, TX Enable=Low, Temp=-20°C to +85°C
			150	mA	V_{RAMP}=0.26V, TX Enable=High
Overall Control Signals					
Band Select "Low"	0	0	0.5	V	
Band Select "High"	1.5	2.0	3.0	V	
Band Select "High" Current		20	50	µA	
TX Enable "Low"	0	0	0.5	V	
TX Enable "High"	1.5	2.0	3.0	V	
TX Enable "High" Current		1	2	µA	

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (GSM850 Mode)					Nominal conditions: Temp=+25 °C, V_{BATT}=3.5V, V_{RAMP}=V_{RAMP_RP}, P_{IN}=3dBm, Freq=824MHz to 849MHz, 12.5% Duty Cycle, Pulse Width=1154µs
Operating Frequency Range		824 to 849		MHz	
Maximum Output Power 1	34.2			dBm	Temp=+25°C, V_{BATT}=3.5V, V_{RAMP}=V_{RAMP_RP}
Maximum Output Power 2	32.0			dBm	Temp=+85°C, V_{BATT}=3.0V, V_{RAMP}≤2.1V
Total Efficiency	45	51		%	At $P_{OUT\ MAX}$, V_{BATT}=3.5V, V_{RAMP}=2.1V
Input Power Range	0	+3	+5	dBm	Maximum output power guaranteed at minimum drive level
Output Noise Power		-85		dBm	RBW=100kHz, 869MHz to 894MHz, P_{OUT} ≤ +34.2dBm
Forward Isolation 1		-45	-30	dBm	TXEnable=Low, P_{IN}=+5dBm
Forward Isolation 2		-30	-10	dBm	TXEnable=High, P_{IN}=+5dBm, V_{RAMP}=0.26V
Cross Band Isolation at $2f_0$		-30	-20	dBm	V_{RAMP}=0.26V to V_{RAMP_RP}
Second Harmonic		-15	-10	dBm	V_{RAMP}=0.26V to V_{RAMP_RP}
Third Harmonic		-30	-15	dBm	V_{RAMP}=0.26V to V_{RAMP_RP}
All Other Non-Harmonic Spurious			-36	dBm	V_{RAMP}=0.26V to V_{RAMP_RP}
Input Impedance		50		Ω	
Input VSWR			2.5:1		
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR=8:1; all phase angles (V_{RAMP} set for P_{OUT}≤34.2dBm into 50Ω load; load switched to VSWR=8:1; RBW=3MHz)
Output Load VSWR Ruggedness	No damage or permanent degradation to device				VSWR=10:1; all phase angles (V_{RAMP} set for P_{OUT}≤34.2dBm into 50Ω load; load switched to VSWR=10:1)
Output Load Impedance		50		Ω	Load impedance presented at RF OUT pad
Power Control V_{RAMP}					
Power Control Range	50	55		dB	V_{RAMP}=0.26V to V_{RAMP_RP}
Transient Spectrum		-35	-23	dBm	V_{RAMP}=V_{RAMP_RP}

Notes:

V_{RAMP_RP}=V_{RAMP} set for 34.2dBm at nominal conditions.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (GSM900 Mode)					Nominal conditions: Temp=+25 °C, V_{BATT}=3.5V, V_{RAMP}=V_{RAMP_RP}, P_{IN}=3dBm, Freq=880MHz to 915MHz, 12.5% Duty Cycle, Pulse Width=1154µs
Operating Frequency Range		880 to 915		MHz	
Maximum Output Power 1	34.2			dBm	Temp=+25°C, V_{BATT}=3.5V, V_{RAMP}=V_{RAMP_RP}
Maximum Output Power 2	32.0			dBm	Temp=+85°C, V_{BATT}=3.0V, V_{RAMP}≤2.1V
Total Efficiency	50	56		%	At $P_{OUT\ MAX}$, V_{BATT}=3.5V, V_{RAMP}=2.1V
Input Power Range	0	+3	+5	dBm	Maximum output power guaranteed at minimum drive level
Output Noise Power		-83		dBm	RBW=100kHz, 925MHz to 935MHz, P_{OUT} ≤ +34.2dBm
		-85		dBm	RBW=100kHz, 935MHz to 960MHz, P_{OUT} ≤ +34.2dBm
Forward Isolation 1		-40	-30	dBm	TXEnable=Low, P_{IN}=+5dBm
Forward Isolation 2		-30	-10	dBm	TXEnable=High, P_{IN}=+5dBm, V_{RAMP}=0.26V
Cross Band Isolation $2f_0$		-30	-20	dBm	V_{RAMP}=0.26V to V_{RAMP_RP}
Second Harmonic		-15	-10	dBm	V_{RAMP}=0.26V to V_{RAMP_RP}
Third Harmonic		-30	-15	dBm	V_{RAMP}=0.26V to V_{RAMP_RP}
All Other Non-Harmonic Spurious			-36	dBm	V_{RAMP}=0.26V to V_{RAMP_RP}
Input Impedance		50		Ω	
Input VSWR			2.5:1		
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR=8:1; all phase angles (V_{RAMP} set for P_{OUT}≤34.2dBm into 50Ω load; load switched to VSWR=8:1; RBW=3MHz)
Output Load VSWR Ruggedness	No damage or permanent degradation to device				VSWR=10:1; all phase angles (V_{RAMP} set for P_{OUT}≤34.2dBm into 50Ω load; load switched to VSWR=10:1)
Output Load Impedance		50		Ω	Load impedance presented at RF OUT pad
Power Control V_{RAMP}					
Power Control Range	50	55		dB	V_{RAMP}=0.26V to V_{RAMP_RP}
Transient Spectrum		-35	-23	dBm	V_{RAMP}=V_{RAMP_RP}

Notes:

V_{RAMP_RP}=V_{RAMP} set for 34.2dBm at nominal conditions.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (DCS Mode)					Nominal conditions: Temp=25°C, V_{BATT}=3.5V, V_{RAMP}=V_{RAMP_RP}, P_{IN}=3dBm, Freq=1710MHz to 1785MHz, 12.5% Duty Cycle, pulse width=1154µs
Operating Frequency Range		1710 to 1785		MHz	
Maximum Output Power 1	32.0			dBm	Temp=+25°C, V_{BATT}=3.5V, V_{RAMP}=$V_{RAMP_R_P}$
Maximum Output Power 2	30.0			dBm	Temp=+85°C, V_{BATT}=3.0V, V_{RAMP}≤2.1V
Total Efficiency	45	51		%	At $P_{OUT\ MAX}$, V_{BATT}=3.5V, V_{RAMP}=2.1V
Input Power Range	0	+3	+5	dBm	Maximum output power guaranteed at minimum drive level
Output Noise Power		-85		dBm	RBW=100kHz, 1805MHz to 1880MHz, P_{OUT} ≤ 32dBm
Forward Isolation 1		-40	-30	dBm	TX Enable=Low, P_{IN}=+5dBm
Forward Isolation 2		-25	-10	dBm	TX Enable=High, V_{RAMP}=0.26V, P_{IN}=+5dBm
Second Harmonic		-15	-10	dBm	V_{RAMP}=0.26V to V_{RAMP_RP}
Third Harmonic		-30	-15	dBm	V_{RAMP}=0.26V to V_{RAMP_RP}
All Other Non-Harmonic Spurious			-36	dBm	V_{RAMP}=0.26V to V_{RAMP_RP}
Input Impedance		50		Ω	
Input VSWR			2.5:1		
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR=8:1; all phase angles (V_{RAMP} set for P_{OUT}≤32dBm into 50Ω load; load switched to VSWR=8:1; RBW=3MHz)
Output Load VSWR Ruggedness	No damage or permanent degradation to device				VSWR=10:1; all phase angles (V_{RAMP} set for P_{OUT}≤32dBm into 50Ω load; load switched to VSWR=10:1)
Output Load Impedance		50		Ω	Load impedance presented at RF OUT pad
Power Control V_{RAMP}					
Power Control Range	45	50		dB	V_{RAMP}=0.26V to V_{RAMP_RP}
Transient Spectrum		-35	-23	dBm	V_{RAMP}=V_{RAMP_RP}

Notes:

$V_{RAMP_R_P}$=V_{RAMP} set for 32dBm at nominal conditions.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall (PCS Mode)					Nominal conditions: Temp=25°C, V_{BATT}=3.5V, V_{RAMP}=V_{RAMP_RP}, P_{IN}=3dBm, Freq=1850MHz to 1910MHz, 12.5% Duty Cycle, pulse width=1154µs
Operating Frequency Range		1850 to 1910		MHz	
Maximum Output Power 1	32.0			dBm	Temp=+25°C, V_{BATT}=3.5V, V_{RAMP}=V_{RAMP_RP}
Maximum Output Power 2	30.0			dBm	Temp=+85°C, V_{BATT}=3.0V, V_{RAMP}≤2.1V
Total Efficiency	45	51		%	At $P_{OUT\ MAX}$, V_{BATT}=3.5V, V_{RAMP}=2.1V
Input Power Range	0	+3	+5	dBm	Maximum output power guaranteed at minimum drive level
Output Noise Power		-85		dBm	RBW=100kHz, 1930MHz to 1990MHz, P_{OUT} ≤ 32dBm
Forward Isolation 1		-35	-30	dBm	TXEnable=Low, P_{IN}=+5dBm
Forward Isolation 2		-25	-10	dBm	TXEnable=High, V_{RAMP}=0.26V, P_{IN}=+5dBm
Second Harmonic		-15	-10	dBm	V_{RAMP}=0.26V to V_{RAMP_RP}
Third Harmonic		-30	-15	dBm	V_{RAMP}=0.26V to V_{RAMP_RP}
All Other Non-Harmonic Spurious			-36	dBm	V_{RAMP}=0.26V to $V_{RAMP_R_P}$
Input Impedance		50		Ω	
Input VSWR			2.5:1		
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR=8:1; all phase angles (V_{RAMP} set for P_{OUT}≤32dBm into 50Ω load; load switched to VSWR=8:1; RBW=3MHz)
Output Load VSWR Ruggedness	No damage or permanent degradation to device				VSWR=10:1; all phase angles (V_{RAMP} set for P_{OUT}≤32dBm into 50Ω load; load switched to VSWR=10:1)
Output Load Impedance		50		Ω	Load impedance presented at RF OUT pad
Power Control V_{RAMP}					
Power Control Range	45	50		dB	V_{RAMP}=0.26V to V_{RAMP_RP}
Transient Spectrum		-35	-23	dBm	V_{RAMP}=V_{RAMP_RP}

Notes:

$V_{RAMP_R_P}$=V_{RAMP} set for 32dBm at nominal conditions.

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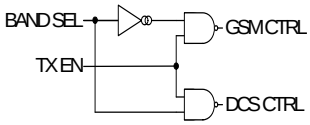
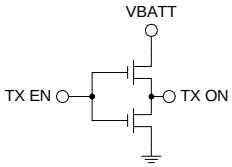
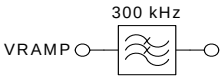
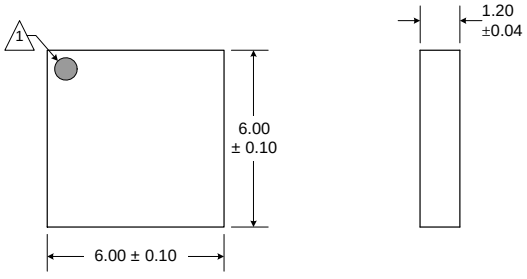
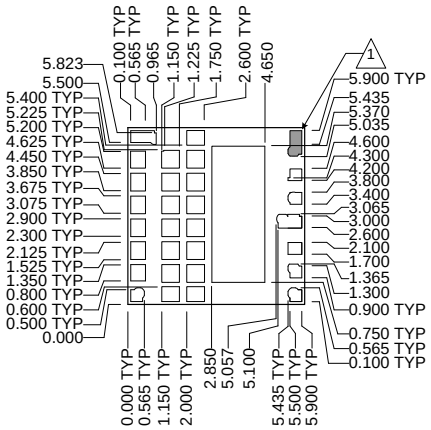
Pin	Function	Description	Interface Schematic
1	DCS/PCS IN	RF input to the DCS band. This is a 50Ω input.	
2	BAND SELECT	Allows external control to select the GSM or DCS band with a logic high or low. A logic low enables the GSM band whereas a logic high enables the DCS band.	
3	TX ENABLE	This signal enables the PA module for operation with a logic high.	
4	VBATT	Power supply for the module. This should be connected to the battery.	
5	GND		
6	VRAMP	Ramping signal from DAC. A 300kHz lowpass filter is integrated into the CMOS. No external filtering is required.	
7	GSM IN	RF input to the GSM band. This is a 50Ω input.	
8	GSM OUT	RF output for the GSM band. This is a 50Ω output. The output load line matching is contained internal to the package.	
9	DCS/PCS OUT	RF output for the DCS band. This is a 50Ω output. The output load line matching is contained internal to the package.	
Pkg Base	GND		

Package Drawing



Shaded areas represent pin 1.

Dimensions in mm.



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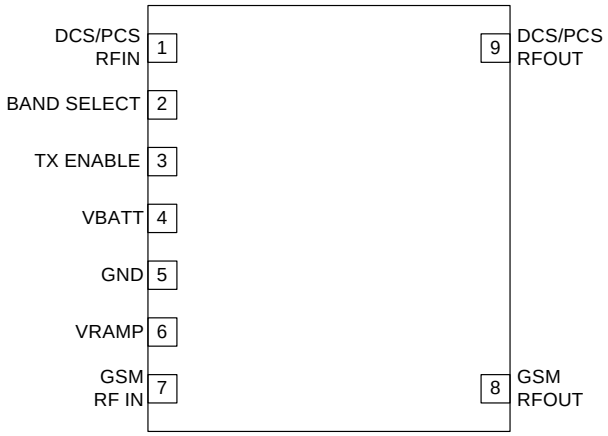
Pin Out

Top Down View



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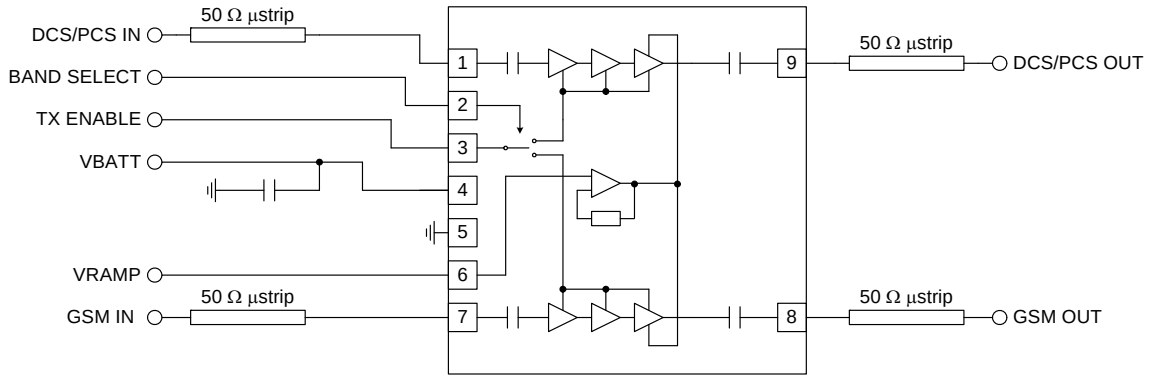
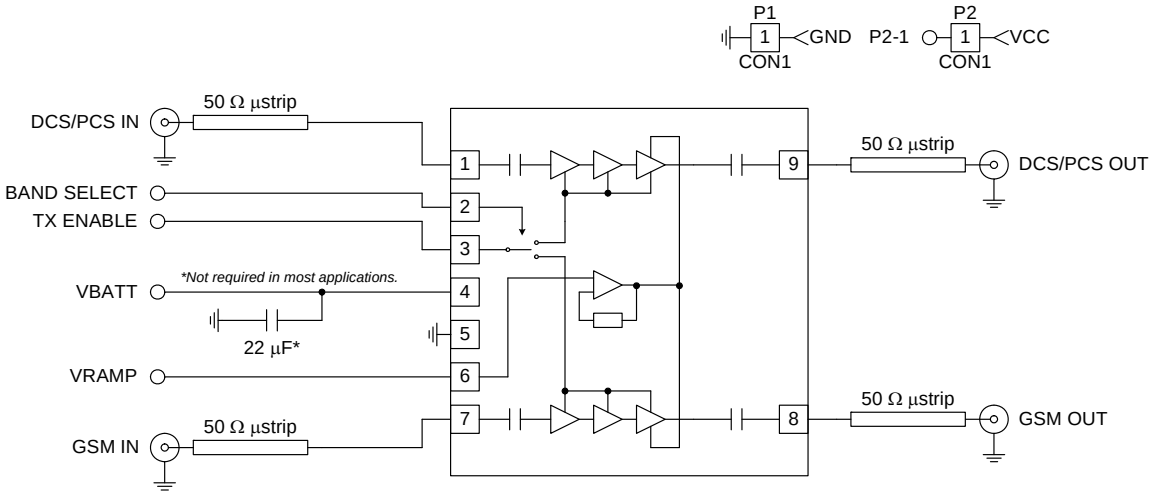
Application Schematic



Evaluation Board Schematic



Notes:

1. All the PA output measurements are referenced to the PA output pad (pins 8 and 9).
2. The 50 Ω μstrip between the PA output pad and the SMA connector has an approximate insertion loss of 0.1 dB for GSM900/EGSM900 and 0.2 dB for DCS1800/PCS1900 bands.

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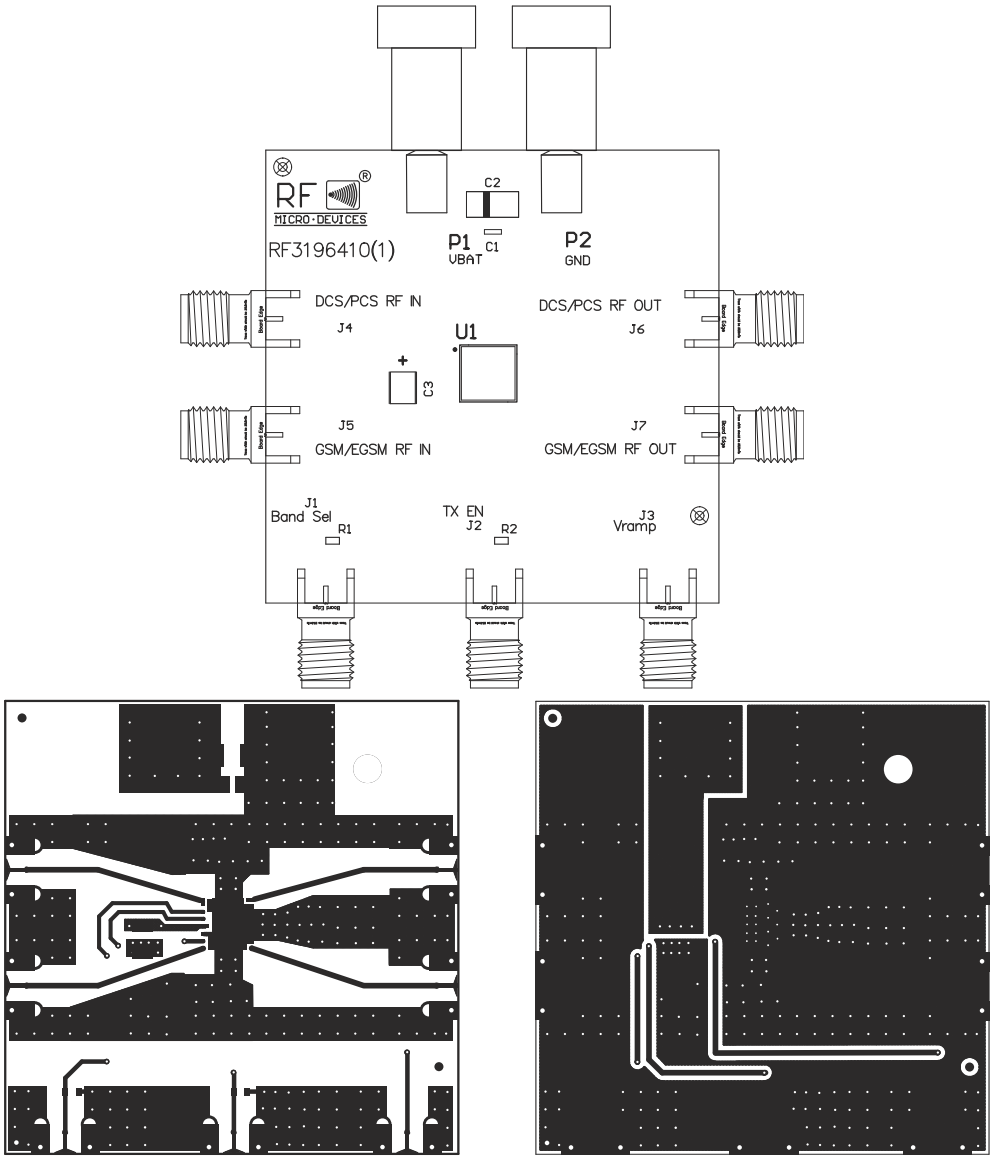
Evaluation Board Layout

Board Size 2.0” x 2.0”

Board Thickness 0.032”, Board Material FR-4, Multi-Layer



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Theory of Operation

Overview

Building on previous generations of PowerStar® modules, the RF3196 has integrated Power Control with additional features such as V_{BATT} tracking, and a power flattening circuit that reduces power and current variation into mismatch conditions.

Theory of Operation

The type of power control used in the RF3196 is a closed loop method that regulates the collector voltage of the amplifier while the stages are held at a constant bias. As the required output power is decreased from full power down to minimum PCLs, the collector voltage is also decreased. This process is repeatable and enables the user to implement a single point calibration, thereby increasing production by saving valuable time in the factory. The basic circuit is shown below in Figure 1.

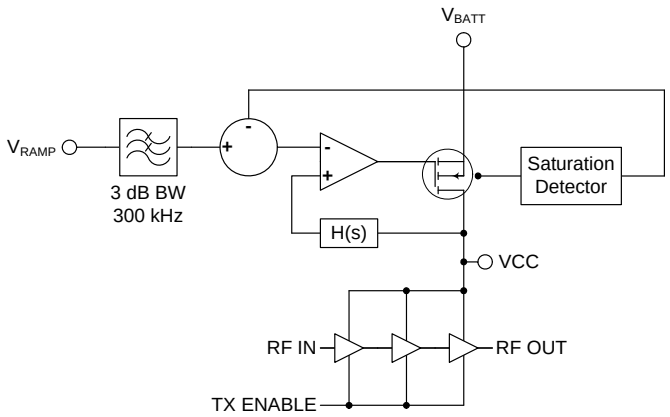

Figure 1. Power Control Circuit

Output power does not vary due to supply voltage under normal operating conditions if V_{CC} is sufficiently lower than V_{BATT}. Regulating the collector voltage to the PA essentially eliminates voltage sensitivity. This covers most cases where the PA will be operated. However, as the battery discharges and approaches its lower voltage range, the maximum output power from the PA will also drop slightly. In this case it is important to decrease V_{RAMP} to prevent the power control circuitry from inducing switching transients. These transients occur as a result of the control loop slowing down and not regulating power in accordance with V_{RAMP}..

In the RF3196, is a V_{BATT} tracking circuit that reduces the level of V_{RAMP} as the battery voltage decreases. The limiter is integrated into the CMOS controller and requires no additional input from the user. In the circuit, a feedback loop is implemented that compares V_{BATT} to V_{CC} and produces a correction so that V_{RAMP} is decreased. This prevents the switch transistor from being driven into saturation and inducing switching transients.

In addition to the V_{BATT} tracking circuit, the RF3196 has an integrated power flattening circuit that reduces the amount of current variation when a mismatch is presented to the output of the PA. When a mismatch is presented to the output of the PA, its output impedance is varied and could present a load that will increase output power. As the output power increases, so does current consumption. The current consumption can become very high if not monitored and limited. The power flattening circuit, like the V_{BATT} tracking circuit, is also integrated onto the CMOS controller and requires no input from the user.

Into a mismatch, the current varies as the phase changes. The power flattening circuit monitors current through an internal sense resistor. As the current changes, the loop is adjusted in order to maintain current. The result is flatter power and reduced current into mismatch. When compared to the RF3166, the RF3196 shows less current variation and has less power variation. Below, in Figure 2, is the power variation comparison.

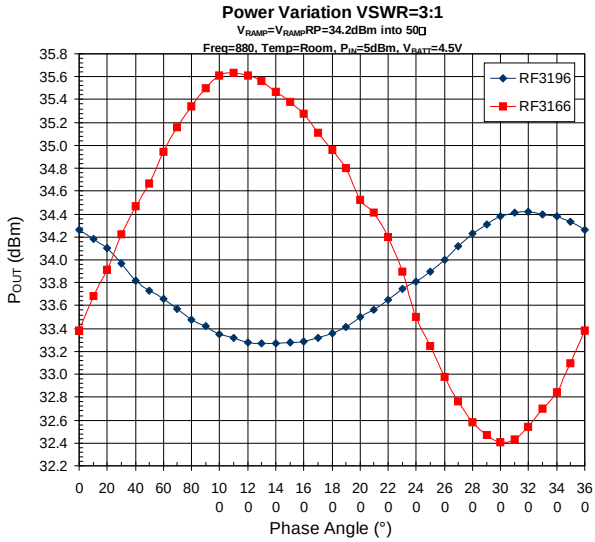

Figure 2. Power Variation into Mismatch

As previously discussed, reducing the power variation results in reduced current variation. Below, in Figure 3, is the current variation comparison.

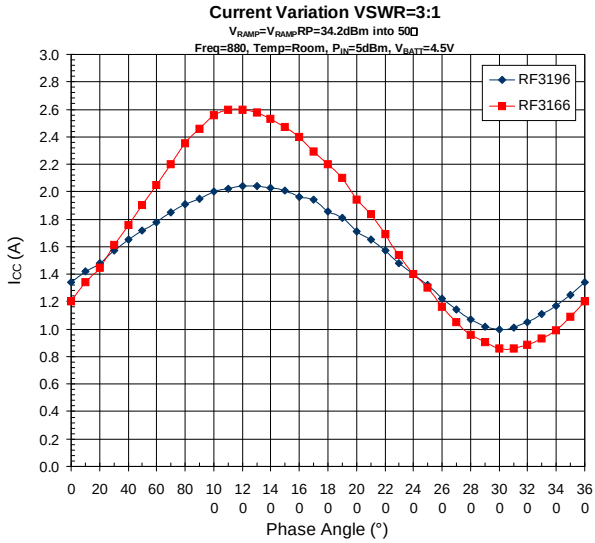

Figure 3. Current Variation into Mismatch

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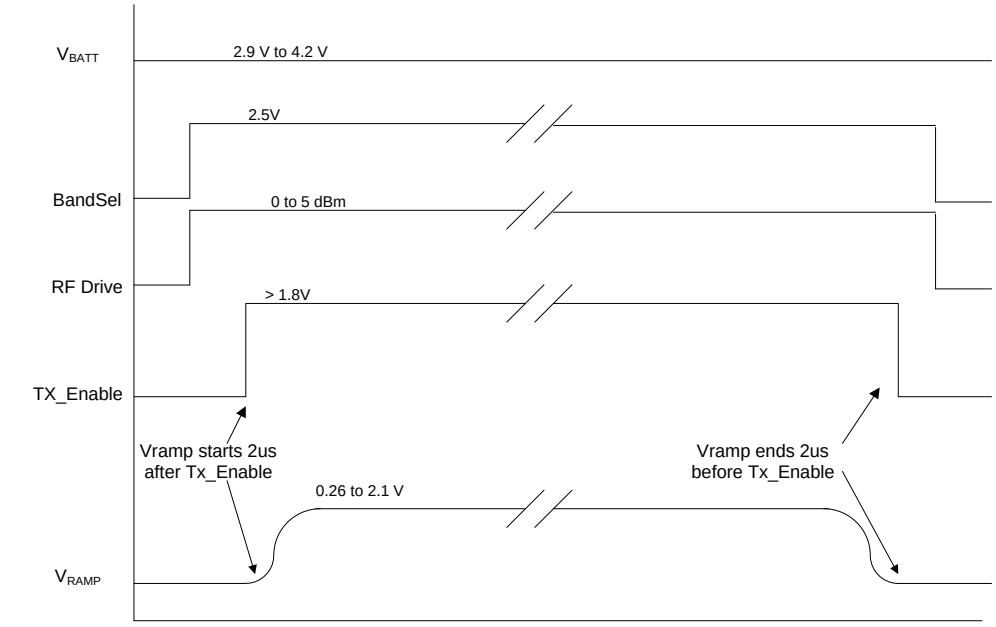
The power control functionality provides 50dB continuous control range and 70dB total control range, using a DAC compatible analog voltage input referred to as V_{RAMP}. The timing of the control signals is important for maintaining transient performance and superior isolation between the bursts. To ensure that the part ramps up properly, a timing diagram is provided below in Figure 4. It is important that ramping begins at least 2us after TXEN goes high. An offset voltage of 0.26V provides the greatest dynamic range for the best transient performance.



Power On Sequence:
Apply V_{BATT}
Apply Band Select
Apply RF drive
Apply TX_Enable & V_{RAMP} in unison

The Power Down sequence is in opposite order of the Power On Sequence

Figure 4. RF3196 Timing Diagram

As described in the above figure, V_{BATT} is applied first to provide bias to the silicon control chip. Then the RF drive is applied. Finally, when TX_ENABLE is high, the V_{RAMP} signal is held at constant 0.26V, and 2uS later, V_{RAMP} begins to ramp up.

The shape of V_{RAMP} is important for maintaining the switching transients. The basic shape of the ramping function should be the first 90° of a raised sine function. This is shown in Equation 1 where A is the desired peak power in mW, B is the minimum output power of the power amplifier in mW, K determines the duration of the ramp, and t is time. The down-ramp function uses the same equation except a cosine function is used in the place of the sine function. The exponent "n" determines the steepness of the ramp and is typically set to 5.

$$P_{OUT}(mW) = (A-B)\cdot(\sin(Kt))^{n} + B \quad \text{(Eq. 1)}$$

The value of K is calculated using Equation 2.

$$K = \frac{\pi}{2 \cdot t_{ramp}} \quad \text{(Eq. 2)}$$

The Ramp synthesis tool provided by RFMD generates the ramp profiles automatically. It will generate ramps for all power levels and output the waveform for 8, 10, and 12 bit DACs in decimal, voltage, or hex formats.

The spectrum is maintained at all power levels. The following figures show power ramping at max and backed off power.

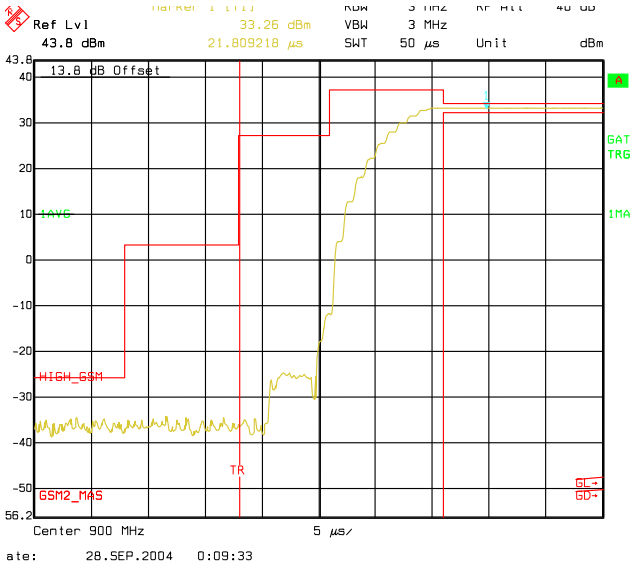


Figure 5. Full Power Ramping

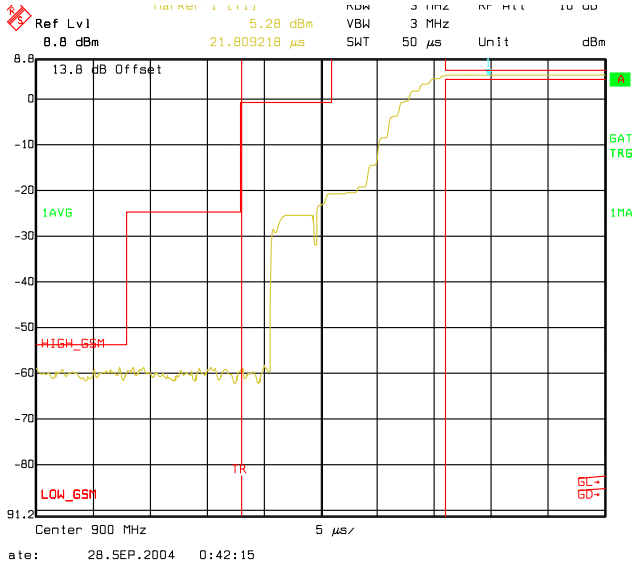


Figure 6. Low Power Ramping

Summary

The RF3196 is the next generation of PowerStar® Power Amplifiers. The type of power control used in the RF3196 is a closed loop method that regulates the collector voltage of the amplifier while the stages are held at a constant bias. The V_{BATT} tracking circuit monitors V_{BATT} levels so that the transient spectrum never degrades and the new power flattening circuit reduces power and current variation in high current situations.

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PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

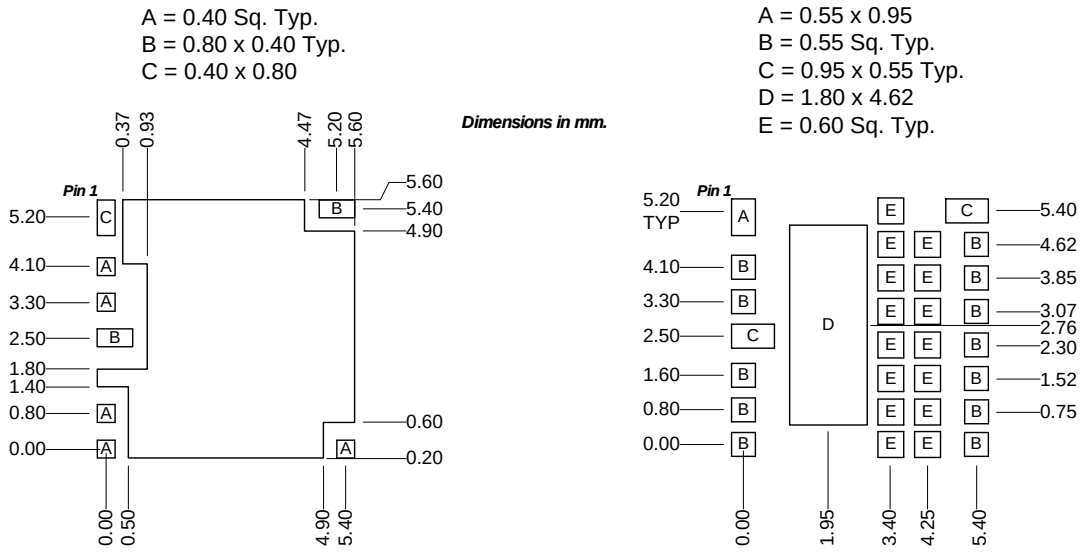

Figure 1. PCB Metal Land and Solder Mask Patterns (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

Thermal Pad and Via Design

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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Material Declaration

RoHS* Banned Material Content

RoHS Compliant: **Yes**
Package total weight in grams (g): **0.117**
Compliance Date Code: **N/A**
Bill of Materials Revision: **3196E4.9 Rev.B**
Pb Free Category: **e4**

Bill of Materials	Parts Per Million (PPM)					
	Pb	Cd	Hg	Cr VI	PBB	PBDE
Permissible Concentration Limits per EU Decision 2005/618/EC	1000	0	0	0	0	0
Substrate	0	0	0	0	0	0
Passive Components	335	0	0	0	0	0
Die	0	0	0	0	0	0
Molding Compound	0	0	0	0	0	0
Die Attach Epoxy	0	0	0	0	0	0
Wire	0	0	0	0	0	0
Solder Plating	0	0	0	0	0	0

This RoHS banned material content declaration was prepared solely on information, including analytical data, provided to RFMD by its suppliers, and applies to the Bill of Materials (BOM) revision noted above.

* DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Pb noted in this material declaration is used in glass or ceramics in electronic components which is an allowed exemption from the RoHS regulations, see Annex to Directive 2002/95/EC and amendment 2005/747/EC.

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