

VN0610LL, VN10LM

N-Channel Enhancement-Mode MOS Transistors

VN0610LL / VN10LM

FEATURES

- Low $r_{DS(on)} < 5\Omega$

APPLICATIONS

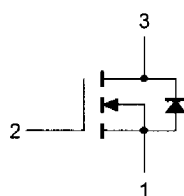
- Switching
- Amplification

ORDERING INFORMATION

Part	Package	Temperature Range
VN0610LL	Plastic TO-92	-55°C to +150°C
VN10LM	Plastic TO-237	-55°C to +150°C

For sorted chips in carriers see 2N7000

PIN CONNECTIONS



CD5



TO-92
(TO-226AA)

BOTTOM VIEW



1. SOURCE
2. GATE
3. DRAIN



TO-237

BOTTOM VIEW



1. SOURCE
2. GATE
3. TAB-DRAIN

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

SYMBOL	PARAMETERS/TEST CONDITIONS	LIMITS		UNITS
		VN0610LL	VN10LM	
V_{DS}	Drain-Source Voltage	60	60	V
V_{GS}	Gate-Source Voltage	± 30	± 30	V
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$ $T_A = 100^\circ\text{C}$	0.28 0.32	A
I_{DM}	Pulsed Drain Current ¹	1.3	1.4	A
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$ $T_A = 100^\circ\text{C}$	0.8 0.4	W
T_J, T_{stg}	Operating Junction & Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_L	Lead Temperature (1/16" from case for 10 sec.)	300		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

SYMBOL	THERMAL RESISTANCE	LIMITS		UNITS
		VN0610LL	VN10LM	
R_{thJA}	Junction-to-Ambient	156	125	K/W

¹Pulse width limited by maximum junction temperature.

VN0610LL / VN10LM

SPECIFICATIONS ^a		LIMITS				
SYMBOL	PARAMETER	TYP ^b	MIN	MAX	UNIT	TEST CONDITIONS
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	70	60		V	I _D = 100μA, V _{GS} = 0V
V _{GS(th)}	Gate-Threshold Voltage	2.3	0.8	2.5		V _{DS} = V _{GS} , I _D = 1mA
I _{GSS}	Gate-Body Leakage			±100	nA	V _{GS} = ±30V, V _{DS} = 0V
I _{DSS}	Zero Gate Voltage Drain Current			10	μA	V _{DS} = 50V, V _{GS} = 0V
				500		T _J = 125°C
I _{D(ON)}	On-State Drain Current ^d	1000	750		mA	V _{DS} = 10V, V _{GS} = 10V
r _{DS(ON)}	Drain-Source On-Resistance ^c	5		7.5	Ω	V _{GS} = 5V, I _D = 0.2A
		2.5		5		V _{GS} = 10V, I _D = 0.5A
		4.4		9		T _J = 125°C
g _{FS}	Forward Transconductance ^c	230	100		mS	V _{DS} = 10V, I _D = 0.5A
g _{OS}	Common Source Output Conductance ^c	500			μS	V _{DS} = 5V, I _D = 50mA
DYNAMIC						
C _{iss}	Input Capacitance	16		60	pF	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz
C _{oss}	Output Capacitance	11		25		
C _{rss}	Reverse Transfer Capacitance	2		5		
SWITCHING						
t _{ON}	Turn-On Time	7		10	ns	V _{DD} = 15V, R _L = 23Ω, I _D = 0.6A V _{GEN} = 10V, R _G = 25Ω
t _{OFF}	Turn-Off Time	7		10		(Switching time is essentially independent of operating temperature)

Notes:

- T_A = 25°C unless otherwise noted.
- For design aid only, not subject to production testing.
- Pulse test; PW = ≤300μS, duty cycle ≤2%.
- Pulse width limited by maximum junction temperature.