1 PRODUCT OVERVIEW

OVERVIEW

The KS57C5404 single-chip CMOS microcontroller is designed for high-performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

With a versatile 8-bit timer/counter and a D/A converter, the KS57C5404 offers an excellent design solution for a wide variety of telecommunication applications.

Up to 17 pins of the 24-pin SDIP package can be dedicated to I/O. Four vectored interrupts provide fast response to internal and external events. In addition, the KS57C5404's advanced CMOS technology has realized substantially lower power consumption with a wide operating voltage range — all at a substantially lower cost.

OTP

The KS57C5404 microcontroller is also available in OTP (One Time Programmable) version, KS57P5404. KS57P5404 microcontroller has an on-chip 4-Kbyte one-time-programmable EPROM instead of masked ROM. The KS57P5404 is comparable to KS57C5404, both in function and in pin configuration.

FEATURES SUMMARY

Memory

- 512 × 4-bit RAM
- 4096 × 8-bit ROM

I/O Pins

- 17 pins I/O
- N-channel open-drain I/O: 8 pins

8-Bit Basic Timer

- Programmable interval timer
- Watchdog timer

Interval 8-Bit Timer/Counter

- Programmable interval timer
- External event counter function
- Timer/counter clock output to TCLO0 pin

Buzzer Output

- Four frequency output to BUZ pin

D/A Converter

- 8-bit D/A converter

Interrupts

- Two external interrupt vectors
- Two internal interrupt vectors
- One quasi-interrupt

Memory-Mapped I/O Structure

- Data memory bank 15

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (system clock stops)

Oscillation Sources

- Crystal, or ceramic for system clock
- Crystal, ceramic: 0.4–6.0 MHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, and 15.3 μs at 4.19 MHz
- 0.67, 1.33, 10.7 μs at 6.0 MHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V (at 3 MHz)
- 2.7 V to 5.5 V (at 6 MHz)

Package Types

- 24-pin SOP-375
- 24-pin SDIP-300

BLOCK DIAGRAM

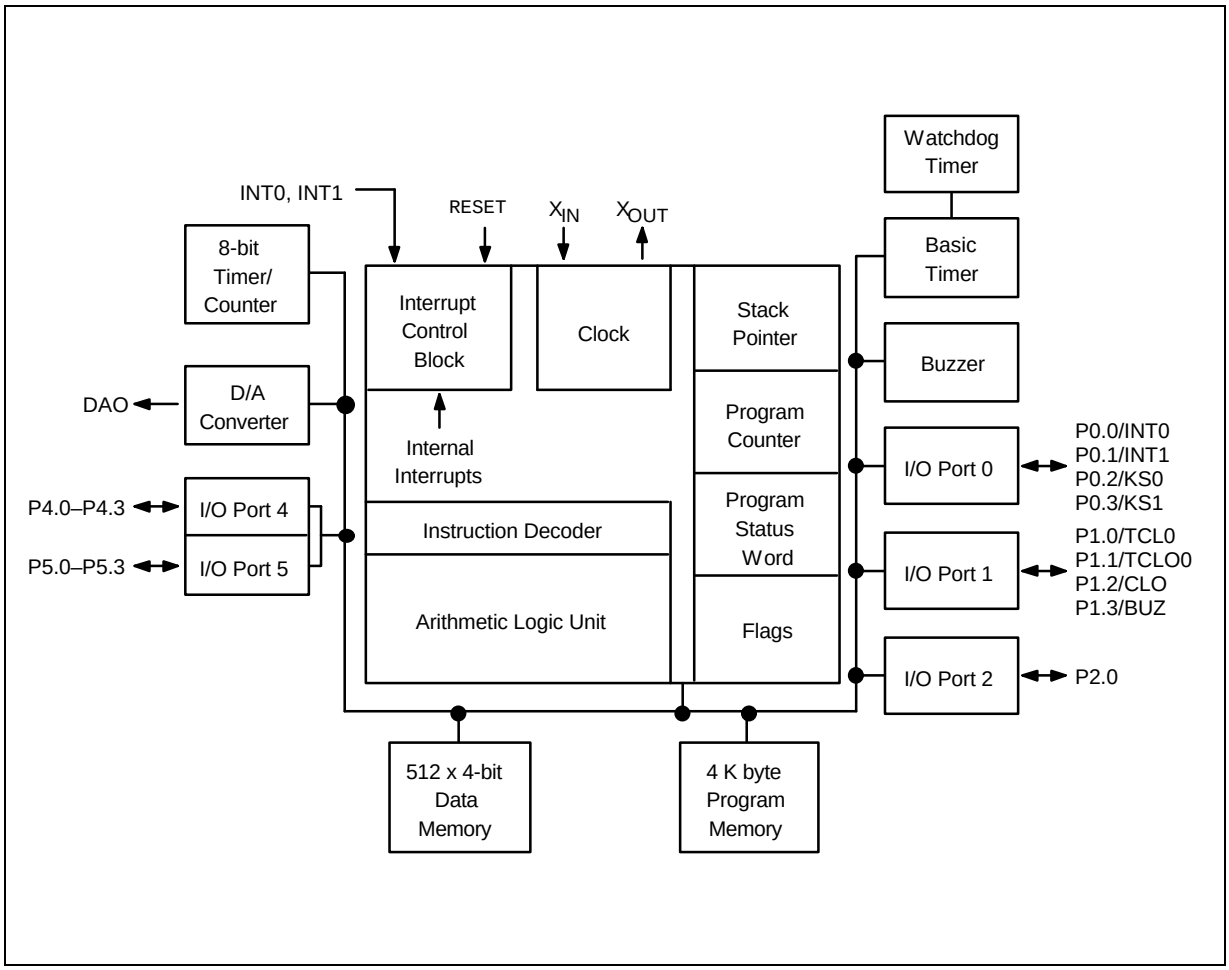


Figure 1-1. KS57C5404 Simplified Block Diagram

PIN ASSIGNMENTS

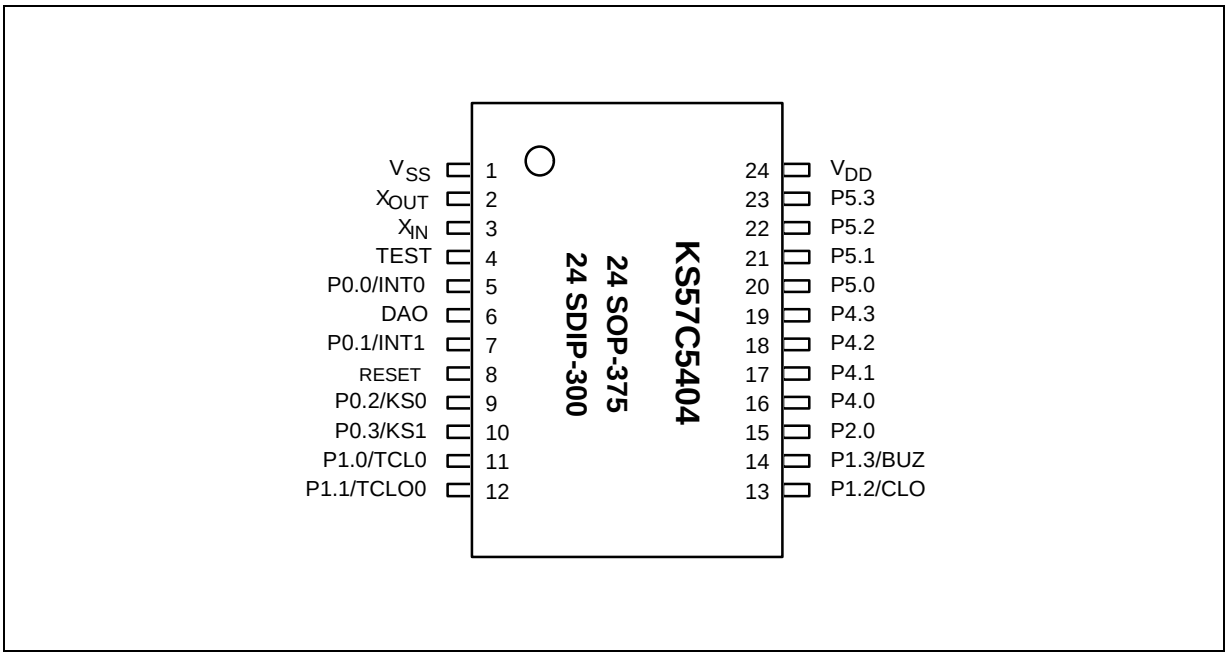


Figure 1-2. KS57C5404 Pin Assignment Diagrams

PIN DESCRIPTIONS

Table 1-1. KS57C5404 Pin Descriptions

Pin Name	Pin Type	Description	Share Pin
P0.0 P0.1 P0.2 P0.3	I	4-bit I/O port. 1- or 4-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins are individually configurable as input or output.	INT0 INT1 KS0 KS1
P1.0 P1.1 P1.2 P1.3	I/O	4-bit I/O port. 1- or 4-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins are individually configurable as input or output.	TCL0 TCLO0 CLO BUZ
P2.0	I/O	1-bit I/O port. 1- or 4-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins.	–
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O port. 1- or 4-bit read/write and test is possible. Pins are individually configurable as input or output. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. The N-channel open drain or push-pull output can be selected by software (1-bit unit).	–
INT0	I/O	External interrupts with rising/falling edge detection	P0.0
INT1	I/O	External interrupts with rising/falling edge detection	P0.1
KS0 KS1	I/O	Quasi-interrupt input with falling edge detection	P0.2 P0.3
TCL0	I/O	External clock input for timer/counter	P1.0
TCLO0	I/O	Timer/counter clock output	P1.1
CLO	I/O	CPU clock output	P1.2
BUZ	I/O	0.5, 1, 2, or 4 kHz frequency output at 4.19 MHz for buzzer sound	P1.3
DAO	O	8-bit D/A converter output	–
VDD	–	Main power supply	–
VSS	–	Ground	–
RESET	I	Reset signal	–
TEST	I	Chip test input pin. Hold GND when the device is operating.	–
X_{IN}, X_{OUT}	–	Crystal, ceramic oscillator signal for system clock	–

Table 1-2. Overview of KS57C5404 Pin Data

SDIP Pin Numbers	Share Pins	I/O Type	Reset Value	Circuit Type
V_{SS}	–	–	–	–
X_{OUT}, X_{IN}	–	–	–	–
TEST	–	I	–	–
P0.0, P0.1	INT0, INT1	I/O	Input	D-4
RESET	–	I	–	B
P0.2 P0.3	KS0 KS1	I/O	Input	D-4
P1.0 P1.1 P1.2 P1.3	TCL0 TCLO0 CLO BUZ	I/O	Input	D-2
P2.0	–	I/O	Input	D-2
DAO	–	O	Output	–
P4.0–P4.3	–	I/O	Input	E-2
P5.0–P5.3	–	I/O	Input	E-2
V_{DD}	–	–	–	–

PIN CIRCUIT DIAGRAMS

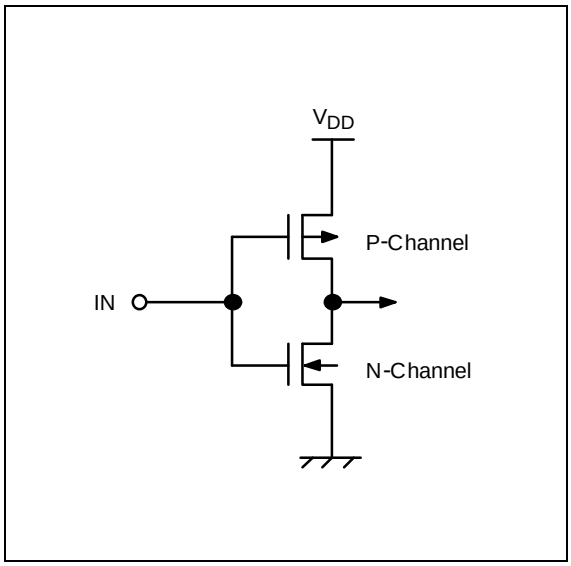


Figure 1-3. Pin Circuit Type A

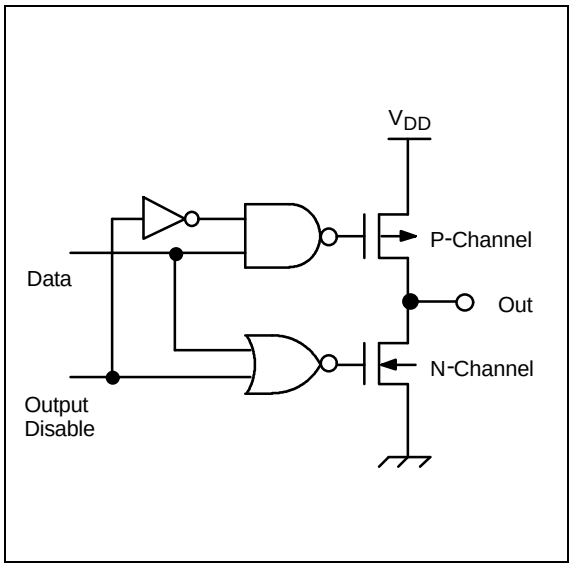


Figure 1-5. Pin Circuit Type C

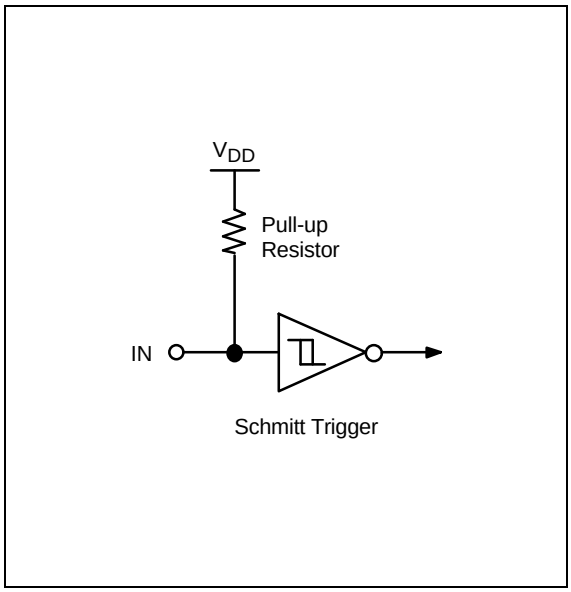


Figure 1-4. Pin Circuit Type B

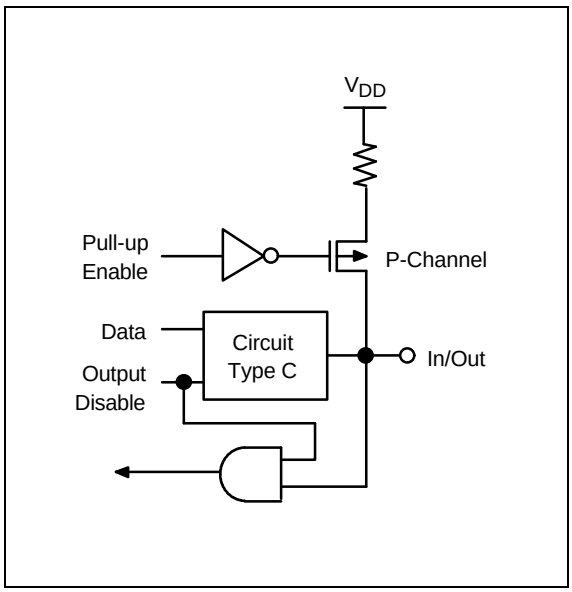


Figure 1-6. Pin Circuit Type D-2

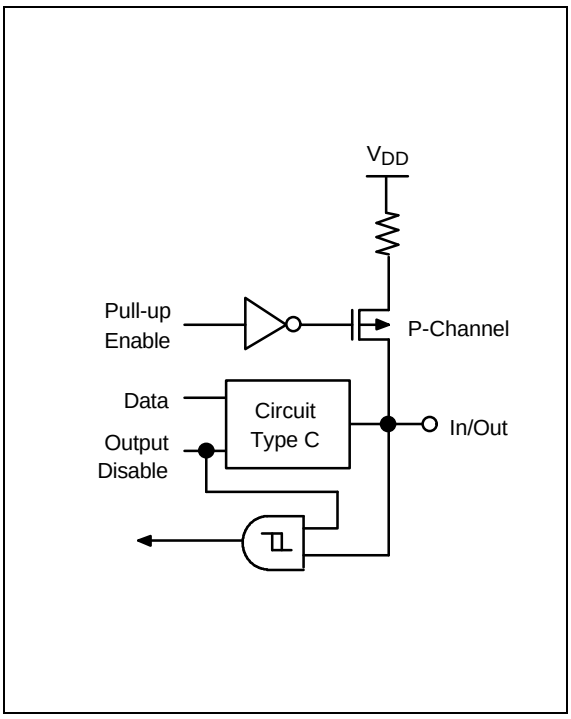


Figure 1-7. Pin Circuit Type D-4

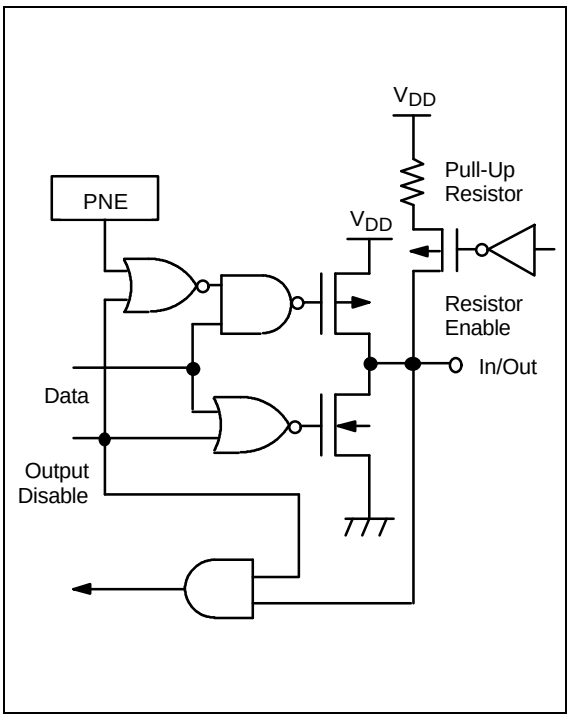


Figure 1-8. Pin Circuit Type E-2

14 ELECTRICAL DATA

OVERVIEW

In this section, KS57C5404 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

Standard Electrical Characteristics

— Absolute maximum ratings
— D.C. electrical characteristics
— Main system clock oscillator characteristics
— Subsystem clock oscillator characteristics
— I/O capacitance
— A.C. electrical characteristics
— Operating voltage range

Miscellaneous Timing Waveforms

— A.C timing measurement point
— Clock timing measurement at X_{in}
— Clock timing measurement at XT_{in}
— TCL timing
— Input timing for RESET
— Input timing for external interrupts
— Serial data transfer timing

Stop Mode Characteristics and Timing Waveforms

— RAM data retention supply voltage in stop mode
— Stop mode release timing when initiated by RESET
— Stop mode release timing when initiated by an interrupt request

Table 14-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_I	All I/O ports	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O port active	– 5	mA
		All I/O ports active	– 35	
Output Current Low	I_{OL}	One I/O port active	+ 30 (peak)	mA
			+ 15 (note)	
		All I/O ports active	+ 100 (peak)	
			+ 60 (note)	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	°C

NOTE: The values for output current low (I_{OL}) are calculated as peak value $\times \sqrt{\text{Duty}}$.

Table 14-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins except V_{IH2}–V_{IH3}	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	P0 and RESET	0.8 V_{DD}	–	V_{DD}	
	V_{IH3}	X_{IN} and X_{OUT}	V_{DD} – 0.1	–	V_{DD}	
Input Low Voltage	V_{IL1}	All input pins except V_{IH2}–V_{IH3}	–	–	0.3 V_{DD}	V
	V_{IL2}	P0 and RESET			0.2 V_{DD}	
	V_{IL3}	X_{IN} and X_{OUT}			0.1	

Table 14-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Voltage	V_{OH}	V_{DD} = 4.5 V to 5.5 V I_{OH} = – 1 mA	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA Ports 4, 5	–	–	2	V
		V_{DD} = 1.8 V to 5.5 V I_{OL} = 1.6 mA			0.4	
	V_{OL2}	V_{DD} = 4.5V to 5.5 V I_{OL} = 4 mA All out ports except ports 4, 5			2	
		V_{DD} = 1.8 V to 5.5 V I_{OL} = 1.6 mA			0.6	
Input High Leakage Current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{IN} and X_{OUT}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN} and X_{OUT}			20	
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}, X_{OUT} and RESET	–	–	– 3	µA
	I_{LIL2}	V_{IN} = 0 V X_{IN} and X_{OUT}			– 20	
Output High Leakage Current	I_{LOH}	V_O = V_{DD} All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V All output pins	–	–	– 3	µA
Pull-up Resistor	R_{L1}	V_{DD} = 5 V; V_I = 0 V except RESET	25	45	100	kΩ
		V_{DD} = 3 V	50	90	200	
	R_{L2}	V_{DD} = 5 V; V_I = 0 V; RESET	100	220	400	
		V_{DD} = 3 V	200	450	800	

Table 14-2. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	I_{DD1} (DAC on)	Run mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	3.4	10.0	mA
		Crystal oscillator; C1 = C2 = 22pF	4.19MHz		2.7	8.0	
	I_{DD2} (DAC off)	Run mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	2.3	8.0	mA
		Crystal oscillator; C1 = C2 = 22pF	4.19MHz		1.7	5.5	
		V_{DD} = 3 V ± 10%	6.0MHz		1.1	4.0	
			4.19MHz		0.8	3.0	
	I_{DD3}	Idle mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	0.7	2.5	mA
		Crystal oscillator; C1 = C2 = 22pF	4.19MHz		0.5	1.8	
		V_{DD} = 3 V ± 10%	6.0MHz		0.3	1.5	
			4.19MHz		0.2	1.0	
	I_{DD4}	Stop mode; V_{DD} = 5.0 V ± 10%		–	0.2	3.0	µA
		Stop mode; V_{DD} = 3.0 V ± 10%			0.1	2.0	

NOTES:
1. D.C. electrical values for supply current (I_{DD1} to I_{DD3}) do not include the current drawn through internal pull-up resistors.
2. I_{DD1} typical values are measured when DADATA register value is 055H.

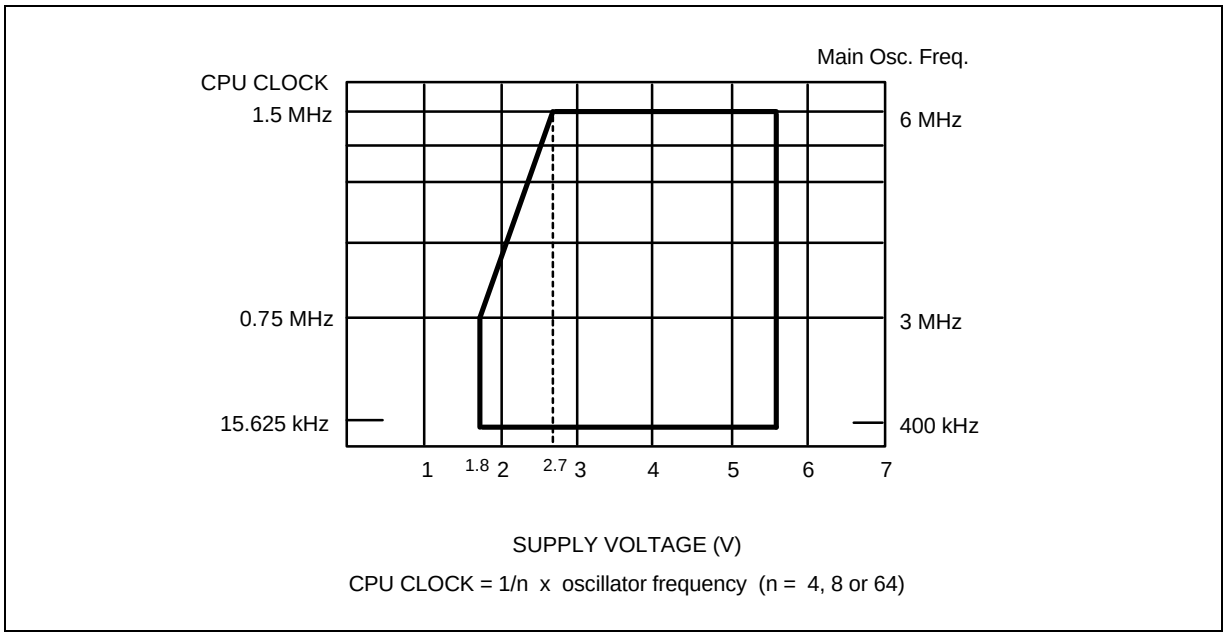
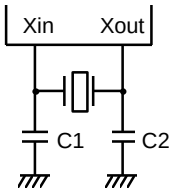
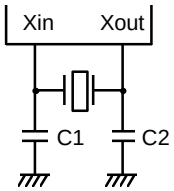
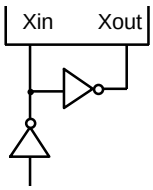


Figure 14-1. Standard Operating Voltage Range

Table 14-3. Oscillators Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3	
		Stabilization time (2)	V_{DD} = 3.0 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3	
		Stabilization time (2)	V_{DD} = 3.0 V	–	–	10	ms
External Clock		X_{IN} input frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3	
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1250	ns

NOTES:

1. Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 14-4. Recommended Oscillator Constants

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Manufacturer	Series Number (1)	Frequency Range	Load Cap (pF)		Oscillator Voltage Range (V)		Remarks
			C1	C2	MIN	MAX	
TDK	FCR ðÿM5	3.58 MHz–6.0 MHz	33	33	2.0	5.5	Leaded Type
	FCR ðÿMC5	3.58 MHz–6.0 MHz	(2)	(2)	2.0	5.5	On-chip C Leaded Type
	CCR ðÿMC3	3.58 MHz–6.0 MHz	(3)	(3)	2.0	5.5	On-chip C SMD Type

NOTES:
1. Please specify normal oscillator frequency.
2. On-chip C: 30pF built in.
3. On-chip C: 38pF built in.

Table 14-5. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}				15	pF
I/O Capacitance	C_{IO}				15	pF

Table 14-6. D/A Converter Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 3.5 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Resolution	–	–	–	–	8	bits
Absolute Accuracy	–		– 3	–	3	LSB
Differential Linearity Error	DLE		– 1	–	1	LSB
Setup Time	t_{su}		–	–	5	µs
Output Resistance	R_O		4.5	5	5.5	KΩ

Table 14-7. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 1.8 V to 5.5 V	1.33			
TCL0 Input Frequency	f_{TI}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 1.8 V to 5.5 V			1	MHz
TCL0 Input High, Low Width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	µs
		V_{DD} = 1.8 V to 5.5 V	1.8			
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0, INT1, KS0–KS1	10	–	–	µs
RESET Input Low Width	t_{RSL}	Input	–	–	10	µs

Table 14-8. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17}/fx	–	ms
		Released by interrupt	–	(2)	–	ms

NOTES:
1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay the execution of CPU instructions during the wait time.

TIMING WAVEFORMS

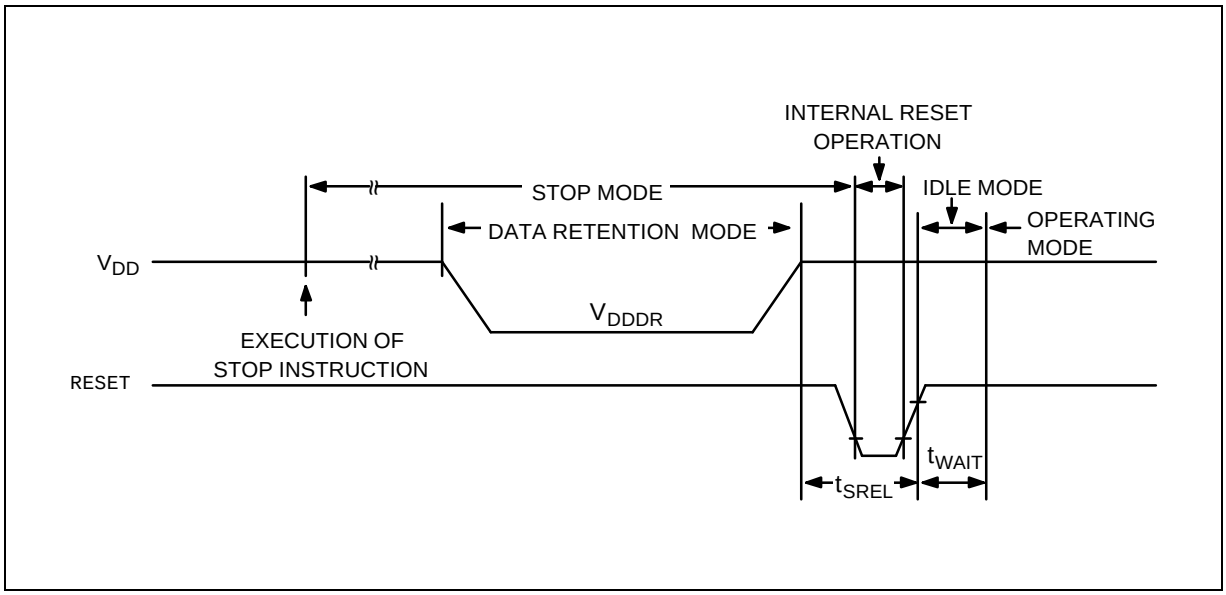


Figure 14-2. Stop Mode Release Timing When Initiated by RESET

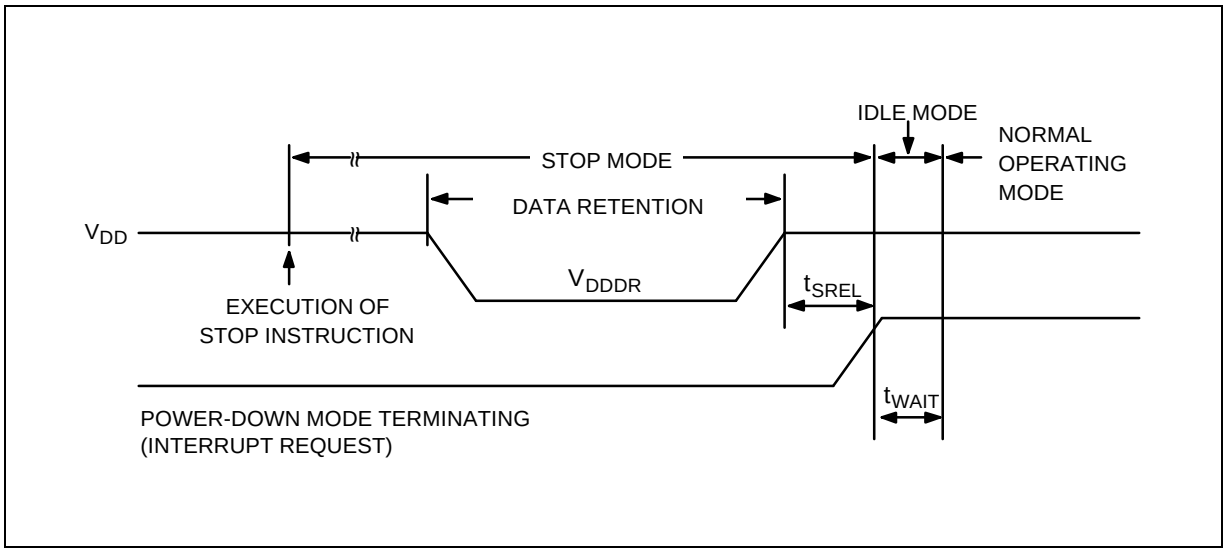


Figure 14-3. Stop Mode Release Timing When Initiated by Interrupt Request

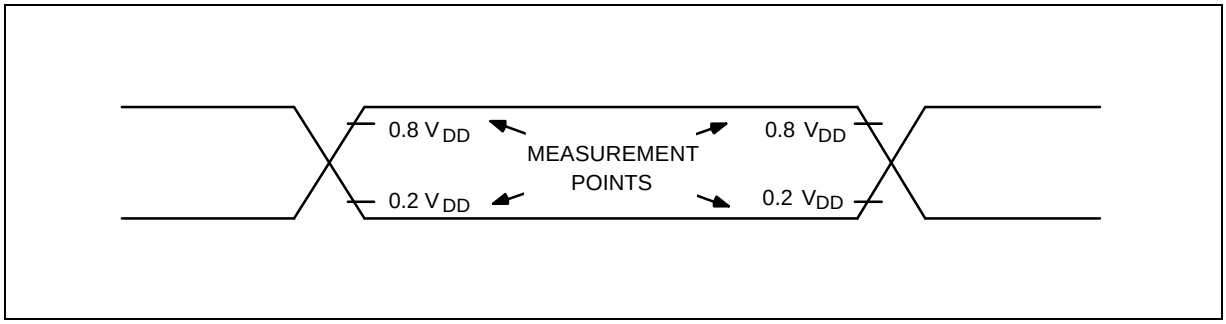


Figure 14-4. A.C. Timing Measurement Points (Except for X_{IN})

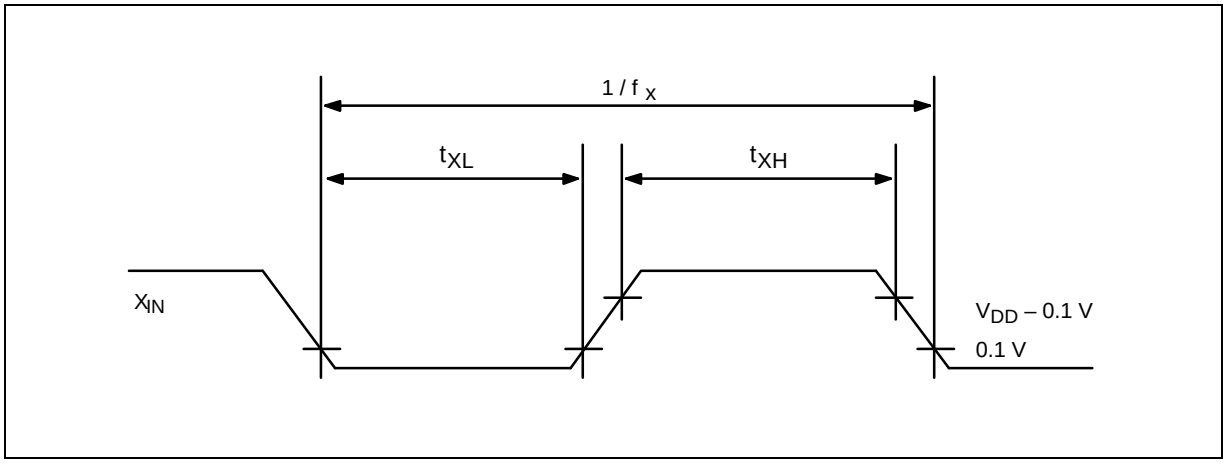


Figure 14-5. Clock Timing Measurement at X_{IN}

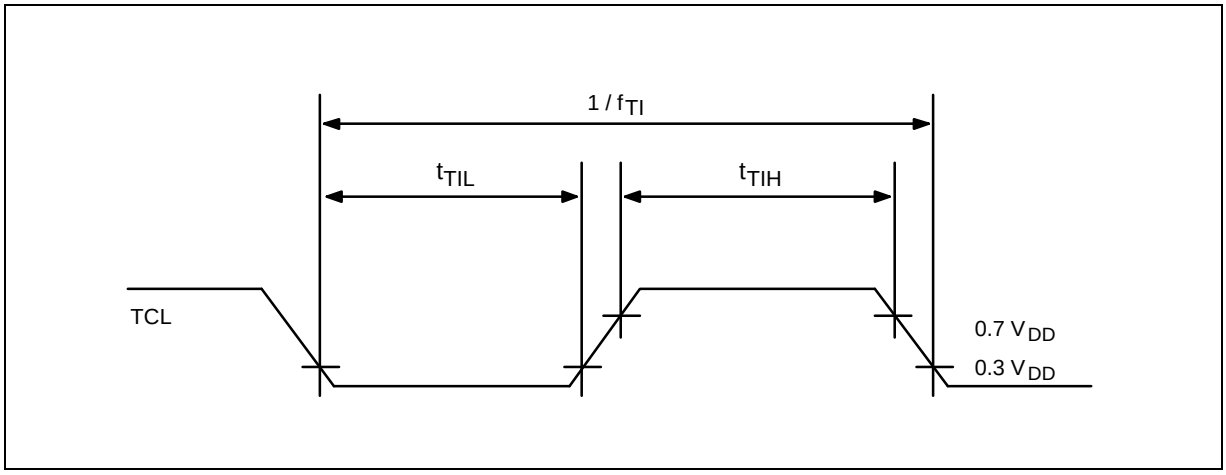


Figure 14-6. TCL Timing

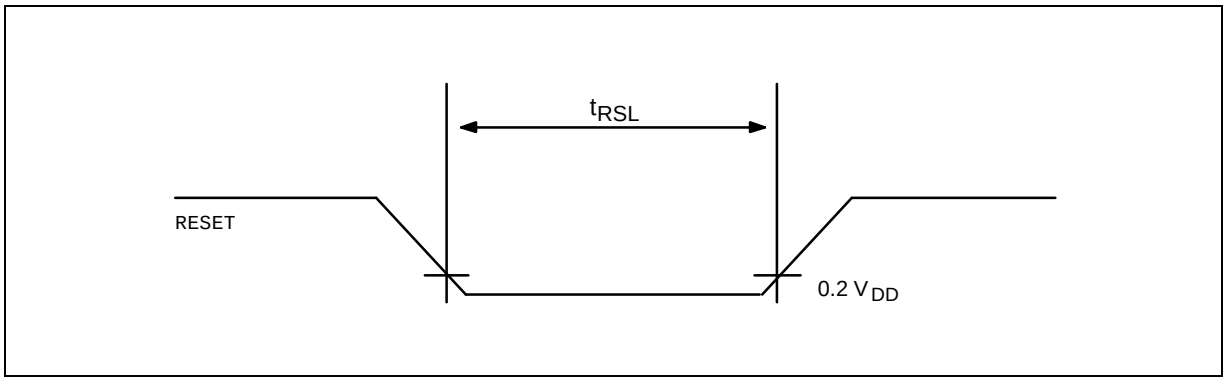


Figure 14-7. Input Timing for RESET Signal

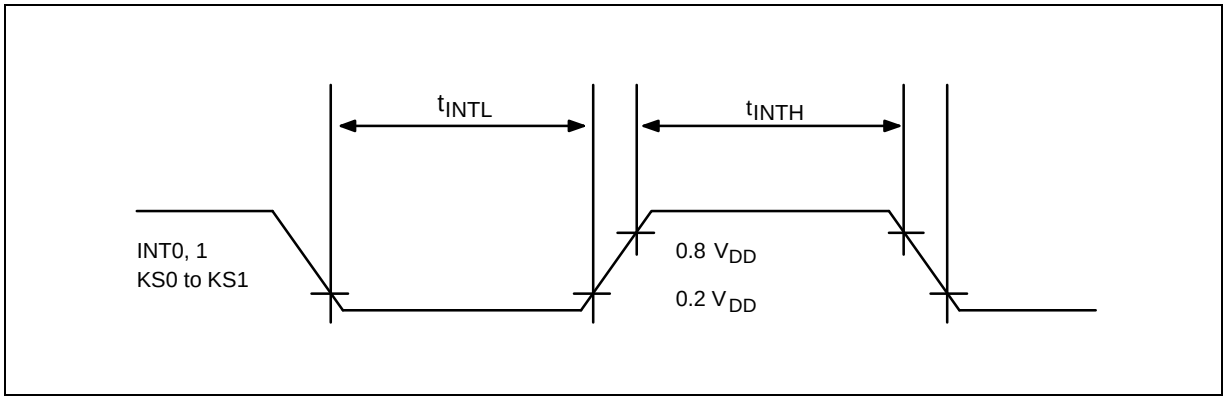


Figure 14-8. Input Timing for External Interrupts

15 MECHANICAL DATA

This section contains the following information about the device package:

— Package dimensions in millimeters
— Pad diagram
— Pad/pin coordinate data table

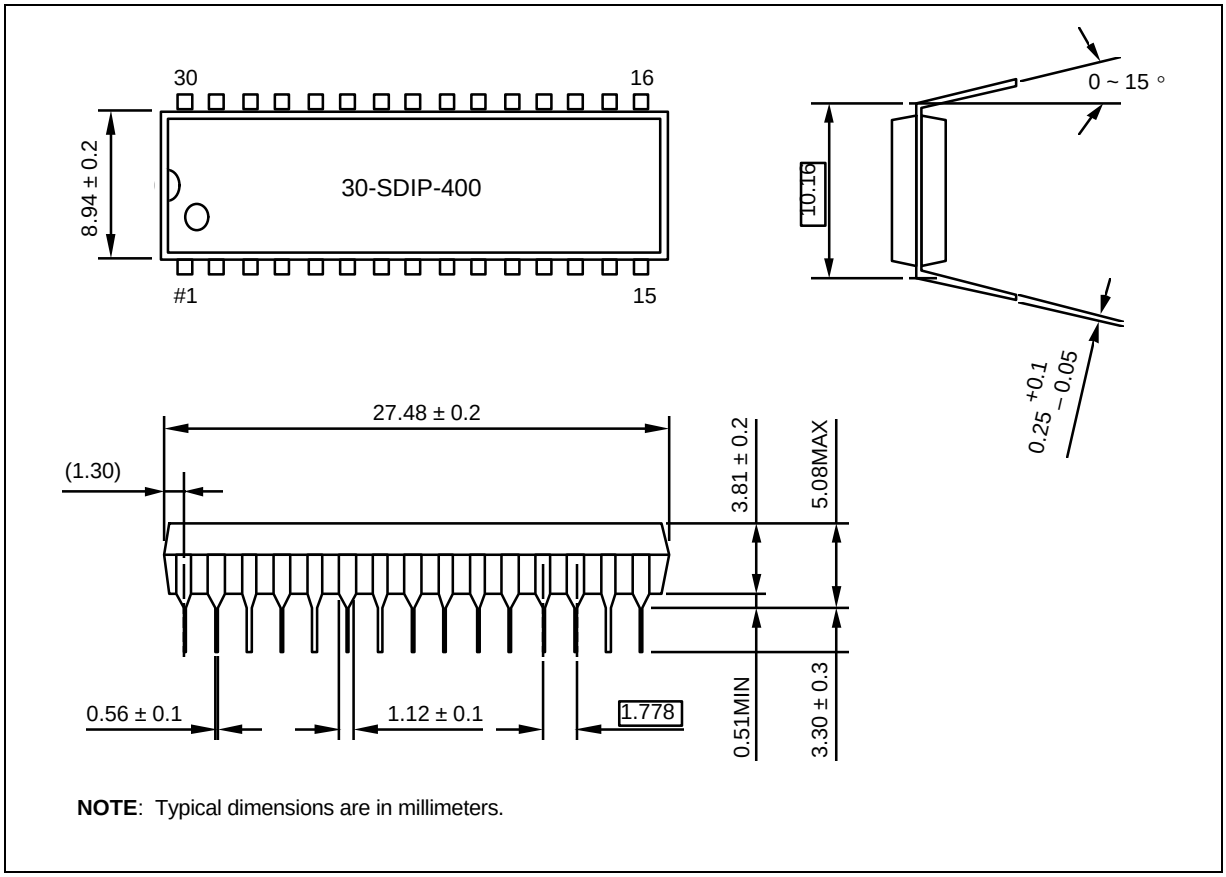


Figure 15-1. 30-SDIP-400 Package Dimensions

NOTES

16 KS57P5404 OTP

OVERVIEW

The KS57P5404 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the KS57C5404 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The KS57P5404 is fully compatible with the KS57C5404, both in function and in pin configuration. Because of its simple programming requirements, the KS57P5404 is ideal for use as an evaluation chip for the KS57C5404.

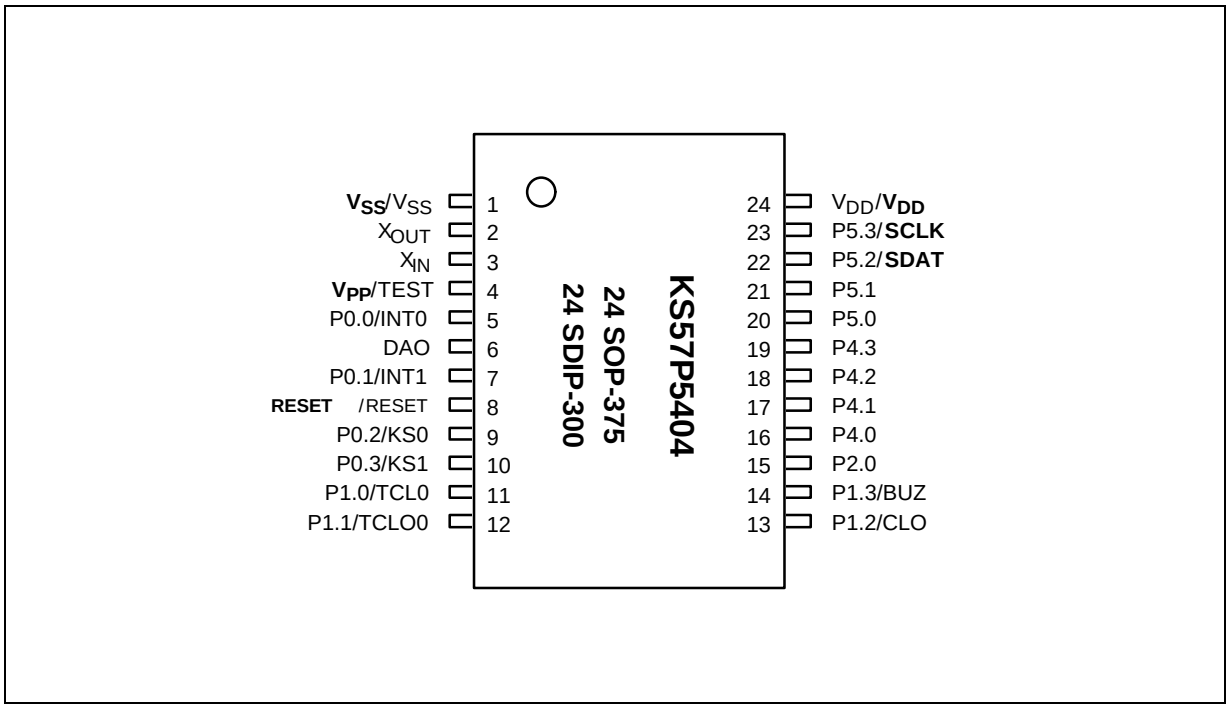


Figure 16-1. KS57P5404 Pin Assignments (24 SOP-375, 24 SDIP-300 Package)

Table 16-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P5.2	SDAT	22	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input / push-pull output port.
P5.3	SCLK	23	I/O	Serial clock pin. Input only pin.
TEST	TEST	4	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option) Hold GND when OTP is operating.
RESET	RESET	8	I	Chip initialization
V_{DD}/V_{SS}	V_{DD}/V_{SS}	24/1	–	Logic power supply pin. VDD should be tied to +5 V during programming.

NOTE: ( ) means the 32-SOP OTP pin number.

Table 16-2. Comparison of KS57P5404 and KS57C5404 Features

Characteristic	KS57P5404	KS57C5404
Program Memory	4 K-byte EPROM	4 K-byte mask ROM
Operating Voltage (V_{DD})	1.8 V (3 MHz) to 5.5 V	1.8 V (3 MHz) to 5.5 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (TEST) = 12.5 V	–
Pin Configuration	24 SOP, 24 SDIP	24 SOP, 24 SDIP
EPROM Programmability	User Program one time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP}(TEST) pin of the KS57P5404, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 16-3 below.

Table 16-3. Operating Mode Selection Criteria

V_{DD}	VPP (TEST)	REG/ MEM	ADDRESS (A15-A0)	R/W	MODE
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

OTP ELECTRICAL DATA

Table 16-4. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_I	All I/O ports	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O port active	– 5	mA
		All I/O ports active	– 35	
Output Current Low	I_{OL}	One I/O port active	+ 30 (peak)	mA
			+ 15 (note)	
		All I/O ports active	+ 100 (peak)	
			+ 60 (note)	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	°C

NOTE: The values for output current low (I_{OL}) are calculated as peak value $\times \sqrt{\text{Duty}}$.

Table 16-5. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins except V_{IH2}–V_{IH3}	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	P0 and RESET	0.8 V_{DD}	–	V_{DD}	
	V_{IH3}	X_{IN} and X_{OUT}	V_{DD} – 0.1	–	V_{DD}	
Input Low Voltage	V_{IL1}	All input pins except V_{IH2}–V_{IH3}	–	–	0.3 V_{DD}	V
	V_{IL2}	P0 and RESET			0.2 V_{DD}	
	V_{IL3}	X_{IN} and X_{OUT}			0.1	

Table 16-5. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Voltage	V_{OH}	V_{DD} = 4.5 V to 5.5 V I_{OH} = – 1 mA	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA Ports 4, 5	–	–	2	V
		V_{DD} = 1.8 V to 5.5 V I_{OL} = 1.6 mA			0.4	
	V_{OL2}	V_{DD} = 4.5V to 5.5 V I_{OL} = 4 mA All out ports except ports 4, 5			2	
		V_{DD} = 1.8 V to 5.5 V I_{OL} = 1.6 mA			0.6	
Input High Leakage Current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{IN} and X_{OUT}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN} and X_{OUT}			20	
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}, X_{OUT} and RESET	–	–	– 3	µA
	I_{LIL2}	V_{IN} = 0 V X_{IN} and X_{OUT}			– 20	
Output High Leakage Current	I_{LOH}	V_O = V_{DD} All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V All output pins	–	–	– 3	µA
Pull-up Resistor	R_{L1}	V_{DD} = 5 V; V_I = 0 V except RESET	25	50	100	kΩ
		V_{DD} = 3 V	50	100	200	
	R_{L2}	V_{DD} = 5 V; V_I = 0 V; RESET	100	250	400	
		V_{DD} = 3 V	200	500	800	

Table 16-5. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	I_{DD1} (DAC on)	Run mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	3.4	10.0	mA
		Crystal oscillator; C1 = C2 = 22pF	4.19MHz		2.7	8.0	
	I_{DD2} (DAC off)	Run mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	2.3	8.0	mA
		Crystal oscillator; C1 = C2 = 22pF	4.19MHz		1.7	5.5	
		V_{DD} = 3 V ± 10%	6.0MHz		1.1	4.0	
			4.19MHz		0.8	3.0	
	I_{DD3}	Idle mode; V_{DD} = 5.0 V ± 10%	6.0MHz	–	0.7	2.5	mA
		Crystal oscillator; C1 = C2 = 22pF	4.19MHz		0.5	1.8	
		V_{DD} = 3 V ± 10%	6.0MHz		0.3	1.5	
			4.19MHz		0.2	1.0	
	I_{DD4}	Stop mode; V_{DD} = 5.0 V ± 10%		–	0.2	3.0	µA
		Stop mode; V_{DD} = 3.0 V ± 10%			0.1	2.0	

NOTES:
1. D.C. electrical values for supply current (I_{DD1} to I_{DD3}) do not include the current drawn through internal pull-up resistors.
2. I_{DD1} typical values are measured when DADATA register value is 055H .

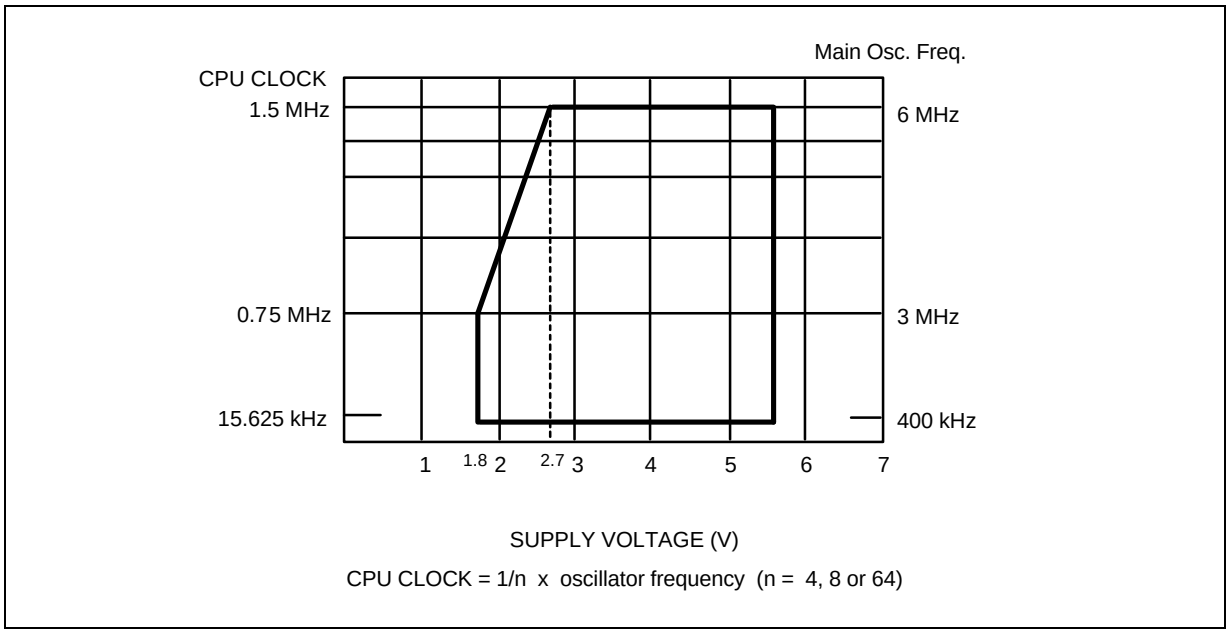
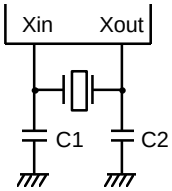
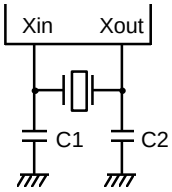
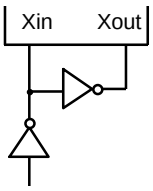


Figure 16-2. Standard Operating Voltage Range

Table 16-6. Oscillators Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3	
		Stabilization time (2)	V_{DD} = 3.0 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3	
		Stabilization time (2)	V_{DD} = 3.0 V	–	–	10	ms
External Clock		X_{IN} input frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3	
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1250	ns

NOTES:

1. Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 16-7. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}				15	pF
I/O Capacitance	C_{IO}				15	pF

Table 16-8. Comparator Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 3.5 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Resolution	–	–	–	–	8	bits
Absolute Accuracy	–		– 3	–	3	LSB
Differential Linearity Error	DLE		– 1	–	1	LSB
Setup Time	t_{su}		–	–	5	µs
Output Resistance	R_O		4.5	5	5.5	KΩ

Table 16-9. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 1.8 V to 5.5 V	1.33			
TCL0 Input Frequency	f_{TI}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 1.8 V to 5.5 V			1	MHz
TCL0 Input High, Low Width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	µs
		V_{DD} = 1.8 V to 5.5 V	1.8			
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0, INT1, KS0–KS1	10	–	–	µs
RESET Input Low Width	t_{RSL}	Input	–	–	10	µs

Table 16-10. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17}/fx	–	ms
		Released by interrupt	–	(2)	–	ms

NOTES:
1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay the execution of CPU instructions during the wait time.