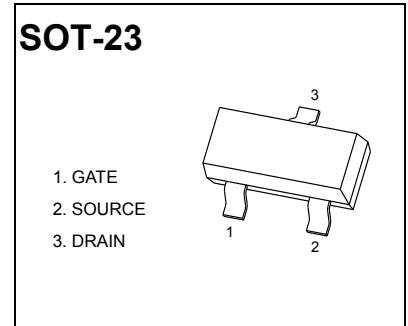


## SOT-23 Plastic-Encapsulate MOSFETS

### 50V N-Channel Enhancement Mode MOSFET

$V_{(BR)DSS}$	$R_{DS(on)MAX}$	$I_D$
50V	0.9Ω@10V	500mA
	1.1Ω@4.5V	



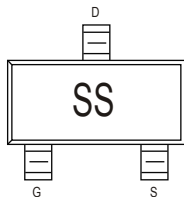
### FEATURE

- High density cell design for low  $R_{DS(ON)}$
- Rugged and Reliable
- Voltage controlled small signal switch
- High saturation current capability
- HMB ESD protected (2000V)

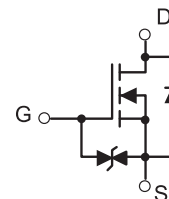
### APPLICATION

- Direct Logic-Level Interface: TTL/CMOS
- Drivers: Relays, Solenoids, Lamps, Hammers, Display, Memories, Transistors, etc.
- Battery Operated Systems
- Solid-State Relays

### MARKING



### Equivalent circuit



### PACKAGE SPECIFICATIONS

Package	Reel Size	Reel DIA. (mm)	Q'TY/Reel (pcs)	Box Size (mm)	QTY/Box (pcs)	Carton Size (mm)	Q'TY/Carton (pcs)
SOT-23	7'	178	3000	203×203×195	45000	438×438×220	180000

### MAXIMUM RATINGS ( $T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	$V_{DS}$	50	V	
Gate-Source Voltage	$V_{GS}$	±12		
Continuous Drain Current	$I_D$	$T_A=25^\circ\text{C}$	0.5	A
		$T_A=70^\circ\text{C}$	0.4	
Maximum Power Dissipation <sup>2)</sup>	$P_D$	$T_A=25^\circ\text{C}$	0.3	W
		$T_A=70^\circ\text{C}$	0.2	
Pulsed Drain Current <sup>1)</sup>	$I_{DM}$	1.8	A	
Operating Junction and Storage Temperature Range	$T_J$	150	°C	
Storage Temperature Range	$T_{stg}$	-50 to 150	°C	
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	400	°C/W	

Notes

1) Pulse width limited by maximum junction temperature.

2) Surface Mounted on FR4 Board,  $t \leq 5$  sec.



**MOSFET ELECTRICAL CHARACTERISTICS**

**T<sub>a</sub>=25 °C unless otherwise specified**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off characteristics</b>						
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	50			V
Gate-body leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V			±10	μA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V			1	μA
		V <sub>DS</sub> =40V, V <sub>GS</sub> =0V			100	μA
<b>On characteristics</b>						
Gate-threshold voltage (note 1)	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.60	1.0	1.5	V
Static drain-source on-resistance (note 1)	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =0.5A		0.9	2	Ω
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =0.3A		1.1	2.5	
		V <sub>GS</sub> =3.3V, I <sub>D</sub> =0.2A		1.5	4	
Forward transconductance (note 1)	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =0.25A	100			mS
<b>Dynamic characteristics (note 2)</b>						
Total Gate C harge	Q <sub>g</sub>	V <sub>DS</sub> =30V, I <sub>D</sub> =0.5A, V <sub>GS</sub> =10V		0.93		nC
Gate-Source Charge	Q <sub>gs</sub>			0.18		
Gate-Drain Charge	Q <sub>gd</sub>			0.31		
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, f=1MHz		23.8		pF
Output capacitance	C <sub>oss</sub>			3.9		
Reverse transfer capacitance	C <sub>rss</sub>			1.5		
<b>Switching characteristics</b>						
Turn-on delay time (note 1,2)	t <sub>d(on)</sub>	V <sub>DD</sub> =30V, V <sub>GS</sub> =10V, I <sub>D</sub> =0.3A, R <sub>GEN</sub> =3.3Ω		6		ns
Rise time (note 1,2)	t <sub>r</sub>			3.5		
Turn-off delay time (note 1,2)	t <sub>d(off)</sub>			20		
Fall time (note 1,2)	t <sub>f</sub>			5.9		
<b>Drain-source body diode characteristics</b>						
Source drain current(Body Diode)	I <sub>SD</sub>				0.2	A
Body diode forward voltage (note 1)	V <sub>SD</sub>	I <sub>S</sub> =0.5A, V <sub>GS</sub> = 0V		0.78	1.2	V

**Notes :**

1. Pulse Test : Pulse Width≤ 300μs, Duty Cycle 2%.
2. These parameters have no way to verify.

Typical Characteristics

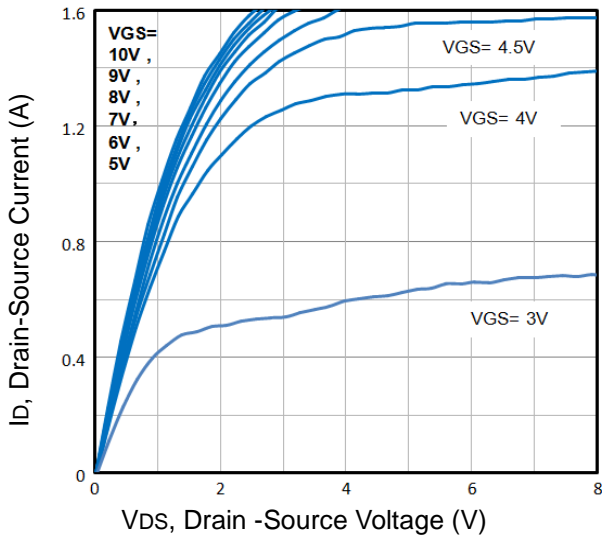


Fig1. Typical Output Characteristics

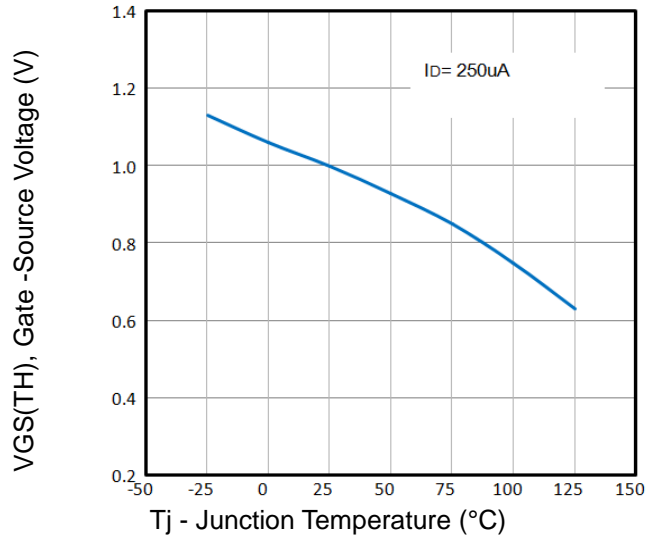


Fig2. Normalized Threshold Voltage Vs. Temperature

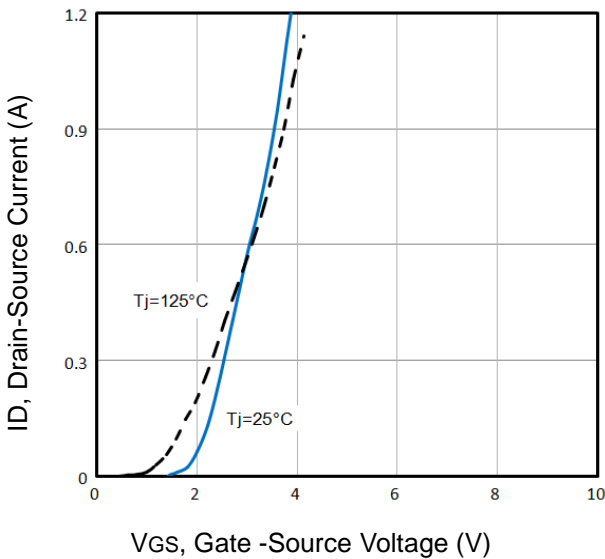


Fig3. Typical Transfer Characteristics

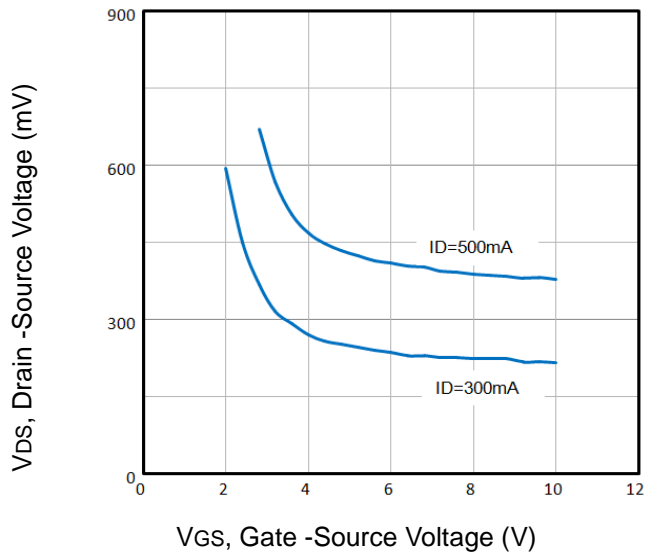


Fig4. Drain-Source Voltage vs Gate-Source Voltage

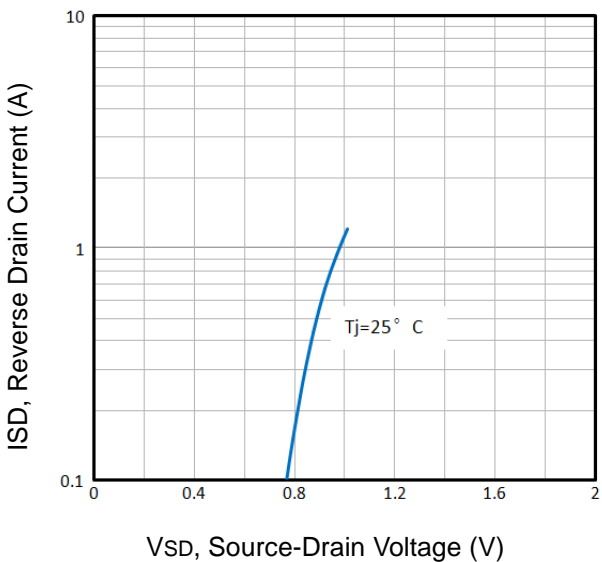


Fig5. Typical Source-Drain Diode Forward Voltage

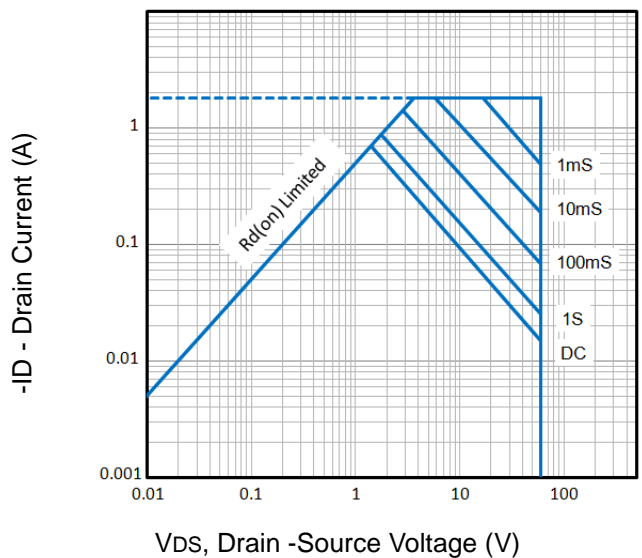
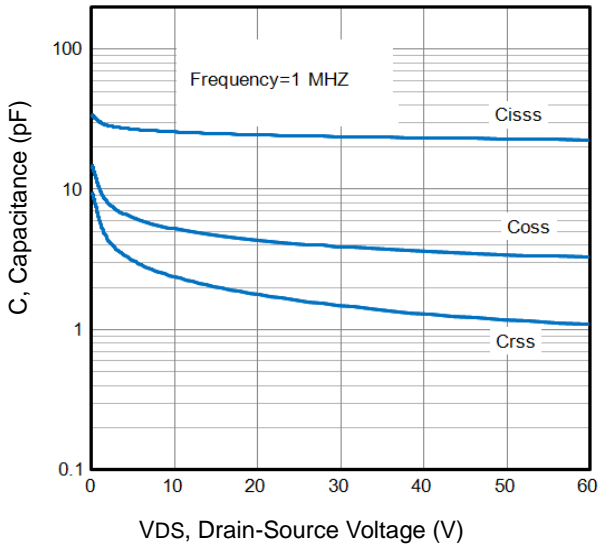


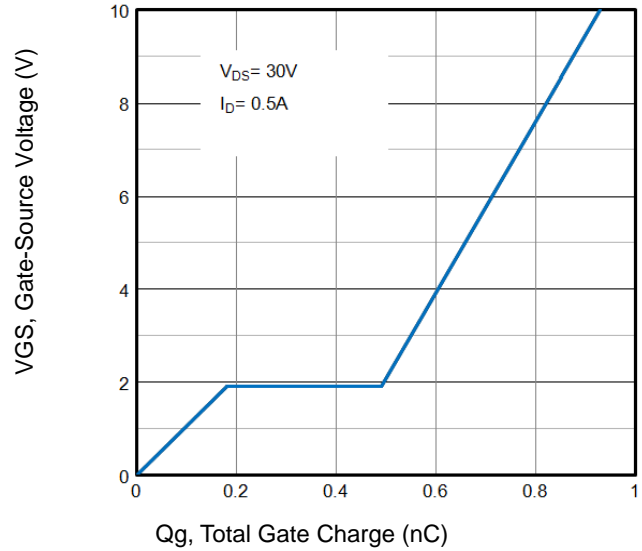
Fig6. Maximum Safe Operating Area

The curve above is for reference only.

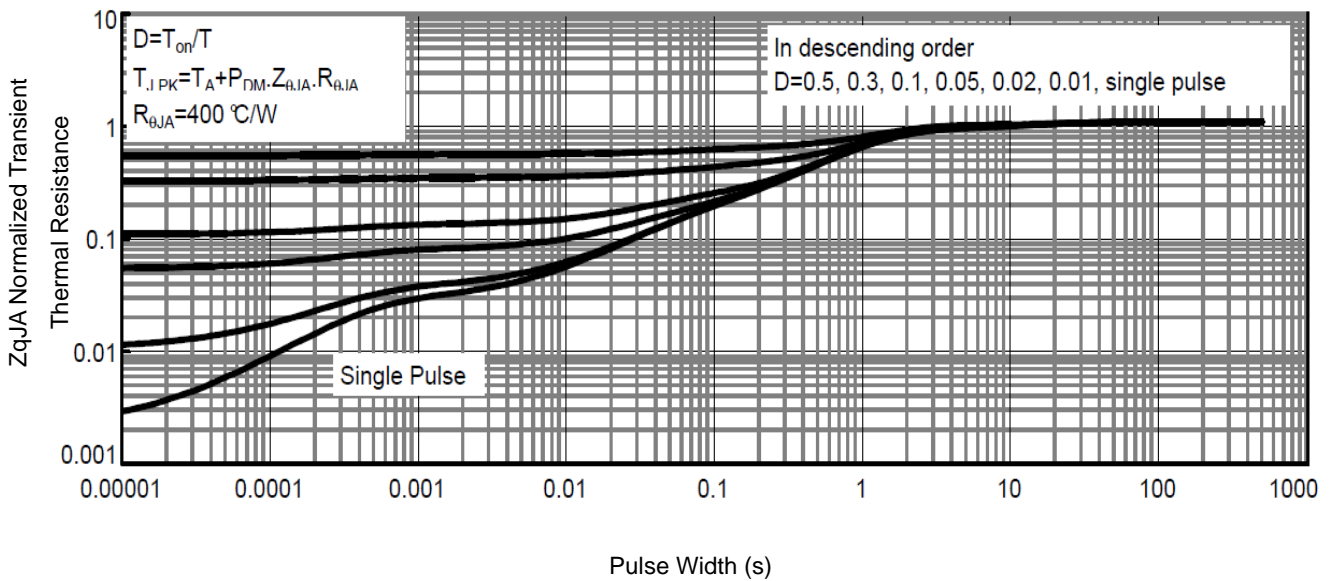
## Typical Characteristics



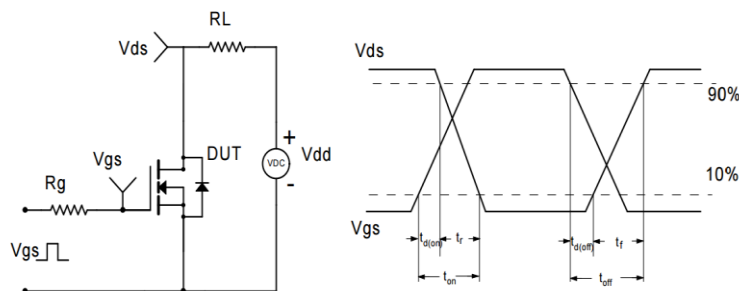
**Fig7.** Typical Capacitance Vs. Drain-Source Voltage



**Fig8.** Typical Gate Charge Vs. Gate-Source Voltage



**Fig9.** Normalized Maximum Transient Thermal Impedance

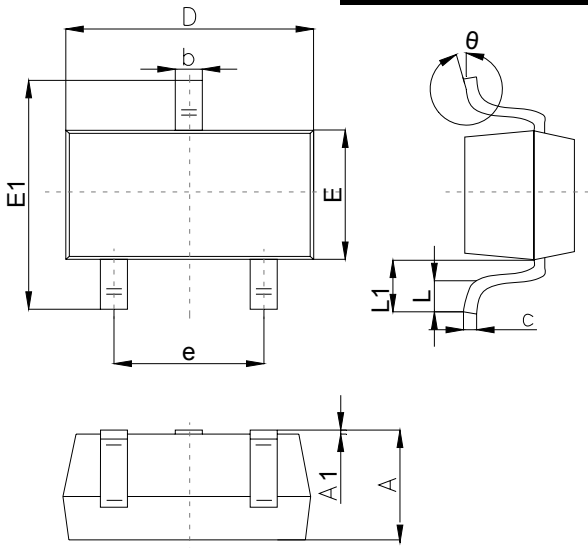


**Fig10.** Switching Time Test Circuit and waveforms

The curve above is for reference only.

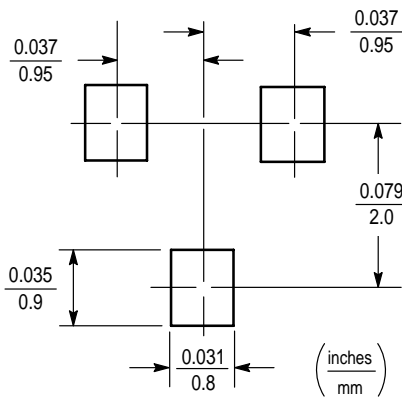
**Outlitne Drawing**

**SOT-23 Package Outline Dimensions**



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	0.90		1.40
A1	0.00		0.10
b	0.30		0.50
c	0.08		0.20
D	2.80	2.90	3.10
E	1.20		1.60
E1	2.25		2.80
e	1.80	1.90	2.00
L	0.10		0.50
L1	0.4		0.55
θ	0°		10°

**Suggested Pad Layout**



Note:

1. Controlling dimension: in/millimeters.
2. General tolerance: ±0.05mm.
3. The pad layout is for reference purposes only.