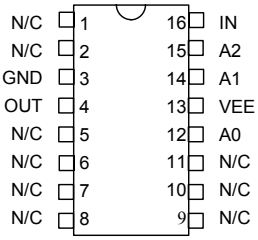
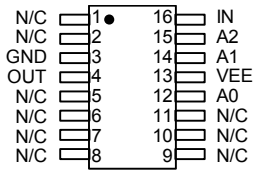
3-BIT, ECL-INTERFACED PROGRAMMABLE DELAY LINE (SERIES PDU53)

FEATURES

- Digitally programmable in 8 delay steps
- Monotonic delay-versus-address variation
- Precise and stable delays
- Input & outputs fully 100K-ECL interfaced & buffered
- Available in 16-pin DIP (600 mil) socket or SMD

PACKAGES





PDU53-xx DIP PDU53-xxC3 SMD
PDU53-xxM Military DIP PDU53-xxMC3 Mil SMD

FUNCTIONAL DESCRIPTION

The PDU53-series device is a 3-bit digitally programmable delay line. The delay, TD_A, from the input pin (IN) to the output pin (OUT) depends on the address code (A2-A0) according to the following formula:

$$TD_A = TD_0 + T_{INC} * A$$

where A is the address code, T_{INC} is the incremental delay of the device, and TD_0 is the inherent delay of the device. The incremental delay is specified by the dash number of the device and can range from 100ps through 3000ps, inclusively. The address is not latched and must remain asserted during normal operation.

PIN DESCRIPTIONS

IN	Signal Input
OUT	Signal Output
A2	Address Bit 2
A1	Address Bit 1
A0	Address Bit 0
VEE	-5 Volts
GND	Ground

SERIES SPECIFICATIONS

- **Total programmed delay tolerance:** 5% or 40ps, whichever is greater
- **Inherent delay (TD_0):** 2.2ns typical
- **Address to input setup (T_{AIS}):** 2.9ns
- **Operating temperature:** 0° to 85° C
- **Temperature coefficient:** 100PPM/°C (excludes TD_0)
- **Supply voltage V_{EE}:** -5VDC ± 0.7V
- **Power Supply Current:** -150ma typical (50Ω to -2V)
- **Minimum pulse width:** 3ns or 15% of total delay, whichever is greater
- **Minimum period:** 8ns or 2 x pulse width, whichever is greater

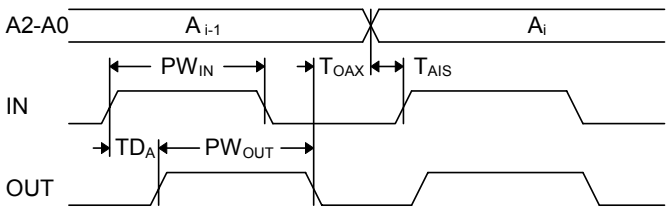


Figure 1: Timing Diagram

DASH NUMBER SPECIFICATIONS

Part Number	Incremental Delay Per Step (ps)	Total Delay Change (ns)
PDU53-100	100 ± 50	0.70
PDU53-200	200 ± 60	1.40
PDU53-250	250 ± 60	1.75
PDU53-400	400 ± 80	2.80
PDU53-500	500 ± 100	3.50
PDU53-750	750 ± 100	5.25
PDU53-1000	1000 ± 200	7.00
PDU53-1200	1200 ± 200	8.40
PDU53-1500	1500 ± 200	10.50
PDU53-2000	2000 ± 400	14.00
PDU53-2500	2500 ± 400	17.50
PDU53-3000	3000 ± 500	21.00

NOTE: Any dash number between 100 and 3000 not shown is also available.

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APPLICATION NOTES

ADDRESS UPDATE

The PDU53 is a memory device. As such, special precautions must be taken when changing the delay address in order to prevent spurious output signals. The timing restrictions are shown in Figure 1.

After the last signal edge to be delayed has appeared on the OUT pin, a minimum time, T_{OAX}, is required before the address lines can change. This time is given by the following relation:

$$T_{OAX} = \max \{ (A_i - A_{i-1}) * T_{INC} , 0 \}$$

where A_{i-1} and A_i are the old and new address codes, respectively. Violation of this constraint may, depending on the history of the input signal, cause spurious signals to appear on the OUT pin. The possibility of spurious signals persists until the required T_{OAX} has elapsed.

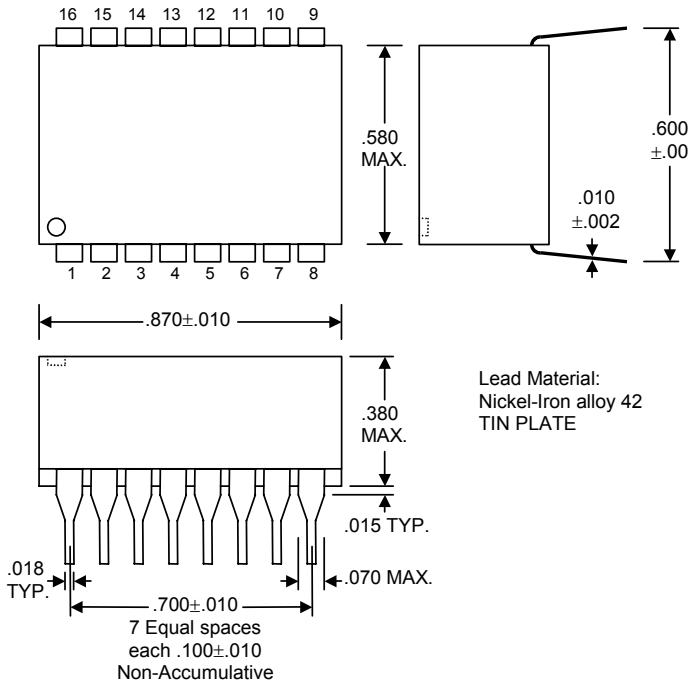
INPUT RESTRICTIONS

There are three types of restrictions on input pulse width and period listed in the **AC Characteristics** table. The **recommended** conditions are those for which the delay tolerance specifications and monotonicity are guaranteed. The **suggested** conditions are those for which signals will propagate through the unit without significant distortion. The **absolute** conditions are those for which the unit will produce some type of output for a given input.

When operating the unit between the recommended and absolute conditions, the delays may deviate from their values at low frequency. However, these deviations will remain constant from pulse to pulse if the input pulse width and period remain fixed. In other words, the delay of the unit exhibits frequency and pulse width dependence when operated beyond the recommended conditions. Please consult the technical staff at Data Delay Devices if your application has specific high-frequency requirements.

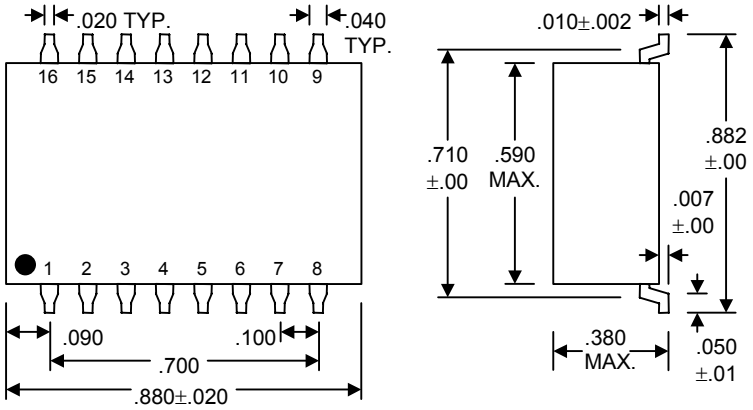
Please note that the increment tolerances listed represent a design goal. Although most delay increments will fall within tolerance, they are not guaranteed throughout the address range of the unit. Monotonicity is, however, guaranteed over all addresses.

PACKAGE DIMENSIONS



PDU53-xx (Commercial DIP)
PDU53-xxM (Military DIP)

PACKAGE DIMENSIONS (cont'd)



PDU53-xxC3 (Commercial SMD)
PDU53-xxMC3 (Military SMD)

DEVICE SPECIFICATIONS

TABLE 1: AC CHARACTERISTICS

PARAMETER		SYMBOL	MIN	TYP	UNITS
Total Programmable Delay		TD_T		7	T_{INC}
Inherent Delay		TD_0		2.2	ns
Address to Input Setup Time		T_{AIS}	2.9		ns
Output to Address Change		T_{OAX}	See Text		
Input Period	Absolute	PER_{IN}	30		% of TD_T
	Suggested	PER_{IN}	50		% of TD_T
	Recommended	PER_{IN}	200		% of TD_T
Input Pulse Width	Absolute	PW_{IN}	15		% of TD_T
	Suggested	PW_{IN}	25		% of TD_T
	Recommended	PW_{IN}	100		% of TD_T

TABLE 2: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{EE}	-7.0	0.3	V	
Input Pin Voltage	V_{IN}	V_{EE} - 0.3	0.3	V	
Storage Temperature	T_{STRG}	-65	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 3: DC ELECTRICAL CHARACTERISTICS

(0C to 85C)

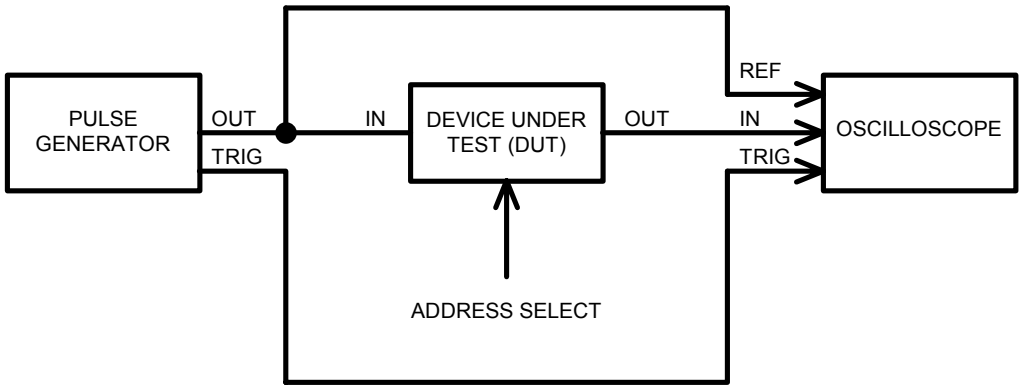
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
High Level Output Voltage	V_{OH}	-1.025	-0.880	V	V_{IH} = MAX,50Ω to -2V
Low Level Output Voltage	V_{OL}	-1.810	-1.620	V	V_{IL} = MIN, 50Ω to -2V
High Level Input Voltage	V_{IH}	-1.165	-0.880	V	
Low Level Input Voltage	V_{IL}	-1.810	-1.475	V	
High Level Input Current	I_{IH}		340	μA	V_{IH} = MAX
Low Level Input Current	I_{IL}	0.5		μA	V_{IL} = MIN

DELAY LINE AUTOMATED TESTING

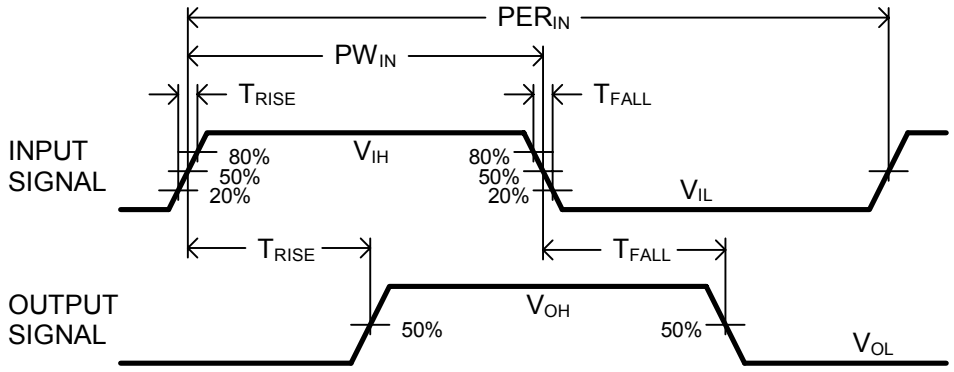
TEST CONDITIONS

INPUT:		**OUTPUT:**	
Ambient Temperature:	25°C ± 3°C	**Load:**	50Ω to -2V
Supply Voltage (Vcc):	-4.5V ± 0.1V	**C_{load}:**	5pf ± 10%
Input Pulse:	Standard 100K ECL levels	**Threshold:**	(V_{OH} + V_{OL}) / 2 (Rising & Falling)
Source Impedance:	50Ω Max.		
Rise/Fall Time:	1.0 ns Max. (measured between 20% and 80%)		
Pulse Width:	PW_{IN} = 10ns		
Period:	PER_{IN} = 100ns		

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Test Setup



Timing Diagram For Testing