THS3491 900-MHz, High-Power Output, Current Feedback Amplifier

1 Features

- Bandwidth:
  - 900 MHz (V_O = 2 V_{PP}, A_V = 5 V/V)
  - 320 MHz (V_O = 10 V_{PP}, A_V = 5 V/V)
- Bipolar Supply Range: ±7.0 V to ±16.0 V
- Single Supply Operation Capable
- 16.8-mA Trimmed Supply Current (Low Tempco)
- Output Swing: 28-V_{PP} (±16-V Supplies, 100-Ω Load)
- Slew Rate: 8000 V/µs
- THD: < –65 dBc (50 MHz, V_O = 10 V_{PP}, 100-Ω Load)
- Linear Output Current: ±380 mA
- Input Voltage Noise: 1.85 nV/√Hz
- Rise Time: < 1.5 ns (10-V Step, A_V = 5 V/V)
- Overshoot: < 4% (10-V Step, A_V = 5 V/V)
- Current Limit and Thermal Shutdown Protection
- Optional Power Disable

2 Applications

- High-Voltage, Arbitrary Waveform Generators
- LCR Meter Power Output Drivers
- Power FET Drivers
- High Capacitive Load Piezo Element Drivers
- VDSL Line Drivers
- Pin-Compatible Upgrade to THS3095 (DDA)

3 Description

The THS3491 device current-feedback amplifier (CFA) provides a new level of performance for applications requiring the lowest distortion at very high output power levels through > 100-MHz operating frequencies at 100 ohm loads. Although specified at a gain of 5 V/V, this current feedback design holds almost constant bandwidth and distortion over a wide range of gains.

The remarkable 8000 V/µs slew rate delivers 10-V_{PP} output into demanding loads with very low distortion through 320 MHz. The 900-MHz, small-signal bandwidth delivers a low overshoot of < 0.5-ns rise time for a step of < 4 V.

New designs can benefit from the lowest distortion using the VQFN-16 (RGT) package; whereas, the 8-pin SO PowerPAD™ (DDA) package can be used to upgrade existing THS3091 or THS3095 designs. Lower output headroom for the THS3491 gives more output swing on the same ±15-V supplies versus legacy THS3091 or THS3095 solutions.

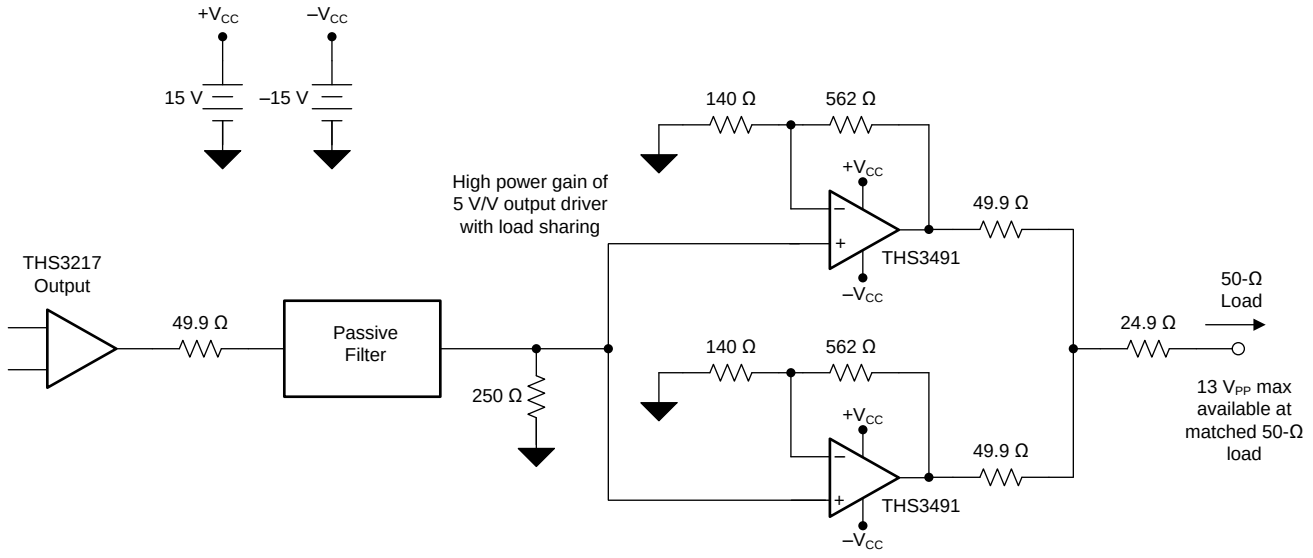
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS3491	VQFN (16)	3.00 mm × 3.00 mm
	SO PowerPAD (8)	4.89 mm × 3.90 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

ADVANCE INFORMATION

Typical Arbitrary Waveform Generator Output Drive Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2017	*	Advance information release.

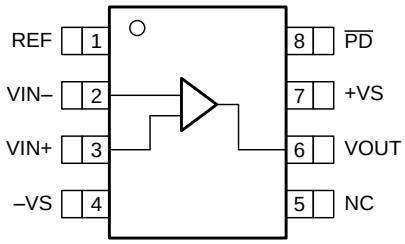
5 Device Comparison Table

DEVICE	SUPPLY, V_S (V)	SSBW, A_V = 5 (MHz)	MAXIMUM ICC AT 25°C (mA)	INPUT NOISE, V_n (nV/√Hz)	THD, 2 V_{PP} AT 10 kHz (dBc)	SLEW RATE (V/µs)	LINEAR OUTPUT CURRENT (mA)
THS3491	±15	900	17.3	1.7	–56	8000	±380
THS3095	±15	190	9.5	1.6	–37	1200 (1)	±250
THS3001	±15	350	9	1.6	–25	1400 (2)	±120
THS3201	±7.5	565	21	1.65	N/A	3900 (3)	±80

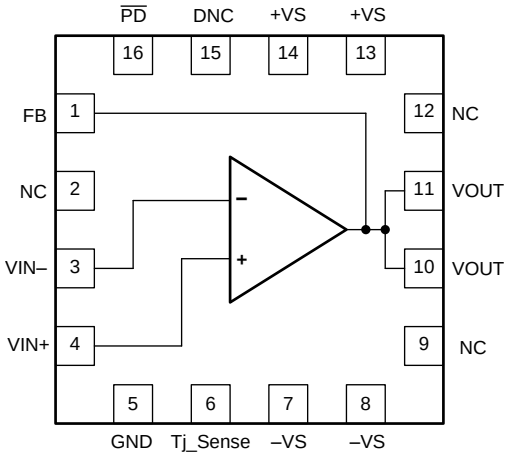
(1) Slew rate from FPBW of 135 MHz, 4 V_{PP}.
(2) Slew rate from FPBW of 32 MHz, 20 V_{PP}.
(3) Slew rate from FPBW of 880 MHz, 2 V_{PP}.

6 Pin Configuration and Functions

DDA Package
8-Pin SO PowerPAD™
Top View



RGT Package
16-Pin VQFN With Thermal Pad
Top View



Pin Functions

PIN (1)			I/O	DESCRIPTION
NAME	VQFN-16	SO-8 PowerPAD		
DNC	15	—	—	Do not connect (there may be a function on this pin internally)
GND	5	—	GND	Ground, $\overline{PD}$ logic reference on the VQFN-16 (RGT) package
FB	1	—	O	Input side feedback pin
NC	2, 9, 12	5	—	No connect (there is no internal connection)
$\overline{PD}$	16	8	I	Amplifier power down: low = amplifier disabled, high (default) = amplifier enabled
REF	—	1	I	$\overline{PD}$ logic reference on the SOIC-8 (DDA) package
Tj_Sense	6	—	O	Voltage proportional to die temperature
VIN–	3	2	I	Inverting input
VIN+	4	3	I	Noninverting input
VOUT	10, 11	6	O	Output of amplifier
–VS	7, 8	4	Power	Negative power supply
+VS	13, 14	7	Power	Positive power supply

(1) Both packages include a backside thermal pad. The thermal pad can be connected to a heat spreading plane that can be at any voltage because the device die is electrically isolated from this metal plate. The thermal pad can also be unused (not connected to any heat spreading plane or voltage) giving higher thermal impedance.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage	Supply voltage, $(+V_S) – (–V_S)$			33	V
	Supply voltage turn on, turn off maximum dV/dT(2)			1	V/µs
	Input/output voltage range		$(–V_S) – 0.5$	$(+V_S) + 0.5$	V
	Differential input voltage			±0.5	
Current	Continuous input current(3)			±10	mA
	Continuous output current(3)			±100	
Temperature	Operating, T_A		TBD	TBD	°C
	Junction, T_J(4)	Normal operation		150	
		Continuous operation, long-term reliability		125	
	Storage(5), T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Stay below this dV/dT supply turn on and off edge rate to make sure that the edge-triggered ESD absorption device across the supply pins remains open. Exceeding this supply edge rate may transiently show a short circuit across the supplies.
(3) Long-term continuous current for electro-migration limits.
(4) Thermal shutdown at approximately 165°C junction temperature and recovery at approximately 145°C
(5) See the MSL/Reflow Rating information provided with the material, or see the TI web site at www.ti.com for the latest information.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$(+V_S) – (–V_S)$	Supply voltage	Dual supply	±7	±15	±16	V
		Single supply	14	30	32	
T_A	Operating free-air temperature		–40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		THS3491		UNIT
		DDA (SO PowerPAD™)	RGT (VQFN With Thermal Pad)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.5	49.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.8	55.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.2	23.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.4	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.5	23.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.5	7.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics: V_S = ±15 V

at $+V_S$ = 15 V, $-V_S$ = –15 V, T_A = 25°C, R_{LOAD} = 100 Ω, noninverting gain = 5 V/V, and RGT package: R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_O = 2 V_{PP}, < 0.5-dB peaking		900		MHz	C
LSBW	Large-signal bandwidth	V_O = 10 V_{PP}, < 1-dB peaking		320		MHz	C
BW_{FLAT}	Bandwidth for 0.2-dB flatness	V_O = 2 V_{PP}		350		MHz	C
SR	Slew rate	V_O = 20 V_{PP}		8000		V/µs	C
OS/US	Overshoot and undershoot	V_O = 10-V step, G = 5, R_{LOAD} = 100 Ω, input t_r = 1.0 ns		1.5%			C
t_r	Rise time	V_O = 10-V step, G = 5, R_{LOAD} = 100 Ω, input t_r = 1.0 ns		1.3		ns	C
t_f	Fall time	V_O = 10-V step, G = 5, R_{LOAD} = 100 Ω, input t_f = 1.0 ns		1.3		ns	C
t_s	Settling time to 0.1%	V_O = 10-V step, G = 5, R_{LOAD} = 100 Ω, input t_r = 1.0 ns		7		ns	C
HD2	Second-order harmonic distortion	f = 20 MHz, R_{LOAD} = 100 Ω, V_O = 10 V_{PP}		–78		dBc	C
		f = 50 MHz, R_{LOAD} = 100 Ω, V_O = 10 V_{PP}		–76		dBc	C
		f = 70 MHz, R_{LOAD} = 100 Ω, V_O = 10 V_{PP}		–76		dBc	C
		f = 100 MHz, R_{LOAD} = 100 Ω, V_O = 10 V_{PP}		–76		dBc	C
		f = 20 MHz, R_{LOAD} = 100 Ω, V_O = 20 V_{PP}		–58		dBc	C
		f = 50 MHz, R_{LOAD} = 100 Ω, V_O = 20 V_{PP}		–55		dBc	C
		f = 70 MHz, R_{LOAD} = 100 Ω, V_O = 20 V_{PP}		–52		dBc	C
		f = 100 MHz, R_{LOAD} = 100 Ω, V_O = 20 V_{PP}		–45		dBc	C
HD3	Third-order harmonic distortion	f = 20 MHz, R_{LOAD} = 100 Ω, V_O = 10 V_{PP}		–83		dBc	C
		f = 50 MHz, R_{LOAD} = 100 Ω, V_O = 10 V_{PP}		–69		dBc	C
		f = 70 MHz, R_{LOAD} = 100 Ω, V_O = 10 V_{PP}		–59		dBc	C
		f = 100 MHz, R_{LOAD} = 100 Ω, V_O = 10 V_{PP}		–49		dBc	C
		f = 20 MHz, R_{LOAD} = 100 Ω, V_O = 20 V_{PP}		–55		dBc	C
		f = 50 MHz, R_{LOAD} = 100 Ω, V_O = 20 V_{PP}		–50		dBc	C
		f = 70 MHz, R_{LOAD} = 100 Ω, V_O = 20 V_{PP}		–40		dBc	C
		f = 100 MHz, R_{LOAD} = 100 Ω, V_O = 20 V_{PP}		–38		dBc	C
IMD2	2nd-order two-tone intermodulation distortion	f = 20 MHz, 5 V_{PP} each, 100-kHz tone spacing		–75		dBc	C
IMD3	3rd-order two-tone intermodulation distortion	f = 20 MHz, 5 V_{PP} each, 100-kHz tone spacing		–85		dBc	C
e_n	Input-referred voltage noise	f > 10 kHz		1.70		nV/√Hz	C
e_{ip}	Noninverting, input-referred current noise	f > 10 kHz		15		pA/√Hz	C
e_{in}	Inverting, input-referred current noise	f > 10 kHz		20		pA/√Hz	C
Z_{OUT}	Close-loop output impedance	f = 100 MHz		1		Ω	C
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain	V_O = ±10 V, R_{LOAD} = 500 Ω	6	10		MΩ	A
V_{OS}	Input offset voltage		–1.0	1	2.0	mV	A
V_{OS} drift	Input offset voltage drift	–40°C ≤ T_J ≤ +125°C		3		µV/°C	B
I_{b+}	Noninverting input bias current		–5	1.5	5	µA	A
I_{b+} drift	Noninverting input bias current drift	–40°C ≤ T_J ≤ +125°C		15		nA/°C	B
I_{b-}	Inverting input bias current		–15	4	15	µA	A

ADVANCE INFORMATION

Electrical Characteristics: V_S = ±15 V (continued)

at $+V_S$ = 15 V, $-V_S$ = –15 V, T_A = 25°C, R_{LOAD} = 100 Ω, noninverting gain = 5 V/V, and RGT package: R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
I_{b-} drift	Inverting input bias current drift	–40°C ≤ T_J ≤ +125°C		15		nA/°C	B
	Internal trace resistance to feedback pin	RGT only, pins 10 and 11 to pin 1	1.1	1.5	1.9	Ω	A
CMRR	Common-mode rejection ratio	f = dc	63	75		dBc	C
INPUT							
HR_{IN}	Headroom to either supply	CMRR > 60 dB		4.1	4.3	V	C
Z_{IN+}	Noninverting input impedance	Closed-loop measurement		50		kΩ	C
Z_{IN-}	Inverting input impedance	Open-loop measurement		15		Ω	C
OUTPUT							
HR_{OUT}	Headroom to either supply	R_{LOAD} = 100 Ω	1.3	1.5	1.7	V	A
$Iout_{MAX}$	Maximum current output	R_{LOAD} = 24 Ω, V_O = ±12.67 V, magnitude, both polarities	480	520	550	mA	A
	Linear output current	R_{LOAD} = 24 Ω, V_O = ±9.4 V, Z_{OL} > 1M Ω, magnitude, both polarities	380	420		mA	A
	Peak output current in transition (zero-crossing I_{OUT} peak)	V_O = 0 V, ±620 mA, R_O < 0.5 Ω, magnitude, both polarities	500	540		mA	B
ISC	Output short-circuit current	V_S = ±9 V, V_O = ±6 V, magnitude, both polarities	550	620		mA	C
Z_{OUT}	DC output impedance	Closed-loop ±50 mA		0.17		Ω	C
POWER SUPPLY							
I_Q	Quiescent current	V_S = ±15 V, no load	16.3	16.75	17.3	mA	A
		V_S = ±16 V, no load	16.4	16.85	17.4	mA	A
		V_S = ±7 V, no load	15.4	15.8	16.5	mA	A
I_Q TC	Supply current tempco	V_S = ±15 V, –40°C ≤ T_J ≤ +125°C, no load	–4		4	µA/°C	B
PSRP	Power-supply rejection positive		78	82		dB	A
PSRN	Power-supply rejection negative		77	80		dB	A
POWER DOWN							
	Allowed REF pin voltage range	REF pin can be floated. $\overline{PD}$ pin must be floated or held above REF pin. If REF is tied to $+V_S$, the device is enabled with $\overline{PD}$ floating. Range is $-V_S$ to ($+V_S$ – 5 V)	–15		10	V	C
	Recommended REF pin voltage	For bipolar supplies, normally ground REF pin		0		V	C
	REF current to ground	REF pin = 0 V, $\overline{PD}$ floated, positive out of the pin.	33	42	51	µA	A
V_{IL}	Disable voltage threshold	PD below REF pin voltage turns amplifier off, turn off is within 0.8 V above REF, REF pin = 0 V			0.8	V	A
V_{IH}	Enable voltage threshold	$\overline{PD}$ above REF pin voltage turns amplifier on, turn on is 1.6 V above REF, REF pin = 0 V	1.6			V	A
	$\overline{PD}$ pin low-input bias current	$\overline{PD}$ = REF = ground, positive out of the pin.	35	46	52	µA	A
	$\overline{PD}$ pin high-input bias current	$\overline{PD}$ = REF + 3 V, REF = ground, positive out of the pin.	–1	0	1	µA	A
	$+V_S$ Disabled supply current	Supply current magnitude only	650	795	880	µA	A
	$-V_S$ Disabled supply current	Supply current magnitude only	600	723	820	µA	A
t_{ON}	Turn-on time delay	DC input to 90% of final value		50		ns	C
t_{OFF}	Turn-off time delay	DC input to 10% of final value		4		µs	C

ADVANCE INFORMATION

Electrical Characteristics: V_S = ±15 V (continued)

at $+V_S$ = 15 V, $–V_S$ = –15 V, T_A = 25°C, R_{LOAD} = 100 Ω, noninverting gain = 5 V/V, and RGT package: R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
JUNCTION-TEMPERATURE SENSE, T_J-sense (QFN-16 only, pin 6)							
	T_J-sense 25°C value	Device disabled (22°C to 32°C ATE ambient temperature)	0.915	1.06	1.15	V	A
	T_J-sense temperature coefficient	T_J = 0°C to 125°C	2.9	3	3.3	mV/°C	B
	T_J-sense input impedance	Internally connected to REF pin	32.4	35	38	kΩ	A

7.6 Electrical Characteristics: V_S = ±7.5 V

at $+V_S$ = 7.5 V, $–V_S$ = –7.5 V, T_A = 25°C, R_{LOAD} = 100 Ω, noninverting gain = 5 V/V, and RGT package: R_F = 576 Ω, R_G = 143 Ω, or DDA Package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
AC PERFORMANCE							
SSBW	Small-signal bandwidth	V_O = 2 V_{PP}, < 0.5-dB peaking		800		MHz	C
LSBW	Large-signal bandwidth	V_O = 5 V_{PP}, < 1-dB peaking		550		MHz	C
SR	Slew rate (10%-90%)	V_O = 10 V_{PP}		6000		V/µs	C
HD2	Second-order harmonic distortion	f = 20 MHz, R_{LOAD} = 100 Ω, V_O = 5 V_{PP}		–76		dBc	C
HD3	Third-order harmonic distortion	f = 20 MHz, R_{LOAD} = 100 Ω, V_O = 5 V_{PP}		–82		dBc	C
e_n	Input-referred voltage noise	f > 10 kHz		1.7		nV/√Hz	C
e_{ip}	Noninverting, input-referred current noise	f > 10 kHz		15		pA/√Hz	C
e_{in}	Inverting, input-referred current noise	f > 10 kHz		20		pA/√Hz	C
Z_{OUT}	Close-loop output impedance	f = 50 MHz		1		Ω	C
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain	V_O = ±5 V, R_{LOAD} = 500 Ω	8	14		MΩ	A
V_{OS}	Input offset voltage		–1.0	1	2	mV	A
V_{OS} drift	Input offset-voltage drift	–40°C ≤ T_J ≤ +125°C		3		µV/°C	B
I_{b+}	Noninverting input bias current		–5	1.5	5	µA	A
I_{b+} drift	Noninverting input bias-current drift	–40°C ≤ T_J ≤ +125°C		15		nA/°C	B
I_{b-}	Inverting input bias current		–15	4	15	µA	A
I_{b-} drift	Inverting input bias-current drift	–40°C ≤ T_J ≤ +125°C		15		nA/°C	B
INPUT							
Z_{IN+}	Noninverting input impedance	Closed-loop measurement		50		kΩ	C
Z_{IN-}	Inverting input impedance	Open-loop measurement		15		Ω	C
HR_{IN}	Headroom to either supply	CMRR > 60 dB		4.1	4.3	V	C
OUTPUT							
HR_{OUT}	Headroom to either supply	R_{LOAD} = 100 Ω	1.3	1.5	1.7	V	A
	Linear output current	R_{LOAD} = 24 Ω, V_O = ±5 V, Z_{OL} > 1M Ω, Bipolar each polarity	200	250		mA	A
POWER SUPPLY							
I_Q	Quiescent current	No load	15.4	15.8	16.4	mA	A

ADVANCE INFORMATION

Electrical Characteristics: V_S = ±7.5 V (continued)

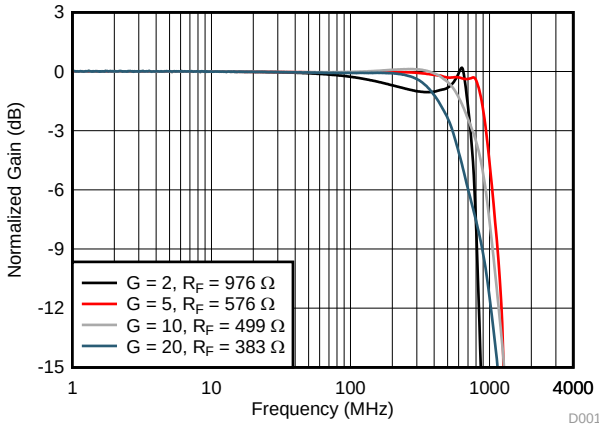
at $+V_S$ = 7.5 V, $-V_S$ = –7.5 V, T_A = 25°C, R_{LOAD} = 100 Ω, noninverting gain = 5 V/V, and RGT package: R_F = 576 Ω, R_G = 143 Ω, or DDA Package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
POWER DOWN							
	Allowed REF pin voltage range	REF pin can be floated. $\overline{PD}$ pin must be floated or held above REF pin. If REF is tied to $+V_S$, the device is enabled with $\overline{PD}$ floating. Range is $-V_S$ to ($+V_S$ – 5 V)	–7.5		2.5	V	C
	Recommended REF pin voltage	For bipolar supplies, normally ground REF pin		0		V	C
	REF pin current to ground	REF = 0 V, $\overline{PD}$ floated, positive out of the pin	35	37	52	µA	A
V_{IL}	Disable voltage threshold	$\overline{PD}$ below REF pin voltage turns amplifier off, $\overline{PD}$ within 0.8 V of REF is off, REF pin = 0 V			0.8	V	A
V_{IH}	Enable voltage threshold	$\overline{PD}$ above REF pin voltage turns amplifier on, $\overline{PD}$ > 1.6 V above REF is on, REF pin = 0 V	1.6			V	A
	$\overline{PD}$ pin low-input bias current	$\overline{PD}$ = REF = gnd, positive out of the pin	17	21	25	µA	A
	$\overline{PD}$ pin high-input bias current	$\overline{PD}$ = REF + 3 V, REF = ground, positive out of the pin	–1	2	1	µA	A
	$+V_S$ Disabled supply current		600	700	850	µA	A
	$-V_S$ Disabled supply current		550	642	770	µA	A
JUNCTION-TEMPERATURE SENSE, T_J-sense (QFN-16 only, pin 6)							
	T_J-sense temperature coefficient	T_J = 0°C to 125°C	2.9	3	3.3	mV/°C	B
	T_J-sense input impedance	Internally connected to REF pin	32.4	35	38	kΩ	A
	T_J-sense 25°C value	Device disabled (22°C to 32°C ATE ambient temperature)	0.915	1.06	1.15	V	A

ADVANCE INFORMATION

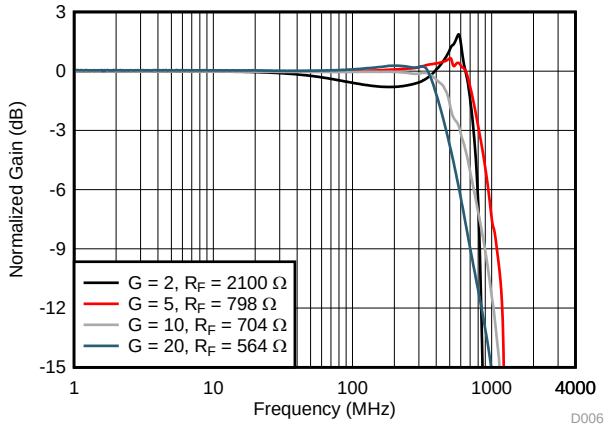
7.7 Typical Characteristics: ±15 V

at $+V_S$ = 15 V, $-V_S$ = –15 V, T_A = 25°C, R_{LOAD} = 100 Ω, noninverting gain = 5 V/V, and RGT package: R_F = 576 Ω, R_G = 143 Ω, or DDA package: R_F = 798 Ω, R_G = 200 Ω (unless otherwise noted)



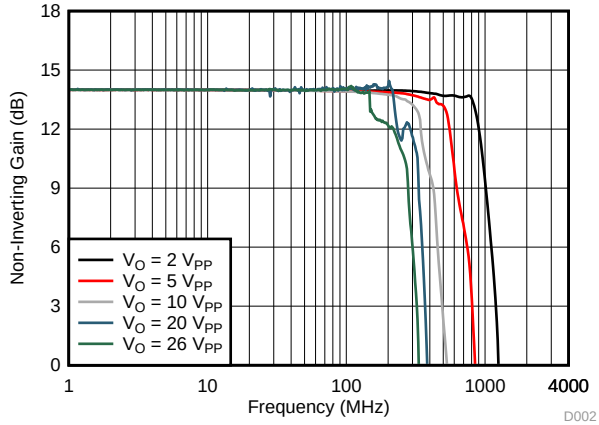
$V_O = 2V_{PP}$ RGT package

Figure 1. Noninverting Small-Signal Frequency Response



$V_O = 2V_{PP}$ DDA package

Figure 2. Noninverting Small-Signal Frequency Response



G = +5, R_F = 576-Ω RGT package

Figure 3. Frequency Response vs Output Swing

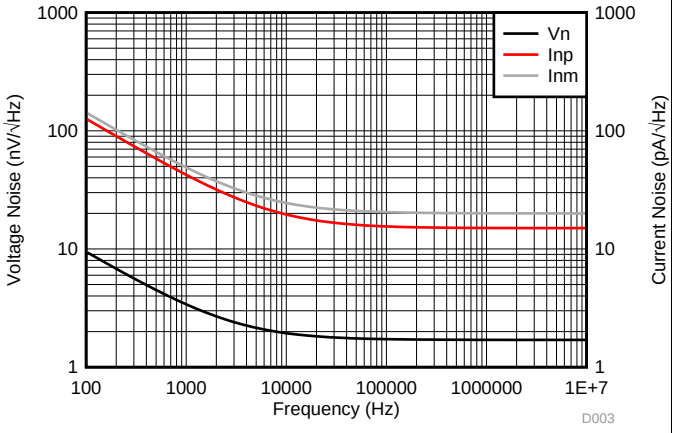
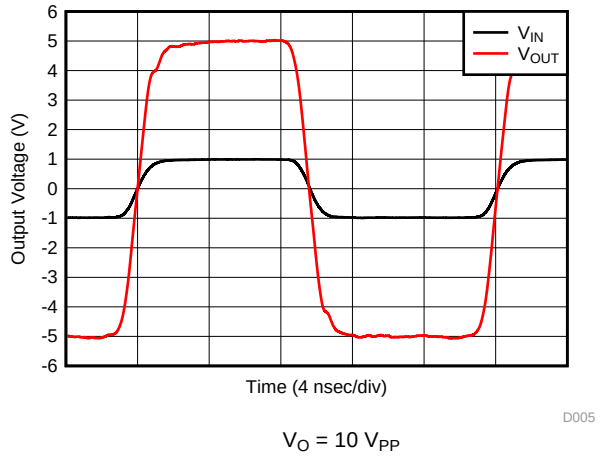
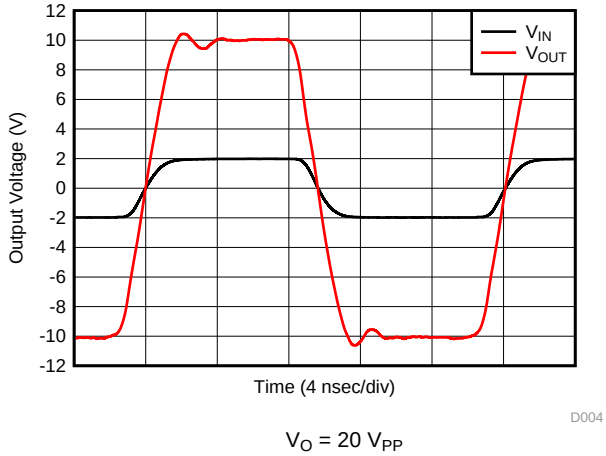


Figure 4. Spot Input Noise vs Frequency



$V_O = 10\ V_{PP}$

Figure 5. Pulse Response



$V_O = 20\ V_{PP}$

Figure 6. Pulse Response

ADVANCE INFORMATION

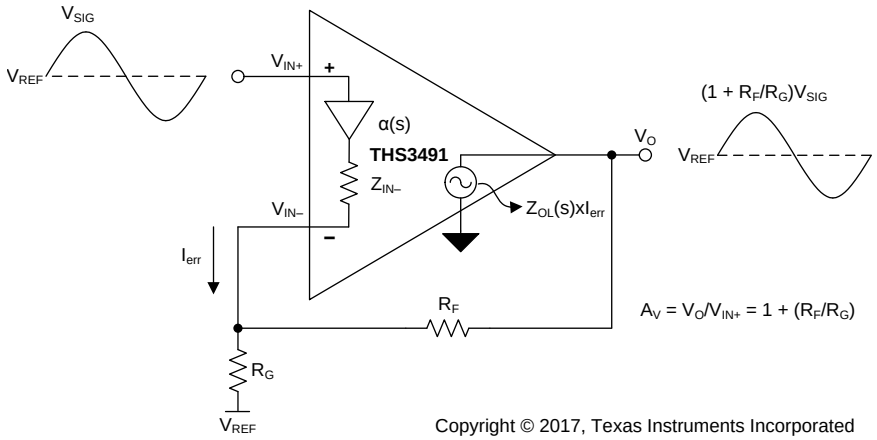
8 Detailed Description

8.1 Overview

The THS3491 is a high-voltage, low-distortion, high-speed, current-feedback amplifier designed to operate over a wide supply range of ±7 V to ±16 V for applications requiring large, linear output swings such as arbitrary waveform generators.

The THS3491 features a power-down pin that puts the amplifier in low power standby mode, and lowers the quiescent current from 16.5 mA to 750 µA.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power-Down ($\overline{PD}$) Pin

The THS3491 features a power-down ($\overline{PD}$) pin that lowers the quiescent current from 16.8 mA down to 800 µA, ideal for reducing system power.

The power-down pin of the amplifier defaults to 2 V below the positive supply voltage in the absence of an externally applied voltage, putting the amplifier in the power-on mode of operation. To turn off the amplifier in an effort to conserve power, the power-down pin can be driven towards the negative rail. The threshold voltages for power on and power down are relative to the REF pin and are given in the *Electrical Characteristics: V_S = ±15 V* and *Electrical Characteristics: V_S = ±7.5 V* tables. Above the enable threshold voltage, the device is on. Below the disable threshold voltage, the device is off. Behavior in between these threshold voltages is not specified.

This power-down functionality helps the amplifier consume less power in power-down mode. Power-down mode is not intended to provide a high-impedance output. In other words, the power-down functionality is not intended for use as a tri-state bus driver. When in power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain-setting resistors, but the output impedance of the device itself varies depending on the voltage applied to the outputs.

As with most current-feedback amplifiers, the internal architecture places some limitations on the system when in power-down mode. Most notably is the fact that the amplifier actually turns on if there is a ±1 V or greater difference between the two input nodes (VIN+ and VIN–) of the amplifier. If this difference exceeds ±1 V, the output of the amplifier creates an output voltage equal to approximately [(VIN+ – VIN–) –0.7 V] × gain. This also implies that if a voltage is applied to the output while in power-down mode, the VIN– node voltage is equal to $V_{O(applied)} \times R_G / (R_F + R_G)$. For low-gain configurations and a large applied voltage at the output, the amplifier may actually turn on because of the aforementioned behavior.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach either 10% or 90% of the final output voltage. The time delays are in the order of nanoseconds during power on, and microseconds during power off because the amplifier moves out of the linear mode of operation for power-off condition.

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Feature Description (continued)

8.3.2 Power-Down Reference (REF) Pin

In addition to the power-down pin, the DDA package features a reference pin (REF) that allows control over the enable or disable power-down voltage levels applied to the $\overline{PD}$ pin. This reference pin is explicitly pinned out on the DDA package as the REF pin. However, on the RGT package, the reference pin refers to pin 5 (GND), which must be connected to GND. In most split-supply applications, the reference pin is connected to ground. In either case, be aware of voltage-level thresholds that apply to the power-down pin. Table 1 shows examples and illustrates the relationship between the reference voltage and the power-down thresholds. In Table 1, the threshold levels are derived by these conditions:

- $\overline{PD} \leq$ REF + 0.8 V for disable
- $\overline{PD} \geq$ REF + 1.3 V for enable

where the usable range at the REF pin is:

- $V_{S-} \leq V_{REF} \leq (V_{S+} - 5\ V)$

Table 1. Example Power-Down Threshold Voltage Levels

SUPPLY VOLTAGE (V)	REFERENCE PIN VOLTAGE (V)	ENABLE LEVEL (V)	DISABLE LEVEL (V)
±15, ±7	0	1.3	0.8
±15	2	3.3	2.8
±15	–2	–0.7	–1.2
±7	1	2.3	1.8
±7	–1	0.3	–0.2
30	15	16.3	15.8
14	7	8.3	7.8

The recommended mode of operation is to tie the REF pin to ground for both single and split-supply operation, thus setting the enable and disable thresholds to 1.3 V and 0.8 V, respectively.

If the REF pin is left unterminated, the pin floats to about 1 V below the positive rail and falls outside of the recommended operating range ($-V_S \leq V_{(REF)} \leq +V_S - 5$ V). As a result, the REF pin no longer serves as a reliable reference for the $\overline{PD}$ pin ,and the enable and disable thresholds given previously no longer apply. If the $\overline{PD}$ pin is also left unterminated, the $\overline{PD}$ pin also floats to 2 V below the positive rail. The internal disable circuitry is actually off when both REF and $\overline{PD}$ pin are floated, but the device remains enabled. As a result, the THS3491 DDA package can be a drop-in replacement for the THS3091 DDA pinout and operate if pins 1 and 8 are floated. If balanced, split supplies are used ($\pm V_S$) and the REF and $\overline{PD}$ pins are grounded, the device is disabled.

8.3.3 Internal Junction Temperature Sense (Tj_Sense) Pin

The RGT package includes an internal, junction-temperature sense pin, Tj_Sense. This pin is a temperature-dependent current source from the positive supply into one side of the internal resistor, where the other side of the internal resistor is connected to pin 5 (GND), the $\overline{PD}$ logic reference pin on the die. For simplicity, and to keep the Tj_Sense output ground referenced, tie pin 5 to ground (internally, the $\overline{PD}$ logic reference pin). If pin 5 is tied to a voltage in the same range as the REF pin voltage for the DDA package, the output of the Tj_sense voltage and input threshold voltages of the $\overline{PD}$ pin are level shifted.

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8.4 Device Functional Modes

8.4.1 Wideband, Noninverting Operation

The THS3491 is a 900-MHz current-feedback operational amplifiers, designed to operate from a ±7-V to ±16-V power supply.

Figure 7 shows the THS3491 in a noninverting, gain of 5 V/V configuration typically used to generate the performance curves. Most of the curves were characterized using signal sources with 50-Ω source impedance, and with measurement equipment presenting a 50-Ω load impedance.

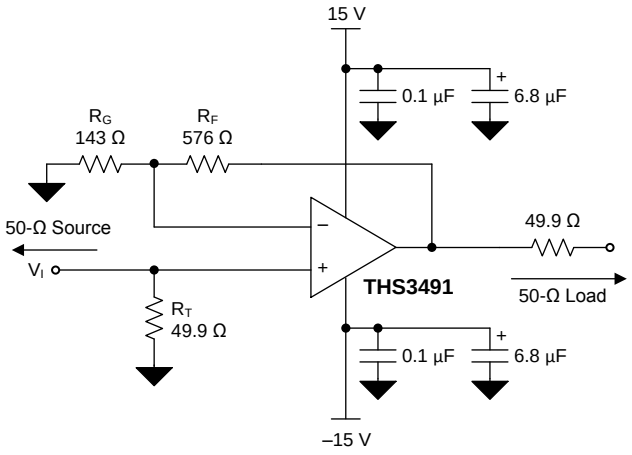

Figure 7. Wideband, Noninverting Gain of 5 V/V Configuration

Current-feedback amplifiers are highly dependent on the feedback resistor, R_F, for maximum performance and stability. Table 2 shows the optimal resistor values for R_F and R_G at different gains in order to achieve maximum bandwidth with minimal peaking in the frequency response. Higher bandwidths can be achieved by using even lower values for R_F, at the expense of added peaking in the frequency response. Conversely, increasing R_F decreases the bandwidth, but stability is improved.

Table 2. Recommended Resistor Values for Minimum Peaking and Optimal Frequency Response With R_L = 100 Ω and V_S = ±15-V

GAIN (V/V)	RGT PACKAGE		DDA PACKAGE	
	R_G (Ω)	R_F (Ω)	R_G (Ω)	R_F (Ω)
2	976	976	2.1k	2.1k
5	143	576	200	798
10	54.9	499	78.7	704
20	20	383	29.4	564

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Device Functional Modes (continued)

8.4.2 Wideband, Inverting Operation

Figure 8 shows the THS3491 in a typical inverting gain configuration where the input and output impedances and signal gain from Figure 7 are retained in an inverting circuit configuration.

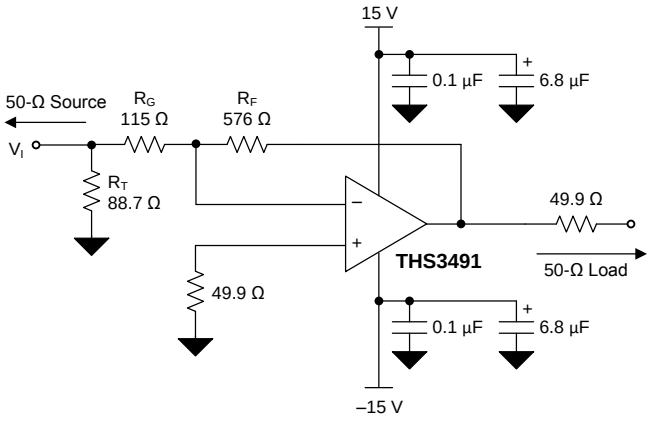

Figure 8. Wideband, Inverting Gain of -5 V/V Configuration

8.4.3 Single-Supply Operation

The THS3491 can operate from a single-supply voltage ranging from 14 V to 32 V. When operating from a single power supply, biasing the input and output at midsupply allows for the maximum output voltage swing. The circuits shown in Figure 9 show noninverting (a) and inverting (b) amplifiers configured for single-supply operations.

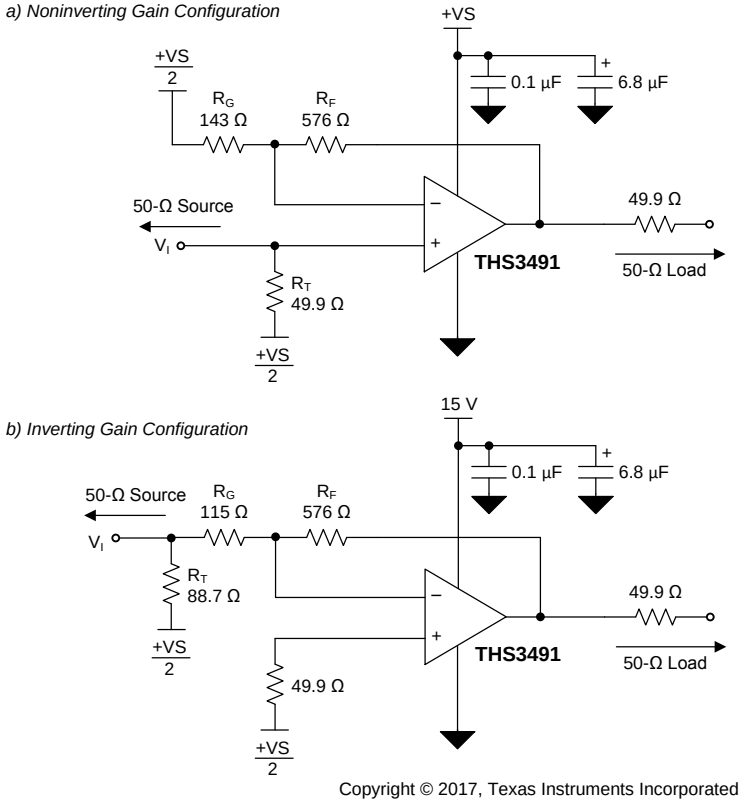

Figure 9. DC-Coupled, Single-Supply Operation

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Video Distribution

The wide bandwidth, high slew rate, and high output drive current of the THS3491 matches the demands for video distribution for delivering video signals down multiple cables. For high signal quality with minimal degradation of performance, use a 0.1-dB gain flatness that is at least 7x the passband frequency to minimize group delay variations from the amplifier. A high slew rate minimizes distortion of the video signal, and supports component video and RGB video signals that require fast transition times and fast settling times for high signal quality.

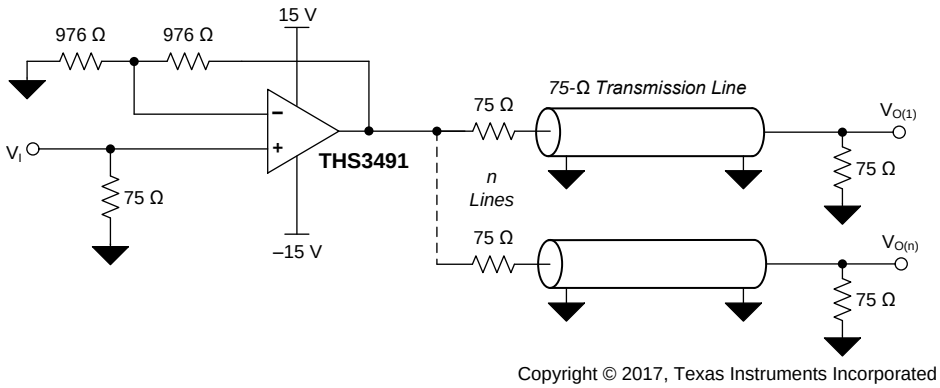

Figure 10. Video Distribution Amplifier Application

9.1.2 Driving Capacitive Loads

Applications such as power JFET and MOSFET (powerFET) drivers can be highly capacitive and cause stability problems for high-speed amplifiers.

Figure 11 and Figure 12 show recommended methods for driving capacitive loads. The basic idea is to use a resistor or ferrite chip to isolate the phase shift at high frequency caused by the capacitive load from the amplifier feedback path. See *Effect of Parasitic Capacitance in Op Amp Circuits* for recommended resistor values versus capacitive load.

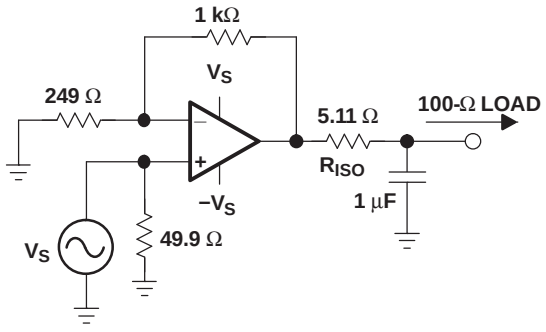

Figure 11. Driving a Large Capacitive Load Using an Output Series Isolation Resistor

Application Information (continued)

Placing a small series resistor, R_{ISO}, between the amplifier output and the capacitive load, as shown in Figure 11, is an easy way of isolating the load capacitance.

Figure 12 is shown using two amplifiers in parallel to double the output drive current to larger capacitive loads. This technique is used when more output current is needed to charge and discharge the load faster like when driving large FET transistors.

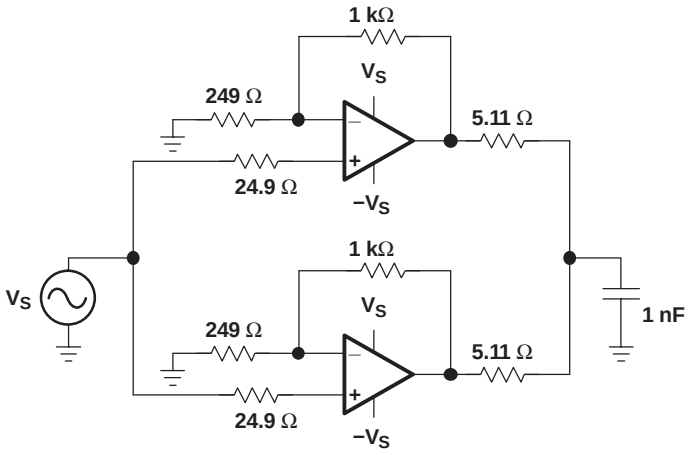

Figure 12. Driving a Large Capacitive Load Using Two Parallel Amplifier Channels

Figure 13 shows a push-pull FET driver circuit typical of ultrasound applications with isolation resistors to isolate the gate capacitance from the amplifier.

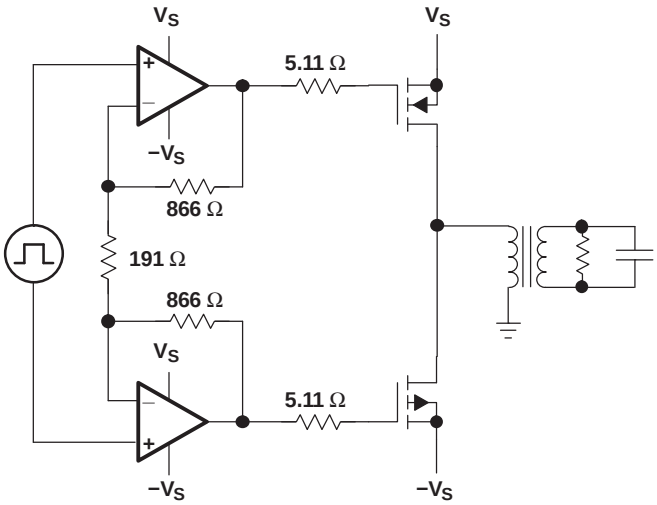

Figure 13. PowerFET Drive Circuit

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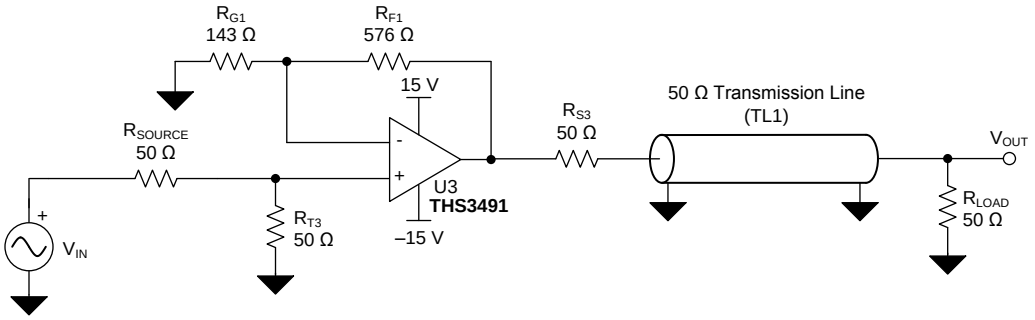
9.2 Typical Application

The fundamental concept of load sharing is to drive a load using two or more of the same operational amplifiers. Each amplifier is driven by the same source. Figure 14 shows two THS3491 amplifiers sharing the same load. This concept effectively reduces the current load of each amplifier by 1/N, where N is the number of amplifiers.

a) Single THS3491 Amplifier Driving a Transmission Line



b) Two THS3491 Amplifiers Driving a Transmission Line

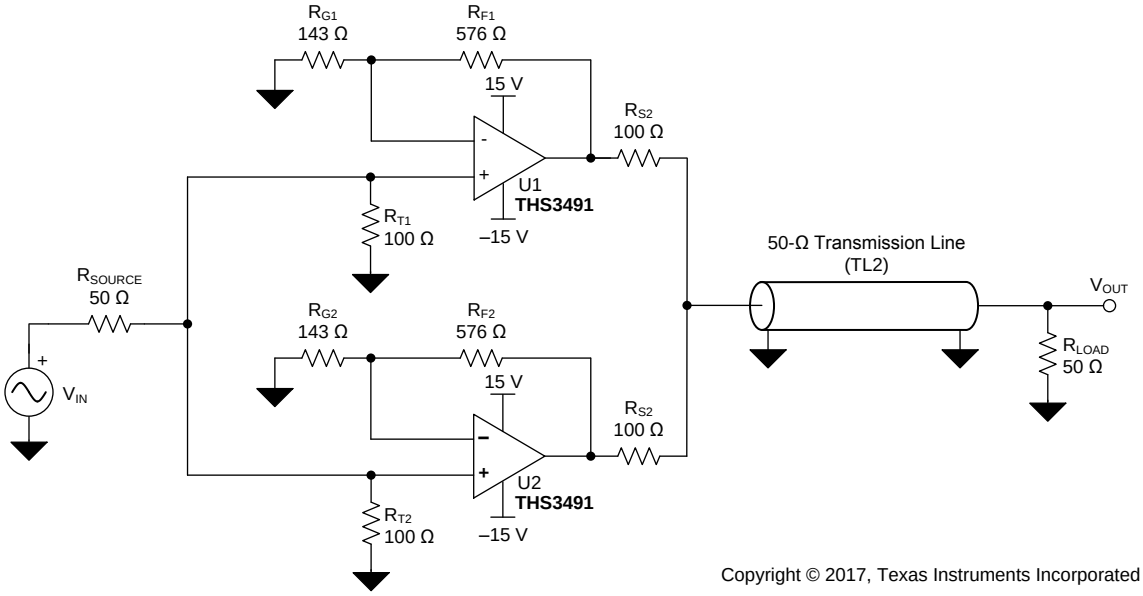


Figure 14. Load Sharing Driver Application

Typical Application (continued)

9.2.1 Design Requirements

Use two THS3491 amplifiers in a parallel load-sharing circuit to improve distortion performance.

Table 3. Design Parameters

DESIGN PARAMETER	VALUE
V_{OPP}	20 V
R_{LOAD}	100 Ω

9.2.2 Detailed Design Procedure

In addition to providing higher output current drive to the load, the load sharing configuration can also provide improved distortion performance. In many cases, an operational amplifier shows better distortion performance as the load current decreases (that is, for higher resistive loads) until the feedback resistor starts to dominate the current load. In a load sharing configuration of *N* amplifiers in parallel, the equivalent current load that each amplifier drives is 1/N times the total load current. For example, in a two-amplifier load sharing configuration with matching resistance (refer to Figure 14) driving a resistive load (R_{LOAD}), each series resistance is 2 × R_{LOAD} and each amplifier drives 2 × R_{LOAD}.

Two test circuits are shown in Figure 14, one for a single THS3491 amplifier driving a double-terminated, 50-Ω cable and one with two THS3491 amplifiers in a load sharing configuration. In the load sharing configuration, the two 100-Ω series output resistors act in parallel to provide 50-Ω back-matching to the 50-Ω cable.

10 Power Supply Recommendations

The THS3491 can operate off a single supply or with dual supplies as long as the input CM voltage range (CMIR) has the required headroom (4.3 V) to either supply rail. Supplies should be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. The use of ground plane is recommended, and as in most high-speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs. An optional supply decoupling capacitor across the two power supplies (for split supply operation) improves second harmonic distortion performance.

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11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier, like the THS3491, requires careful attention to board layout parasitic and external component types.

Recommendations that optimize performance include:

- Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- Minimize the distance [< 0.25 inch (6.35 mm)] from the power supply pins to high-frequency 0.1-μF and 100-pF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (6.8 μF or more) tantalum decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the printed circuit board (PCB).
- Careful selection and placement of external components preserve the high-frequency performance of the THS3491. Resistors should be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Again, keep their leads and PCB trace length as short as possible. Never use wire-bound type resistors in a high-frequency application. Because the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Other network components, such as input termination resistors, should be placed close to the gain-setting resistors. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 2 kΩ, this parasitic capacitance can add a pole and/or a zero that can effect circuit operation. Keep resistor values as low as possible, consistent with load-driving considerations.
- Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces of 0.05 inch to 0.1 inch (1.3 mm to 2.54 mm), preferably with ground and power planes opened up around them. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low parasitic capacitive loads (< 4 pF) may not need series resistance because the THS3491 are nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without a series resistance are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS3491 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series terminated at the source end only. Treat the trace as a capacitive load in this case. This termination does not preserve signal integrity as well as a doubly terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.
- Do not socket a high-speed device like the THS3491. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS3491 devices directly onto the board.

Layout Guidelines (continued)

11.1.1 PowerPAD™ Design Considerations (DDA Package Only)

The THS3491 is available in a thermally-enhanced PowerPAD package. These packages are constructed using a downset leadframe on which the die is mounted, as shown in the (a) and (b) sections of Figure 15. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package, a shown in Figure 15(c). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad. Devices such as the THS3491 have no electrical connection between the PowerPAD and the die.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

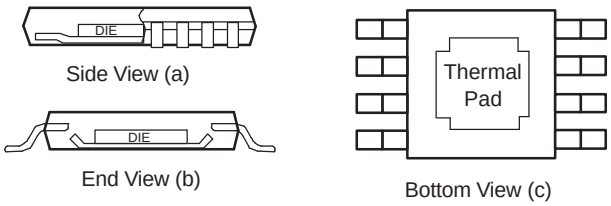

Figure 15. Views of Thermally Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following section illustrates the recommended approach.

11.1.1.1 PowerPAD™ Layout Considerations

The DDA package top-side etch and via pattern is shown in Figure 16.

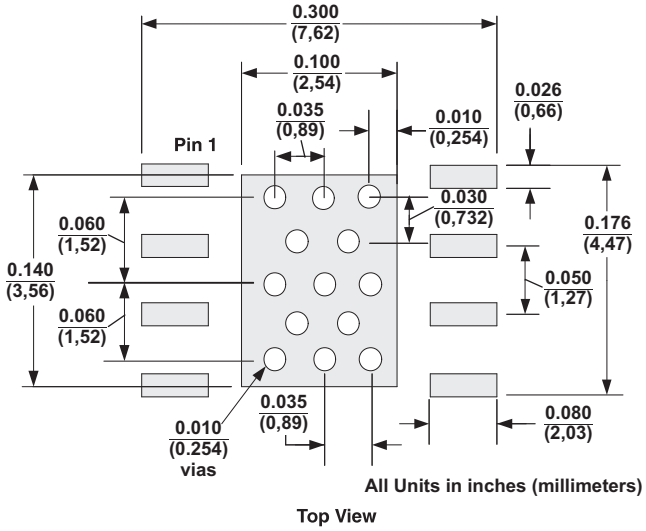

Figure 16. DDA PowerPAD™ PCB Etch and Via Pattern

1. Use etch for the leads as well as etch for the thermal pad.
2. Drill 13 holes in the area of the thermal pad. These holes must be 0.01 inch (0.254 mm) in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area, and help dissipate the heat generated by the THS3491 device. These additional vias may be larger than the 0.01-inch

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Layout Guidelines (continued)

(0.254 mm) diameter vias directly under the thermal pad because they are not in the thermal pad area to be soldered so that wicking is not a problem.

4. Connect all holes to the internal ground plane. The PowerPAD package is electrically isolated from the silicon and all leads. Connecting the PowerPAD package to any potential voltage such as $-V_S$ is acceptable because there is no electrical connection to the silicon.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web and spoke connections have a high thermal resistance that slows the heat transfer during soldering operations. Avoiding these connection methods makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS3491 PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask must leave the terminals of the package and the thermal pad area with its 13 holes exposed. The bottom-side solder mask must cover the 13 holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the device terminals.
8. With these preparatory steps in place, the device is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a device that is properly installed.

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11.1.1.2 Power Dissipation and Thermal Considerations

The THS3491 incorporates automatic thermal shutoff protection. This protection circuitry shuts down the amplifier if the junction temperature exceeds approximately 160°C. When the junction temperature reduces to approximately 140°C, the amplifier turns on again. However, for maximum performance and reliability, make sure that the design does not exceed a junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade and long-term reliability suffers. The thermal characteristics of the device are dictated by the package and the PCB. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}} \quad (1)$$

where

- PD_{max} is the maximum power dissipation in the amplifier (W).
- T_{max} is the absolute maximum junction temperature (°C).
- T_A is the ambient temperature (°C).
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
- θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

The thermal coefficient for the PowerPAD packages are substantially improved over the traditional SOIC. The data for the PowerPAD packages assume a board layout that follows the PowerPAD package layout guidelines referenced above and detailed in *PowerPAD™ Thermally Enhanced Package*. Maximum power dissipation levels are depicted in the graph titled *Comparison of θ_{JA} for Various Packages*. If the PowerPAD package is not soldered to the PCB, the thermal impedance increases substantially, and may cause serious heat and performance issues. Be sure to always solder the PowerPAD package to the PCB for optimum performance.

When determining whether or not the device satisfies the maximum power dissipation requirement, make sure to consider not only quiescent power dissipation, but also dynamic power dissipation. Often times, this dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

11.2 Layout Example

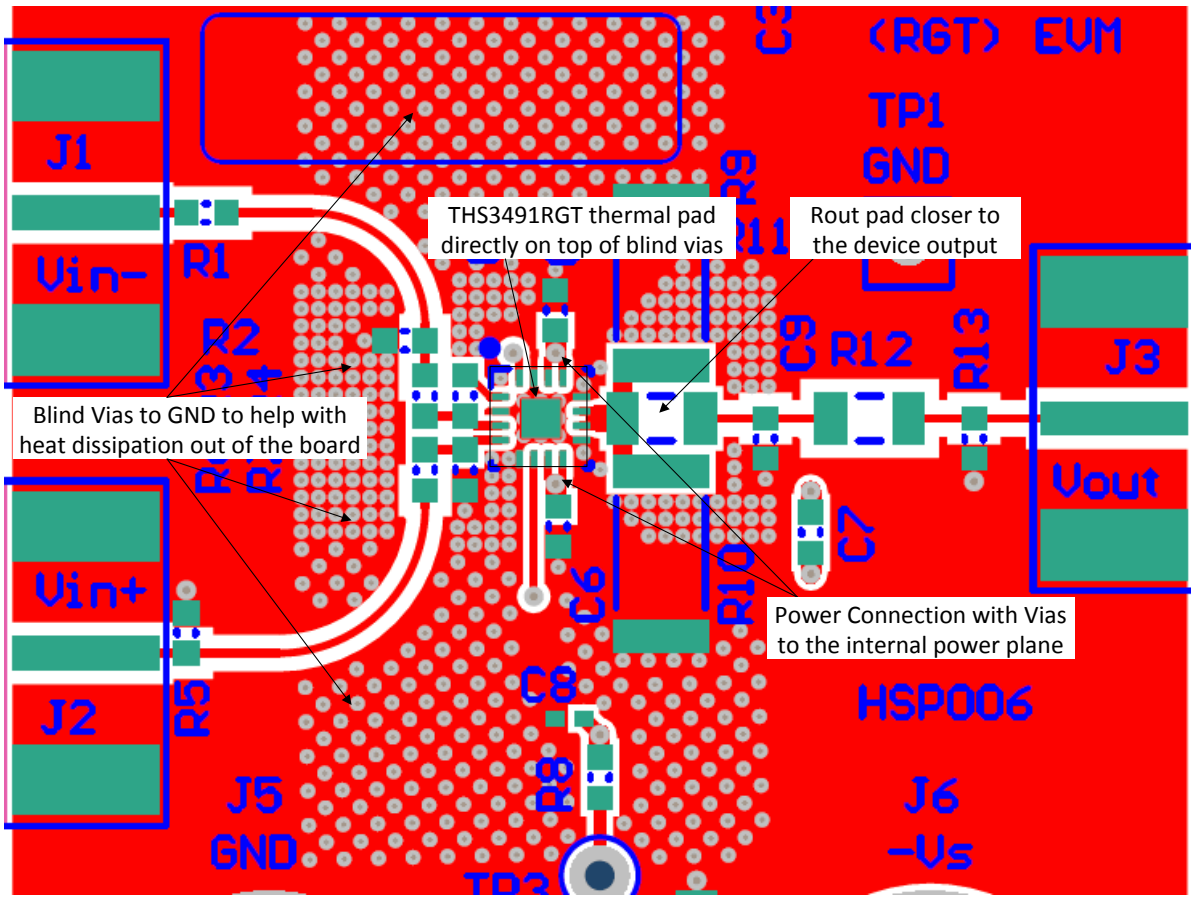

Figure 17. RGT Package Layout Example

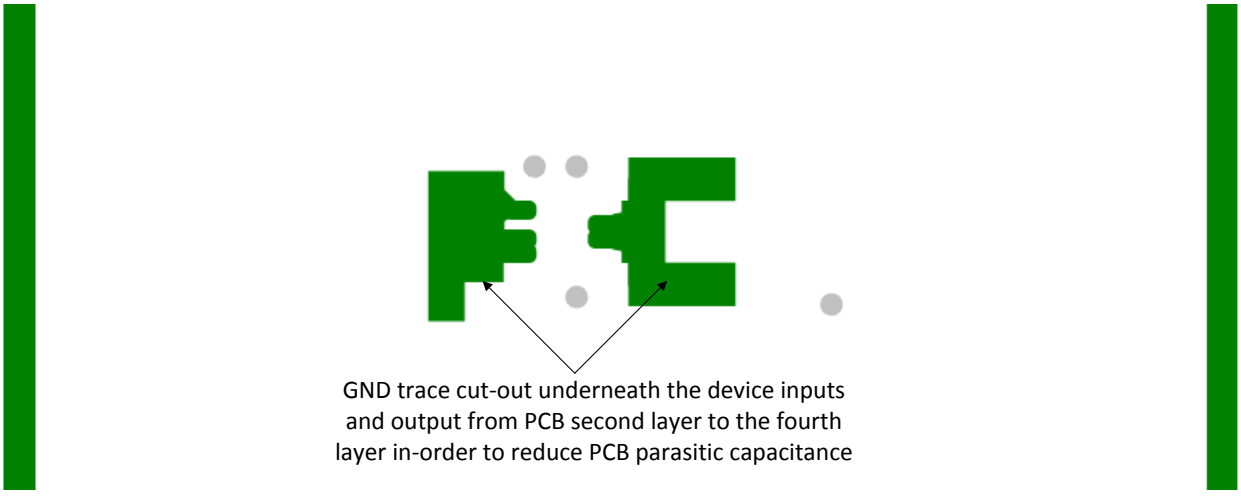

Figure 18. Ground Trace Cutout Beneath the Device Inputs and Output

ADVANCE INFORMATION

Layout Example (continued)

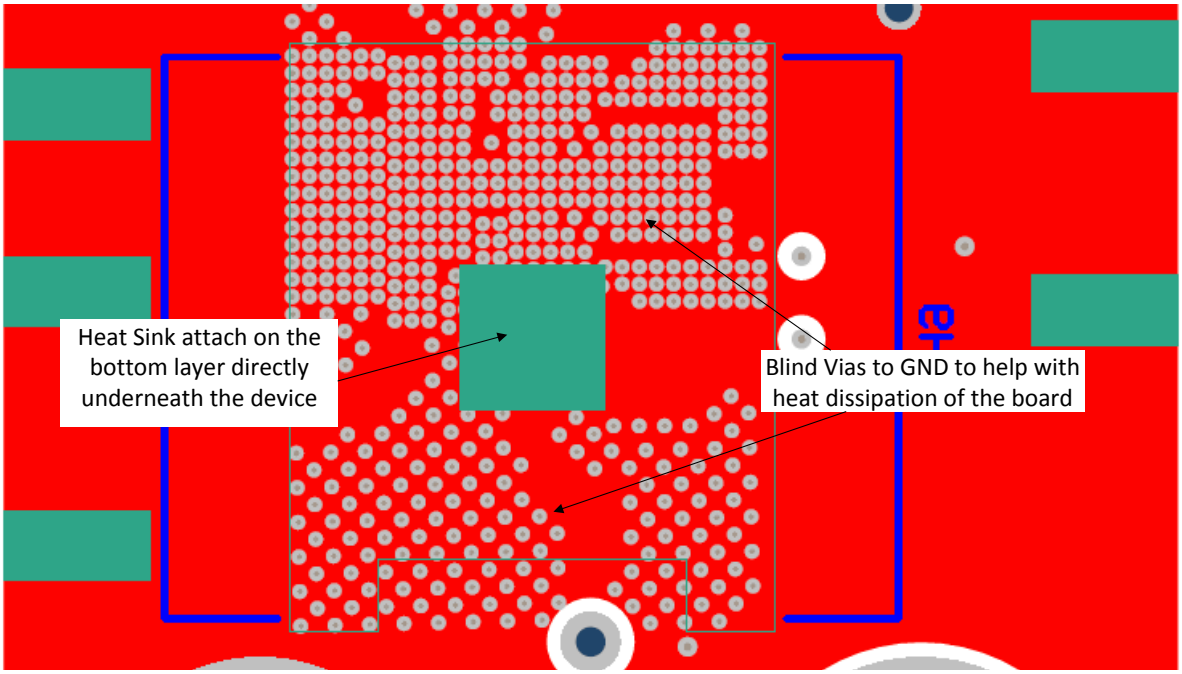

Figure 19. Heat Sink Attachment to Bottom Layer

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *PowerPAD™ Made Easy*
- *PowerPAD™ Thermally Enhanced Package*
- *Voltage Feedback vs Current Feedback Op Amps*
- *Current Feedback Amplifier Analysis and Compensation*
- *Current Feedback Amplifiers: Review, Stability Analysis, and Applications*
- *Effect of Parasitic Capacitance in Op Amp Circuits*)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS3491IDDAR	PREVIEW	SO PowerPAD	DDA	8	2500	TBD	Call TI	Call TI	-40 to 85		
THS3491IDDAT	PREVIEW	SO PowerPAD	DDA	8	250	TBD	Call TI	Call TI	-40 to 85		
THS3491IRGTR	PREVIEW	VQFN	RGT	16	2500	TBD	Call TI	Call TI	-40 to 85		
THS3491IRGTT	PREVIEW	VQFN	RGT	16	250	TBD	Call TI	Call TI	-40 to 85		
XTHS3491IDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	TBD	Call TI	Call TI	-40 to 85		Samples
XTHS3491IRGTR	ACTIVE	VQFN	RGT	16	2500	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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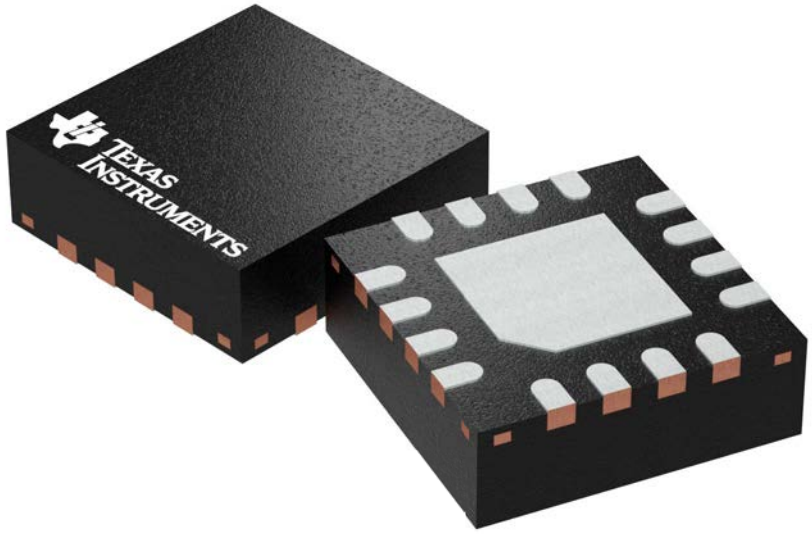
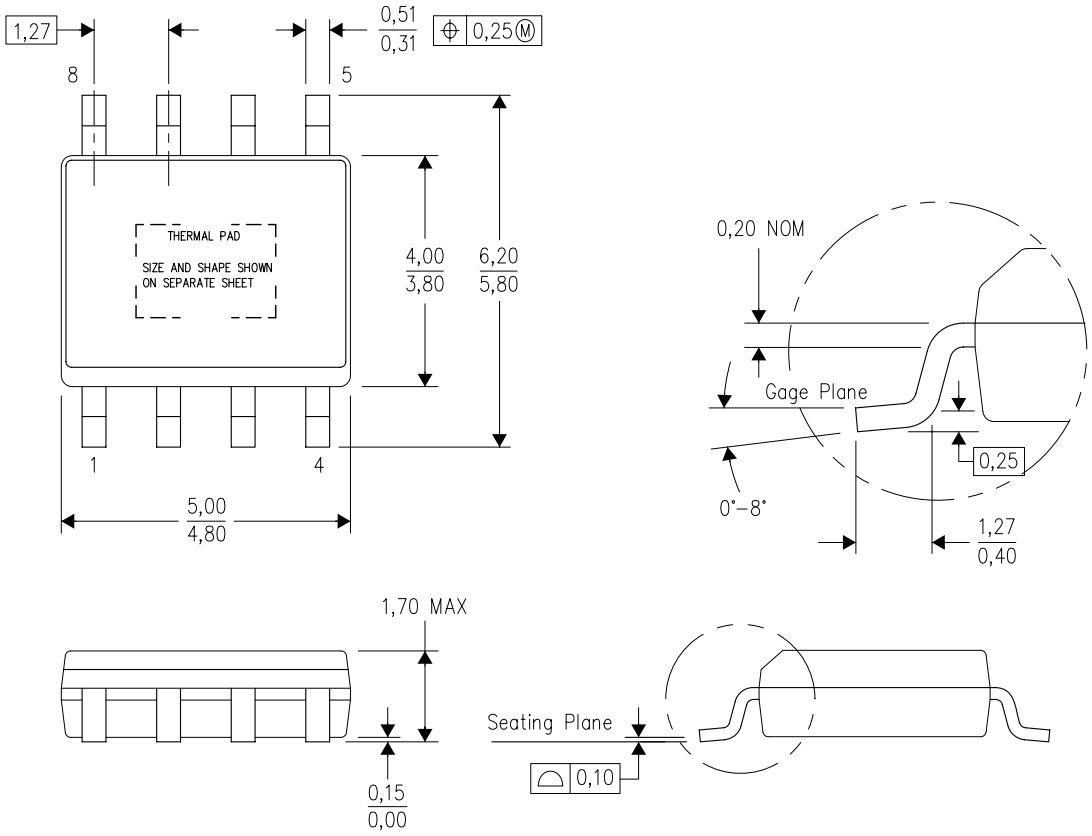
RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

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