3-A Step-Down Regulator with Integrated Switcher

Check for Samples: TPS53310

FEATURES

- **>95% Maximum Efficiency**
- **Continuous 3-A Output Current**
- **Hiccup Overcurrent Protection**
- **Supports All MLCC Output Capacitor**
- **SmoothPWM™ Auto-Skip Eco-mode™ for Light-Load Efficiency**
- **Voltage Mode Control**
- **Supports Master-Slave Interleaved Operation**
- **Synchronization up to ±20% of Nominal Frequency**
- **Conversion Voltage Range Between 2.9 V and 6.0 V**
- **Soft-Stop Output Discharge During Disable**
- **Adjustable Output Voltage Ranging Between 0.6 V and 0.84 V × V_{IN}**
- **Undervoltage, Overvoltage and Over-Temperature Protection**
- **Small 3 × 3 , 16-Pin QFN Package**
- **Open-Drain Power Good Indication**
- **Internal Boot Strap Switch**
- **Low $R_{DS(on)}$, 24 mΩ with 3.3-V Input and 19-mΩ with 5-V Input**
- **Supports Pre-bias Start Up**

LOW VOLTAGE APPLICATIONS

- **5-V Step-down Rail**
- **3.3-V Step-down Rail**

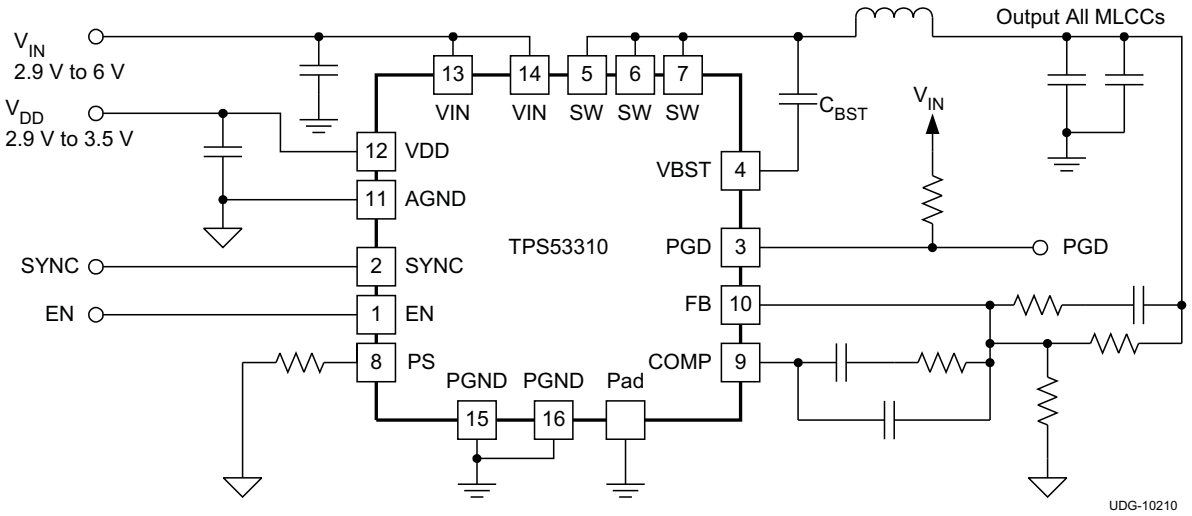
DESCRIPTION

The TPS53310 provides a fully integrated 3-V to 5-V VIN integrated synchronous FET converter solution with 16 total components, in 200 mm^2 of PCB area. Due to the low $R_{DS(on)}$ and TI's proprietary SmoothPWM™ Skip mode of operation, it enables 95.5% peak efficiency, and over 90% efficiency at loads as light as 100 mA. It requires only two 22-µF ceramic output capacitors for a power dense 3-A solution.

The TPS53310 features a 1.1-MHz switching frequency, SKIP mode operation support, pre-bias startup, internal softstart, output soft discharge, internal VBST switch, power good, EN/input UVLO, overcurrent, overvoltage, undervoltage and over-temperature protections and all ceramic output capacitor support. It supports supply voltage from 2.9 V to 3.5 V and conversion voltage from 2.9 V to 6.0 V, and output voltage is adjustable from 0.6 V to 0.84 V × V_{IN}.

The TPS53310 is available in the 3 mm × 3 mm 16-pin QFN package (Green RoHs compliant and Pb free) and operates between –40°C and 85°C.

TYPICAL APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE	ORDER NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY	ECO PLAN
–40°C to 85°C	Plastic QFN (RGT)	TPS53310RGTR	16	Tape and reel	3000	Green (RoHS and no Pb/Br)
		TPS53310RGTT	16	Mini reel	250	

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE		UNIT
			MIN	MAX	
Input voltage range	VIN, EN		–0.3	7	V
	VBST		–0.3	17	
	VBST(with respect to SW)		–0.3	7	
	FB, PS, VDD		–0.3	3.7	
Output voltage range	SW	DC	–0.3	7	V
		Pulse < 20ns, E= 5μJ	–3	10	
	PGD		–0.3	7	
	COMP, SYNC		–0.3	3.7	
	PGND		–0.3	0.3	
Electrostatic Discharge	Human Body Model (HBM)			2000	V
	Charged Device Model (CDM)			500	
Ambient temperature	T_A		–40	85	°C
Storage temperature	T_{stg}		–55	150	°C
Junction temperature	T_J		–40	150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				300	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS

		VALUE			UNIT
		MIN	NOM	MAX	
Input voltage range	VIN	2.9		6	V
	VDD	2.9	3.3	3.5	
	VBST	–0.1		13.5	
	VBST(with respect to SW)	–0.1		6	
	EN	–0.1		6	
	FB, PS	–0.1		3.5	
Output voltage range	SW	–1		6.5	V
	PGD	–0.1		6	
	COMP, SYNC	–0.1		3.5	
	PGND	–0.1		0.1	
Junction temperature range, T_J		–40		125	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	THERMAL IMPEDANCE, JUNCTION TO THERMAL PAD	THERMAL IMPEDANCE, JUNCTION TO CASE	THERMAL IMPEDANCE, JUNCTION TO AMBIENT
16-Pin Plastic QFN (RGT)	5°C/W	16°C/W	40°C/W

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ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, V_{IN} = 3.3 V, V_{VDD} = 3.3 V, PGND = GND (Unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY: VOLTAGE, CURRENTS, and UVLO						
V_{IN}	VIN supply voltage	Nominal input voltage range	2.9		6.0	V
I_{VINSDN}	VIN shutdown current	EN = 'LO'			3	µA
V_{UVLO}	VIN UVLO threshold	Ramp up; EN = 'HI'		2.8		V
$V_{UVLOHYS}$	VIN UVLO hysteresis	VIN UVLO Hysteresis		130		mV
V_{DD}	Internal circuitry supply voltage	Nominal 3.3-V input voltage range	2.9	3.3	3.5	V
I_{DDSDN}	VDD shut down current	EN = 'LO'			5	µA
I_{DD}	Standby current	EN = 'HI', no switching		2.2	3.5	mA
V_{DDUVLO}	3.3V UVLO threshold	Ramp up; EN ='HI'		2.8		V
$V_{DDUVLOHYS}$	3.3V UVLO hysteresis			75		mV
VOLTAGE FEEDBACK LOOP: VREF AND ERROR AMPLIFIER						
V_{VREF}	VREF	Internal precision reference voltage		0.6		V
$TOLV_{REF}$	VREF Tolerance	0°C ≤ T_A ≤ 85°C	–1%		1%	
		–40°C ≤ T_A ≤ 85°C	–1.25%		1.25%	
UGBW(1)	Unity gain bandwidth		14			MHz
A_{OL}(1)	Open loop gain		80			dB
I_{FBINT}	FB input leakage current	Sourced from FB pin			30	nA
I_{EAMAX}(1)	Output sinking and sourcing current	C_{COMP} = 20 pF		5		mA
SR(1)	Slew rate			5		V/µs
OCP: OVERCURRENT AND ZERO CROSSING						
I_{OCPL}	Overcurrent limit on upper FET	When I_{OUT} exceeds this threshold for 4 consecutive cycles. V_{IN}=3.3 V, V_{OUT}=1.5 V with 1-µH inductor, T_A = 25°C	4.2	4.5	4.8	A
I_{OCPH}	One time overcurrent latch off on the lower FET	Immediately shut down when sensed current reach this value. V_{IN}=3.3 V, V_{OUT}=1.5 V with 1-µH inductor, T_A = 25°C	4.8	5.1	5.5	A
V_{ZXOFF}(1)	Zero crossing comparator internal offset	PGND – SW, SKIP mode	–4.5	–3.0	–1.5	mV
t_{HICCUP}	Hiccup time interval		12.5	14.5	16.5	ms
PROTECTION: OVP, UVP, PGD, AND INTERNAL THERMAL SHUTDOWN						
V_{OVP}	Overvoltage protection threshold voltage	Measured at FB wrt. VREF	114%	117%	120%	
V_{UVP}	Undervoltage protection threshold voltage	Measured at FB wrt. VREF	80%	83%	86%	
V_{PGDL}	PGD low threshold	Measured at FB wrt. VREF	80%	83%	86%	
V_{PGDU}	PGD upper threshold	Measured at FB wrt. VREF.	114%	117%	120%	
$V_{INMINPG}$	Minimum Vin voltage for valid PGD at start up.	Measured at V_{IN} with 1-mA (or 2-mA) sink current on PGD pin at start up		1		V
THSD(1)	Thermal shutdown	Latch off controller, attempt soft-stop	130	140	150	°C
$THSD_{HYS}$(1)	Thermal Shutdown hysteresis	Controller restarts after temperature has dropped		40		°C

(1) Ensured by design. Not production tested.

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ELECTRICAL CHARACTERISTICS (continued)

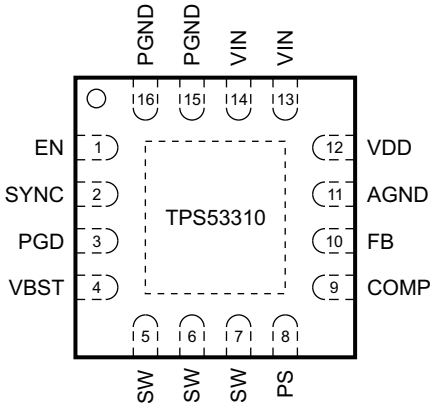
over recommended free-air temperature range, V_{IN} = 3.3 V, V_{VDD} = 3.3 V, PGND = GND (Unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC PINS: I/O VOLTAGE AND CURRENT						
V_{PGPD}	PGD pull down voltage	Pull-down voltage with 4-mA sink current		0.2	0.4	V
I_{PGLK}	PGD leakage current	Hi-Z leakage current, apply 3.3-V in off state	–2	0	2	µA
R_{ENPU}	Enable pull up resistor			1.35		MΩ
V_{ENH}	EN logic high threshold		1.10	1.18	1.30	V
V_{ENHYS}	EN hysteresis			0.18	0.24	V
PS_{THS}	PS mode threshold voltage	Level 1 to level 2 (2)		0.12		V
		Level 2 to level 3		0.4		
		Level 3 to level 4		0.8		
		Level 4 to level 5		1.4		
		Level 5 to level 6		2.2		
I_{PS}	PS source	10-µA pull-up current when enabled.	8	10	12	µA
f_{SYNCSL}	Slave SYNC frequency range	Versus nominal switching frequency	–20%		20%	
PW_{SYNC}	SYNC low pulse width			110		ns
I_{SYNC}	SYNC pin sink current	T_A = 25°C		10		µA
$V_{SYNCTHS}$ (3)	SYNC threshold	Falling edge		1.0		V
$V_{SYNCHYS}$ (3)	SYNC hysteresis			0.5		V
BOOT STRAP: VOLTAGE AND LEAKAGE CURRENT						
I_{VBSTLK}	VBST leakage current	V_{IN} = 3.3V, V_{VBST} = 6.6 V, T_A = 25°C			1	µA
TIMERS: SS, FREQUENCY, RAMP, ON-TIME AND I/O TIMING						
t_{SS_1}	Delay after EN asserting	EN = 'HI', master or HEF mode		0.2		ms
t_{SS_2}	Delay after EN asserting	EN = 'HI', slave waiting time		0.5		ms
t_{SS_3}	Soft-start ramp-up time	Rising from V_{SS} = 0 V to V_{SS} = 0.6 V		0.4		ms
$t_{PGDENDLY}$	PGD startup delay time	Rising from V_{SS} = 0 V to V_{SS} = 0.6 V, from V_{SS} reaching 0.6 V to V_{PGD} going high		0.4		ms
t_{OVPDLY}	Overvoltage protection delay time	Time from FB out of +20% of VREF to OVP fault	1.0	1.7	2.5	µs
t_{UVPDLY}	Undervoltage protection delay time	Time from FB out of -20% of VREF to UVP fault		11		µs
f_{SW}	Switching frequency control	Forced CCM mode	0.99	1.1	1.21	MHz
	Ramp amplitude (3)	2.9 V < V_{IN} < 6.0 V		V_{IN}/4		V
$t_{MIN(off)}$	Minimum OFF time	FCCM mode or DE mode		100	140	ns
		HEF mode		175	250	
D_{MAX}	Maximum duty cycle, FCCM mode and DE mode	f_{SW} = 1.1 MHz, 0°C ≤ T_A ≤ 85°C	84%	89%		
	Maximum duty cycle, HEF mode		75%	81%		
R_{SFTSTP}	Soft-discharge transistor resistance	V_{EN} = Low, V_{IN} = 3.3 V, V_{OUT} = 0.5 V		60		Ω

(2) See PS pin description for levels.
(3) Ensured by design. Not production tested.

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RGT Package
(Top View)



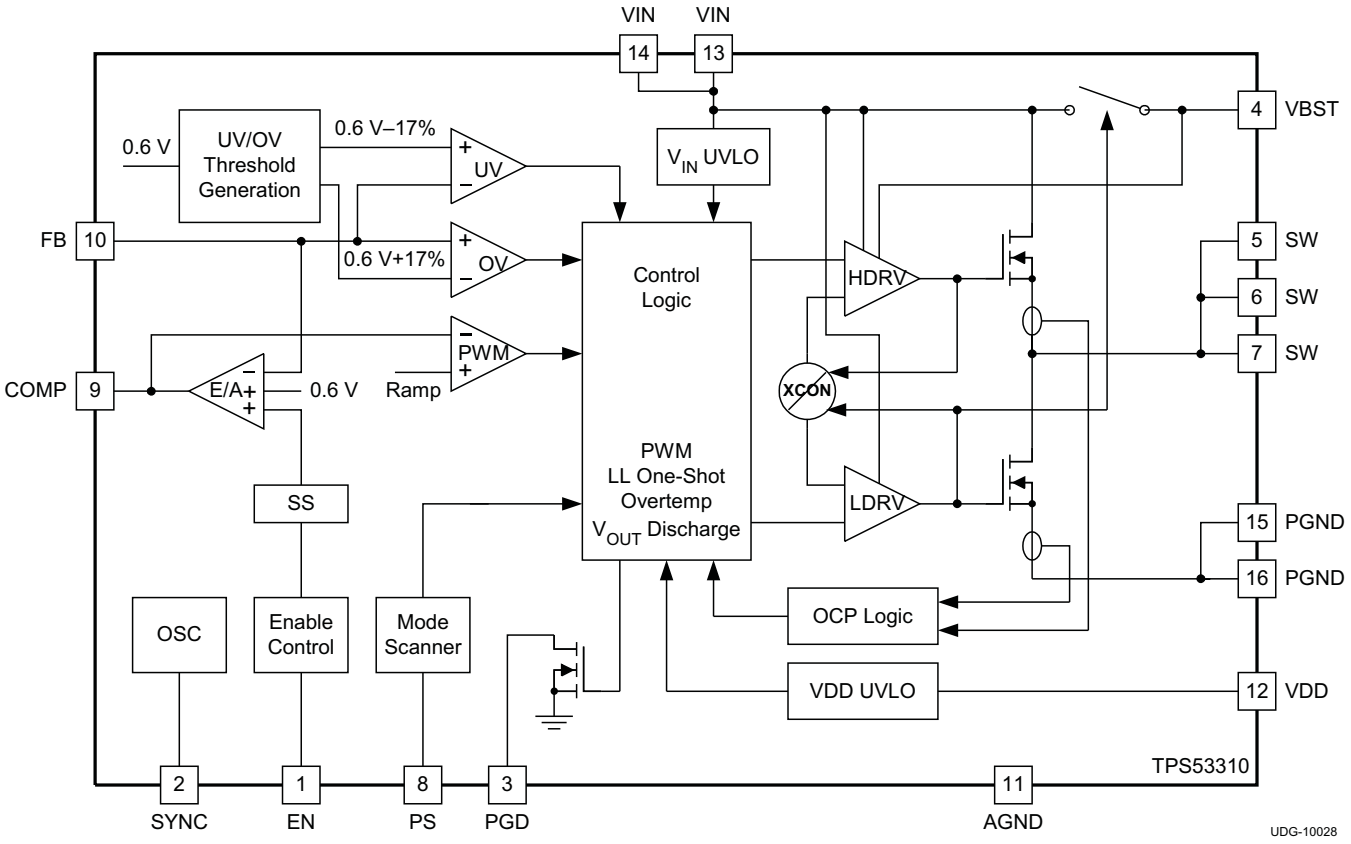
PIN DESCRIPTIONS

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AGND	11	G	Device analog ground terminal.
COMP	9	O	Error amplifier compensation terminal. Type III compensation method is recommended for stability.
EN	1	I	Enable. Internally pulled up to VDD with a 1.35-MΩ resistor.
FB	10	I	Voltage feedback. Also used for OVP, UVP and PGD determination.
PGD	3	O	Power good output flag. Open drain output. Pull up to an external rail via a resistor.
PGND	15	P	Power ground terminal.
	16		
PS	8	I	Mode configuration pin (with 10 µA current): Connecting to ground: Forced CCM slave Pulled high or floating (internal pulled high): Forced CCM master Connect with 24.3 kΩ to GND: DE slave Connect with 57.6 kΩ to GND: HEF mode Connect with 105 kΩ to GND : reserved mode Connect with 174 kΩ to GND: DE master.
SYNC	2	B	Synchronization signal for input interleaving. Master SYNC pin sends out 180° out-of-phase signal to slave SYNC. SYNC frequency must be within ±20% of slave nominal frequency.
SW	5	B	Output inductor connection to integrated power devices.
	6		
	7		
VBST	4	P	Supply input for high-side MOSFET (bootstrap terminal). Connect capacitor from this pin to SW terminal.
VDD	12	P	Input bias supply for analog functions.
VIN	13	P	Gate driver supply and power conversion voltage.
	14		

(1) I – Input; B – Bidirectional; O – Output; G – Ground; P – Supply (or Ground)

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FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Inductor IN06142 (1 µH, 5.4 mΩ) is used.

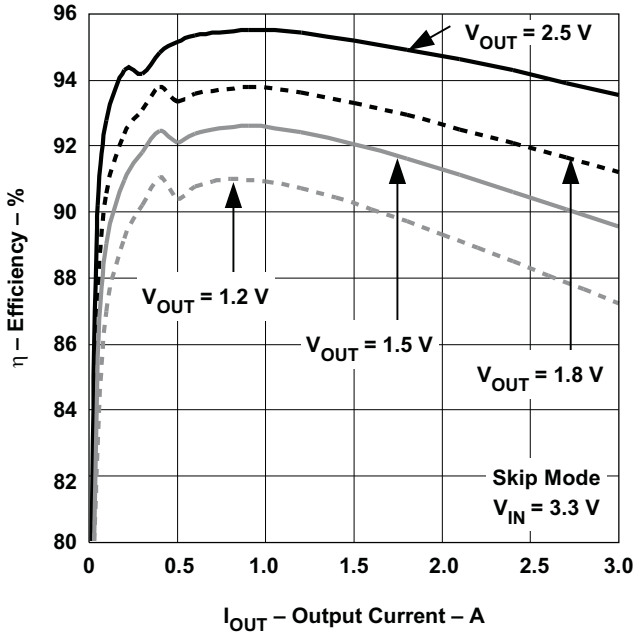


Figure 1. Efficiency vs. Output Current, Skip Mode, V_{IN} = 3.3 V

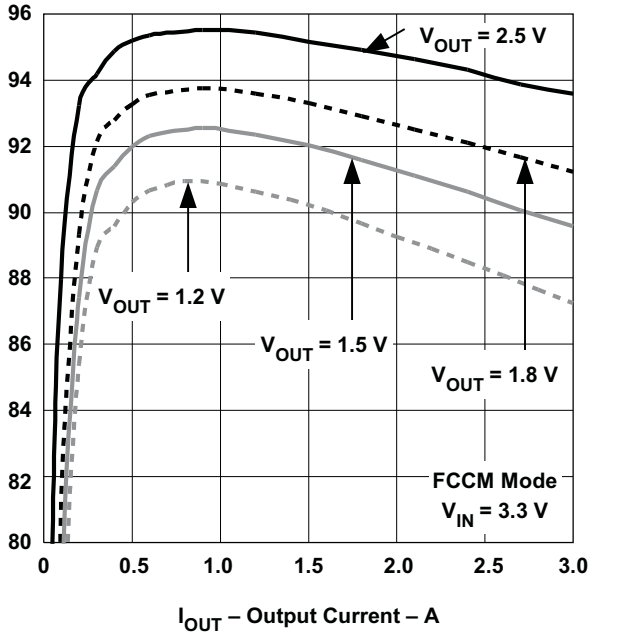


Figure 2. Efficiency vs. Output Current, FCCM, V_{IN} = 3.3 V

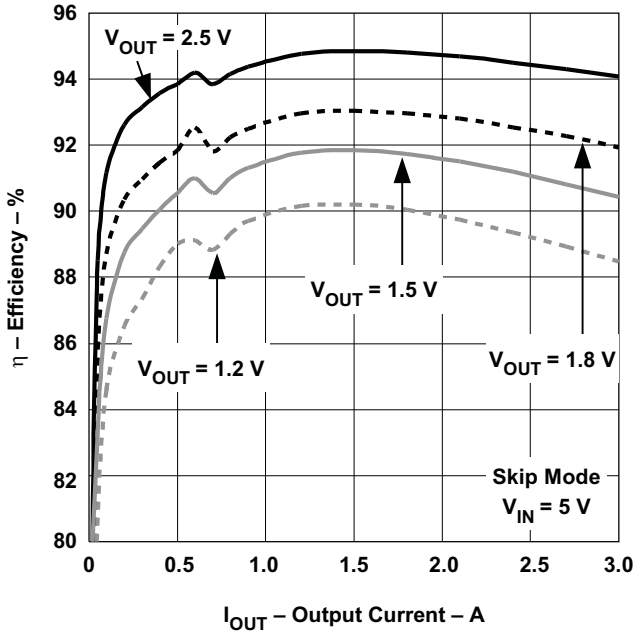


Figure 3. Efficiency vs. Output Current, Skip Mode, V_{IN} = 5 V

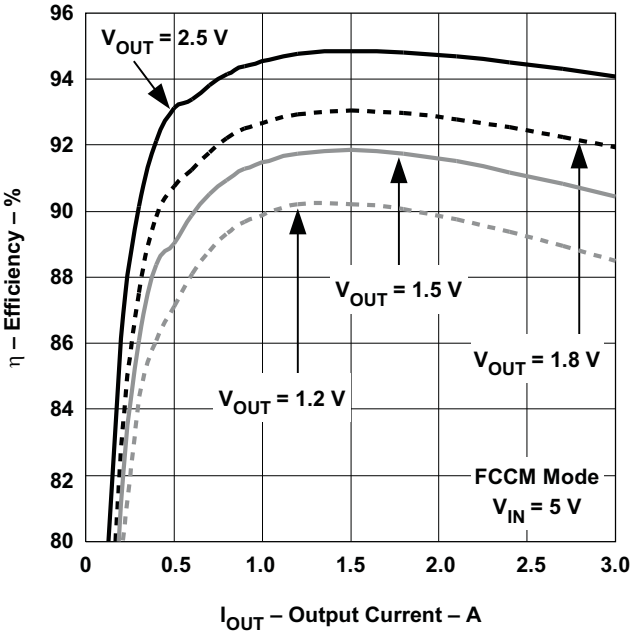


Figure 4. Efficiency vs. Output Current, FCCM, V_{IN} = 5 V

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TYPICAL CHARACTERISTICS (continued)

Inductor IN06142 (1 µH, 5.4 mΩ) is used.

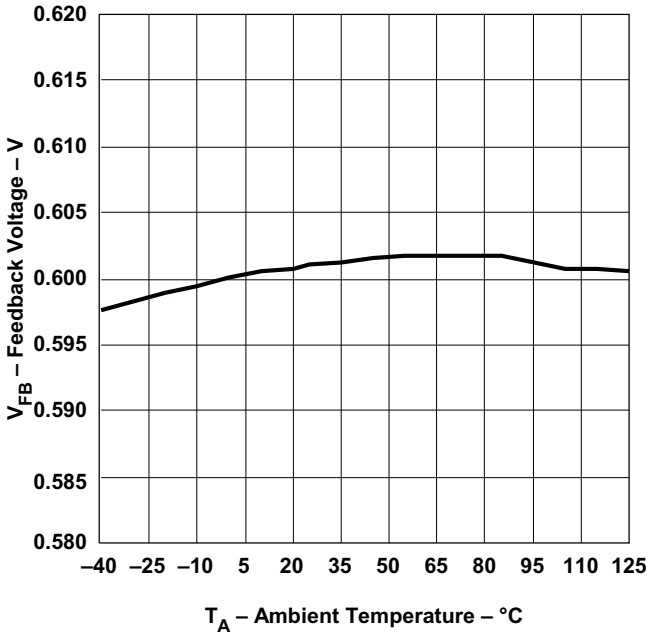


Figure 5. Feedback Voltage vs. Ambient Temperature

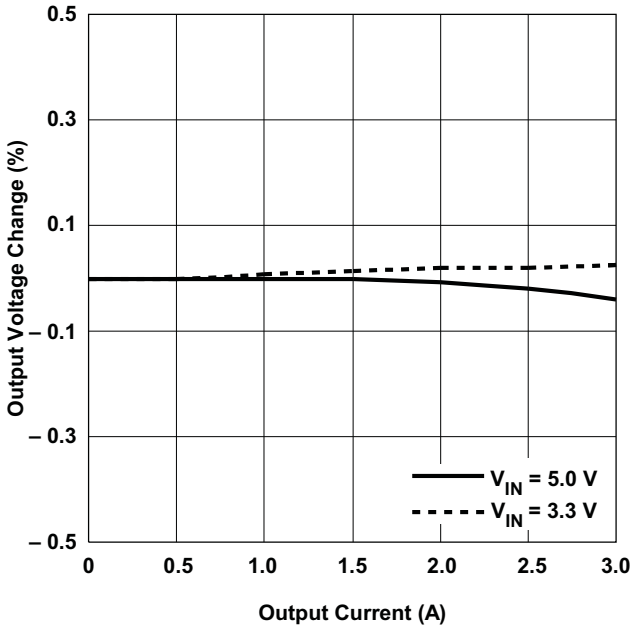


Figure 6. Output Voltage Change vs. Output Current

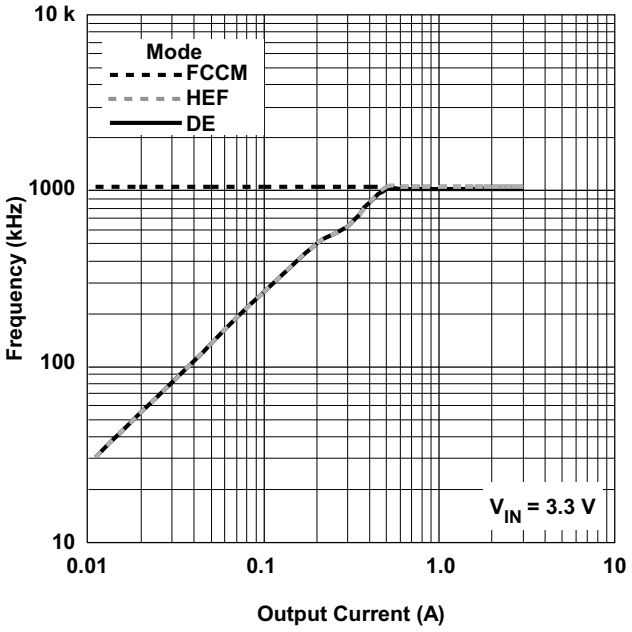


Figure 7. Frequency vs. Output Current at V_{IN} = 3.3 V

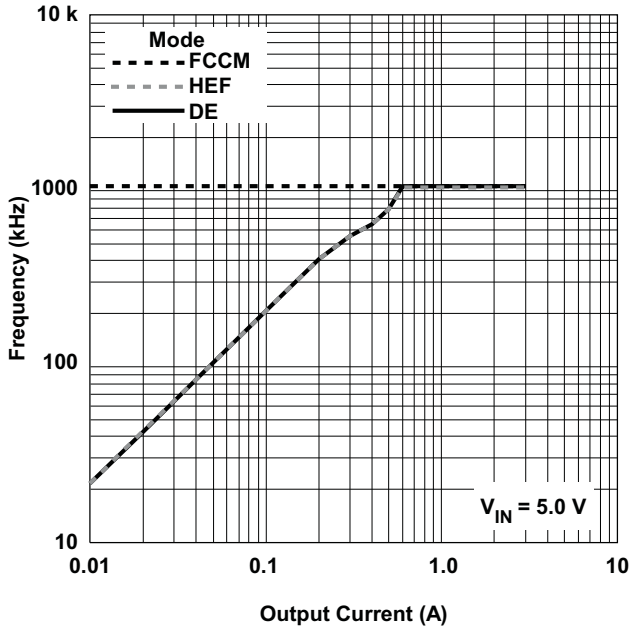


Figure 8. Frequency vs. Output Current at V_{IN} = 5.0 V

TYPICAL CHARACTERISTICS (continued)

Inductor IN06142 (1 µH, 5.4 mΩ) is used.

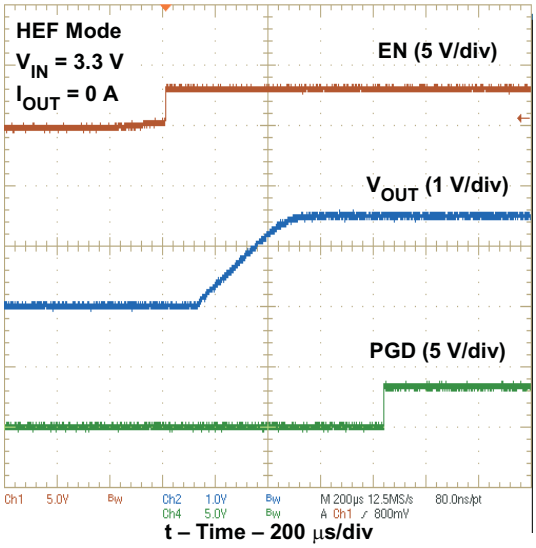


Figure 9. Normal Start Up Waveform

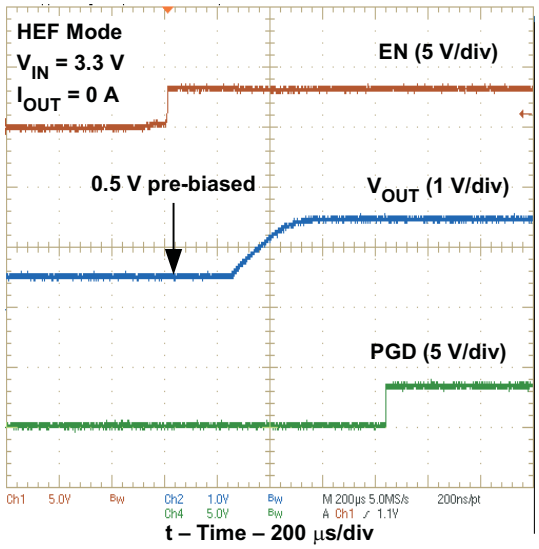


Figure 10. Pre-Bias Start Up Waveform

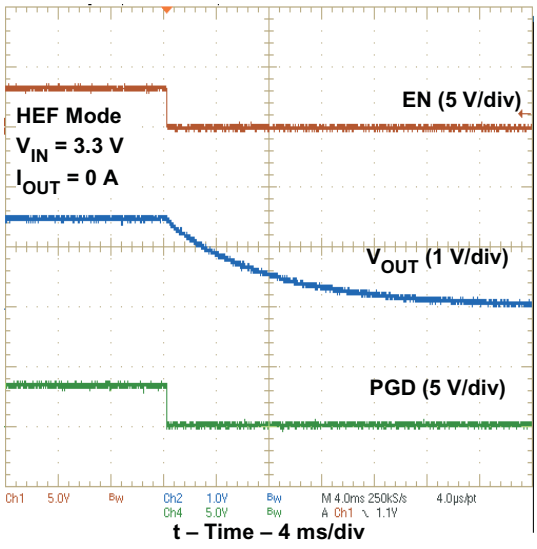


Figure 11. Soft-Stop Waveform

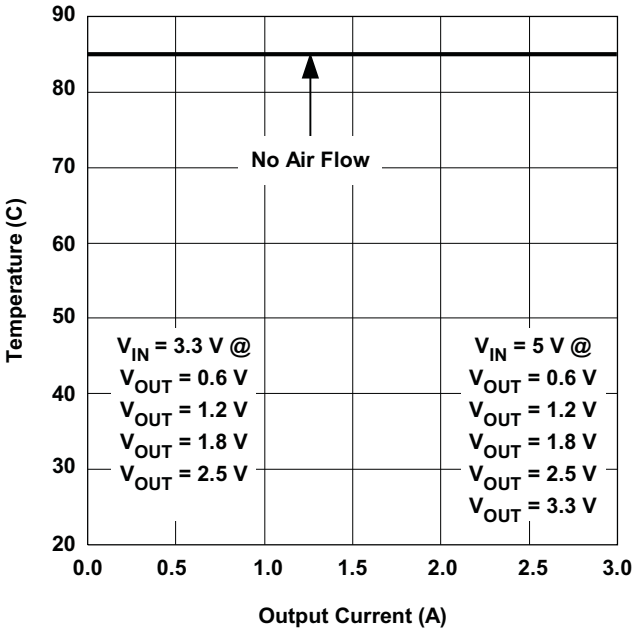


Figure 12. Safe Operating Area

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APPLICATION INFORMATION

Application Circuit Diagram

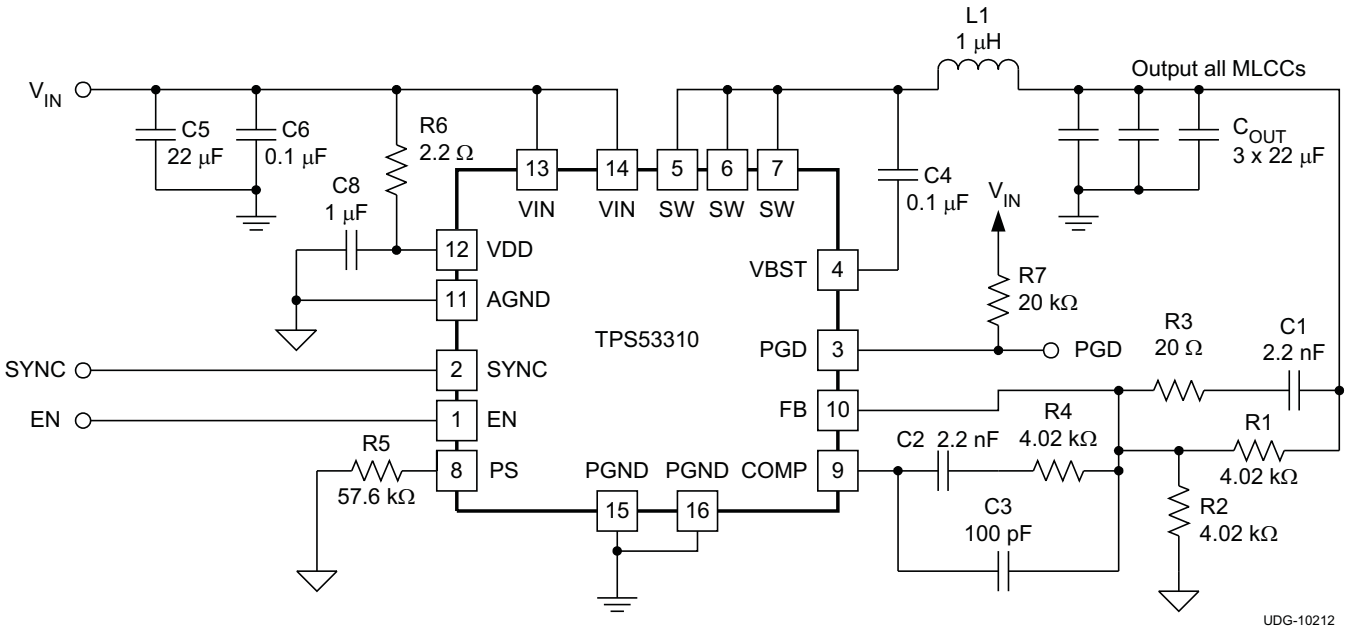


Figure 13. Typical 3.3-V input Application Circuit Diagram

Overview

The TPS53310 is a high-efficiency switching regulator with two integrated N-channel MOSFETs and is capable of delivering up to 3 A of load current. The TPS53310 provides output voltage between 0.6 V and 0.84 × V_{IN} from 2.9 V to 6.0 V wide input voltage range.

This device employs five operation modes to fit various application needs. The *master/slave* mode enables a two-phase interleaved operation to reduce input ripple. The *skip* mode operation provides reduced power loss and increases the efficiency at light load. The unique, patented PWM modulator enables smooth light load to heavy load transition while maintaining fast load transient.

Operation Mode

The TPS53310 offers five operation modes determined by the PS pin connections listed in Table 1.

Table 1. Operation Mode Selection

PS PIN CONNECTION	OPERATION MODE	AUTO-SKIP AT LIGHT LOAD	MASTER/SLAVE SUPPORT
GND	FCCM Slave		Slave
24.3 kΩ to GND	DE Slave	√	Slave
57.6 kΩ to GND	HEF Mode	√	
174 kΩ to GND	DE Master	√	Master
Floating or pulled to VDD	FCCM Master		Master

In *forced continuous conduction mode* (FCCM), the high-side FET is ON during the on-time and the low-side FET is ON during the off-time. The switching is synchronized to the internal clock thus the switching frequency is fixed.

In *diode emulation* mode (DE), the high-side FET is ON during the on-time and low-side FET is ON during the off-time until the inductor current reaches zero. An internal zero-crossing comparator detects the zero crossing of inductor current from positive to negative. When the inductor current reaches zero, the comparator sends a signal to the logic control and turns off the low-side FET.

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When the load is increased, the inductor current is always positive and the zero-crossing comparator does not send a zero-crossing signal. The converter enters into *continuous conduction mode* (CCM) when no zero-crossing is detected for two consecutive PWM pulses. The switching synchronizes to the internal clock and the switching frequency is fixed.

In *high-efficiency* mode (HEF), the operation is the same as diode emulation mode at light load. However, the converter does not synchronize to the internal clock during CCM. Instead, the PWM modulator determines the switching frequency.

Eco-mode™ Light-Load Operation

In skip modes (DE and HEF) when the load current is less than one-half of the inductor peak current, the inductor current becomes negative by the end of off-time. During light load operation, the low-side MOSFET is turned off when the inductor current reaches zero. The energy delivered to the load per switching cycle is increased compared to the normal PWM mode operation and the switching frequency is reduced. The switching loss is reduced, thereby improving efficiency.

In both DE and HEF mode, the switching frequency is reduced in discontinuous conduction mode (DCM). When the load current is 0 A, the minimum switching frequency is reached. The difference between V_{VBST} and V_{SW} must be maintained at a value higher than 2.4 V.

Forced Continuous Conduction Mode (FCCM)

When the PS pin is grounded or greater than 2.2 V, the TPS53310 is operating in *forced continuous conduction mode* in both light-load and heavy-load conditions. In this mode, the switching frequency remains constant over the entire load range, making it suitable for applications that need tight control of switching frequency at a cost of lower efficiency at light load.

Soft Start

The soft-start function reduces the inrush current during the start up sequence. A slow-rising reference voltage is generated by the soft-start circuitry and sent to the input of the error amplifier. When the soft-start ramp voltage is less than 600 mV, the error amplifier uses this ramp voltage as the reference. When the ramp voltage reaches 600 mV, the error amplifier switches to a fixed 600-mV reference. The typical soft-start time is 400 µs.

Power Good

The TPS53310 monitors the voltage on the FB pin. If the FB voltage is between 83% and 117% of the reference voltage, the power good signal remains high. If the FB voltage falls outside of these limits, the internal open drain output pulls the power good pin (PGD) low.

During start-up, V_{IN} needs to be higher than 1-V in order to have valid power good logic, and the power good signal is delayed for 400 µs after the FB voltage falls to within the power good limits. There is also 10-µs delay during the shut down sequence.

Undervoltage Lockout (UVLO) Function

The TPS53310 provides undervoltage lockout (UVLO) protection for both power input (V_{IN}) and bias input (VDD) voltage. If either of them is lower than the UVLO threshold voltage minus the hysteresis, the device shuts off. When the voltage rises above the threshold voltage, the device restarts. The typical UVLO rising threshold is 2.8 V for both V_{IN} and V_{VDD}. A hysteresis voltage of 130 mV for V_{IN} and 75 mV for V_{VDD} is also provided to prevent glitch.

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Overcurrent Protection

The TPS53310 continuously monitors the current flowing through the high-side and the low-side MOSFETs. If the current through the high-side FET exceeds 4.5 A, the high-side FET turns off and the low-side FET turns on until the next PWM cycle. An overcurrent (OC) counter starts to increment each occurrence of an overcurrent event. The converter shuts down immediately when the OC counter reaches four. The OC counter resets if the detected current is less 4.5 A after an OC event.

Another set of overcurrent circuitry monitors the current flowing through low-side FET. If the current through the low-side FET exceeds 5.1 A, the overcurrent protection is enabled and immediately turns off both the high-side and the low-side FETs and shuts down the converter . The device is fully protected against overcurrent during both on-time and off-time.

The device attempts to restart after a hiccup delay (14.5-ms typical). If the overcurrent condition is cleared before restart, the device starts up normally. Please refer to the TPS53311 datasheet (SLUSA41) for information on latch-off overcurrent protection.

Overvoltage Protection

The TPS53310 monitors the voltage divided feedback voltage to detect overvoltage and undervoltage conditions. When the feedback voltage is greater than 117% of the reference, the high-side MOSFET turns off and the low-side MOSFET turns on. The output voltage then drops until it reaches the undervoltage threshold. At that point the low-side MOSFET turns off and the device enters a high-impedance state.

Undervoltage Protection

When the feedback voltage is lower than 83% of the reference voltage, the undervoltage protection timer starts. If the feedback voltage remains lower than the undervoltage threshold voltage after 10 μs, the device turns off both the high-side and the low-side MOSFETs and goes into a high-impedance state. The device attempts to restart after a hiccup delay (14.5 ms typical).

Overtemperature Protection

The TPS53310 continuously monitors the die temperature. If the die temperature exceeds the threshold value (140˚C typical), the device shuts off. When the device temperature falls to 40˚C below the overtemperature threshold, it restarts and returns to normal operation.

Output Discharge

When the enable pin is low, the TPS53310 discharges the output capacitors through an internal MOSFET switch between SW and PGND while high-side and low-side MOSFETs remain off. The typical discharge switch-on resistance is 60 Ω. This function is disabled when V_{IN} is less than 1 V.

Master/Slave Operation and Synchronization

Two TPS53310 can operate interleaved when configured as master/slave. The SYNC pins of the two devices are connected together for synchronization. In CCM, the master device sends the 180° out-of-phase pulse to the slave device through the SYNC pin, which determines the leading edge of the PWM pulse. If the slave device does not receive the SYNC pulse from the master device or if the SYNC connection is broken during operation, the slave device continues to operate using its own internal clock.

In DE mode, the master/slave switching nodes do not synchronize to each other if either one of them is operating in DCM. when both master and slave enters CCM, the switching nodes of master and slave synchronized to each other.

The SYNC pin of the slave device can also connect to external clock source within ±20% of the 1.1-MHz switching frequency. The falling edge of the SYNC triggers the rising edge of the PWM signal.

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External Components Selection

1. DETERMINE THE VALUE OF R1 AND R2

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in Figure 13. R1 is connected between the FB pin and the output, and R2 is connected between the FB pin and GND. The recommended value for R1 is from 1 kΩ to 5 kΩ. Determine R2 using equation in Equation 1.

$$R2 = \frac{0.6}{V_{OUT} - 0.6} \times R1 \quad (1)$$

2. CHOOSE THE INDUCTOR

The inductance value should be determined to give the ripple current of approximately 20% to 40% of maximum output current. The inductor ripple current is determined by Equation 2:

$$I_{L(ripple)} = \frac{1}{L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation.

3. CHOOSE THE OUTPUT CAPACITOR(S)

The output capacitor selection is determined by output ripple and transient requirement. When operating in CCM, the output ripple has three components:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} \quad (3)$$

$$V_{RIPPLE(C)} = \frac{I_{L(ripple)}}{8 \times C_{OUT} \times f_{SW}} \quad (4)$$

$$V_{RIPPLE(ESR)} = I_{L(ripple)} \times ESR \quad (5)$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN} \times ESL}{L} \quad (6)$$

When ceramic output capacitors are used, the ESL component is usually negligible. In the case when multiple output capacitors are used, ESR and ESL should be the equivalent of ESR and ESL of all the output capacitor in parallel.

When operating in DCM, the output ripple is dominated by the component determined by capacitance. It also varies with load current and can be expressed as shown in Equation 7.

$$V_{RIPPLE(DCM)} = \frac{\left(\alpha \times I_{L(ripple)} - I_{OUT}\right)^2}{2 \times C_{OUT} \times f_{SW} \times I_{L(ripple)}}$$

where

- α is the DCM on-time coefficient and can be expressed in Equation 8 (typical value 1.25) (7)

$$\alpha = \frac{t_{ON(DCM)}}{t_{ON(CCM)}} \quad (8)$$

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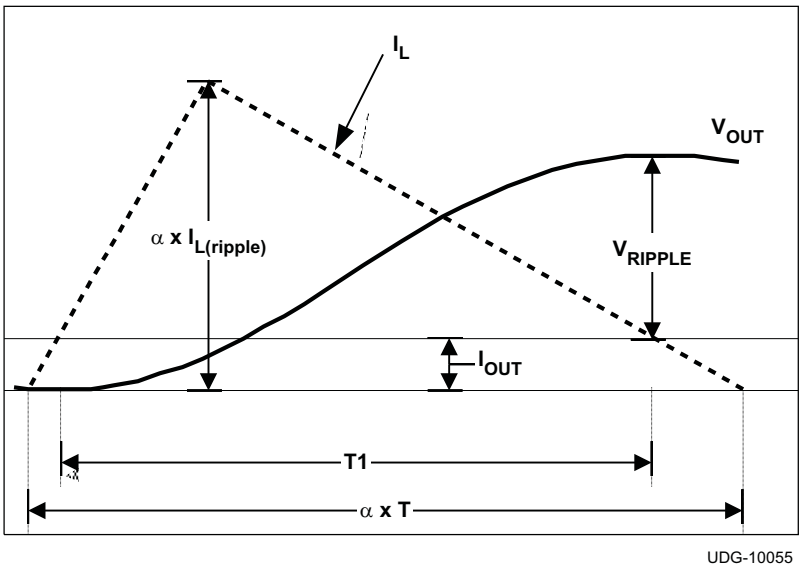


Figure 14. DCM V_{OUT} Ripple Calculation

4. CHOOSE THE INPUT CAPACITOR

The selection of input capacitor should be determined by the ripple current requirement. The ripple current generated by the converter needs to be absorbed by the input capacitors as well as the input source. The RMS ripple current from the converter can be expressed in Equation 9.

$$I_{IN(ripple)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

where

- D is the duty cycle and can be expressed as shown in Equation 10

(9)

$$D = \frac{V_{OUT}}{V_{IN}} \tag{10}$$

To minimize the ripple current drawn from the input source, sufficient input decoupling capacitors should be placed close to the device. The ceramic capacitor is recommended because it provides low ESR and low ESL. The input voltage ripple can be calculated as shown in Equation 11 when the total input capacitance is determined.

$$V_{IN(ripple)} = \frac{I_{OUT} \times D}{f_{SW} \times C_{IN}} \tag{11}$$

5. COMPENSATION DESIGN

The TPS53310 uses voltage mode control. To effectively compensate the power stage and ensure fast transient response, Type III compensation is typically used.

The control to output transfer function can be described in Equation 12.

$$G_{CO} = 4 \times \frac{1 + s \times C_{OUT} \times ESR}{1 + s \times \left(\frac{L}{DCR + R_{LOAD}} + C_{OUT} \times (ESR + DCR) \right) + s^2 \times L \times C_{OUT}} \tag{12}$$

The output L-C filter introduces a double pole which can be calculated as shown in Equation 13.

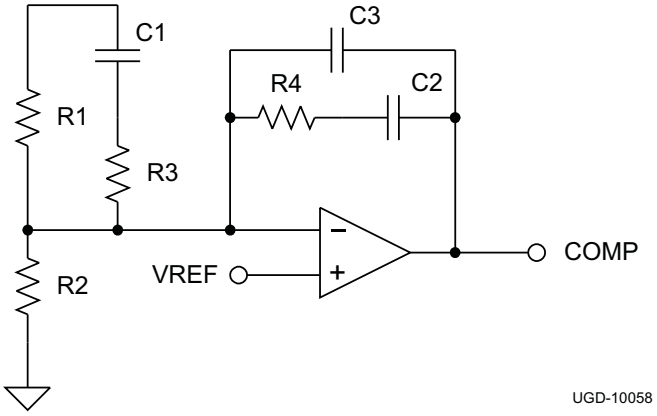
$$f_{DP} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}} \tag{13}$$

The ESR zero can be calculated as shown in Equation 14.

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$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \quad (14)$$

Figure 15 and Figure 16 show the configuration of Type III compensation and typical pole and zero locations. Equation 16 through Equation 20 describe the compensator transfer function and poles and zeros of the Type III network.



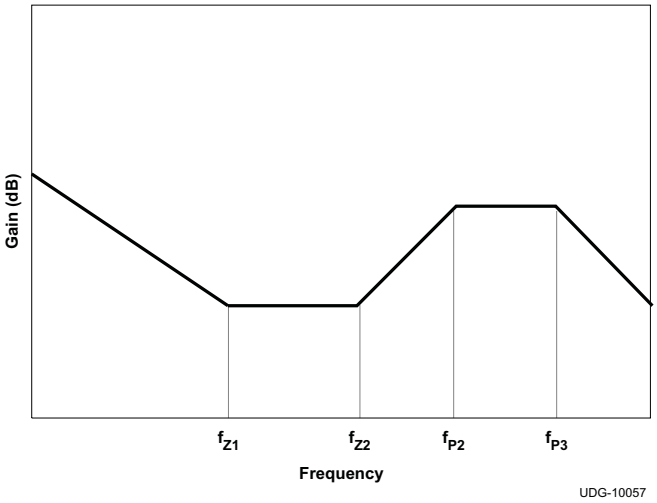


Figure 15. Type III Compensation Network Configuration Schematic

Figure 16. Type III Compensation Gain Plot and Zero/Pole Placement

$$G_{EA} = \frac{(1 + s \times C_1 \times (R_1 + R_3))(1 + s \times R_4 \times C_2)}{(s \times R_1 \times (C_2 + C_3)) \times (1 + s \times C_1 \times R_3) \times \left(1 + s \times R_4 \frac{C_2 \times C_3}{C_2 + C_3}\right)} \quad (15)$$

$$f_{Z1} = \frac{1}{2 \times \pi \times R_4 \times C_2} \quad (16)$$

$$f_{Z2} = \frac{1}{2 \times \pi \times (R_1 + R_3) \times C_1} \cong \frac{1}{2 \times \pi \times R_1 \times C_1} \quad (17)$$

$$f_{P1} = 0 \quad (18)$$

$$f_{P2} = \frac{1}{2 \times \pi \times R_3 \times C_1} \quad (19)$$

$$f_{P3} = \frac{1}{2 \times \pi \times R_4 \times \left(\frac{C_2 \times C_3}{C_2 + C_3}\right)} \cong \frac{1}{2 \times \pi \times R_4 \times C_3} \quad (20)$$

The two zeros can be placed near the double pole frequency to cancel the response from the double pole. One pole can be used to cancel ESR zero, and the other non-zero pole can be placed at half switching frequency to attenuate the high frequency noise and switching ripple. Suitable values can be selected to achieve a compromise between high phase margin and fast response. A phase margin higher than 45 degrees is required for stable operation.

For DCM operation, a C3 between 56 pF and 150 pF is recommended for output capacitance between 20 µF to 200 µF.

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Figure 17 shows the master/slave configuration schematic for a design with a 3.3-V input.

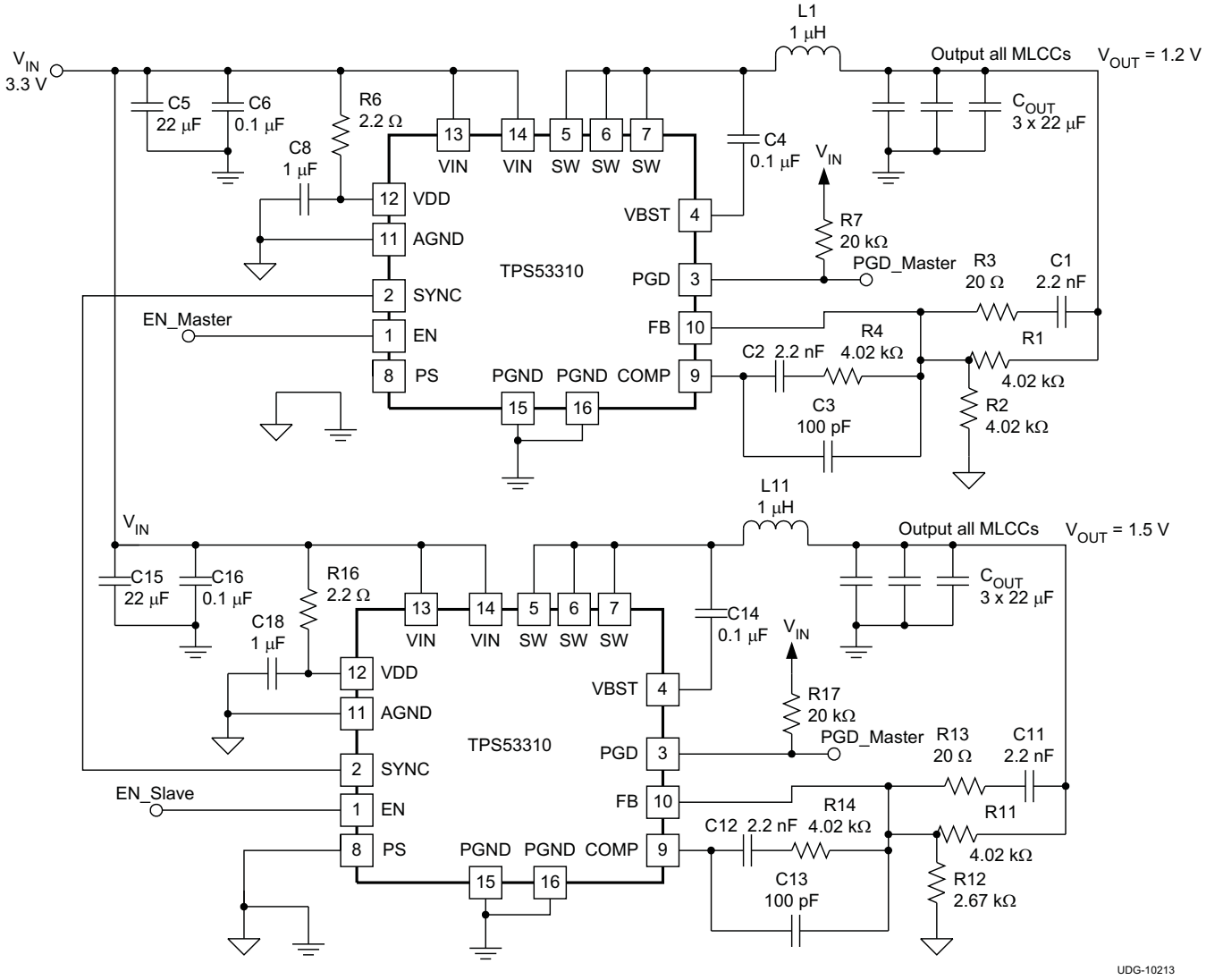


Figure 17. Master/Slave Configuration Schematic

Layout Considerations

Good layout is essential for stable power supply operation. Follow these guidelines for a clean PCB layout:

- Separate the power ground and analog ground planes. Connect them together at one location.
- Use four vias to connect the thermal pad to power ground.
- Place VIN and VDD decoupling capacitors as close to the device as possible.
- Use wide traces for V_{IN}, V_{OUT}, PGND and SW. These nodes carry high current and also serve as heat sinks.
- Place feedback and compensation components as close to the device as possible.
- Keep analog signals (FB, COMP) away from noisy signals (SW, SYNC, VBST).
- Refer to TPS53310 evaluation module for a layout example.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS53310RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
TPS53310RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

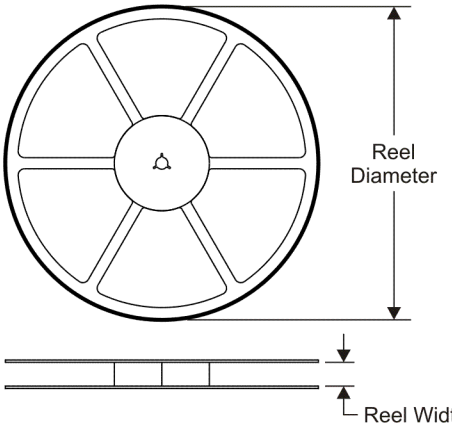
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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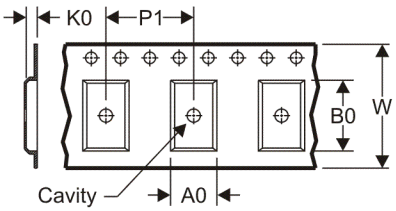
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REEL DIMENSIONS

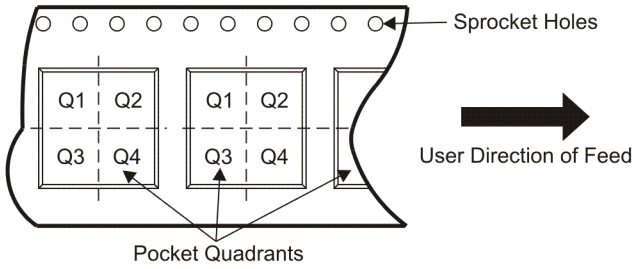


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

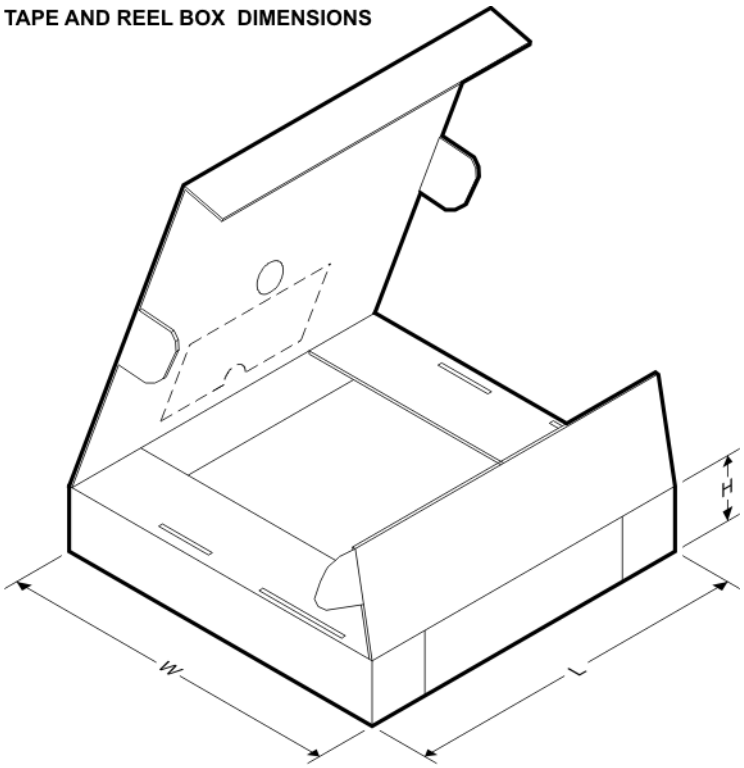
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53310RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS53310RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

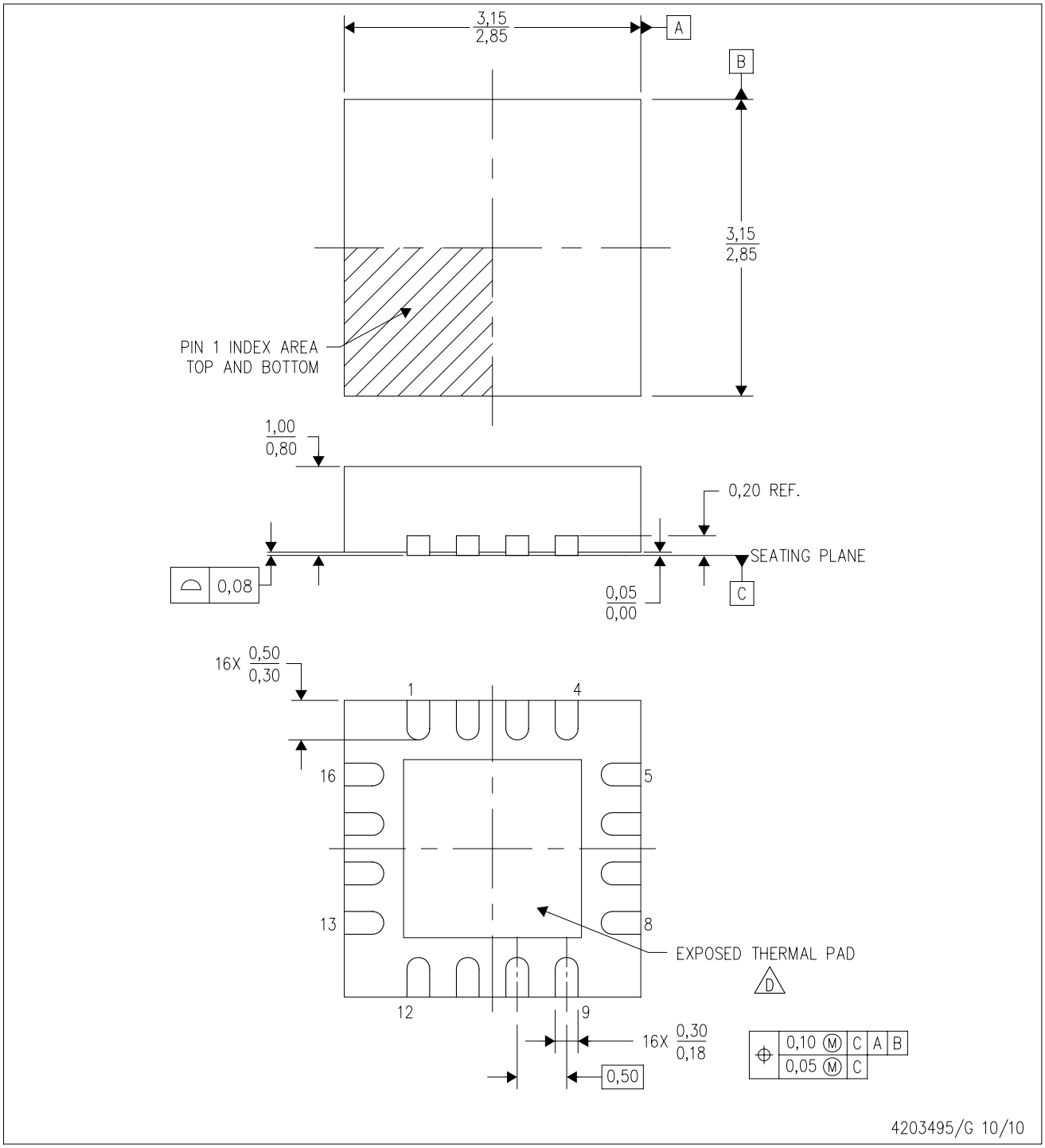
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53310RGTR	QFN	RGT	16	3000	346.0	346.0	29.0
TPS53310RGTT	QFN	RGT	16	250	190.5	212.7	31.8

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

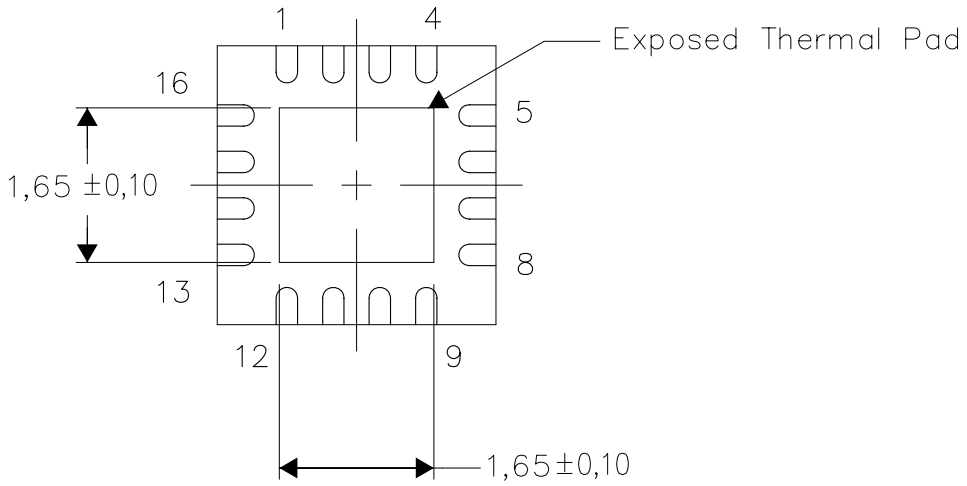
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



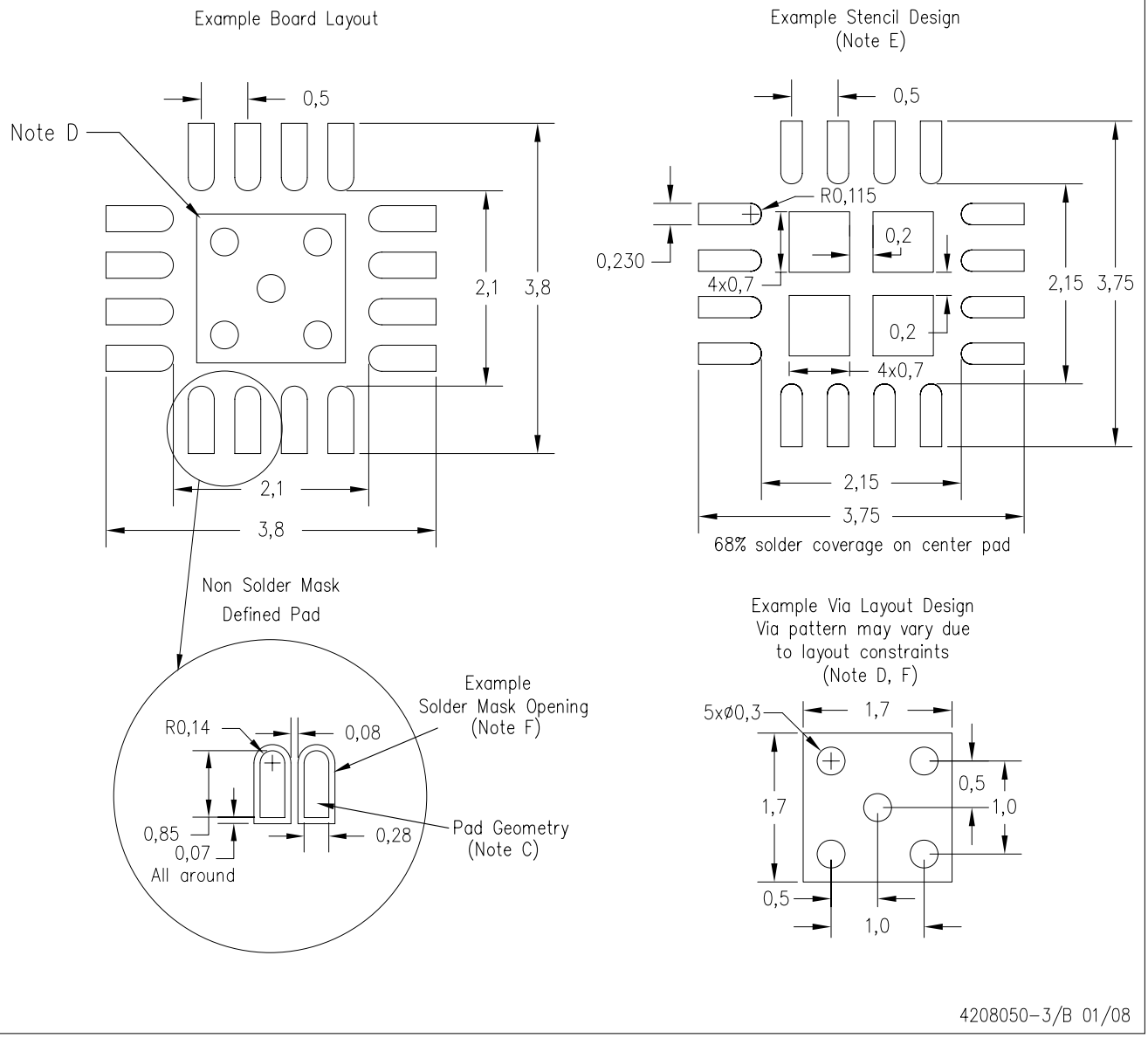
Bottom View

Exposed Thermal Pad Dimensions

4206349–7/0 11/10

NOTE: A. All linear dimensions are in millimeters

RGT (S–PQFP–N16)



4208050–3/B 01/08

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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