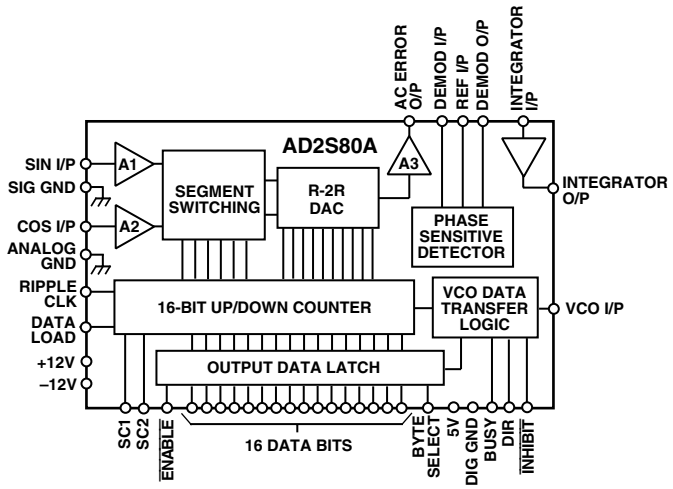
Variable Resolution, Monolithic Resolver-to-Digital Converter

AD2S80A

FEATURES
Monolithic (BiMOS II) Tracking R/D Converter
40-Lead DIP Package
44-Terminal LCC Package
10-,12-,14-, and 16-Bit Resolution Set by User
Ratiometric Conversion
Low Power Consumption: 300 mW Typ
Dynamic Performance Set by User
High Max Tracking Rate 1040 RPS (10 Bits)
Velocity Output
Industrial Temperature Range Versions
Military Temperature Range Versions
ESD Class 2 Protection (2,000 V Min)
/883 B Parts Available

APPLICATIONS
DC Brushless and AC Motor Control
Process Control
Numerical Control of Machine Tools
Robotics
Axis Control
Military Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S80A is a monolithic 10-, 12-, 14-, or 16-bit tracking resolver-to-digital converter contained in a 40-lead DIP or 44-terminal LCC ceramic package. It is manufactured on a BiMOS II process that combines the advantages of CMOS logic and bipolar high accuracy linear circuits on the same chip.

The converter allows users to *select their own resolution and dynamic performance with external components*. This allows the users great flexibility in defining the converter that best suits their system requirements. The converter allows users to select the resolution to be 10, 12, 14, or 16 bits and to track resolver signals rotating at up to 1040 revs per second (62,400 rpm) when set to 10-bit resolution.

The AD2S80A converts resolver format input signals into a parallel natural binary digital word using a ratiometric tracking conversion method. This ensures high-noise immunity and tolerance of lead length when the converter is remote from the resolver.

The 10-, 12-, 14- or 16-bit output word is in a three-state digital logic available in 2 bytes on the 16 output data lines. BYTE SELECT, $\overline{\text{ENABLE}}$ and $\overline{\text{INHIBIT}}$ pins ensure easy data transfer to 8- and 16-bit data buses, and outputs are provided to allow for cycle or pitch counting in external counters.

An analog signal proportional to velocity is also available and can be used to replace a tachogenerator.

The AD2S80A operates over 50 Hz to 20,000 Hz reference frequency.

PRODUCT HIGHLIGHTS

Monolithic. A one chip solution reduces the package size required and increases the reliability.

Resolution Set by User. Two control pins are used to select the resolution of the AD2S80A to be 10, 12, 14, or 16 bits allowing the user to use the AD2S80A with the optimum resolution for each application.

Ratiometric Tracking Conversion. Conversion technique provides continuous output position data without conversion delay and is insensitive to absolute signal levels. It also provides good noise immunity and tolerance to harmonic distortion on the reference and input signals.

Dynamic Performance Set by the User. By selecting external resistor and capacitor values the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The external components required are all low cost preferred value resistors and capacitors, and the component values are easy to select using the simple instructions given.

Velocity Output. An analog signal proportional to velocity is available and is linear to typically one percent. This can be used in place of a velocity transducer in many applications to provide loop stabilization in servo controls and velocity feedback data.

Low Power Consumption. Typically only 300 mW.

Military Product. The AD2S80A is available processed in accordance with MIL-STD-883B, Class B.

MODELS AVAILABLE

Information on the models available is given in the section "Ordering Information."

REV. B

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AD2S80A–SPECIFICATIONS (typical at 25°C unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
SIGNAL INPUTS					
Frequency		50		20,000	Hz
Voltage Level		1.8	2.0	2.2	V rms
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
Maximum Voltage				8	V pk
REFERENCE INPUT					
Frequency		50		20,000	Hz
Voltage Level		1.0		8.0	V pk
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
CONTROL DYNAMICS					
Repeatability				1	LSB
Allowable Phase Shift	(Signals to Reference)	–10		+10	Degrees
Tracking Rate	10 Bits			1040	rps
	12 Bits			260	rps
	14 Bits			65	rps
	16 Bits			16.25	rps
Bandwidth[1]	User Selectable				
ACCURACY					
Angular Accuracy	A, J, S			**±8 +1 LSB**	arc min
	B, K, T			**±4 +1 LSB**	arc min
	L, U			**±2 +1 LSB**	arc min
Monotonicity	Guaranteed Monotonic				
Missing Codes (16-Bit Resolution)	A, B, J, K, S, T			**4**	Codes
	L, U			**1**	Code
VELOCITY SIGNAL					
Linearity	Over Full Range		±1	**±3**	% FSD
Reversion Error			±1	±2	% FSD
DC Zero Offset[2]				**6**	mV
DC Zero Offset Tempco			–22		µV/°C
Gain Scaling Accuracy				±10	% FSD
Output Voltage	1 mA Load	±8	±9	±10.5	V
Dynamic Ripple	Mean Value			1.5	% rms O/P
Output Load				1.0	kΩ
INPUT/OUTPUT PROTECTION					
Analog Inputs	Overvoltage Protection		±8		V
Analog Outputs	Short Circuit O/P Protection	±5.6	±8	±10.4	mA
DIGITAL POSITION					
Resolution	10, 12, 14, and 16				
Output Format	Bidirectional Natural Binary				
Load				3	LSTTL
$\overline{\text{INHIBIT}}$[3]					
Sense	Logic LO to Inhibit				
Time to Stable Data				600	ns
$\overline{\text{ENABLE}}$[3]	Logic LO Enables Position Output. Logic HI Outputs in				
$\overline{\text{ENABLE}}$ Time	High Impedance State	35		110	ns
BYTE SELECT[3]					
Sense	MS Byte DB1–DB8, LS Byte DB9–DB16				
LOGIC LO	LS Byte DB1–DB8, LS Byte DB9–DB16				
Time to Data Available		60		140	ns
SHORT CYCLE INPUTS	Internally Pulled High (100 kΩ) to $+V_S$				
SC1 SC2					
0 0	10 Bit				
0 1	12 Bit				
1 0	14 Bit				
1 1	16 Bit				

Parameter	Conditions	Min	Typ	Max	Unit
DATA LOAD					
Sense	Internally Pulled High (100 kΩ) to V_S. Logic LO Allows Data to be Loaded into the Counters from the Data Lines		150	300	ns
BUSY[3]					
Sense	Logic HI When Position O/P Changing				
Width		**200**		**600**	ns
Load	Use Additional Pull-Up			1	LSTTL
DIRECTION[3]					
Sense	Logic HI Counting Up Logic LO Counting Down				
Max Load				3	LSTTL
RIPPLE CLOCK[3]					
Sense	Logic HI All 1s to All 0s All 0s to All 1s				
Width	Dependent on Input Velocity	**300**			
Reset	Before Next Busy				
Load				3	LSTTL
DIGITAL INPUTS					
High Voltage, V_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 10.8$ V, $V_L = 5.0$ V	**2.0**			V
Low Voltage, V_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 13.2$ V, $V_L = 5.0$ V			**0.8**	V
DIGITAL INPUTS					
High Current, I_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16 $\pm V_S = \pm 13.2$ V , $V_L = 5.5$ V			**±100**	µA
Low Current, I_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 13.2$ V, $V_L = 5.5$ V			**±100**	µA
DIGITAL INPUTS					
Low Voltage, V_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, Data Load $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			**1.0**	V
Low Current, I_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, Data Load $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			**–400**	µA
DIGITAL OUTPUTS					
High Voltage, V_{OH}	DB1–DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 4.5$ V $I_{OH} = 100$ µA	**2.4**			V
Low Voltage, V_{OL}	DB1–DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $I_{OL} = 1.2$ mA			**0.4**	V
THREE-STATE LEAKAGE	DB1–DB16 Only				
Current I_L	$\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OL} = 0$ V			±100	µA
	$\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OH} = 5.0$ V			±100	µA

NOTES
[1]Refer to small signal bandwidth.
[2]Output offset dependent on value for R6.
[3]Refer to timing diagram.
Specifications subject to change without notice.
All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test.

AD2S80A–SPECIFICATIONS (typical at 25°C unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
RATIO MULTIPLIER					
AC Error Output Scaling	10 Bit		**177.6**		mV/Bit
	12 Bit		**44.4**		mV/Bit
	14 Bit		**11.1**		mV/Bit
	16 Bit		**2.775**		mV/Bit
PHASE SENSITIVE DETECTOR					
Output Offset Voltage				**12**	mV
Gain					
In Phase	w.r.t. REF	–0.882	–0.9	–0.918	V rms/V dc
In Quadrature	w.r.t. REF			±0.02	V rms/V dc
Input Bias Current			60	**150**	nA
Input Impedance		1			MΩ
Input Voltage				±8	V
INTEGRATOR					
Open-Loop Gain	At 10 kHz	57		63	dB
Dead Zone Current (Hysteresis)			100		nA/LSB
Input Offset Voltage			1	5	mV
Input Bias Current			60	150	nA
Output Voltage Range	$\pm V_S$ = ±10.8 V dc	±7			V
VCO					
Maximum Rate	$\pm V_S$ = ±12 V dc			**1.1**	MHz
VCO Rate	Positive Direction	**7.1**	**7.9**	**8.7**	kHz/μA
	Negative Direction	**7.1**	**7.9**	**8.7**	kHz/μA
VCO Power Supply Sensitivity					
Increase	$+V_S$		+0.5		%/V
	$-V_S$		–8.0		%/V
Decrease	$+V_S$		–8.0		%/V
	$-V_S$		+2.0		%/V
Input Offset Voltage			1	5	mV
Input Bias Current			70	**380**	nA
Input Bias Current Tempco			–1.22		nA/°C
Input Voltage Range				±8	V
Linearity of Absolute Rate					
Full Range				**<2**	% FSD
Over 0% to 50% of Full Range				**<1**	% FSD
Reversion Error				1.5	% FSD
Sensitivity of Reversion Error to Symmetry of Power Supplies			±8		%/V of Asymmetry
POWER SUPPLIES					
Voltage Levels					
$+V_S$		**+10.8**		**+13.2**	V
$-V_S$		**–10.8**		**–13.2**	V
$+V_L$		**+5**		**+13.2**	V
Current					
$\pm I_S$	$\pm V_S$ @ ±12 V		**±12**	**±23**	mA
$\pm I_S$	$\pm V_S$ @ 13.2 V		**±19**	**±30**	mA
$\pm I_L$	$+V_L$ @ ±5.0 V		**±0.5**	**±1.5**	mA

Specification subject to change without notice.
All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD2S80A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage ($+V_S$, $-V_S$) . . . . . ±12 V dc ± 10%
Power Supply Voltage V_L . . . . . 5 V dc ± 10%
Analog Input Voltage (SIN and COS) . . . . . 2 V rms ± 10%
Analog Input Voltage (REF) . . . . . 1 V to 8 V peak
Signal and Reference Harmonic Distortion . . . . . 10% (max)
Phase Shift Between Signal and Reference . . . ±10 Degrees (max)
Ambient Operating Temperature
  Commercial (JD, KD, LD) . . . . . 0°C to 70°C
  Industrial (AD, BD) . . . . . –40°C to +85°C
  Extended (SD, SE, TD, TE, UD, UE) . . . –55°C to +125°C

ABSOLUTE MAXIMUM RATINGS[1] (with respect to GND)

$+V_S$[2] . . . . . +14 V dc
$-V_S$ . . . . . –14 V dc
$+V_L$ . . . . . V_S
Reference . . . . . 14 V to $-V_S$
SIN . . . . . 14 V to $-V_S$
COS . . . . . 14 V to $-V_S$
Any Logical Input . . . . . –0.4 V dc to $+V_L$ dc
Demodulator Input . . . . . 14 V to $-V_S$
Integrator Input . . . . . 14 V to $-V_S$
VCO Input . . . . . 14 V to $-V_S$
Power Dissipation . . . . . 860 mW
Operating Temperature
  Commercial (JD, KD, LD) . . . . . 0°C to 70°C
  Industrial (AD, BD) . . . . . –40°C to +85°C
  Extended (SD, SE, TD, TE, UD, UE) . . . –55°C to +125°C
θ_{JC}[3] (40-Lead DIP 883 Parts Only) . . . . . 11°C/W
θ_{JC}[3] (44-Terminal LCC 883 Parts Only) . . . . . 10°C/W
Storage Temperature (All Grades) . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

CAUTION NOTES:

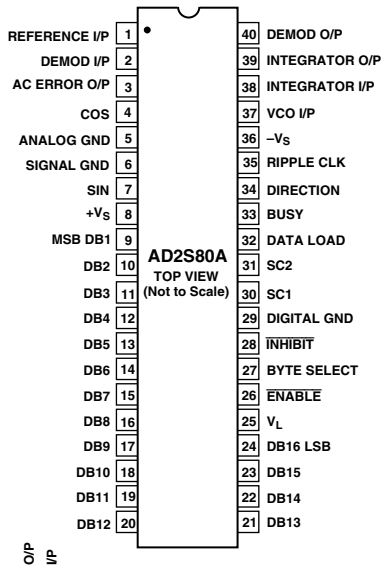
[1]Absolute Maximum Ratings are those values beyond which damage to the device may occur.
[2]Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
[3]With reference to Appendix C of MIL-M-38510.

Bit Weight Table

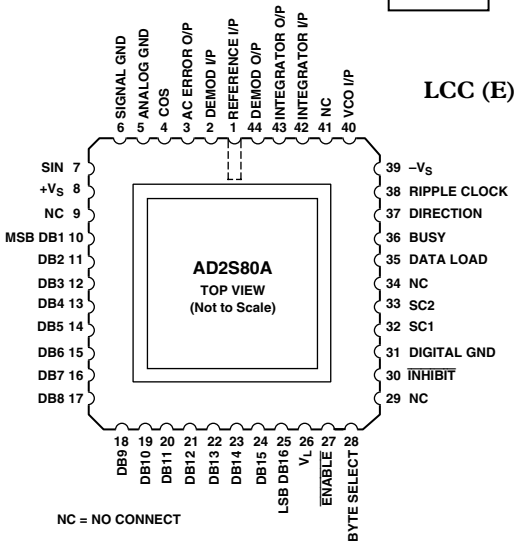
Binary Bits (N)	Resolution (2^N)	Degrees /Bit	Minutes /Bit	Seconds /Bit
0	1	360.0	21600.0	1296000.0
1	2	180.0	10800.0	648000.0
2	4	90.0	5400.0	324000.0
3	8	45.0	2700.0	162000.0
4	16	22.5	1350.0	81000.0
5	32	11.25	675.0	40500.0
6	64	5.625	337.5	20250.0
7	128	2.8125	168.75	10125.0
8	256	1.40625	84.375	5062.5
9	512	0.703125	42.1875	2531.25
10	1024	0.3515625	21.09375	1265.625
11	2048	0.1757813	10.546875	632.8125
12	4096	0.0878906	5.273438	316.40625
13	8192	0.0439453	2.636719	158.20313
14	16384	0.0219727	1.318359	79.10156
15	32768	0.0109836	0.659180	39.55078
16	65536	0.0054932	0.329590	19.77539
17	131072	0.0027466	0.164795	9.88770
18	262144	0.0013733	0.082397	4.94385

PIN CONFIGURATIONS

DIP (D) Package



LCC (E) Package



PIN DESIGNATIONS

MNEMONIC	DESCRIPTION
REFERENCE I/P	REFERENCE SIGNAL INPUT
DEMOD I/P	DEMODULATOR INPUT
AC ERROR O/P	RATIO MULTIPLIER OUTPUT
COS	COSINE INPUT
ANALOG GROUND	POWER GROUND
SIGNAL GROUND	RESOLVER SIGNAL GROUND
SIN	SINE INPUT
$+V_S$	POSITIVE POWER SUPPLY
DB1–DB16	PARALLEL OUTPUT DATA
V_L	LOGIC POWER SUPPLY
$\overline{\text{ENABLE}}$	LOGIC HI-OUTPUT DATA IN HIGH IMPEDANCE STATE, LOGIC LO PRESENTS DATA TO THE OUTPUT LATCHES
BYTE SELECT	LOGIC HI-MOST SIGNIFICANT BYTE TO DB1–DB8 LOGIC LO-LEAST SIGNIFICANT BYTE TO DB1–DB8
$\overline{\text{INHIBIT}}$	LOGIC LO INHIBITS DATA TRANSFER TO OUTPUT LATCHES
DIGITAL GROUND	DIGITAL GROUND
SC1–SC2	SELECT CONVERTER RESOLUTION
DATA LOAD	LOGIC LO DB1–DB16 INPUTS LOGIC HI DB1–D16 OUTPUTS
BUSY	CONVERTER BUSY, DATA NOT VALID WHILE BUSY HI
DIRECTION	LOGIC STATE DEFINES DIRECTION OF INPUT SIGNAL ROTATION
RIPPLE CLOCK	POSITIVE PULSE WHEN CONVERTER OUTPUT CHANGES FROM 1S TO ALL 0S OR VICE VERSA
$-V_S$	NEGATIVE POWER SUPPLY
VCO I/P	VCO INPUT
INTEGRATOR I/P	INTEGRATOR INPUT
INTEGRATOR O/P	INTEGRATOR OUTPUT
DEMOD O/P	DEMODULATOR OUTPUT

CONNECTING THE CONVERTER

The power supply voltages connected to $+V_S$ and $-V_S$ pins should be +12 V dc and –12 V dc and must not be reversed. The voltage applied to V_L can be 5 V dc to $+V_S$.

It is recommended that the decoupling capacitors are connected in parallel between the power lines $+V_S$, $-V_S$ and ANALOG GROUND adjacent to the converter. Recommended values are 100 nF (ceramic) and 10 µF (tantalum). Also capacitors of 100 nF and 10 µF should be connected between $+V_L$ and DIGITAL GROUND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter.

The resolver connections should be made to the SIN and COS inputs, REFERENCE INPUT and SIGNAL GROUND as shown in Figure 7 and described in section "CONNECTING THE RESOLVER."

The two signal ground wires from the resolver should be joined at the SIGNAL GROUND pin of the converter to minimize the coupling between the sine and cosine signals. For this reason it is also recommended that the resolver is connected using individually screened twisted pair cables with the sine, cosine and reference signals twisted separately.

SIGNAL GROUND and ANALOG GROUND are connected internally. ANALOG GROUND and DIGITAL GROUND must be connected externally.

The external components required should be connected as shown in Figure 1.

CONVERTER RESOLUTION

Two major areas of the AD2S80A specification can be selected by the user to optimize the total system performance. The resolution of the digital output is set by the logic state of the inputs SC1 and SC2 to be 10, 12, 14, or 16 bits; and the dynamic characteristics of bandwidth and tracking rate are selected by the choice of external components.

The choice of the resolution will affect the values of R4 and R6 which scale the inputs to the integrator and the VCO respectively (see section COMPONENT SELECTION). If the resolution is changed, then new values of R4 and R6 must be switched into the circuit.

Note: When changing resolution under dynamic conditions, do it when the BUSY is low, i.e., when Data is not changing.

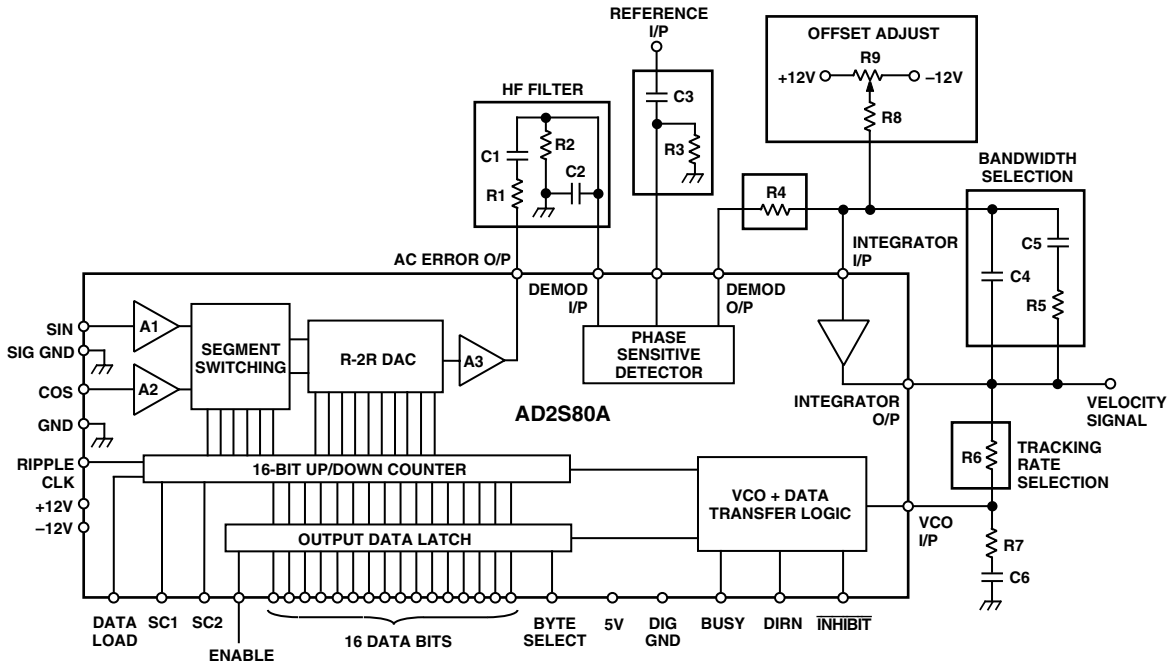


Figure 1. AD2S80A Connection Diagram

CONVERTER OPERATION

When connected in a circuit such as shown in Figure 1 the AD2S80A operates as a tracking resolver-to-digital converter and forms a Type 2 closed-loop system. The output will automatically follow the input for speeds up to the selected maximum tracking rate. No convert command is necessary as the conversion is automatically initiated by each LSB increment, or decrement, of the input. Each LSB change of the converter initiates a BUSY pulse.

The AD2S80A is remarkably tolerant of input amplitude and frequency variation because the conversion depends only on the ratio of the input signals. Consequently there is no need for accurate, stable oscillator to produce the reference signal. The inclusion of the phase sensitive detector in the conversion loop ensures a high immunity to signals that are not coherent or are in quadrature with the reference signal.

SIGNAL CONDITIONING

The amplitude of the SINE and COSINE signal inputs should be maintained within 10% of the nominal values if full performance is required from the velocity signal.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a loss in accuracy due to internal overload. Reducing levels will result in a steady decline in accuracy. With the signal levels at 50% of the correct value, the angular error will increase to an amount equivalent to 1.3 LSB. At this level the repeatability will also degrade to 2 LSB and the dynamic response will also change, since the dynamic characteristics are proportional to the signal level.

The AD2S80A will not be damaged if the signal inputs are applied to the converter without the power supplies and/or the reference.

REFERENCE INPUT

The amplitude of the reference signal applied to the converter's input is not critical, but care should be taken to ensure it is kept within the recommended operating limits.

The AD2S80A will not be damaged if the reference is supplied to the converter without the power supplies and/or the signal inputs.

HARMONIC DISTORTION

The amount of harmonic distortion allowable on the signal and reference lines is 10%.

Square waveforms can be used but the input levels should be adjusted so that the average value is 1.9 V rms. (For example, a square wave should be 1.9 V peak.) Triangular and sawtooth waveforms should have a amplitude of 2 V rms.

Note: The figure specified of 10% harmonic distortion is for calibration convenience only.

POSITION OUTPUT

The resolver shaft position is represented at the converter output by a natural binary parallel digital word. As the digital position output of the converter passes through the major carries, i.e., all "1s" to all "0s" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The direction of input rotation is indicated by the DIRECTION (DIR) logic output. This direction data is always valid in advance of a RIPPLE CLOCK pulse and, as it is internally latched, only changing state (1 LSB min change) with a corresponding change in direction.

Both the RIPPLE CLOCK pulse and the DIRECTION data are unaffected by the application of the $\overline{\text{INHIBIT}}$. The static positional accuracy quoted is the worst case error that can occur over the full operating temperature excluding the effects of offset signals at the INTEGRATOR INPUT (which can be trimmed out—see Figure 1), and with the following conditions: input signal amplitudes are within 10% of the nominal; phase shift between signal and reference is less than 10 degrees.

These operating conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice, the AD2S80A can be used well outside these operating conditions providing the above points are observed.

VELOCITY SIGNAL

The tracking converter technique generates an internal signal at the output of the integrator (the INTEGRATOR OUTPUT pin) that is proportional to the rate of change of the input angle. This is a dc analog output referred to as the VELOCITY signal.

In many applications it is possible to use the velocity signal of the AD2S80A to replace a conventional tachogenerator.

DC ERROR SIGNAL

The signal at the output of the phase sensitive detector (DEMODULATOR OUTPUT) is the signal to be nulled by the tracking loop and is, therefore, proportional to the error between the input angle and the output digital angle. This is the dc error of the converter; and as the converter is a Type 2 servo loop, it will increase if the output fails to track the input for any reason. It is an indication that the input has exceeded the maximum tracking rate of the converter or, due to some internal malfunction, the converter is unable to reach a null. By connecting two external comparators, this voltage can be used as a "built-in-test."

COMPONENT SELECTION

The following instructions describe how to select the external components for the converter in order to achieve the required bandwidth and tracking rate. In all cases the nearest "preferred value" component should be used, and a 5% tolerance will not degrade the overall performance of the converter. Care should be taken that the resistors and capacitors will function over the required operating temperature range. The components should be connected as shown in Figure 1.

PG compatible software is available to help users select the optimum component values for the AD2S80A, and display the transfer gain, phase and small step response.

For more detailed information and explanation, see section "CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE."

1. HF Filter (R1, R2, C1, C2)
   The function of the HF filter is to remove any dc offset and to reduce the amount of noise present on the signal inputs to the AD2S80A, reaching the Phase Sensitive Detector and affecting the outputs. R1 and C2 may be omitted—in which case R2 = R3 and C1 = C3, calculated below—but their use is particularly recommended if noise from switch mode power supplies and brushless motor drive is present.

   Values should be chosen so that

$$C1 = C2 = 15\ k\Omega \le R1 = R2 \le 56\ k\Omega$$

$$C1 = C2 = \frac{1}{2\pi\ R1\ f_{REF}}$$

   and f_{REF} = Reference frequency (Hz)

   This filter gives an attenuation of three times at the input to the phase sensitive detector.

2. Gain Scaling Resistor (R4)
   If R1, C2 are used:

$$R4 = \frac{E_{DC}}{100 \times 10^{-9}} \times \frac{1}{3}\ \Omega$$

   where 100×10^{-9} = current/LSB
   If R1, C2 are not used:

$$R4 = \frac{E_{DC}}{100 \times 10^{-9}}\ \Omega$$

   where E_{DC} = 160×10^{-3} for 10 bits resolution
   = 40×10^{-3} for 12 bits
   = 10×10^{-3} for 14 bits
   = 2.5×10^{-3} for 16 bits
   = Scaling of the DC ERROR in volts

3. AC Coupling of Reference Input (R3, C3)
   Select R3 and C3 so that there is no significant phase shift at the reference frequency. That is,

$$R3 = 100\ k\Omega$$

$$C3 > \frac{1}{R3 \times f_{REF}}\ F$$

   with R3 in Ω.

4. Maximum Tracking Rate (R6)
   The VCO input resistor R6 sets the maximum tracking rate of the converter and hence the velocity scaling as at the max tracking rate, the velocity output will be 8 V.

   Decide on your maximum tracking rate, "T," in revolutions per second. Note that "T" must not exceed the maximum tracking rate or 1/16 of the reference frequency.

$$R6 = \frac{6.32 \times 10^{10}}{T \times n}\ \Omega$$

   where n = bits per revolution
   = 1,024 for 10 bits resolution
   = 4,096 for 12 bits
   = 16,384 for 14 bits
   = 65,536 for 16 bits

5. Closed-Loop Bandwidth Selection (C4, C5, R5)
   a. Choose the closed-loop bandwidth (f_{BW}) required ensuring that the ratio of reference frequency to bandwidth does not exceed the following guidelines:

Resolution	Ratio of Reference Frequency/Bandwidth
10	2.5 : 1
12	4 : 1
14	6 : 1
16	7.5 : 1

   Typical values may be 100 Hz for a 400 Hz reference frequency and 500 Hz to 1000 Hz for a 5 kHz reference frequency.

   b. Select C4 so that

$$C4 = \frac{21}{R6 \times f_{BW}{}^2}\ F$$

   with R6 in Ω and f_{BW}, in Hz selected above.

   c. C5 is given by

$$C5 = 5 \times C4$$

   d. R5 is given by

$$R5 = \frac{4}{2 \times \pi \times f_{BW} \times C5}\ \Omega$$

6. VCO Phase Compensation
   The following values of C6 and R7 should be fitted.

$$C6 = 470\ pF,\ R7 = 68\ \Omega$$

7. Offset Adjust
   Offsets and bias currents at the integrator input can cause an additional positional offset at the output of the converter of 1 arc minute typical, 5.3 arc minutes maximum. If this can be tolerated, then R8 and R9 can be omitted from the circuit.

   If fitted, the following values of R8 and R9 should be used:

$$R8 = 4.7\ M\Omega,\ R9 = 1\ M\Omega\ potentiometer$$

   To adjust the zero offset, ensure the resolver is disconnected and all the external components are fitted. Connect the COS pin to the REFERENCE INPUT and the SIN pin to the SIGNAL GROUND and with the power and reference applied, adjust the potentiometer to give all "0s" on the digital output bits.

   The potentiometer may be replaced with select on test resistors if preferred.

DATA TRANSFER

To transfer data the $\overline{\text{INHIBIT}}$ input should be used. The data will be valid 600 ns after the application of a logic "LO" to the $\overline{\text{INHIBIT}}$. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied and allows time for an active BUSY to clear. By using the $\overline{\text{ENABLE}}$ input the two bytes of data can be transferred after which the $\overline{\text{INHIBIT}}$ should be returned to a logic "HI" state to enable the output latches to be updated.

BUSY Output

The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses at TTL level. A BUSY pulse is initiated each time the input moves by the analog equivalent of one LSB and the internal counter is incremented or decremented.

$\overline{\text{INHIBIT}}$ Input

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and, therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

$\overline{\text{ENABLE}}$ Input

The $\overline{\text{ENABLE}}$ input determines the state of the output data. A logic "HI" maintains the output data pins in the high impedance condition, and the application of a logic "LO" presents the data in the latches to the output pins. The operation of the $\overline{\text{ENABLE}}$ has no effect on the conversion process.

BYTE SELECT Input

The BYTE SELECT input selects the byte of the position data to be presented at the data output DB1 to DB8. The least significant byte will be presented on data output DB9 to DB16 (with the $\overline{\text{ENABLE}}$ input taken to a logic "LO") regardless of the state of the BYTE SELECT pin. Note that when the AD2S80A is used with a resolution less than 16 bits the unused data lines are pulled to a logic "LO." A logic "HI" on the BYTE SELECT input will present the eight most significant data bits on data output DB1 and DB8. A logic "LO" will present the least significant byte on data outputs 1 to 8, i.e., data outputs 1 to 8 will duplicate data outputs 9 to 16.

The operation of the BYTE SELECT has no effect on the conversion process of the converter.

RIPPLE CLOCK

As the output of the converter passes through the major carry, i.e., all "1s" to all "0s" or the converse, a positive going edge on the RIPPLE CLOCK (RC) output is initiated indicating that a revolution, or a pitch, of the input has been completed.

The minimum pulse width of the ripple clock is 300 ns. RIPPLE CLOCK is normally set high before a BUSY pulse and resets before the next positive going edge of the next consecutive pulse.

The only exception to this is when DIR changes while the RIPPLE CLOCK is high. Resetting of the RIPPLE clock will only occur if the DIR remains stable for two consecutive positive BUSY pulse edges.

If the AD2S80A is being used in a pitch and revolution counting application, the ripple and busy will need to be gated to prevent false decrement or increment (see Figure 2).

RIPPLE CLOCK is unaffected by $\overline{\text{INHIBIT}}$.

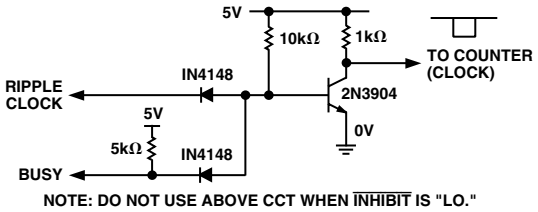
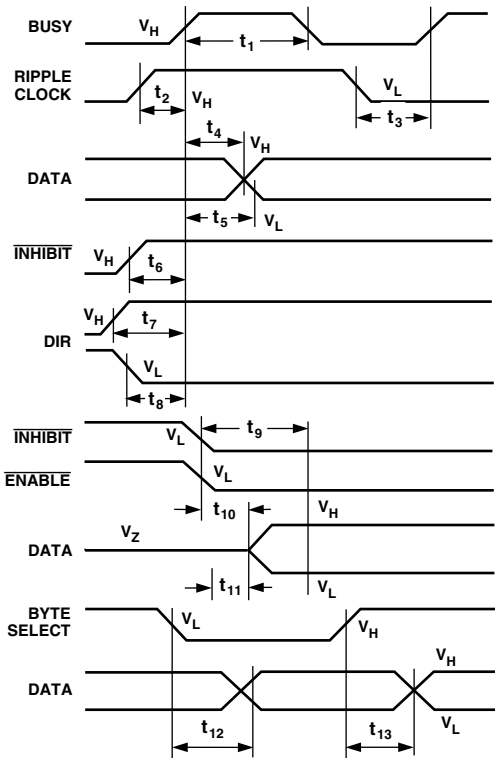


Figure 2. Diode Transistor Logic Nand Gate

DIRECTION Output

The DIRECTION (DIR) logic output indicates the direction of the input rotation. Any change in the state of DIR precedes the corresponding BUSY, DATA and RIPPLE CLOCK updates. DIR can be considered as an asynchronous output and can make multiple changes in state between two consecutive LSB update cycles. This corresponds to a change in input rotation direction but less than 1 LSB.

DIGITAL TIMING



PARAMETER	T_{MIN}	T_{MAX}	CONDITION
t_1	200	600	BUSY WIDTH V_H–V_H
t_2	10	25	RIPPLE CLOCK V_H TO BUSY V_H
t_3	470	580	RIPPLE CLOCK V_L TO NEXT BUSY V_H
t_4	16	45	BUSY V_H TO DATA V_H
t_5	3	25	BUSY V_H TO DATA V_L
t_6	70	140	$\overline{\text{INHIBIT}}$ V_H TO BUSY V_H
t_7	485	625	MIN DIR V_H TO BUSY V_H
t_8	515	670	MIN DIR V_H TO BUSY V_H
t_9	–	600	$\overline{\text{INHIBIT}}$ V_L TO DATA STABLE
t_{10}	40	110	$\overline{\text{ENABLE}}$ V_L TO DATA V_H
t_{11}	35	110	$\overline{\text{ENABLE}}$ V_L TO DATA V_L
t_{12}	60	140	BYTE SELECT V_L TO DATA STABLE
t_{13}	60	125	BYTE SELECT V_H TO DATA STABLE

CIRCUIT FUNCTIONS AND DYNAMIC PERFORMANCE

The AD2S80A allows the user greater flexibility in choosing the dynamic characteristics of the resolver-to-digital conversion to ensure the optimum system performance. The characteristics are set by the external components shown in Figure 1, and the section "COMPONENT SELECTION" explains how to select desired maximum tracking rate and bandwidth values. The following paragraphs explain in greater detail the circuit of the AD2S80A and the variations in the dynamic performance available to the user.

Loop Compensation

The AD2S80A (connected as shown in Figure 1) operates as a Type 2 tracking servo loop where the VCO/counter combination and Integrator perform the two integration functions inherent in a Type 2 loop.

Additional compensation in the form of a pole/zero pair is required to stabilize any Type 2 loop to avoid the loop gain characteristic crossing the 0 dB axis with 180° of additional phase lag, as shown in Figure 5.

This compensation is implemented by the integrator components (R4, C4, R5, C5).

The overall response of such a system is that of a unity gain second order low pass filter, with the angle of the resolver as the input and the digital position data as the output.

The AD2S80A does not have to be connected as tracking converter, parts of the circuit can be used independently. This is particularly true of the Ratio Multiplier which can be used as a control transformer (see Application Note).

A block diagram of the AD2S80A is given in Figure 3.

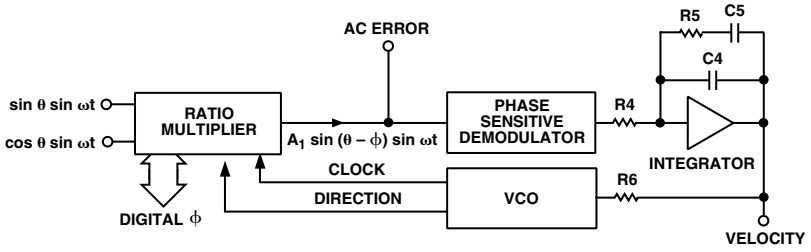


Figure 3. Functional Diagram

Ratio Multiplier

The ratio multiplier is the input section of the AD2S80A and compares the signal from the resolver input angle, θ, to the digital angle, ϕ, held in the counter. Any difference between these two angles results in an analog voltage at the AC ERROR OUTPUT. This circuit function has historically been called a "Control Transformer" as it was originally performed by an electromechanical device known by that name.

The AC ERROR signal is given by

$$A1 \sin(\theta - \phi) \sin \omega t$$

where $\omega = 2 \pi f_{REF}$

f_{REF} = reference frequency

A1, the gain of the ratio multiplier stage is 14.5.

So for 2 V rms inputs signals
AC ERROR output in volts/(bit of error)

$$= 2 \times \sin\left(\frac{360}{n}\right) \times A1$$

where n = bits per rev
= 1,024 for 10 bits resolution
= 4,096 for 12 bits
= 16,384 for 14 bits
= 65,536 for 16 bits

giving an AC ERROR output
= 178 mV/bit @ 10 bits resolution
= 44.5 mV/bit @ 12 bits
= 11.125 mV/bit @ 14 bits
= 2.78 mV/bit @ 16 bits

The ratio multiplier will work in exactly the same way whether the AD2S80A is connected as a tracking converter or as a control transformer, where data is preset into the counters using the DATA LOAD pin.

HF Filter

The AC ERROR OUTPUT may be fed to the PSD via a simple ac coupling network (R2, C1) to remove any dc offset at this point. Note, however, that the PSD of the AD2S80A is a wideband demodulator and is capable of aliasing HF noise down to within the loop bandwidth. This is most likely to happen where the resolver is situated in particularly noisy environments, and the user is advised to fit a simple HF filter R1, C2 prior to the phase sensitive demodulator.

The attenuation and frequency response of a filter will affect the loop gain and must be taken into account in deriving the loop transfer function. The suggested filter (R1, C1, R2, C2) is shown in Figure 1 and gives an attenuation at the reference frequency (f_{REF}) of 3 times at the input to the phase sensitive demodulator .

Values of components used in the filter must be chosen to ensure that the phase shift at f_{REF} is within the allowable signal to reference phase shift of the converter.

Phase Sensitive Demodulator

The phase sensitive demodulator is effectively ideal and develops a mean dc output at the DEMODULATOR OUTPUT pin of

$$\frac{\pm 2\sqrt{2}}{\pi} \times (DEMODULATOR\ \ INPUT\ rms\ voltage)$$

for sinusoidal signals in phase or antiphase with the reference (for a square wave the DEMODULATOR OUTPUT voltage will equal the DEMODULATOR INPUT). This provides a signal at the DEMODULATOR OUTPUT which is a dc level proportional to the positional error of the converter.

DC Error Scaling = 160 mV/bit (10 bits resolution)
= 40 mV/bit (12 bits resolution)
= 10 mV/bit (14 bits resolution)
= 2.5 mV/bit (16 bits resolution)

When the tracking loop is closed, this error is nulled to zero unless the converter input angle is accelerating.

Integrator

The integrator components (R4, C4, R5, C5) are external to the AD2S80A to allow the user to determine the optimum dynamic characteristics for any given application. The section "COMPONENT SELECTION" explains how to select components for a chosen bandwidth.

Since the output from the integrator is fed to the VCO INPUT, it is proportional to velocity (rate of change of output angle) and can be scaled by selection of R6, the VCO input resistor. This is explained in the section "VOLTAGE CONTROLLED OSCILLATOR (VCO)" below.

To prevent the converter from "flickering" (i.e., continually toggling by ±1 bit when the quantized digital angle, ϕ, is not an exact representation of the input angle, θ) feedback is internally applied from the VCO to the integrator input to ensure that the VCO will only update the counter when the error is greater than or equal to 1 LSB. In order to ensure that this feedback "hysteresis" is set to 1 LSB the input current to the integrator must be scaled to be 100 nA/bit. Therefore,

$$R4 = \frac{DC\ Error\ Scaling\ (mV/bit\ )}{100\ (nA/bit)}$$

Any offset at the input of the integrator will affect the accuracy of the conversion as it will be treated as an error signal and offset the digital output. One LSB of extra error will be added for each 100 nA of input bias current. The method of adjusting out this offset is given in the section "COMPONENT SELECTION."

Voltage Controlled Oscillator (VCO)

The VCO is essentially a simple integrator feeding a pair of dc level comparators. Whenever the integrator output reaches one of the comparator threshold voltages, a fixed charge is injected into the integrator input to balance the input current. At the same time the counter is clocking either up or down, dependent on the polarity of the input current. In this way the counter is clocked at a rate proportional to the magnitude of the input current of the VCO.

During the reset period the input continues to be integrated, the reset period is constant at 400 ns.

The VCO rate is fixed for a given input current by the VCO scaling factor:

$$= 7.9\ kHz/\mu A$$

The tracking rate in rps per μA of VCO input current can be found by dividing the VCO scaling factor by the number of LSB changes per rev (i.e., 4096 for 12-bit resolution).

The input resistor R6 determines the scaling between the converter velocity signal voltage at the INTEGRATOR OUTPUT pin and the VCO input current. Thus to achieve a 5 V output at 100 rps (6000 rpm) and 12-bit resolution the VCO input current must be:

$$(100 \times 4096)/(7900) = 51.8\ \mu A$$

Thus, R6 would be set to: $5/(51.8 \times 10^{-6}) = 96\ k\Omega$

The velocity offset voltage depends on the VCO input resistor, R6, and the VCO bias current and is given by

$$Velocity\ Offset\ Voltage = R6 \times (VCO\ bias\ current)$$

The temperature coefficient of this offset is given by

$$Velocity\ Offset\ Tempco = R6 \times (VCO\ bias\ current\ tempco)$$

where the VCO bias current tempco is typically –1.22 nA/°C.

The maximum recommended rate for the VCO is 1.1 MHz which sets the maximum possible tracking rate.

Since the minimum voltage swing available at the integrator output is ±8 V, this implies that the minimum value for R6 is 57 kΩ. As

$$Max\ Current = \frac{1.1 \times 10^6}{7.9 \times 10^3} = 139\ \mu A$$

$$Min\ Value\ R6 = \frac{8}{139 \times 10^{-6}} = 57\ k\Omega$$

Transfer Function

By selecting components using the method outlined in the section "Component Selection," the converter will have a critically damped time response and maximum phase margin. The Closed-Loop Transfer Function is given by:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{14\,(1+s_N)}{(s_N+2.4)(s_N^{\,2}+3.4\,s_N+5.8)}$$

where, s_N, the normalized frequency variable is:

$$s_N = \frac{2}{\pi}\ \frac{s}{f_{BW}}$$

and f_{BW} is the closed-loop 3 dB bandwidth (selected by the choice of external components).

The acceleration K_A, is given approximately by

$$K_A = 6 \times (f_{BW})^2\ \sec^{-2}$$

The normalized gain and phase diagrams are given in Figures 4 and 5.

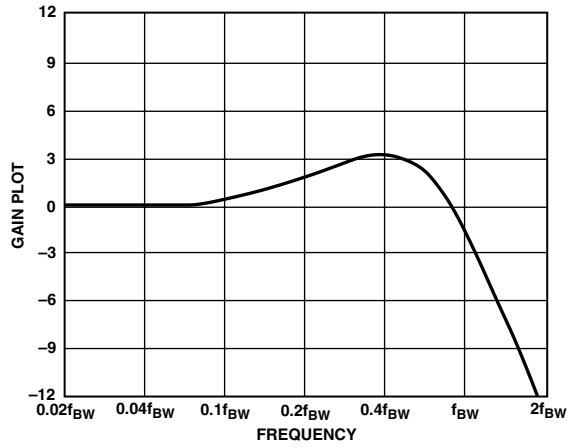


Figure 4. AD2S80A Gain Plot

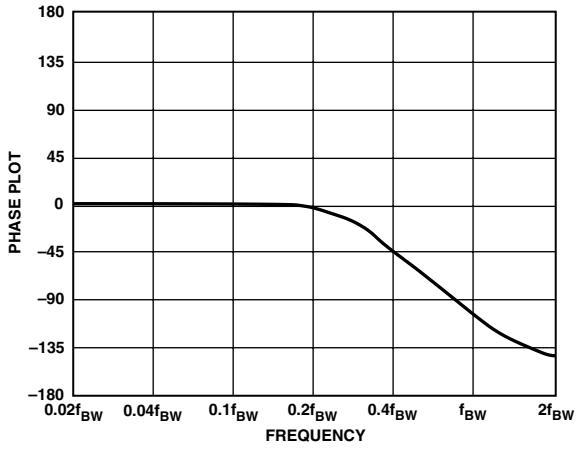


Figure 5. AD2S80A Phase Plot

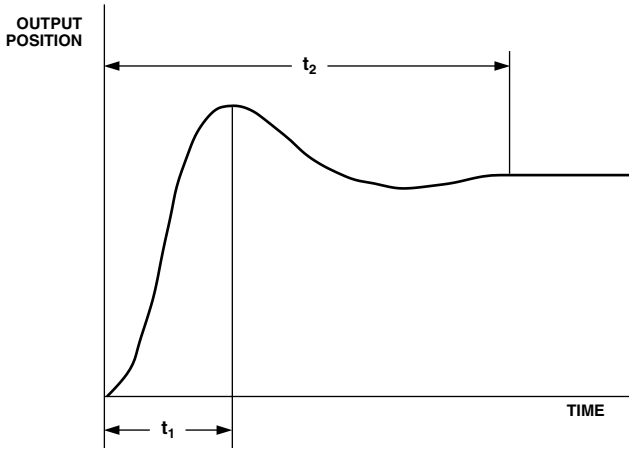


Figure 6. AD2S80A Small Step Response

The small signal step response is shown in Figure 6. The time from the step to the first peak is t_1 and the t_2 is the time from the step until the converter is settled to 1 LSB. The times t_1 and t_2 are given approximately by

$$t_1 = \frac{1}{f_{BW}}$$

$$t_2 = \frac{5}{f_{BW}} \times \frac{R}{12}$$

where R = resolution, i.e., 10, 12, 14, or 16.

The large signal step response (for steps greater than 5 degrees) applies when the error voltage exceeds the linear range of the converter.

Typically the converter will take 3 times longer to reach the first peak for a 179 degrees step.

In response to a velocity step, the velocity output will exhibit the same time response characteristics as outlined above for the position output.

ACCELERATION ERROR

A tracking converter employing a Type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_A of the converter.

$$K_A = \frac{Input\ \ Acceleration}{Error\ in\ Output\ \ Angle}$$

The numerator and denominator must have consistent angular units. For example if K_A is in sec^{-2}, then the input acceleration may be specified in degrees/sec^2 and the error output in degrees. Angular measurement may also be specified using radians, minutes of arc, LSBs, etc.

K_A does not define maximum input acceleration, only the error due to it's acceleration. The maximum acceleration allowable before the converter loses track is dependent on the angular accuracy requirements of the system.

$$Angular\ Accuracy \times K_A = Degrees/sec^2$$

K_A can be used to predict the output position error for a given input acceleration. For example for an acceleration of 100 revs/sec^2, $K_A = 2.7 \times 10^6$ sec^{-2} and 12-bit resolution.

$$Error\ in\ LSBs = \frac{Input\ acceleration\ [LSB/sec^2]}{K_A[\sec^{-2}]}$$

$$= \frac{100\ [rev/sec^2] \times 2^{12}}{2.7 \times 10^6} = 0.15\ LSBs\ or\ 47.5\ seconds\ of\ arc$$

To determine the value of K_A based on the passive components used to define the dynamics of the converter the following should be used.

$$K_A = \frac{4.04 \times 10^{11}}{2^n \bullet R6 \bullet R4 \bullet (C4 + C5)}$$

Where n = resolution of the converter.
R4, R6 in ohms
C5, C4 in farads

SOURCES OF ERRORS

Integrator Offset

Additional inaccuracies in the conversion of the resolver signals will result from an offset at the input to the integrator as it will be treated as an error signal. This error will typically be 1 arc minute over the operating temperature range.

A description of how to adjust from zero offset is given in the section "COMPONENT SELECTION" and the circuit required is shown in Figure 1.

Differential Phase Shift

Phase shift between the sine and cosine signals from the resolver is known as differential phase shift and can cause static error. Some differential phase shift will be present on all resolvers as a result of coupling. A small resolver residual voltage (quadrature voltage) indicates a small differential phase shift. Additional phase shift can be introduced if the sine channel wires and the cosine channel wires are treated differently. For instance, different cable lengths or different loads could cause differential phase shift.

The additional error caused by differential phase shift on the input signals approximates to

$$Error = 0.53\ a \times b\ arc\ minutes$$

where a = differential phase shift (degrees).
b = signal to reference phase shift (degrees).

This error can be minimized by choosing a resolver with a small residual voltage, ensuring that the sine and cosine signals are handled identically and removing the reference phase shift (see section "CONNECTING THE RESOLVER"). By taking these precautions the extra error can be made insignificant.

Under static operating conditions phase shift between the reference and the signal lines alone will not theoretically affect the converter's static accuracy.

However, most resolvers exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{Shaft\ Speed\ (rps) \times Phase\ Shift\ (Degrees)}{Reference\ Frequency}$$

For example, for a phase shift of 20 degrees, a shaft rotation of 22 rps and a reference frequency of 5 kHz, the converter will exhibit an additional error of:

$$\frac{22 \times 20}{5000}\ 0.088\ Degrees$$

This effect can be eliminated by placing a phase shift in the reference to the converter equivalent to the phase shift in the resolver (see section "CONNECTING THE RESOLVER").

Note: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.

VELOCITY ERRORS

The signal at the INTEGRATOR OUTPUT pin relative to the ANALOG GROUND pin is an analog voltage proportional to the rate of change of the input angle. This signal can be used to stabilize servo loops or in the place of a velocity transducer. Although the conversion loop of the AD2S80A includes a digital section there is an additional analog feedback loop around the velocity signal. This ensures against flicker in the digital positional output in both dynamic and static states.

A better quality velocity signal will be achieved if the following points are considered:

1. Protection.
   The velocity signal should be buffered before use.
2. Reversion error.[1]
   The reversion error can be nulled by varying one supply rail relative to the other.
3. Ripple and Noise.
   Noise on the input signals to the converter is the major cause of noise on the velocity signal. This can be reduced to a minimum if the following precautions are taken:

   The resolver is connected to the converter using separate twisted pair cable for the sine, cosine and reference signals.

   Care is taken to reduce the external noise wherever possible.

   An HF filter is fltted before the Phase Sensitive Demodulator (as described in the section HF FILTER).

   A resolver is chosen that has low residual voltage, i.e., a small signal in quadrature with the reference.

   Components are selected to operate the AD2S80A with the lowest acceptable bandwidth.

   Feedthrough of the reference frequency should be removed by a filter on the velocity signal.

   Maintenance of the input signal voltages at 2 V rms will prevent LSB flicker at the positional output. The analog feedback or hysteresis employed around the VCO and the intergrator is a function of the input signal levels (see section "INTEGRATOR") .

Following the preceding precautions will allow the user to use the velocity signal in very noisy environments, for example, PWM motor drive applications. Resolver/converter error curves may exhibit apparent acceleration/deceleration at a constant velocity. This results in ripple on the velocity signal of frequency twice the input rotation.

[1]Reversion error, or side-to-side nonlinearity, is a result of differences in the up and down rates of the VCO.

CONNECTING THE RESOLVER

The recommended connection circuit is shown in Figure 7.

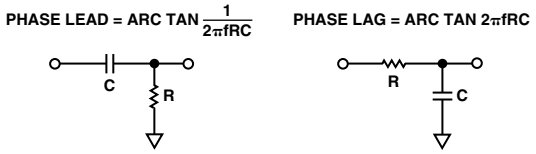
In cases where the reference phase relative to the input signals from the resolver requires adjustment, this can be easily achieved by varying the value of the resistor R2 of the HF filter (see Figure 1).

Assuming that R1 = R2 = R and C1 = C2 = C

and Reference Frequency = $\frac{1}{2\pi RC}$

by altering the value of R2, the phase of the reference relative to the input signals will change in an approximately linear manner for phase shifts of up to 10 degrees.

Increasing R2 by 10% introduces a phase lag of 2 degrees. Decreasing R2 by 10% introduces a phase lead of 2 degrees.



Phase Shift Circuits

TYPICAL CIRCUIT CONFIGURATION

Figure 8 shows a typical circuit configuration for the AD2S80A in a 12-bit resolution mode. Values of the external components have been chosen for a reference frequency of 5 kHz and a maximum tracking rate of 260 rps with a bandwidth of 520 Hz. Placing the values for R4, R6, C4 and C5 in the equation for K_A gives a value of 1.67×10^6. The resistors are 0.125 W, 5% tolerance preferred values. The capacitors are 100 V ceramic, 10% tolerance components.

For signal and reference voltages greater than 2 V rms a simple voltage divider circuit of resistors can be used to generate the correct signal level at the converter. Care should be taken to ensure that the ratios of the resistors between the sine signal line and ground and the cosine signal line and ground are the same. Any difference will result in an additional position error.

For more information on resistive scaling of SIN, COS and REFERENCE converter inputs refer to the application note, "Circuit Applications of the 2S81 and 2S81 Resolver-to-Digital Converters."

RELIABILITY

The AD2S80A Mean Time Between Failures (MTBF) has been calculated according to MIL-HDBK-217E, Figure 10 shows the MTBF in hours in naval sheltered conditions for AD2S80A/883B only.

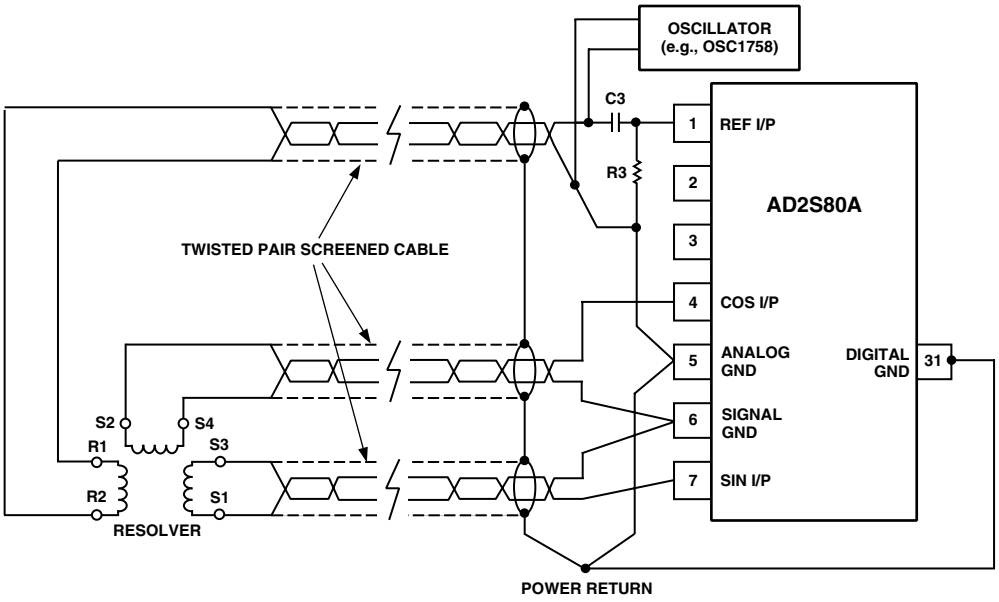


Figure 7. Connecting the AD2S80A to a Resolver

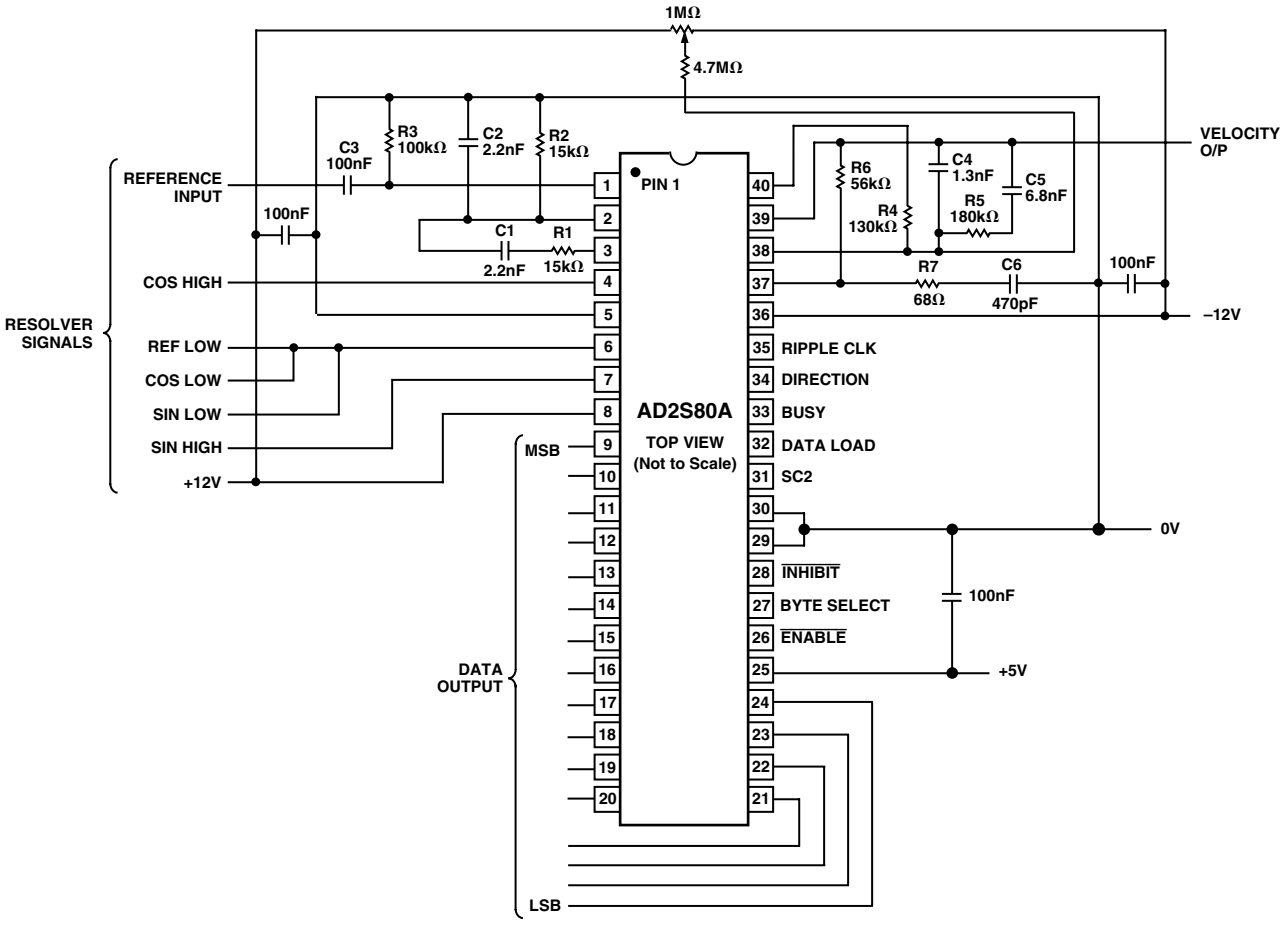


Figure 8. Typical Circuit Configuration

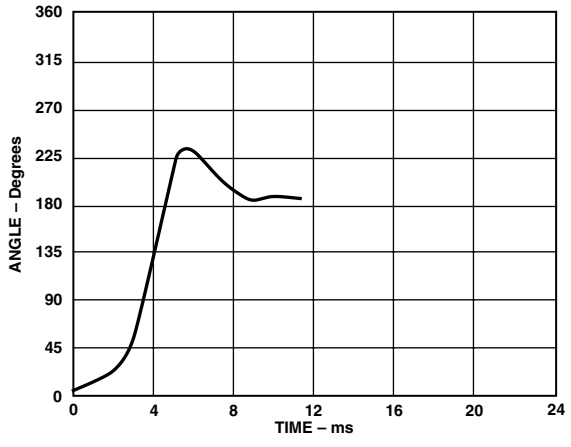


Figure 9. Large Step Response Curves for Typical Circuit Shown in Figure 8

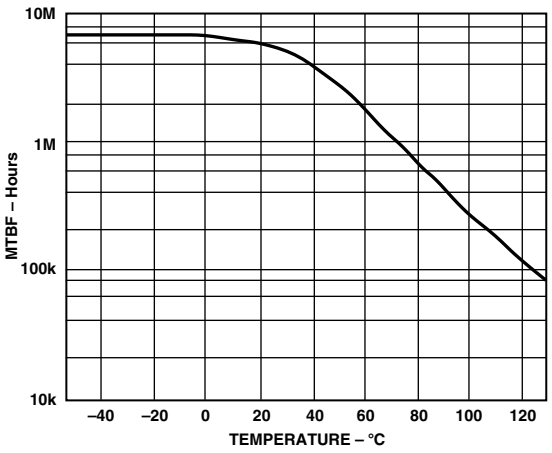


Figure 10. AD2S80A MTBF Curve

APPLICATIONS

Control Transformer

The ratio multiplier of the AD2S80A can be used independently of the loop integrators as a control transformer. In this mode the resolver inputs θ are multiplied by a digital angle ϕ any difference between ϕ and θ will be represented by the AC ERROR output as SIN ωt sin (θ–ϕ) or the DEMOD output as sin (θ–ϕ). To use the AD2S80A in this mode refer to the "Control Transformer" application note.

Dynamic Switching

In applications where the user requires wide band response from the converter, for example 100 rpm to 6000 rpm, superior performance is achieved if the converters control characteristics are switched dynamically. This reduces velocity offset levels at low tracking rates. For more information on the technique refer to "Dynamic Resolution Switching Using the Variable Resolution Monolithic Resolver-to-Digital Converters."

OTHER PRODUCTS

The AD2S82A is a monolithic, variable resolution 10-, 12-, 14- and 16-bit resolver-to-digital converter in a 44-terminal J-leaded PLCC package. In addition to the AD2S80A functions it has a VCO OUTPUT which is a measure of position within a LSB, and a COMPLEMENT Data Output.

The AD2S81A is a low cost, monolithic, 12-bit resolver-to-digital converter in a 28-lead ceramic DIP package.

C00008–2.5–9/00 (rev. B)

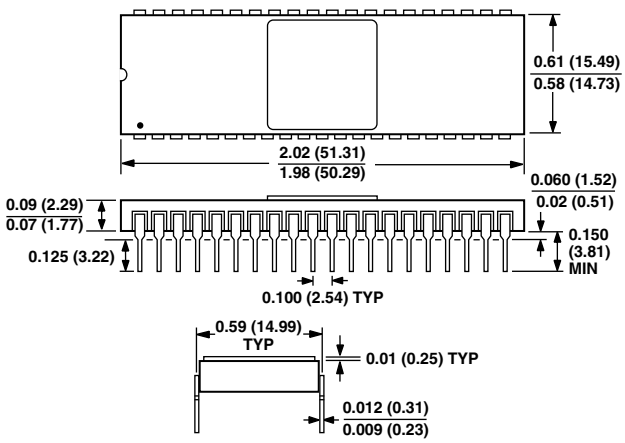
ORDERING GUIDE

Model	Operating Temperature Range	Accuracy	Package Description	Package Option
AD2S80AJD	0°C to 70°C	8 arc min	Side Brazed Ceramic DIP	D-40
AD2S80AKD	0°C to 70°C	4 arc min	Side Brazed Ceramic DIP	D-40
AD2S80ALD	0°C to 70°C	2 arc min	Side Brazed Ceramic DIP	D-40
AD2S80AAD	–40°C to +85°C	8 arc min	Side Brazed Ceramic DIP	D-40
AD2S80ABD	–40°C to +85°C	4 arc min	Side Brazed Ceramic DIP	D-40
AD2S80ASD	–55°C to +125°C	8 arc min	Side Brazed Ceramic DIP	D-40
AD2S80ATD	–55°C to +125°C	4 arc min	Side Brazed Ceramic DIP	D-40
AD2S80AUD	–55°C to +125°C	2 arc min	Side Brazed Ceramic DIP	D-40
AD2S80ASE	–55°C to +125°C	8 arc min	Leadless Ceramic Chip Carrier	E-44A
AD2S80ATE	–55°C to +125°C	4 arc min	Leadless Ceramic Chip Carrier	E-44A
AD2S80AUE	–55°C to +125°C	2 arc min	Leadless Ceramic Chip Carrier	E-44A
AD2S80ASD/883B	–55°C to +125°C	8 arc min	Side Brazed Ceramic DIP	D-40
AD2S80ATD/883B	–55°C to +125°C	4 arc min	Side Brazed Ceramic DIP	D-40
AD2S80ASE/883B	–55°C to +125°C	8 arc min	Leadless Ceramic Chip Carrier	E-44A
AD2S80ATE/883B	–55°C to +125°C	4 arc min	Leadless Ceramic Chip Carrier	E-44A

OUTLINE DIMENSIONS

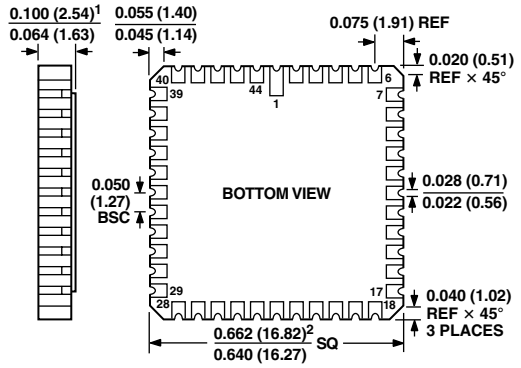
Dimensions shown in inches and (mm).

40-Lead Ceramic DIP (D) Package



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH. LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42.

44-Terminal LCC (E) Package



NOTES
[1]THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
[2]APPLIES TO ALL FOUR SIDES.
ALL TERMINALS ARE GOLD PLATED.

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