2.5A, 15V Monolithic Synchronous Step-Down Regulator

FEATURES

- **Wide Input Voltage Range: 4.5V to 15V**
- **2.5A Output Current**
- **Low $R_{DS(ON)}$ Internal Switches: 45mΩ and 85mΩ**
- **Programmable Frequency: 300kHz to 3MHz**
- **Low Quiescent Current: 75µA**
- 0.6V ±1% Reference Allows Precise, Low Output Voltage
- 99% Maximum Duty Cycle
- Adjustable Burst Mode® Clamp
- Synchronizable to External Clock
- Power Good Output Voltage Monitor
- Overtemperature Protection
- Overvoltage Protection
- Available in 16-Lead Thermally Enhanced MSOP and 4mm × 4mm QFN Packages

APPLICATIONS

- Point-of-Load Supplies
- Portable Instruments
- Communications Infrastructure

DESCRIPTION

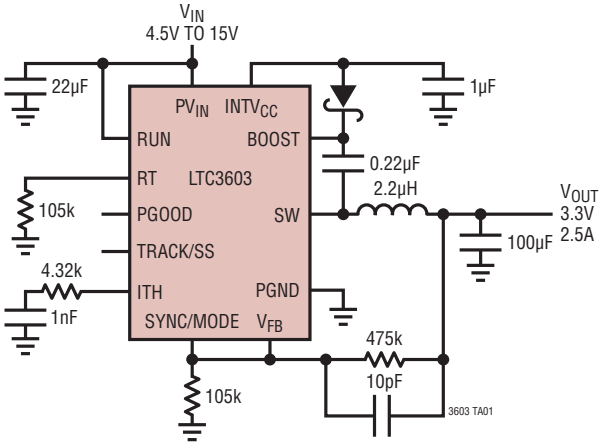
The LTC®3603 is a high efficiency, monolithic synchronous step-down DC/DC converter utilizing a constant-frequency, current mode architecture. It operates from an input voltage range of 4.5V to 15V and provides an adjustable regulated output voltage from 0.6V to 14.5V while delivering up to 2.5A of output current. The internal synchronous power switch with 45mΩ on-resistance increases efficiency and eliminates the need for an external Schottky diode. The switching frequency can either be set by an external resistor or synchronized to an external clock. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

The LTC3603 can be configured for either Burst Mode operation or forced continuous operation. Forced continuous operation reduces noise and RF interference, while Burst Mode operation provides the highest efficiency at light loads. In Burst Mode operation, external control of the burst clamp level allows the output voltage ripple to be adjusted according to the requirements of the application.

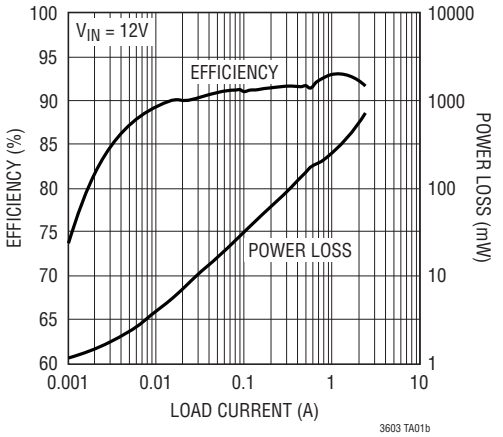
LT, LTC, LTM, Burst Mode, OPTI-LOOP, Linear Technology and the Linear logo are registered trademarks and ThinSOT is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners. Protected by U.S. Patents including 5481178, 6580258, 6498466, 6611131, 6177787, 5705919, 5847554.

TYPICAL APPLICATION

3.3V, 2.5A, 1MHz Step-Down Regulator



Efficiency and Power Loss vs Load Current

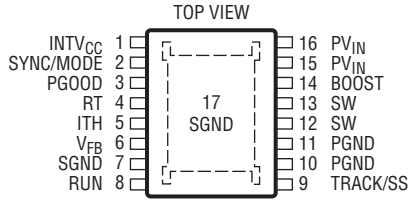


ABSOLUTE MAXIMUM RATINGS (Note 1)

PV_{IN} Supply Voltage (DC) ..... –0.3V to 16V
PV_{IN} Supply Transient Voltage (<1µs) 21V
SW ..... –0.3V to (PV_{IN} + 0.3V)
BOOST ..... (V_{SW} –0.3V) to (V_{SW} + 6V)
RUN ..... –0.3V to 16V
All Other Pins ..... –0.3V to 6V

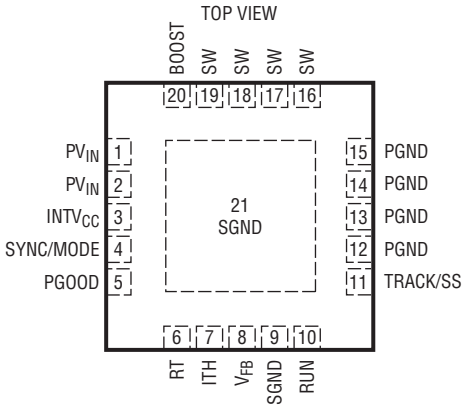
Peak SW Sink and Source Current (Note 7) 6.5A
Operating Junction Temperature Range (Notes 2, 5, 6)
LTC3603E .....–40°C to 85°C
LTC3603I ..... –40°C to 125°C
Lead Temperature (Soldering, 10 seconds)
MSE Package.....300°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 45°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS SGND, MUST BE SOLDERED TO PCB



UF PACKAGE
20-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W, θ_{JC} = 5°C/W
EXPOSED PAD (PIN 21) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3603EMSE#PBF	LTC3603EMSE#TRPBF	3603	16-Lead Plastic MSOP	–40°C to 85°C
LTC3603IMSE #PBF	LTC3603IMSE#TRPBF	3603	16-Lead Plastic MSOP	–40°C to 125°C
LTC3603EUF#PBF	LTC3603EUF#TRPBF	3603	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC3603IUF#PBF	LTC3603IUF#TRPBF	3603	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PV_{IN}	Operating Voltage Range			4.5		15	V
V_{FB}	Regulated Feedback Voltage	ITH = 0.7V (Note 3)	●	0.594	0.6	0.606	V
$\Delta V_{FB(LINEREG)}$	Feedback Voltage Line Regulation	V_{IN} = 5V to 15V, I_{TH} = 0.7V			0.005		%/V
$\Delta V_{FB(LOADREG)}$	Feedback Voltage Load Regulation	ITH = 0.36V to 0.84V	●		0.02	0.1	%
ΔV_{PGOOD}	Power Good Range				±10	±12	%
R_{PGOOD}	Power Good Resistance				55	80	Ω
I_{FB}	FB Input Bias Current				10		nA
g_m	Transconductance Amplifier g_m				1.7		mS
I_S	Supply Current Active Mode Sleep Mode Shutdown	(Note 4)			 500 75 0.2	 700 100 1	 µA µA µA
$INTV_{CC}$	V_{CC} LDO Output Voltage			4.7	4.9	5.1	V
$t_{ON, MIN}$	Minimum Controllable ON-Time				95	115	ns
V_{RUN}	RUN Pin ON Threshold	V_{RUN} Rising	●	0.4	0.7	1	V
$I_{TRACK/SS}$	TRACK/SS Pull-Up Current	TRACK/SS = 1V			1.25		µA
f_{OSC}	Oscillator Frequency	R_T = 105k		0.85	1	1.15	MHz
f_{SYNC}	SYNC Capture Range			0.3		3	MHz
$R_{DS(ON)}$	Top Switch On-Resistance Bottom Switch On-Resistance				85 45		mΩ mΩ
I_{LIM}	Peak Current Limit			3.8	4.5	5.2	A
I_{LSW}	Switch Leakage Current				0.1	1	µA
V_{UVLO}	$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Ramping Up	●	4.1	4.2	4.3	V
$V_{UVLO, HYS}$	$INTV_{CC}$ Undervoltage Lockout Hysteresis				700		mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3603E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3603I is guaranteed over the –40°C to 125°C operating junction temperature range.

Note 3: The LTC3603 is tested in a feedback loop that adjusts V_{FB} to achieve a specified error amplifier output voltage (I_{TH}).

Note 4: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

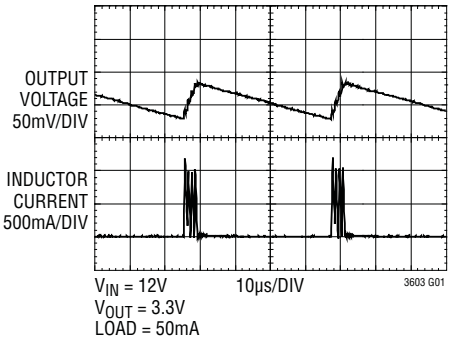
Note 5: T_J is calculated from the ambient temperature T_A and the power dissipation as follows: $T_J = T_A + (P_D)(\theta_{JA}°C/W)$.

Note 6: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

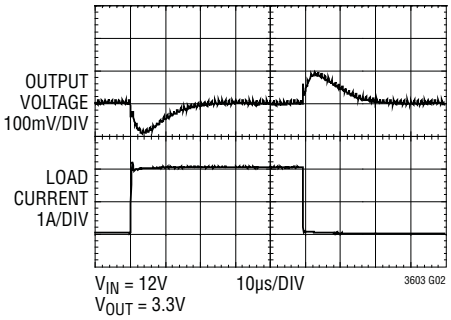
Note 7: This limit indicates the current density limitations of the internal metallization and it is not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

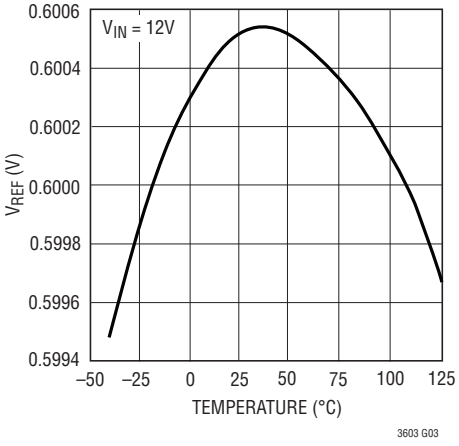
Burst Mode Operation



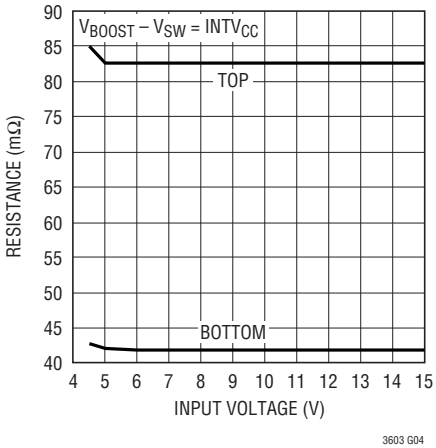
Load Step Transient Forced Continuous



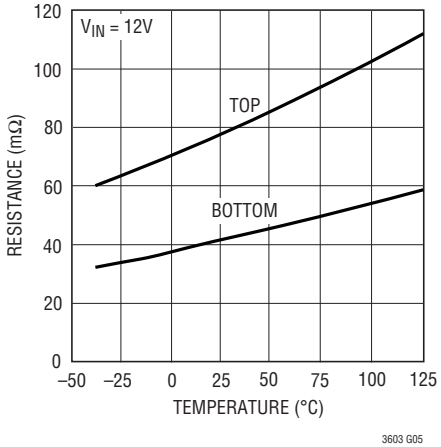
V_{REF} vs Temperature



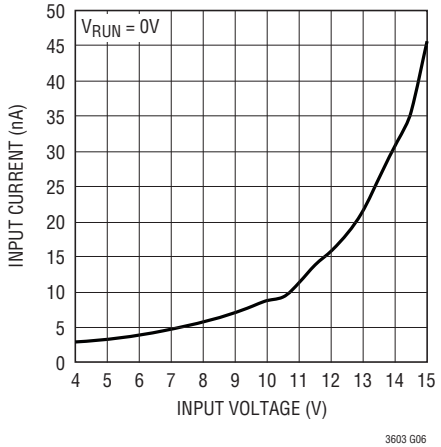
Switch On-Resistance vs Input Voltage



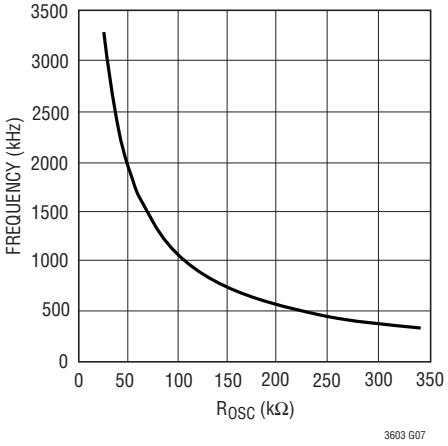
Switch On-Resistance vs Temperature



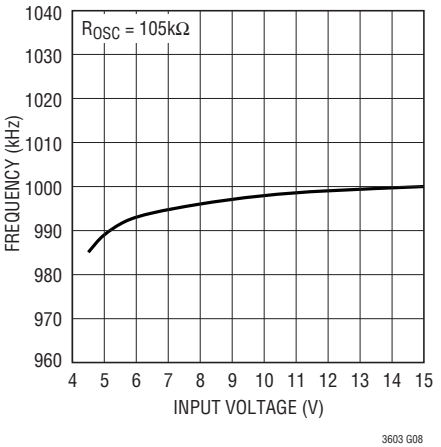
PV_{IN} Leakage Current vs Input Voltage



Frequency vs R_{OSC}

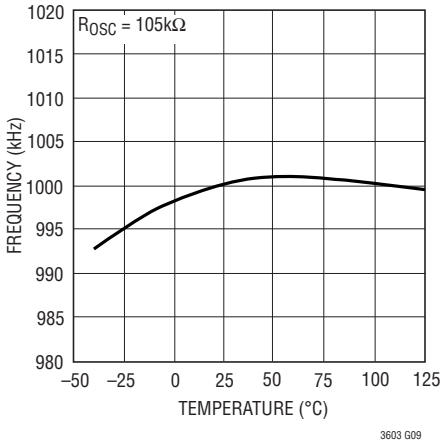


Frequency vs Input Voltage

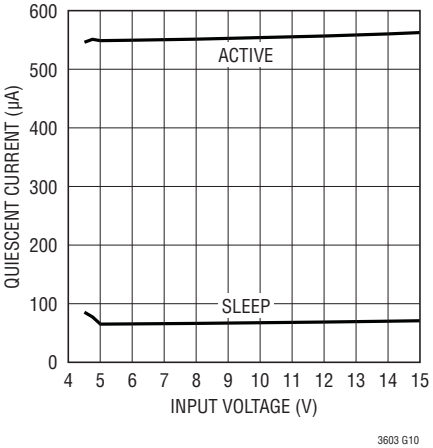


TYPICAL PERFORMANCE CHARACTERISTICS

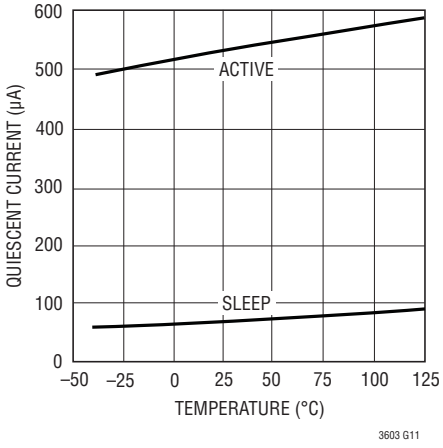
Frequency vs Temperature



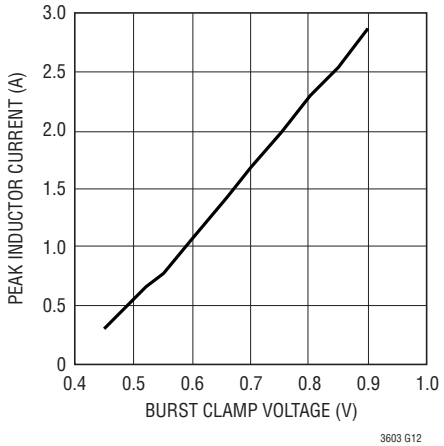
Quiescent Current vs Input Voltage



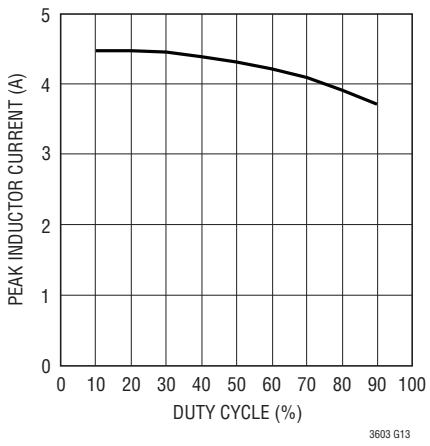
Quiescent Current vs Temperature



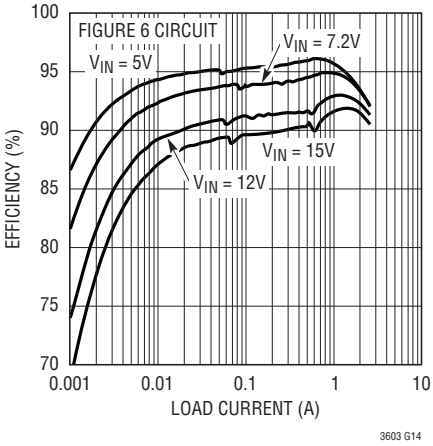
Minimum Peak Inductor Current vs Burst Clamp Voltage



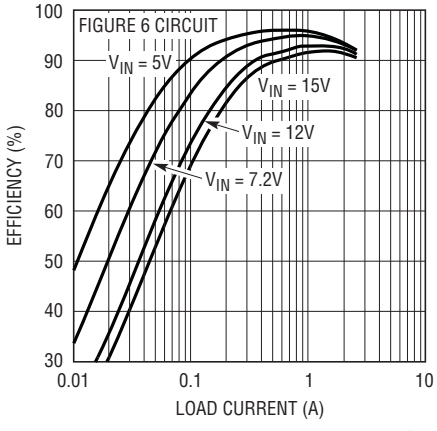
Maximum Peak Inductor Current vs Duty Cycle



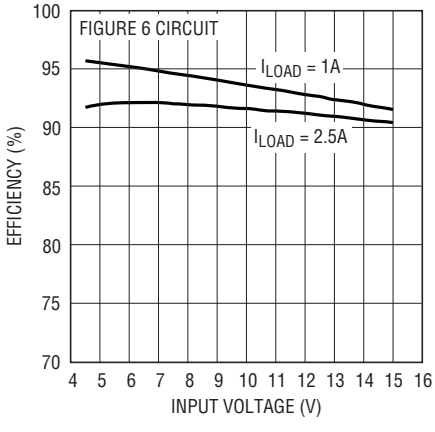
Efficiency vs Load Current, Burst Mode Operation



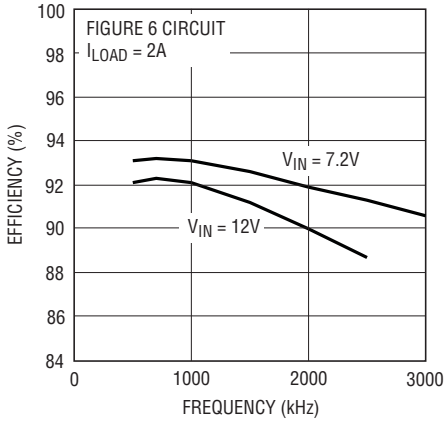
Efficiency vs Load Current, Forced Continuous



Efficiency vs Input Voltage

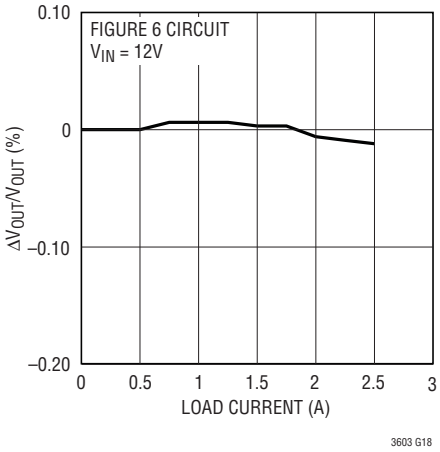


Efficiency vs Frequency

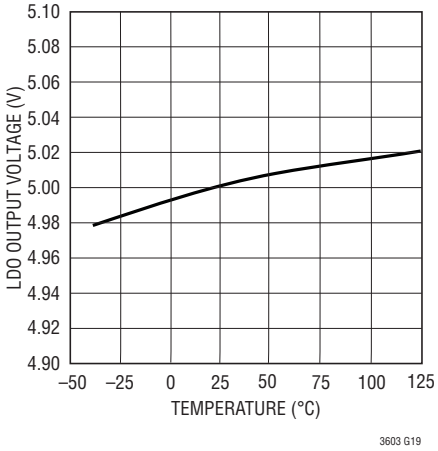


TYPICAL PERFORMANCE CHARACTERISTICS

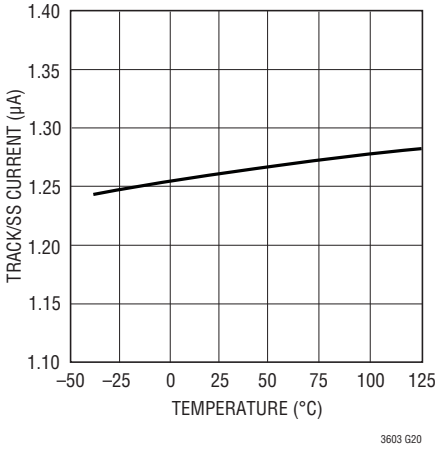
Load Regulation



5V LDO Output Voltage vs Temperature



TRACK/SS Current vs Temperature



PIN FUNCTIONS MSE/UF Package

$INTV_{CC}$ (Pin 1/Pin 3): Output of Internal 5V LDO.

SYNC/MODE (Pin 2/Pin 4): Mode Select and External Clock Synchronization Input.

PGOOD (Pin 3/Pin 5): Power Good Output. Open-drain logic output that is pulled to ground when the output voltage is not within ±10% of regulation point.

RT (Pin 4/Pin 6): Frequency Set Pin.

ITH (Pin 5/Pin 7): Error Amplifier Compensation Point.

V_{FB} (Pin 6/Pin 8): Feedback Pin.

SGND (Pin 7, Exposed Pad Pin 17/Pin 9, Exposed Pad Pin 21): Signal Ground. Exposed pad is signal ground and must be soldered to the PCB for rated thermal performance.

RUN (Pin 8/Pin 10): Run Control Input. This pin may be tied to PV_{IN} to enable the chip.

TRACK/SS (Pin 9/Pin 11): Tracking Input for the Controller or Optional External Soft-Start Input. This pin allows the start-up of V_{OUT} to "track" the external voltage at this pin using an external resistor divider. An external soft-start can be programmed by connecting a capacitor between this pin and ground. Leave this pin floating to use the internal 1ms soft-start clamp. Do not tie this pin to $INTV_{CC}$ or to PV_{IN}.

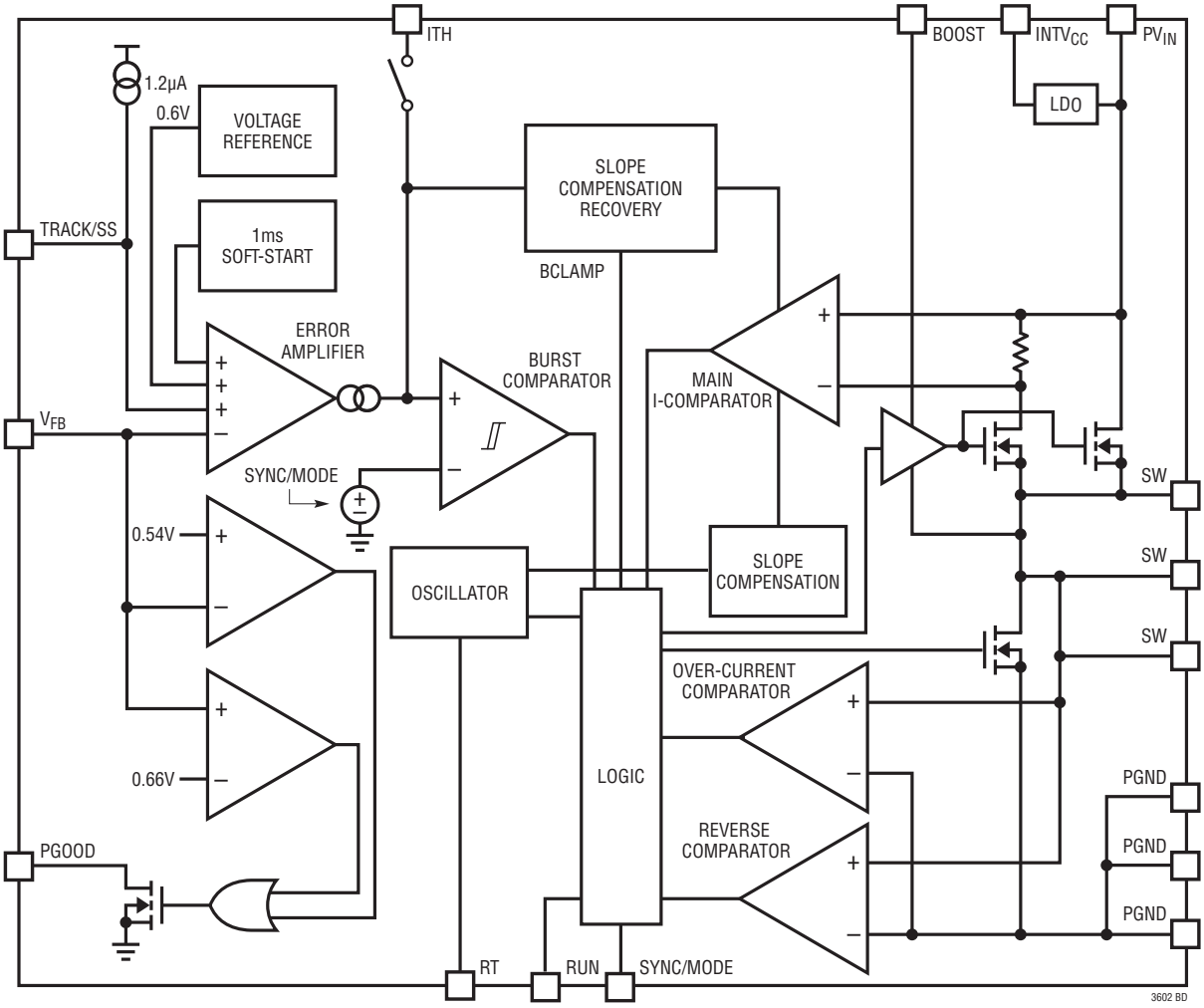
PGND (Pins 10, 11/Pins 12, 13, 14, 15): Power Ground.

SW (Pins 12, 13/Pins 16, 17, 18, 19): Switch Node Connection to the Inductor.

BOOST (Pin 14/Pin 20): Bootstrapped Supply to the Top Side Floating Gate Driver.

PV_{IN} (Pins 15, 16/Pins 1,2): Power Input Supply. Decouple this pin with a capacitor to PGND

BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC3603 is a monolithic, constant-frequency, current mode step-down DC/DC converter. During normal operation, the internal top power switch (N-channel MOSFET) is turned on at the beginning of each clock cycle. Current in the inductor increases until the current comparator trips and turns off the top power MOSFET. The peak inductor current at which the current comparator shuts off the top power switch is controlled by the voltage on the ITH pin. The error amplifier adjusts the voltage on the ITH pin by comparing the feedback signal from a resistor divider on the V_{FB} pin with an internal 0.6V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier raises the ITH voltage until the average inductor current matches the new load current. When the top power MOSFET shuts off, the synchronous power switch (N-channel MOSFET) turns on until either the bottom current limit is reached or the beginning of the next clock cycle. The bottom current limit is set at –2.5A for forced continuous mode and 0A for Burst Mode operation.

The operating frequency is externally set by an external resistor connected between the RT pin and ground. The practical switching frequency can range from 300kHz to 3MHz.

Overvoltage and undervoltage comparators will pull the PGOOD output low if the output voltage comes out of regulation by ±10%. In an overvoltage condition, the top power MOSFET is turned off and the bottom power MOSFET is switched on until either the overvoltage condition clears or the bottom MOSFET's current limit is reached.

Forced Continuous Mode

Connecting the SYNC/MODE pin to $INTV_{CC}$ will disable Burst Mode operation and force continuous current operation. At light loads, forced continuous mode operation is less efficient than Burst Mode operation, but may be desirable in some applications where it is necessary to keep switching harmonics out of a signal band. The output voltage ripple is minimized in this mode.

Burst Mode Operation

Connecting the SYNC/MODE pin to a voltage in the range of 0.42V to 1V enables Burst Mode operation. In Burst Mode operation, the internal power MOSFETs operate intermittently at light loads. This increases efficiency by minimizing switching losses. During Burst Mode operation, the minimum peak inductor current is externally set by the voltage on the SYNC/MODE pin and the voltage on the ITH pin is monitored by the burst comparator to determine when sleep mode is enabled and disabled. When the average inductor current is greater than the load current, the voltage on the ITH pin drops. As the ITH voltage falls below 330mV, the burst comparator trips and enables sleep mode. During sleep mode, the top power MOSFET is held off and the ITH pin is disconnected from the output of the error amplifier. The majority of the internal circuitry is also turned off to reduce the quiescent current to 75µA while the load current is solely supplied by the output capacitor. When the output voltage drops, the ITH pin is reconnected to the output of the error amplifier and the top power MOSFET along with all the internal circuitry is switched back on. This process repeats at a rate that is dependent on the load demand. Pulse-skipping operation is implemented by connecting the SYNC/MODE pin to ground. This forces the burst clamp level to be at 0V. As the load current decreases, the peak inductor current will be determined by the voltage on the ITH pin until the ITH voltage drops below 330mV. At this point, the peak inductor current is determined by the minimum on-time of the current comparator. If the load demand is less than the average of the minimum on-time inductor current, switching cycles will be skipped to keep the output voltage in regulation.

Frequency Synchronization

The internal oscillator of the LTC3603 can be synchronized to an external 5V clock connected to the SYNC/MODE pin. The frequency of the external clock can be in the range of 300kHz to 3MHz. For this application, the oscillator timing resistor should be chosen to correspond to a frequency that is 25% lower than the synchronization frequency. When synchronized, the LTC3603 will operate in pulse-skipping mode.

OPERATION

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the top switch to remain on for more than one cycle until it attempts to stay on continuously. In order to replenish the voltage on the floating BOOST supply capacitor, however, the top switch is forced off and the bottom switch is forced on for approximately 85ns every sixteen clock cycles. This achieves an effective duty cycle that can exceed 99%. The output voltage will then be primarily determined by the input voltage minus the voltage drop across the upper internal N-channel MOSFET and the inductor.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant-frequency architectures by preventing subharmonic oscillations at duty cycles greater than 50%. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 30%. Normally, the maximum inductor peak current is reduced when slope compensation is added. In the LTC3603, however, slope compensation recovery is implemented to reduce the variation of the maximum inductor peak current (and therefore the maximum available output current) over the range of duty cycles.

Short-Circuit Protection

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. To prevent current runaway from occurring, a secondary current limit is imposed on the inductor current. If the inductor valley current increases to more than 4.5A, the top power MOSFET will be held off and switching cycles will be skipped until the inductor current is reduced.

Overtemperature and PV_{IN} Overvoltage Protection

When using the LTC3603 in an application circuit, care must be taken not to exceed any of the ratings specified in the Absolute Maximum Ratings section. As an added safeguard, however, the LTC3603 does incorporate an overtemperature shutdown feature. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance. After the part has cooled to below 115°C, it will restart. Similarly, the LTC3603 contains an overvoltage shutdown feature that monitors the voltage on the PV_{IN} pin. If this voltage exceeds approximately 16.5V, both power switches will be turned off until PV_{IN} voltage is reduced below 16V.

Voltage Tracking and Soft-Start

Some microprocessors and DSP chips need two power supplies with different voltage levels. These systems often require voltage sequencing between the core power supply and the I/O power supply. Without proper sequencing, latch-up failure or excessive current draw may occur that could result in damage to the processor's I/O ports or the I/O ports of a supporting system device such as memory, an FPGA or a data converter. To ensure that the I/O loads are not driven until the core voltage is properly biased, tracking of the core supply and the I/O supply voltage is necessary.

Voltage tracking is enabled by applying a ramp voltage to the TRACK/SS pin. When the voltage on the TRACK pin is below 0.6V, the feedback voltage will regulate to this tracking voltage. When the tracking voltage exceeds 0.6V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage.

The TRACK/SS pin is also used to implement an external soft-start function. A 1.2µA current is sourced from this pin so that an external capacitor may be added to create a smooth ramp. If this ramp is slower than the internal 1ms soft-start, then the output voltage will track this ramp during start-up instead. Leave this pin floating to use the internal 1ms soft-start ramp. **Do not tie the TRACK/SS pin to $INTV_{CC}$ or to PV_{IN}.**

APPLICATIONS INFORMATION

The basic LTC3603 application circuit is shown on the front page of this data sheet. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge and switching losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage. The operating frequency of the LTC3603 is determined by an external resistor that is connected between the RT pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_{OSC} = \frac{1.15 \bullet 10^{11}}{f(Hz)} - 10k$$

Although frequencies as high as 3MHz are possible, the minimum on-time of the LTC3603 imposes a minimum limit on the operating duty cycle. The minimum on-time is typically 95ns. Therefore, the minimum duty cycle is equal to 100 • 95ns • f(Hz).

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{fL}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4(I_{MAX})$, where I_{MAX} is the maximum output current. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f\Delta I_{L(MAX)}}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor value will also have an effect on Burst Mode operation. The transition from low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes this to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of the more expensive ferrite cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates *hard*, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate energy but generally cost more than powdered iron core inductors with similar

APPLICATIONS INFORMATION

characteristics. The choice of which style inductor to use mainly depends on the price vs size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coiltronics, Coilcraft, Toko and Sumida.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \bullet \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R2}{R1} \right)$$

The resistive divider allows the V_{FB} pin to sense a fraction of the output voltage as shown in Figure 1.

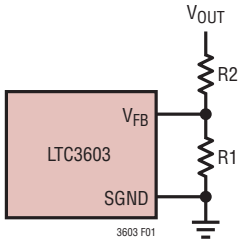


Figure 1. Setting the Output Voltage

APPLICATIONS INFORMATION

Burst Clamp Programming

If the voltage on the SYNC/MODE pin is in the range of 0.42V to 1V, Burst Mode operation is enabled. During Burst Mode operation, the voltage on the SYNC/MODE pin determines the burst clamp level. This level sets the minimum peak inductor current, I_{BURST}, for each switching cycle according to the following equation:

$$V_{BURST} = \frac{I_{BURST}}{6A/V} + 0.42V$$

V_{BURST} is the voltage on the SYNC/MODE pin. I_{BURST} can be programmed in the range of 0A to 3.5A, which corresponds to a V_{BURST} range of 0.42V to 1V. As the output load current drops, the peak inductor current decreases to keep the output voltage in regulation. When the output load current demands a peak inductor current that is less than I_{BURST}, the burst clamp will force the peak inductor current to remain equal to I_{BURST} regardless of further reductions in the load current. Since the average inductor current is therefore greater than the output load current, the voltage on the ITH pin will decrease. When the I_{TH} voltage drops to 330mV, sleep mode is enabled in which both power MOSFETs are shut off along with most of the circuitry to minimize power consumption. All circuitry is turned back on and the power MOSFETs begin switching again when the output voltage drops out of regulation. The value for I_{BURST} is determined by the desired amount of output voltage ripple. As the value of I_{BURST} increases, the sleep time between pulses and the output voltage ripple increases. The burst clamp voltage, V_{BURST}, can be set by a resistor divider from the $INTV_{CC}$ pin. Alternatively, the SYNC/MODE pin may be tied directly to the V_{FB} pin to set V_{BURST} = 0.6V (I_{BURST} = 1A), or through an additional divider resistor (R3) to set V_{BURST} = 0.42V to 0.6V (see Figure 2).

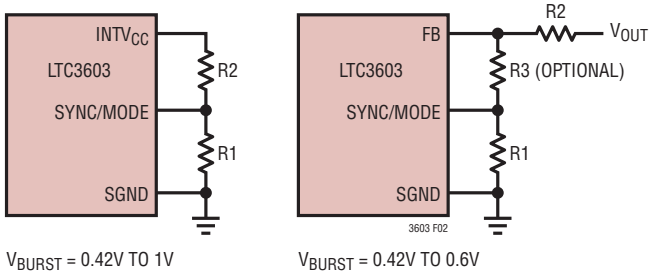


Figure 2. Programing the Burst Clamp

Pulse skipping, which is a compromise between low output voltage ripple and efficiency, can be implemented by connecting the SYNC/MODE pin to ground. This sets I_{BURST} to 0A. In this condition, the peak inductor current is limited by the minimum on-time of the current comparator and the lowest output voltage ripple is achieved while still operating discontinuously. During very light output loads, pulse skipping allows only a few switching cycles to be skipped while maintaining the output voltage in regulation.

Frequency Synchronization

The LTC3603's internal oscillator can be synchronized to an external 5V clock signal. During synchronization, the top MOSFET turn-on is locked to the falling edge of the external frequency source. The synchronization frequency range is 300kHz to 3MHz. Synchronization only occurs if the external frequency is greater than the frequency set by the R_T resistor. Because slope compensation is generated by the oscillator's internal ramp, the external frequency should be set 25% higher than the frequency set by the R_T resistor to ensure that adequate slope compensation is present. When synchronized, the LTC3603 will operate in pulse-skipping mode.

$INTV_{CC}$ Regulator

The LTC3603 features an integrated P-channel low dropout linear regulator (LDO) that supplies power to the $INTV_{CC}$ supply pin from the PV_{IN} pin. This LDO supply has been designed to deliver up to 35mA of load current for the powering of the internal gate drivers and other internal circuitry. A small external load may also be applied provided that the total current from the $INTV_{CC}$ supply does not exceed 35mA. The $INTV_{CC}$ pin should be bypassed with no less than a 0.22µF ceramic capacitor. A 1µF ceramic capacitor is suitable for most applications.

Topside MOSFET Driver Supply (BOOST Pin)

The LTC3603 uses a bootstrapped supply to power the gate of the internal topside MOSFET (Figure 3). When the topside MOSFET is off and the SW pin is low, diode D_{BST} charges capacitor C_{BST} to the voltage on the $INTV_{CC}$ supply. In order to turn on the topside MOSFET, the voltage on the BOOST pin is then applied to its gate. As the topside MOSFET turns on, the SW pin rises to the PV_{IN} voltage

APPLICATIONS INFORMATION

and the BOOST pin rises to PV_{IN} + $INTV_{CC}$, thereby keeping the MOSFET fully enhanced. For most applications, a 0.22µF ceramic capacitor is appropriate for C_{BST}. Schottky diode D_{BST} should have a reverse breakdown voltage that is greater than $PV_{IN(MAX)}$.

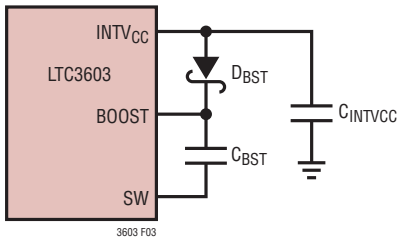


Figure 3. Topside MOSFET Supply

Run and Soft-Start/Tracking Functions

The LTC3603 has a low power shutdown mode which is controlled by the RUN pin. Pulling the RUN pin below 0.7V puts the LTC3603 into a low quiescent current shutdown mode (I_Q < 1µA). When the RUN pin is greater than 0.7V, the controller is enabled. The RUN pin can be driven directly from logic as shown in Figure 4.

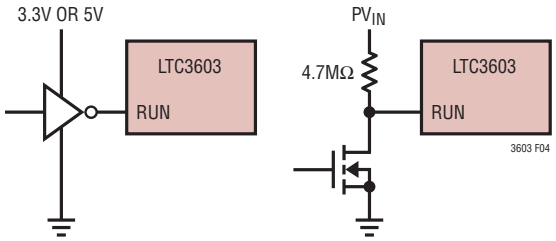


Figure 4. RUN Pin Interfacing

Soft-start and tracking are implemented by limiting the effective reference voltage as seen by the error amplifier. Ramping up the effective reference into the error amp in turn causes a smooth and controlled ramp on the output voltage of the converter. To use the default, internal 1ms soft-start ramp, leave the TRACK/SS pin floating. **Do not tie the TRACK/SS pin to $INTV_{CC}$ or to PV_{IN}.** To increase the soft-start time above 1ms, place a cap on the TRACK/SS pin. A 1.2µA internal pull-up current will charge this capacitor, resulting in a soft-start ramp time given by:

$$t_{SS} = C_{SS} \bullet \frac{0.6V}{1.2\mu A}$$

When the LTC3603 detects a fault condition (either undervoltage lockout or overtemperature), the TRACK/SS pin is quickly pulled to ground and the internal soft-start timer is also reset. This ensures an orderly restart when using an external soft-start capacitor.

To implement tracking, a resistor divider is placed between an external supply (V_X) and the TRACK/SS pin as shown in Figure 5a. This technique can be used to cause V_{OUT} to ratiometrically track the V_X supply (Figure 5b), according to the following:

$$\frac{V_{OUT}}{V_X} = \frac{R_{TA}}{R_A} \bullet \frac{R_A + R_B}{R_{TA} + R_{TB}}$$

For coincident tracking, as shown in Figure 5c, (V_{OUT} = V_X during start-up),

$$R_{TA} = R_A,\ R_{TB} = R_B$$

Note that the 1.2µA current that is sourced from the TRACK/SS pin will cause a slight offset in the voltage seen on the TRACK/SS pin and consequently on the V_{OUT} voltage during tracking. This V_{OUT} offset due to the TRACK/SS current is given by:

$$V_{OS,TRK} = (1\mu A) \bullet \frac{R_{TA}R_{TA}}{R_{TA} + R_{TB}} \bullet \frac{R_A + R_B}{R_A}$$

For most applications, this offset is small and has minimal effect on tracking performance. For improved tracking accuracy, reduce the parallel impedance of R_{TA} and R_{TB}.

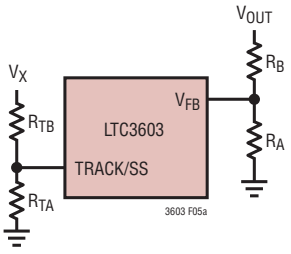


Figure 5a. Using the TRACK/SS Pin to Track V_X

APPLICATIONS INFORMATION

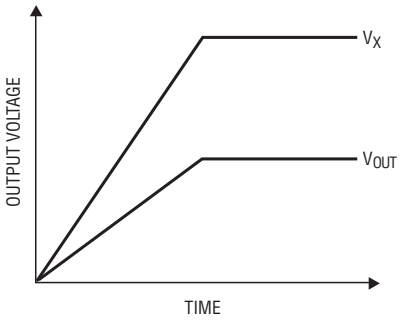


Figure 5b. Ratiometric Tracking

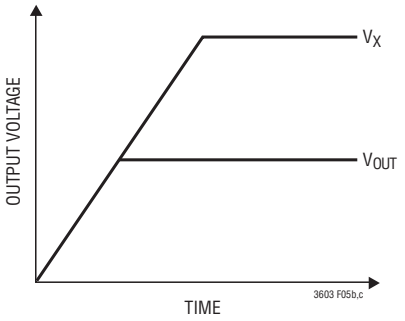


Figure 5c. Coincident Tracking

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

$$\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} operating current and I^2R losses.

The V_{IN} operating current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents.

1. The V_{IN} operating current comprises three components: The DC supply current as given in the electrical characteristics, the internal MOSFET gate charge currents and the internal topside MOSFET transition losses. The MOSFET gate charge current results from switching the gate capacitance of the internal power MOSFET switches. The gates of these switches are driven from the $INTV_{CC}$ supply. Each time the gate is switched from high to low to high again, a packet of charge, dQ, moves from $INTV_{CC}$ to ground. The resulting dQ/dt is the current out of $INTV_{CC}$ that is typically larger than the DC bias current. In continuous mode, the gate charge current can be approximated by $I_{GATECHG} = f(9.5nC)$. Since the $INTV_{CC}$ voltage is generated from V_{IN} by a linear regulator, the current that is internally drawn from the $INTV_{CC}$ supply can be treated as V_{IN} current for the purposes of efficiency considerations.

   Transition losses apply only to the internal topside MOSFET and become more prominent at higher input voltages. Transition losses can be estimated from:

   $$\text{Transition Loss} = (1.7)\ V_{IN}^2 \bullet I_{O(MAX)} \bullet (120pF) \bullet f$$

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L. In continuous mode, the average output current flowing through inductor L is *chopped* between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current:

   $$I^2R\ \text{Loss} = I_O^2(R_{SW} + R_L)$$

   Other losses, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% of the total power loss.

Thermal Considerations

In most applications, the LTC3603 does not dissipate much heat due to its high efficiency. But, in applications where the LTC3603 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

APPLICATIONS INFORMATION

To prevent the LTC3603 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = (P_D) \bullet (\theta_{JA})$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

As an example, consider the LTC3603 in dropout at an input voltage of 8V, a load current of 2.5A and an ambient temperature of 70°C. From the Typical Performance graph of Switch Resistance, the $R_{DS(ON)}$ of the top switch at 70°C is approximately 85mΩ. Therefore, power dissipated by the part is:

$$P_D = (I_{LOAD}^2)(R_{DS(ON)}) = (2.5A)^2(85m\Omega) = 0.53W$$

For the MSOP package, the θ_{JA} is 45°C/W. Thus, the junction temperature of the regulator is:

$$T_J = 70°C + (0.53W)(45°C/W) = 93.85°C$$

which is below the maximum junction temperature of 125°C.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD}•(ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. The I_{TH} pin external components and output capacitor shown in the front page application will provide adequate compensation for most applications.

Design Example

As a design example, consider using the LTC3603 in an application with the following specifications: V_{IN} = 12V, V_{OUT} = 3.3V, $I_{OUT(MAX)}$ = 2.5A, $I_{OUT(MIN)}$ = 100mA, f = 1MHz. Because efficiency is important at both high and low load current, Burst Mode operation will be utilized. First, calculate the timing resistor:

$$R_{OSC} = \frac{1.15 \bullet 10^{11}}{1MHz} - 10k = 105k$$

Next, calculate the inductor value for about 40% ripple current at maximum V_{IN}:

$$L = \left(\frac{3.3V}{(1MHz)(1A)}\right) \bullet \left(1 - \frac{3.3V}{12V}\right) = 2.39\mu H$$

Using a 2.2µH inductor results in a maximum ripple current of:

$$\Delta I_L = \left(\frac{3.3V}{(1MHz)(2.2\mu H)}\right) \bullet \left(1 - \frac{3.3V}{12V}\right) = 1.1A$$

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. In this application, a tantalum capacitor will be used to provide the bulk capacitance and a ceramic capacitor in parallel to lower the total effective ESR. For this design, a 100µF ceramic capacitor will be used. C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = 2.5A \bullet \frac{3.3V}{12V} \bullet \sqrt{\frac{12V}{3.3V} - 1} = 1.12A_{RMS}$$

Decoupling the PV_{IN} pin with a 22µF ceramic capacitor is adequate for most applications.

The output voltage can now be programmed by choosing the values of R1 and R2. Choose R1 = 105k and calculate R2 as:

$$R2 = R1\left(\frac{V_{OUT}}{0.6V} - 1\right) = 472.5k$$

APPLICATIONS INFORMATION

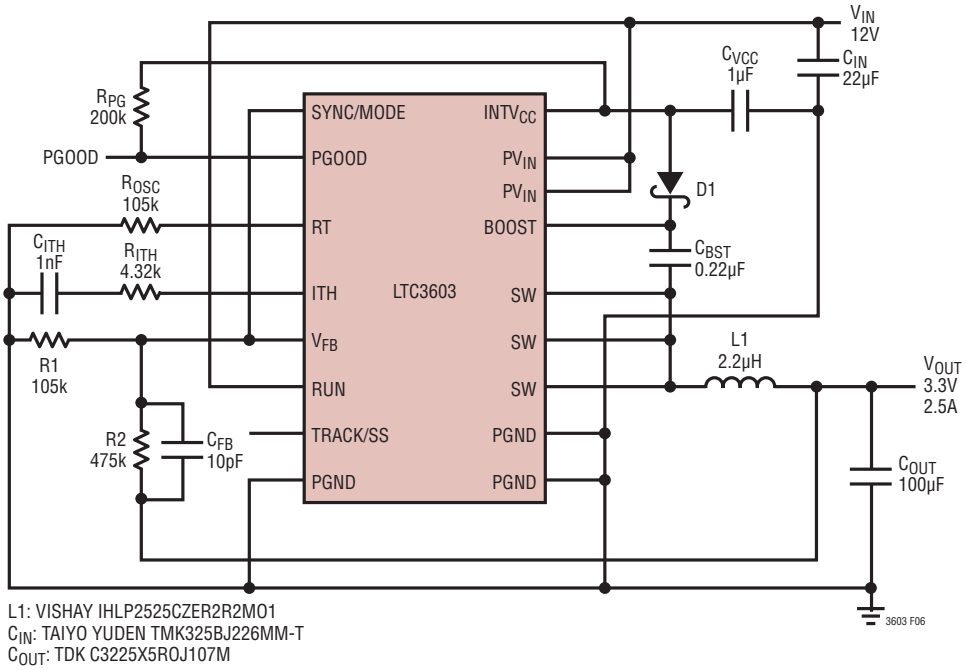


Figure 6. 12V to 3.3V, 2.5A Regulator at 1MHz, Burst Mode Operation

Choose a standard value of R2 = 475k. The voltage on the MODE pin will be set to 0.6V by tying the MODE pin to the FB pin. This will set the burst current equal to approximately 1A. Figure 6 shows a complete schematic for this design example.

How to Reduce SW Ringing

As with any switching regulator, there will be voltage ringing on the SW node, especially for high input voltages. The ringing amplitude and duration is dependent on the switching speed (gate drive), layout (parasitic inductance) and MOSFET output capacitance. This ringing contributes to the overall EMI, noise and high frequency ripple. One way to reduce ringing is to optimize layout. A good layout minimizes parasitic inductance. Adding an RC snubber from SW to GND is also an effective way to reduce ringing. Finally, adding a resistor (10Ω to 100Ω) in series with the BOOST pin will slow down the MOSFET turn-on slew rate and dampen ringing, but at the cost of reduced efficiency. Note that since the IC is buffered from high frequency transients by PCB and bondwire inductances, the ringing by itself is normally not a concern for reliability.

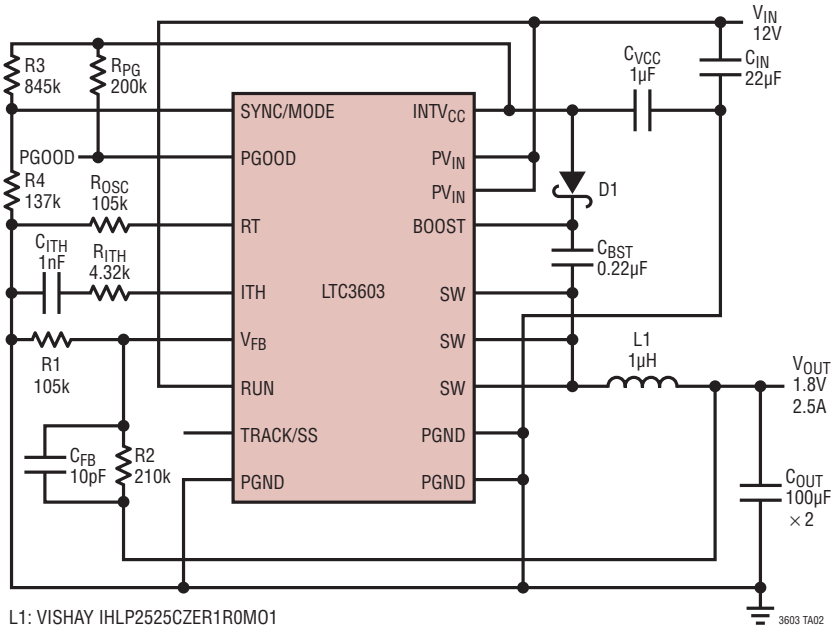
PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3603. Check the following in your layout:

1. A ground plane is recommended. If a ground plane layer is not used, the signal and power grounds should be segregated with all small-signal components returning to the SGND pin at one point which is then connected to the PGND pin close to the LTC3603.
2. Connect the (+) terminal of the input capacitor(s), C_{IN}, as close as possible to the PV_{IN} pin. This capacitor provides the AC current into the internal power MOSFETs.
3. Keep the switching node, SW, away from all sensitive small-signal nodes.
4. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. You can connect the copper areas to any DC net (PV_{IN}, $INTV_{CC}$, V_{OUT}, PGND, SGND, or any other DC rail in your system).

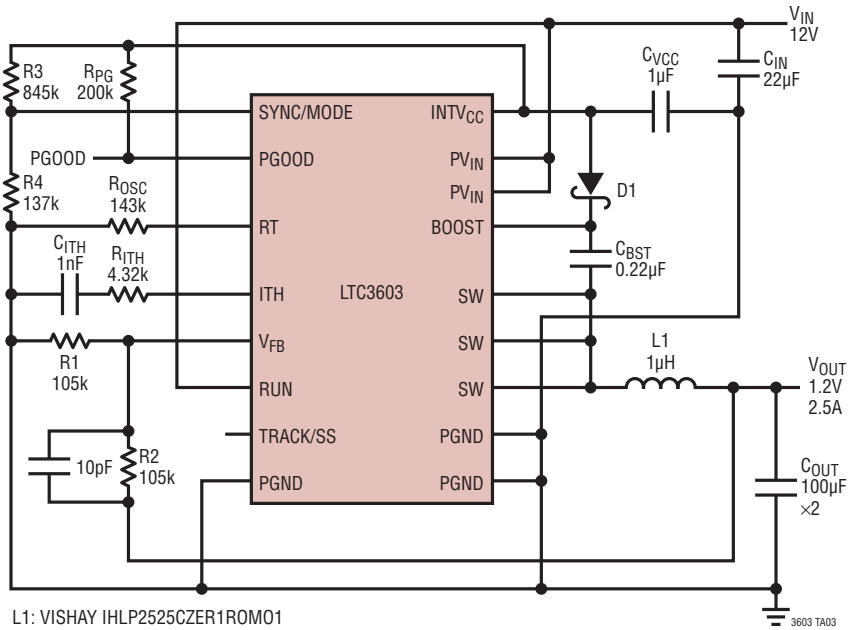
TYPICAL APPLICATIONS

1.8V, 2.5A Regulator at 1MHz, Burst Mode Operation



L1: VISHAY IHLP2525CZER1R0M01
C_{IN}: TAIYO YUDEN TMK325BJ226MM-T
C_{OUT}: TAIYO YUDEN AMK316BJ107ML

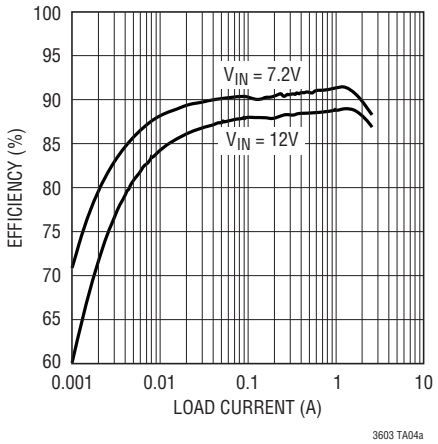
1.2V, 2.5A Regulator at 750kHz, Burst Mode Operation



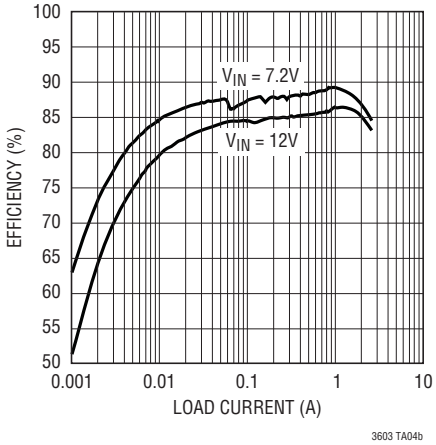
L1: VISHAY IHLP2525CZER1R0M01
C_{IN}: TAIYO YUDEN TMK325BJ226MM-T
C_{OUT}: TAIYO YUDEN AMK316BJ107ML

TYPICAL APPLICATIONS

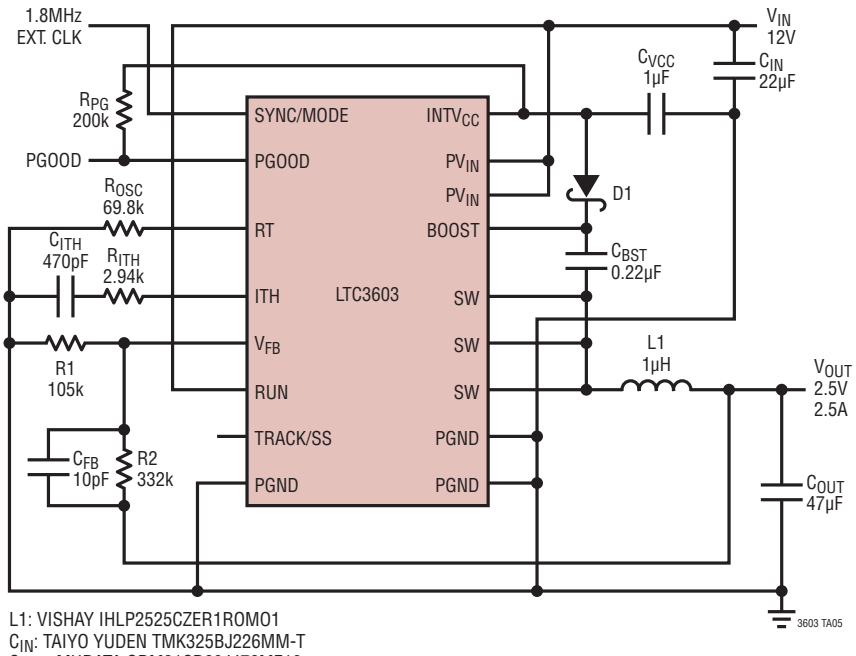
Efficiency vs Load Current, 1.8V Regulator at 1MHz, Burst Mode Operation



Efficiency vs Load Current, 1.2V Regulator at 750kHz, Burst Mode Operation



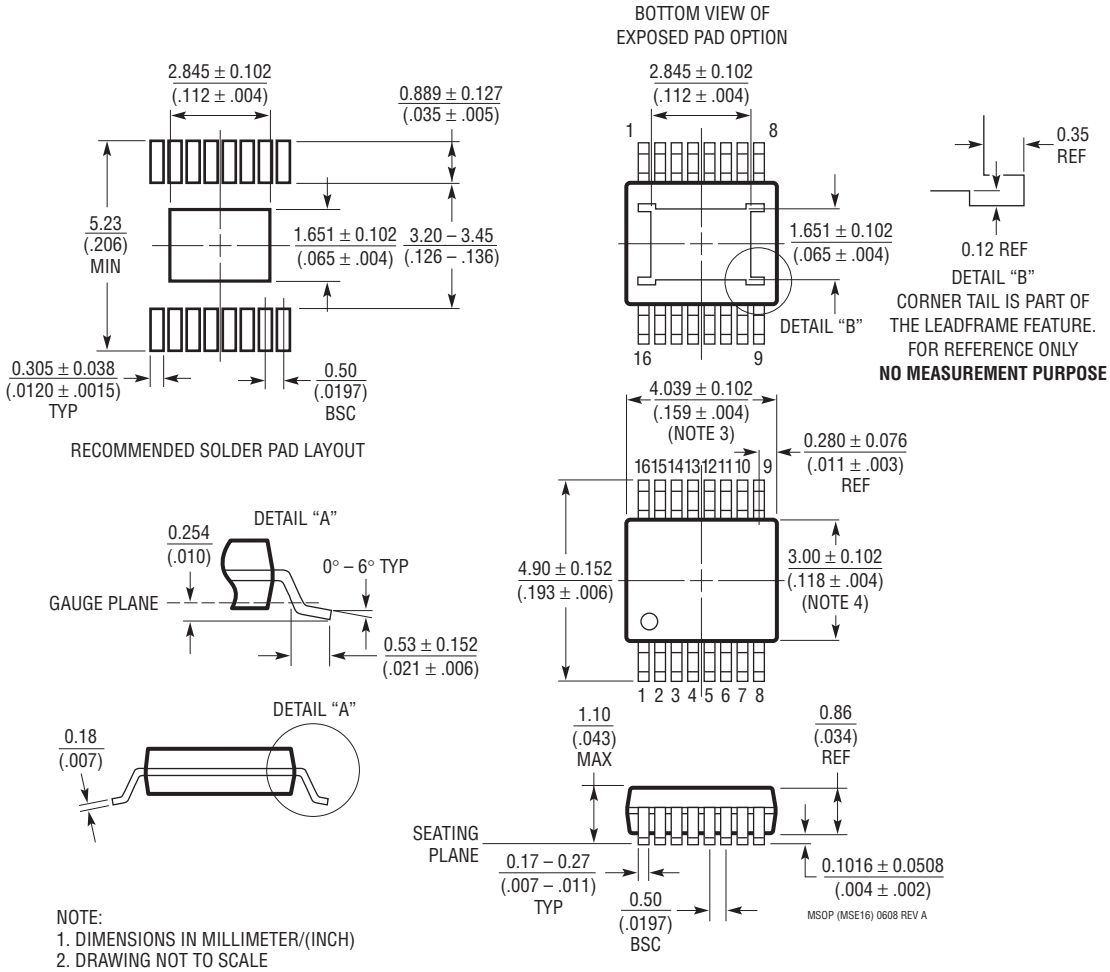
3.3V, 2.5A Regulator, Synchronized to 1.8MHz, Small Size



L1: VISHAY IHLP2525CZER1ROMO1
C_{IN}: TAIYO YUDEN TMK325BJ226MM-T
C_{OUT}: MURATA GRM31CR60J476ME19

PACKAGE DESCRIPTION

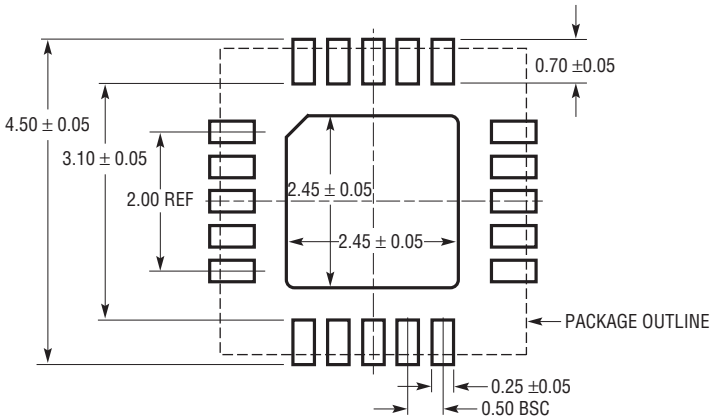
MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev A)



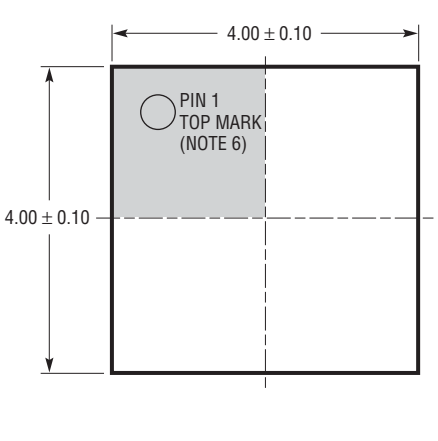
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

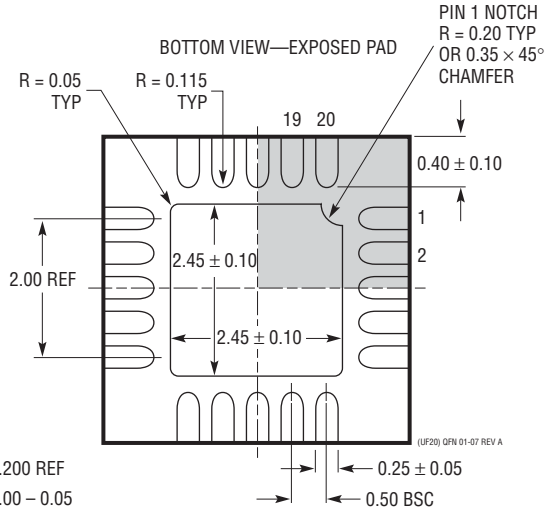
UF Package
20-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1710 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-1)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/09	Changes to Absolute Maximum Ratings	2
		Changes to Pin Configuration	2
		Change to Electrical Characteristics	3
		Text Changes to Pin Functions	6
		Change to Block Diagram	7
		Text Changes to Operation Section	8
		Text Changes to Applications Information Section	10, 12, 15
		“How to Reduce SW Ringing” Section Added	16
		Additions to Related Parts	22

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3601	15V, 1.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 14µA, 3mm × 3mm QFN16, MSOP16E
LTC3605	15V, 5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} < 15µA, 4mm × 4mm QFN24
LTC3609	32V, 6A (I_{OUT}), 1MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 32V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 900µA, I_{SD} < 15µA, 7mm × 8mm QFN52
LTC3612	6V, 3A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 70µA, I_{SD} < 1µA, 3mm × 4mm QFN20, TSSOP20E
LTC3412A	3A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, TSSOP16E, 4mm × 4mm QFN16
LTC3413	3A (I_{OUT} Sink/Source), 2MHz, Monolithic Synchronous Regulator for DDR/QDR Memory Termination	90% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = V_{REF}/2, I_Q = 280µA, I_{SD} < 1µA, TSSOP16E
LTC3414	4A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 64µA, I_{SD} < 1µA, TSSOP20E
LTC3415	7A (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 450µA, I_{SD} < 1µA, 5mm × 7mm QFN38
LTC3416	4A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter with Tracking	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 64µA, I_{SD} < 1µA, TSSOP20E
LTC3418	8A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 380µA, I_{SD} < 1µA, 5mm × 7mm QFN38
LTC3602	10V, 2.5A (I_{OUT}), 3MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 10V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, TSSOP16E, 4mm × 4mm QFN20
LTC3608	18V, 8A (I_{OUT}), 1MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 18V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 900µA, I_{SD} < 15µA, 5mm × 7mm QFN52
LTC3610	24V, 12A (I_{OUT}), 1MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 24V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 900µA, I_{SD} < 15µA, 9mm × 9mm QFN64
LTC3611	32V, 10A (I_{OUT}), 1MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 32V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 900µA, I_{SD} < 15µA, 9mm × 9mm QFN64

ThinSOT is a trademark of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 1209 REV A • PRINTED IN USA
© LINEAR TECHNOLOGY CORPORATION 2009