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June 2014

FQA24N60

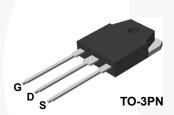
N-Channel QFET® MOSFET 600 V, 23.5 A, 240 m Ω

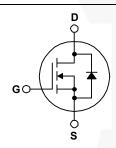
Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 23.5 A, 600 V, $R_{DS(on)}$ = 240 m Ω (Max.) @ V_{GS} = 10 V, I_D = 11.8 A
- · Low Gate Charge (Typ. 110 nC)
- Low Crss (Typ. 56 pF)
- · 100% Avalanche Tested





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQA24N60	Unit
V _{DSS}	Drain-Source Voltage		600	V
I _D	Drain Current - Continuous (T _C = 25°C	C)	23.5	А
	- Continuous (T _C = 100°	°C)	14.9	Α
I _{DM}	Drain Current - Pulsed	(Note 1)	94	А
V _{GSS}	Gate-Source Voltage		± 30	V
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	1300	mJ
I _{AR}	Avalanche Current	(Note 1)	23.5	Α
E _{AR}	Repetitive Avalanche Energy	(Note 1)	31	mJ
dv/dt	Peak Diode Recovery dv/dt (4.5	V/ns
P_{D}	Power Dissipation (T _C = 25°C)		310	W
	- Derate above 25°C		2.5	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQA24N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.4	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.24	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	°C/W

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQA24N60	FQA24N60	TO-3PN	Tube	N/A	N/A	30 units

Electrical Characteristics T_c = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Cha	aracteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	600			V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.6		V/°C
I _{DSS}	Zana Cata Maltana Duain Courset	V _{DS} = 600 V, V _{GS} = 0 V			10	μΑ
Zero Gate Voltage Drain Cu	Zero Gate Voltage Drain Current	V _{DS} = 480 V, T _C = 125°C			100	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Cha	aracteristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	3.0		5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 11.8 A		0.18	0.24	Ω
g _{FS}	Forward Transconductance	V _{DS} = 50 V, I _D = 11.8 A		22.5		S
Dynam	ic Characteristics					
C _{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$		4200	5500	pF
C _{oss}	Output Capacitance	f = 1.0 MHz		550	720	pF
C _{rss}	Reverse Transfer Capacitance			56	75	pF
Switchi	ing Characteristics					
t _{d(on)}	Turn-On Delay Time	V _{DD} = 300 V, I _D = 23.5 A,		90	190	ns
t _r	Turn-On Rise Time	$R_G = 25 \Omega$		270	550	ns
t _{d(off)}	Turn-Off Delay Time			200	410	ns
t _f	Turn-Off Fall Time	(Note 4)		170	350	ns
Qg	Total Gate Charge	V _{DS} = 480 V, I _D = 23.5 A,		110	145	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10 V	/	25		nC
Q _{gd}	Gate-Drain Charge	(Note 4)	/	53		nC
Drain-S	Source Diode Characteristics a	nd Maximum Ratings				
l _S	Maximum Continuous Drain-Source Diode Forward Current				23.5	Α
I _{SM}	Maximum Pulsed Drain-Source Diode F	orward Current			94	Α
V_{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 23.5 A			1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 23.5 A,		470	/	ns
^	n n	41 / 44 - 400 A / 4				

Q_{rr}

- Notes: Notes: A Repetitive rating: pulse-width limited by maximum junction temperature. 2. L = 4.3 mH, I_{AS} = 23.5 A, V_{DD} = 50 V, R_{C} = 25 Ω , starting T_{J} = 25°C. 3. I_{SD} ≤ 23.5 A, di/dt ≤ 200 A/ μ s, V_{DD} ≤ BV $_{DSS}$, starting T_{J} = 25°C. 4. Essentially independent of operating temperature.

Reverse Recovery Charge

μС

6.2

 $dI_F / dt = 100 A/\mu s$

Typical Characteristics

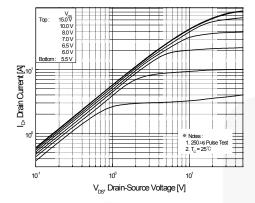


Figure 1. On-Region Characteristics

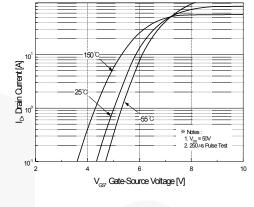


Figure 2. Transfer Characteristics

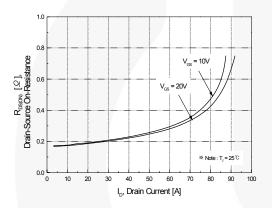


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

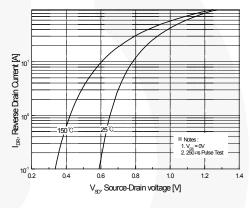


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

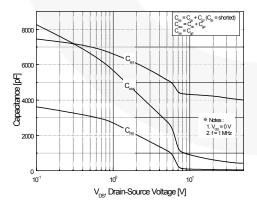


Figure 5. Capacitance Characteristics

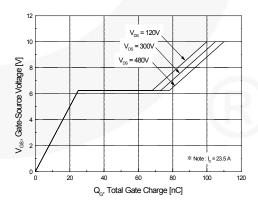


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

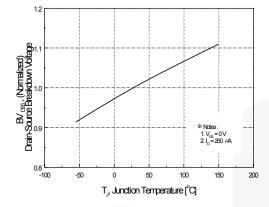


Figure 7. Breakdown Voltage Variation vs. Temperature

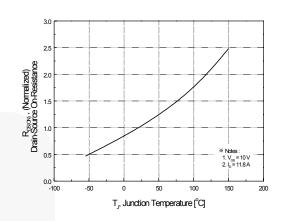


Figure 8. On-Resistance Variation vs. Temperature

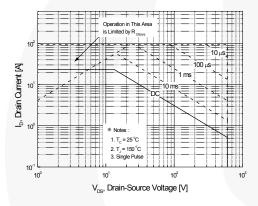


Figure 9. Maximum Safe Operating Area

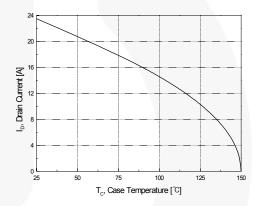


Figure 10. Maximum Drain Current vs. Case Temperature

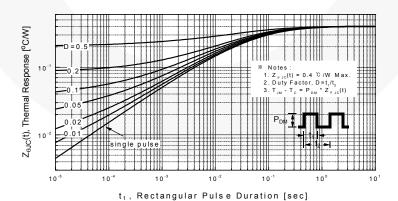


Figure 11. Transient Thermal Response Curve

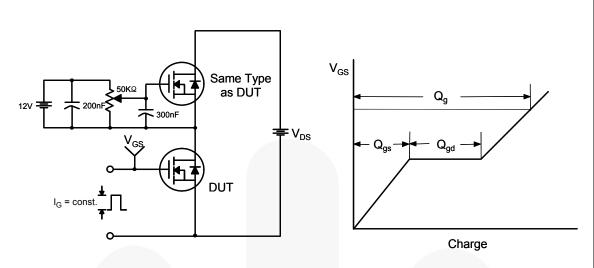


Figure 12. Gate Charge Test Circuit & Waveform

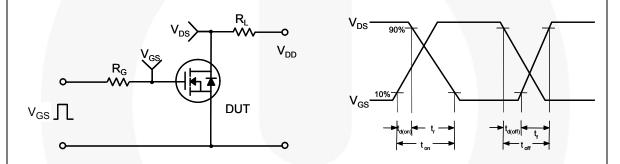


Figure 13. Resistive Switching Test Circuit & Waveforms

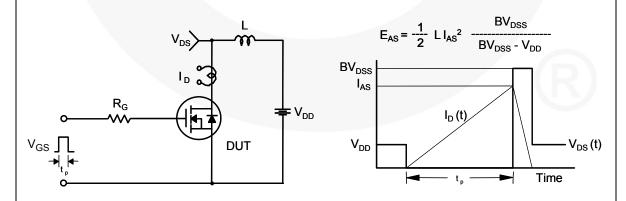
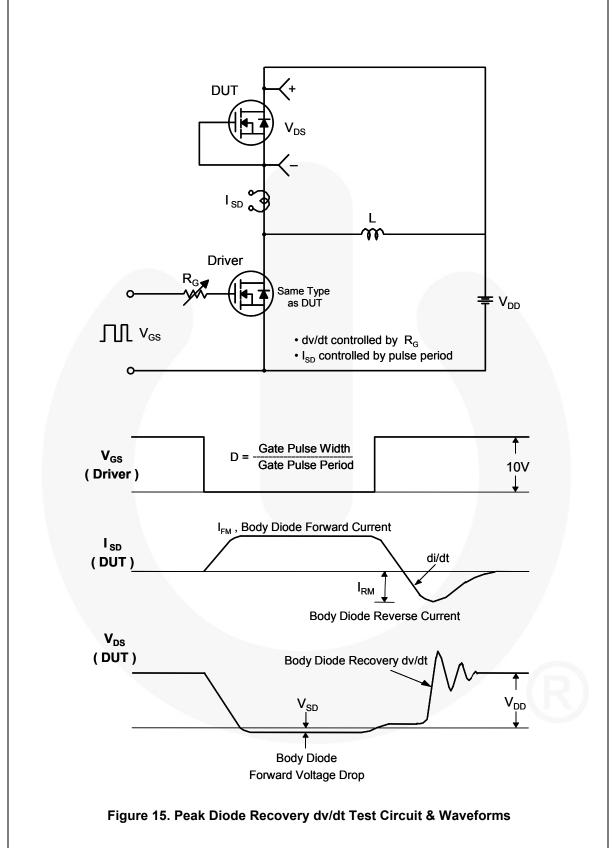
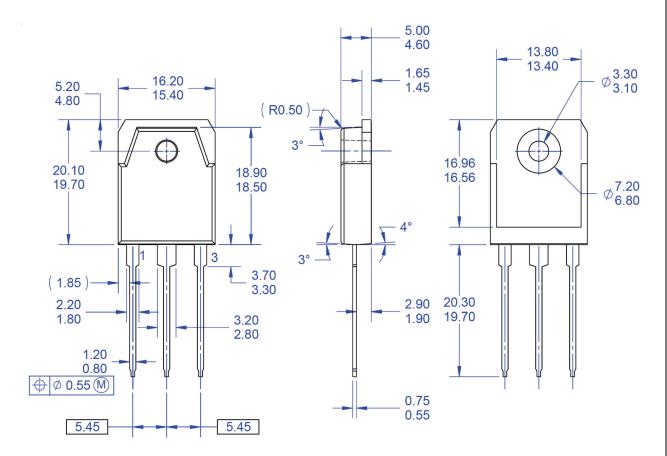
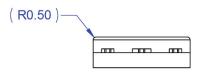


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Mechanical Dimensions





NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSION AND TOLERANCING PER ASME14.5-2009.
- D) DIMENSIONS ARE EXCLUSSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSSIONS. DRAWING FILE NAME: TO3PN03AREV1.
- F) FAIRCHILD SEMICONDUCTOR.

Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65

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