PR601

High performance NFC integrated reader solution

Rev. 3.3 — 10 March 2016
219333

Product data sheet
COMPANY PUBLIC

1. Introduction

Delivering unprecedented integration, these module combines the functionality of multiple discrete ICs in a single package and enables the development of compact, cost-effective contactless reader systems for access and industrial applications. The module includes microcontroller functionality and support of multiple contactless reader protocols based on 13.56 MHz.

The package contains two dies:

1. LPC1227FBD48/301
2. CLRC66301HN1

Not all pins of the LPC1227 specified in the data sheet are available at the reader module. Please refer to Section 9 “Pinning information”.

The device does not implement any interconnection inside the package. This enables easy access to all signals during system development.

2. General description

2.1 CLRC663

The CLRC663 is a highly integrated transceiver IC for contactless communication at 13.56 MHz. This transceiver IC utilizes an outstanding modulation and demodulation concept completely integrated for different kinds of contactless communication methods and protocols at 13.56 MHz.

The CLRC663 transceiver ICs support following different operating modes:

- Reader/Writer mode supporting ISO/IEC 14443A/MIFARE
- Reader/Writer mode supporting ISO/IEC 14443B
- Reader/Writer mode supporting FeliCa scheme
- Reader/Writer mode supporting ISO/IEC 15693
- Reader/Writer mode supporting ICODE EPC UID/ EPC OTP
- Reader/Writer mode supporting ISO/IEC 18000-3 Mode 3
- NFC P2P passive initiator

The CLRC663 internal transmitter is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443A/MIFARE cards and transponders without additional active circuitry. The receiver module provides a robust and efficient implementation for

demodulation and decoding signals from ISO 14443A/MIFARE compatible cards and transponders. The digital module manages the complete ISO 14443A framing and error detection (parity and CRC) functionality. The CLRC663 supports MIFARE 1K, MIFARE 4K, MIFARE Ultralight, MIFARE, Ultralight C, MIFARE PLUS and MIFARE DESFire products. The CLRC663 supports contactless communication and uses MIFARE higher transfer speeds up to 848 kBd in both directions.

The CLRC663 supports all layers of the ISO/IEC 14443B reader/writer communication scheme, given correct implementation of additional components, like oscillator, power supply, coil etc. and provided that standardized protocols, for example, like ISO/IEC 14443-4 and/or ISO/IEC 14443B anticollision are correctly implemented.

Enabled in Reader/Writer mode for FeliCa, the CLRC663 transceiver IC supports the FeliCa communication scheme. The receiver part provides a robust and efficient implementation of the demodulation and decoding circuitry for FeliCa coded signals. The digital part handles the FeliCa framing and error detection like CRC. The CLRC663 supports contactless communication using FeliCa Higher transfer speeds up to 424 kbit/s in both directions. The CLRC663 supports vicinity protocol according to ISO/IEC15693, EPC UID and ISO/IEC 18000-3 mode 3. The complete vicinity product family of NXP is supported and enable a readability for mid-ranger reader applications.

The following host interfaces are provided:

- Serial Peripheral Interface (SPI)
- Serial UART (similar to RS232 with voltage levels dependent on pin voltage supply)
- I^2C-bus interface (two versions are implemented: I2C and I2CL)

2.2 LPC1227

The LPC1227 are ARM Cortex-M0-based microcontrollers for embedded applications featuring a high level of integration and low-power consumption. The ARM Cortex-M0 is a next generation core that offers system enhancements such as enhanced debug features and a higher level of support block integration. In addition to the ARM Cortex-M0, the LPC1X features an event handler API to limit the interrupt load of the ARM Cortex-M0 CPU and to allow for additional power-savings by off-loading event handling from the main CPU.

The LPC1227 operates at CPU frequencies of up to 33 MHz and include up to 128 kB of flash memory and 8 kB of data memory.

Not all connections of the LPC1227 product are implemented by the PR601.

3. Features and benefits

- Fully compliant with ISO/IEC 14443 A and B, ISO/IEC 15693 and FeliCa
- Support for MIFARE technology
- NFC-IP1 peer-to-peer support (Passive Initiator Mode)
- Compatibility with all established smartcard ICs, smart tags, and label technologies
- Support for SAM AV 2.6 interface
- Integrating multiple functions in a single package
- Integrated LPC1227 ARM Cortex-M0 microcontroller

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- Reduced PCB size for development of systems with small physical dimensions
- Compact, single-package: LQFP100
- Fast design-in with supplied firmware

4. Applications

- Highly integrated access systems
- Industrial devices requiring high-performance RF

5. Quick reference data

Table 1. Quick reference data[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD(LPC1227)	supply voltage LPC1227		3.0	3.3	3.6	V
VDD(CLRC663)	supply voltage CLRC663		3.0	5.0	5.5	V
T_{amb}	ambient temperature		–25	+25	+70	°C

[1] Refer to the specification of integrated products for quick reference data details

6. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PR601HL/C1	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

7. Marking

Table 3. Marking codes

Type number	Marking code
PR601HL/C1	
1st line	product type
2nd line	1st die diffusion number
3rd line	weekcode
4th line	2nd and 3rd die diffusion number
5th line (optional)	additional information

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8. Block diagram

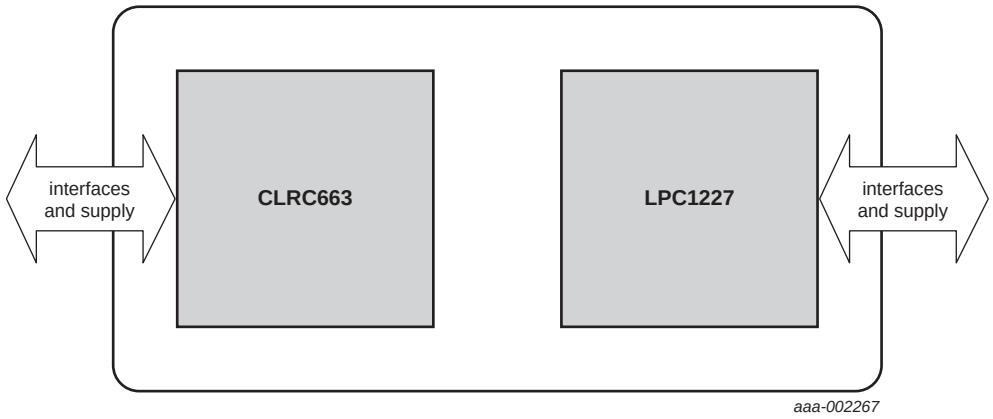

Fig 1. Block diagram

9. Pinning information

9.1 Pinning

Table 4. Pin allocation table

Pin	Symbol	Connection
1	PIO0_10	LPC1227
2	PIO0_11	LPC1227
3	PIO0_12	LPC1227
4	nRESET/PIO0_13	LPC1227
5	PIO0_14	LPC1227
6	PIO0_15	LPC1227
7	PIO0_16	LPC1227
8	PIO0_17	LPC1227
9	PIO0_18	LPC1227
10	PIO0_30	LPC1227
11	PIO0_31	LPC1227
12	PIO1_0	LPC1227
13	PIO1_1	LPC1227
14	GND	all
15	PIO1_2	LPC1227
16	PIO1_3/WAKEUP	LPC1227
17	PIO1_4	LPC1227
18	PIO1_5	LPC1227
19	PIO1_6	LPC1227
20	VSS	LPC1227
21	VDD(3V3)	LPC1227

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Table 4. Pin allocation table *...continued*

Pin	Symbol	Connection
22	RTCXOUT	LPC1227
23	RTCXIN	LPC1227
24	VDDIO	LPC1227
25	VSSIO	LPC1227
26	n.c.	-
27	n.c.	-
28	n.c.	-
29	n.c.	-
30	n.c.	-
31	n.c.	-
32	n.c.	-
33	n.c.	-
34	AVDD	CLRC663
35	AUX1	CLRC663
36	AUX2	CLRC663
37	RXP	CLRC663
38	RXN	CLRC663
39	VMID	CLRC663
40	TX2	CLRC663
41	TVSS	CLRC663
42	GND	CLRC663
43	TX1	CLRC663
44	TVDD	CLRC663
45	XTAL1	CLRC663
46	n.c.	-
47	XTAL2	CLRC663
48	n.c.	-
49	PD	CLRC663
50	n.c.	-
51	CLKOUT	CLRC663
52	SCL	CLRC663
53	SDA	CLRC663
54	PVDD	CLRC663
55	IFSEL0	CLRC663
56	IFSEL1	CLRC663
57	IF0	CLRC663
58	IF1	CLRC663
59	IF2	CLRC663
60	IF3	CLRC663
61	IRQ	CLRC663
62	GND	CLRC663

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Table 4. Pin allocation table *...continued*

Pin	Symbol	Connection
63	TDO	CLRC663
64	TDI	CLRC663
65	TMS	CLRC663
66	TCK	CLRC663
67	SIGIN	CLRC663
68	SIGOUT	CLRC663
69	DVDD	CLRC663
70	VDDS	CLRC663
71	n.c.	-
72	n.c.	-
73	n.c.	-
74	n.c.	-
75	n.c.	-
76	XTALIN	LPC1227
77	XTALOUT	LPC1227
78	VREF_COMP	LPC1227
79	PIO0_19	LPC1227
80	PIO0_20	LPC1227
81	PIO0_21	LPC1227
82	PIO0_22	LPC1227
83	PIO0_23	LPC1227
84	PIO0_24	LPC1227
85	PIO0_25	LPC1227
86	PIO0_26	LPC1227
87	PIO0_27	LPC1227
88	GND	all
89	PIO0_28	LPC1227
90	PIO0_29	LPC1227
91	PIO0_0	LPC1227
92	PIO0_1	LPC1227
93	PIO0_2	LPC1227
94	PIO0_3	LPC1227
95	PIO0_4	LPC1227
96	PIO0_5	LPC1227
97	PIO0_6	LPC1227
98	PIO0_7	LPC1227
99	PIO0_8	LPC1227
100	PIO0_9	LPC1227

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9.2 Pin description

For a description of the detailed pin functionality refer to the relevant product data sheet.

VSS and GND refer to the same signal and need all be connected.

10. Functional description

The functionality of this device is defined by the functionality of the 2chips CLRC663 and LPC1227. No internal connection of the devices had been implemented except for the GND signal. All external available GND signals need to be connected. A design making use of this device shall consider a sufficient low thermal resistance between package and environment. All pins are recommended to be connected to defined signal levels. A PCB design using the PR601 shall make use of state of the art design practices to ensure a sufficient heat dissipation. For a detailed functionality refer to the latest product specifications of the CLRC663 and LPC1227.

11. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
P_{tot}	total power dissipation	ambient temperature 25 °C, package soldered on PCB	-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	1500	-	V

12. Characteristics

Table 6. Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(LPC)}$	supply voltage of LPC1227 die		3.0	3.3	3.6	V
$V_{DD(CLRC)}$	supply voltage of CLRC663 die		3.0	5.0	5.5	V
T_{amb}	ambient temperature		–25	+25	+70	°C
$f_{osc(RC)}$	LPC1227 internal RC oscillator frequency		11.76	12.00	12.24	MHz
$I_{DD(TVDD)}$	TVDD supply current	CLRC663 die transmitter supply current	-	100	200	mA

[1] For a detailed information of the characteristics refer to the data sheets of the packaged products

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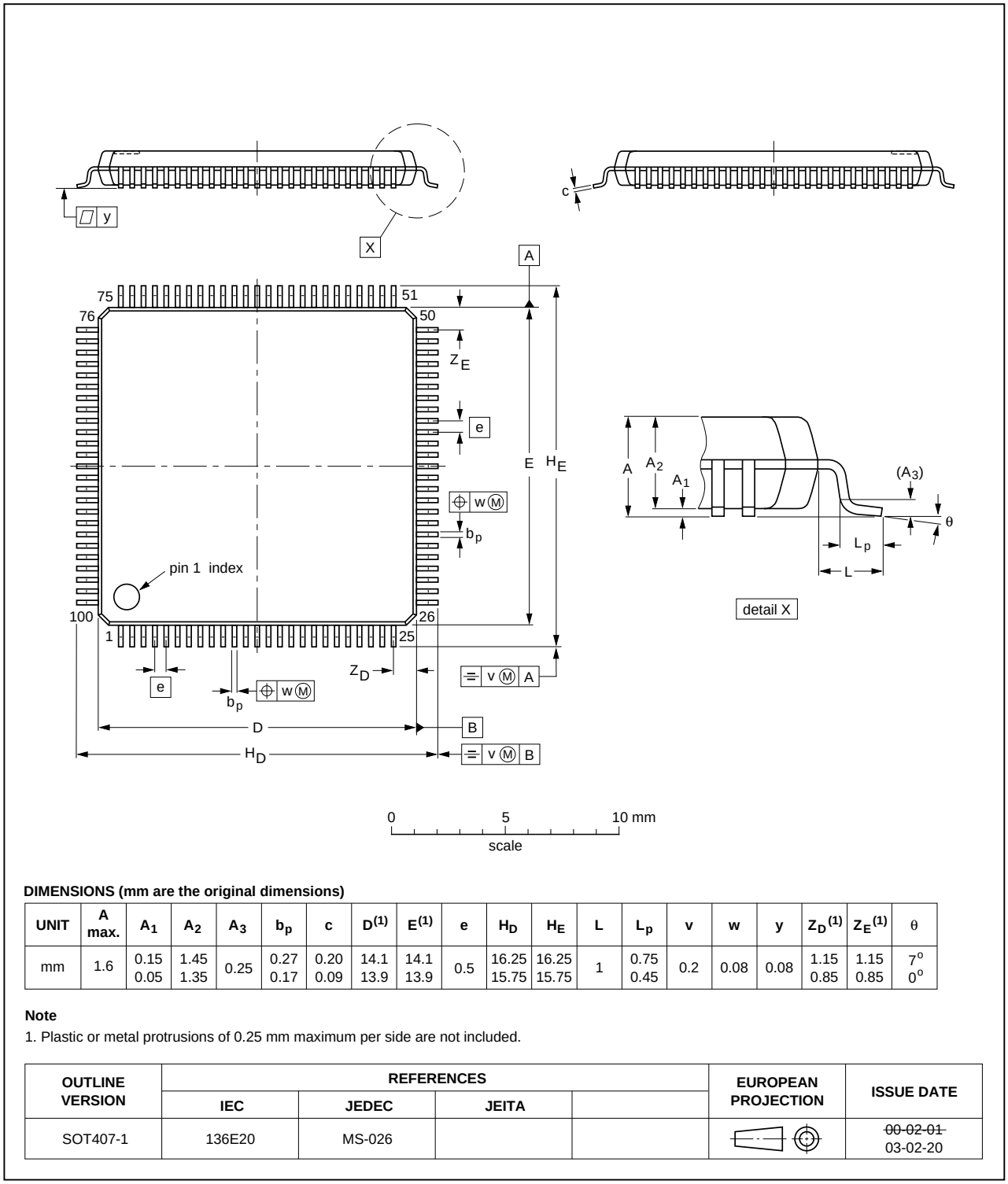
13. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 2. Package outline LQFP100 (SOT407-1)

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14. Handling information

Moisture Sensitivity Level (MSL) evaluation has been performed according to *SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C)*.

MSL for this package is level 2 which means 260 °C convection reflow temperature.

Dry pack is required.

1 year out-of-pack floor life at maximum ambient temperature 30 °C/ 85 % RH.

15. Packing information

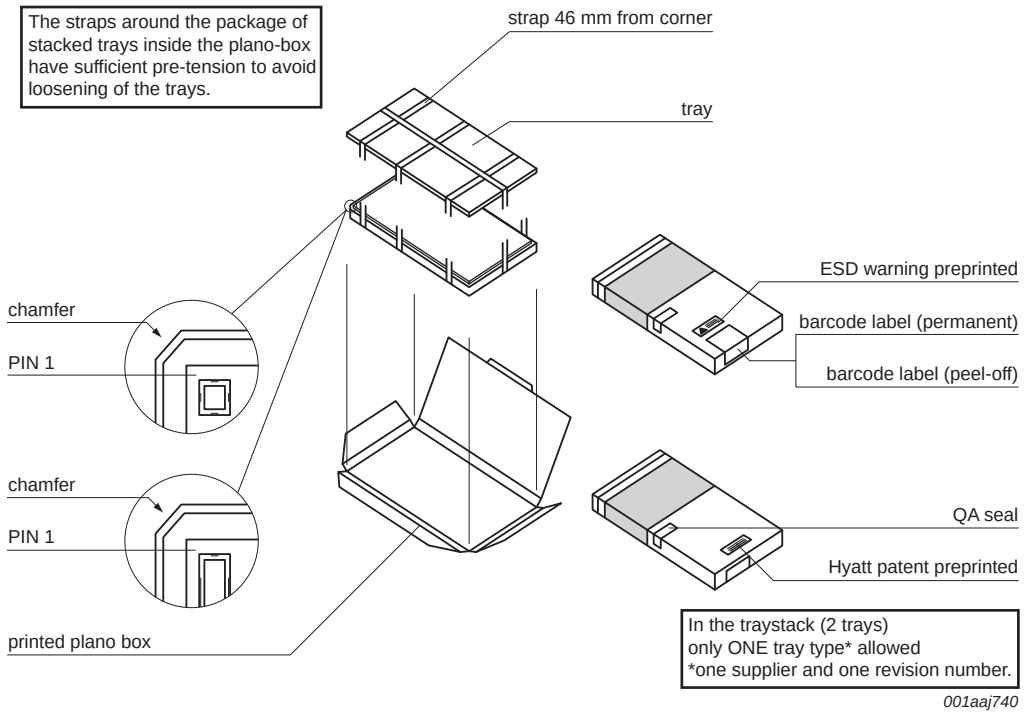

Fig 3. Packing information 1 tray

16. Abbreviations

Table 7. Abbreviations

Acronym	Description
EPC	Electronic Product Code
OTP	One Time Programmable
SPI	Serial Peripheral Interface
UID	Unique IDentification

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17. Glossary

Die — unpackaged chip of a product

18. References

[1] **Data sheet —** *CLRC663, Contactless reader IC*, BU-ID Document number 1711**[1]

[2] **Data sheet —** *LPC122x, 32-bit ARM Cortex-M0 microcontroller; up to 128 kB flash and 8 kB SRAM*

1. ** .. document version number

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19. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PR601 v. 3.3	20160310	Product data sheet	-	PR601 v. 3.2
Modifications:	• Table 6 “Characteristics[1]”: TVDD supply current values added			
PR601 v. 3.2	20160111	Product data sheet	-	PR601 v. 3.1
Modifications:	• Section 2.1 “CLRC663”: License statement updated • Section 20.4 “Licenses”: License statement “Purchase of NXP ICs with NFC technology” updated			
PR601 v. 3.1	20141021	Product data sheet	-	PR601 v. 3.0
Modifications:	• Table 4 “Pin allocation table”: corrected • Section 3 “Features and benefits”: updated • Descriptive title changed			
PR601 v. 3.0	20121112	Product data sheet	-	PR601 v. 1.1
Modifications:	• Figure 1 “Block diagram”: corrected from LPC1127 into LPC1227 • Data sheet status changed to “Product data sheet”			
PR601 v. 1.1	20120919	Objective data sheet	-	PR601 v. 1.0
Modifications:	• General update			
PR601 v. 1.0	20120314	Objective data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
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[2] The term 'short data sheet' is explained in section "Definitions".

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