19-1815; Rev 0; 10/00

EVALUATION KIT AVAILABLE

Low-Jitter, 10-Port LVDS Repeater

General Description

The MAX9150 low-jitter, 10-port, low-voltage differential signaling (LVDS) repeater is designed for applications that require high-speed data or clock distribution while minimizing power, space, and noise. The device accepts a single LVDS input and repeats the signal at 10 LVDS outputs. Each differential output drives a total of 50Ω, allowing point-to-point distribution of signals on transmission lines with 100Ω terminations on each end.

Ultra-low 120ps (max) peak-to-peak jitter (deterministic and random) ensures reliable communication in high-speed links that are highly sensitive to timing error, especially those incorporating clock-and-data recovery, or serializers and deserializers. The high-speed switching performance guarantees 400Mbps data rate and less than 100ps skew between channels while operating from a single +3.3V supply.

Supply current at 400Mbps is 160mA (max) and is reduced to 60µA (max) in low-power shutdown mode. Inputs and outputs conform to the EIA/TIA-644 LVDS standard. A fail-safe feature sets the outputs high when the input is undriven and open, terminated, or shorted. The MAX9150 is available in a 28-pin TSSOP package.

Refer to the MAX9110/MAX9112 and MAX9111/MAX9113 data sheets for LVDS line drivers and receivers.

Applications

Cellular Phone Base Stations

Add/Drop Muxes

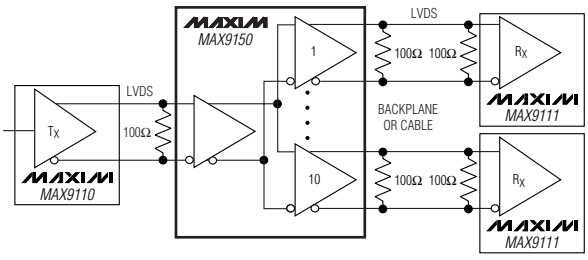
Digital Crossconnects

Network Switches/Routers

Backplane Interconnect

Clock Distribution

Typical Application Circuit



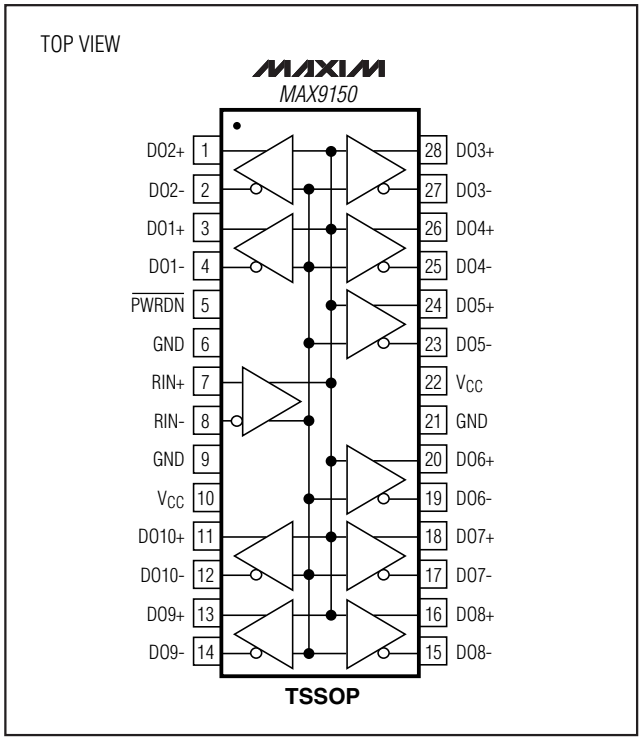
Features

- **Ultra-Low 120ps$_{p-p}$ (max) Total Jitter (Deterministic and Random)**
- **100ps (max) Skew Between Channels**
- **Guaranteed 400Mbps Data Rate**
- **60µA Shutdown Supply Current**
- **Conforms to EIA/TIA-644 LVDS Standard**
- **Single +3.3V Supply**
- **Fail-Safe Circuit Sets Output High for Undriven Inputs**
- **High-Impedance LVDS Input when V_{CC} = 0**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX9150EUI	-40°C to +85°C	28 TSSOP

Pin Configuration



For price, delivery, and to place orders, please contact Maxim Distribution at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Low-Jitter, 10-Port LVDS Repeater

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.0V
RIN+, RIN- to GND .....-0.3V to +4.0V
$\overline{PWRDN}$ to GND.....-0.3V to (V_{CC} + 0.3V)
DO_+, DO_-.....-0.3V to +4.0V
Short-Circuit Duration (DO_+, DO_-) .....Continuous
Continuous Power Dissipation (T_A = +70°C)
28-Pin TSSOP (derate 12.8mW/°C above +70°C) 1026mW
Storage Temperature.....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Operating Temperature Range.....-40°C to +85°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 50Ω ±1%, $|V_{ID}|$ = 0.1V to 1.0V, V_{CM} = $|V_{ID} / 2|$ to 2.4V - $|V_{ID} / 2|$, $\overline{PWRDN}$ = high, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{PWRDN}$						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	V_{IN} = V_{CC} and 0	-15		15	µA
LVDS INPUT						
Differential Input High Threshold	V_{TH}			7	100	mV
Differential Input Low Threshold	V_{TL}		-100	-7		mV
Single-Ended Input Current	I_{IN}	$\overline{PWRDN}$ = high or low; V_{RIN+} = 2.4V, RIN- = open or RIN+ = open, V_{RIN-} = 2.4V	-6		+1	µA
		$\overline{PWRDN}$ = high or low; V_{RIN+} = 0, RIN- = open or RIN+ = open, V_{RIN-} = 0	-18		+1	
Power-Off Single-Ended Input Current	$I_{IN(OFF)}$	V_{CC} = 0; V_{RIN+} = 2.4V, RIN- = open or RIN+ = open, V_{RIN-} = 2.4V	-1		+12	µA
Differential Input Resistance	RI_{DIFF}	V_{CC} = +3.6V or 0, $\overline{PWRDN}$ = high or low	5			kΩ
LVDS DRIVER						
Differential Output Voltage	V_{OD}	Figure 1	250	320	450	mV
Change in VOD Between Complementary Output States	ΔV_{OD}	Figure 1			25	mV
Offset (Common-Mode) Voltage	V_{OS}	Figure 1	0.90	1.25	1.375	V
Change in VOS Between Complementary Output States	ΔV_{OS}	Figure 1			25	mV
Output High Voltage	V_{OH}	Figure 1			1.6	V
Output Low Voltage	V_{OL}	Figure 1	0.7			V
Differential Output Resistance (Note 2)	RO_{DIFF}	V_{CC} = +3.6V or 0, $\overline{PWRDN}$ = high or low	150	240	330	Ω
Differential High Output Voltage in Fail-Safe	V_{OD+}	R_{IN+}, R_{IN-} undriven with short, open, or 100Ω termination	250		450	mV
Output Short-Circuit Current	I_{SC}	V_{ID} = +100mV, V_{DO_+} = GND	-15			mA
		V_{ID} = -100mV, V_{DO_-} = GND				

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, R_L = 50Ω ±1%, $|V_{ID}|$ = 0.1V to 1.0V, V_{CM} = $|V_{ID} / 2|$ to 2.4V - $|V_{ID} / 2|$, $\overline{PWRDN}$ = high, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Single-Ended Output High-Impedance Current	I_{OZ}	V_{CC} = 0, $\overline{PWRDN}$ = GND; V_{DO_+} = 3.6V or 0, DO_- = open; or V_{DO_-} = 3.6V or 0, DO_+ = open		-1		+1	µA
		$\overline{PWRDN}$ = GND; V_{DO_+} = 3.6V or 0, DO_- = open; or V_{DO_-} = 3.6V or 0, DO_+ = open		-1		+1	µA
SUPPLY CURRENT							
Supply Current (Note 2)	I_{CC}	DC	Figure 2		100	140	mA
		200MHz (400Mbps)			130	160	
Power-Down Supply Current	I_{CCZ}	$\overline{PWRDN}$ = GND				60	µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 50Ω ±1%, C_L = 5pF, $|V_{ID}|$ = 0.2V to 1.0V, V_{CM} = $|V_{ID} / 2|$ to 2.4V - $|V_{ID} / 2|$, $\overline{PWRDN}$ = high, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 2–5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Propagation Delay High-to-Low	t_{PHLD}	Figures 2, 3	1.6	2.2	3.5	ns
Differential Propagation Delay Low-to-High	t_{PLHD}	Figures 2, 3	1.6	2.2	3.5	ns
Total Peak-to-Peak Jitter (Random and Deterministic) (Note 6)	t_{JPP}	Figures 2, 3		20	120	ps_{p-p}
Differential Output-to-Output Skew (Note 7)	t_{SKOO}	Figures 2, 3		40	100	ps
Differential Part-to-Part Skew (Note 8)	t_{SKPP}	Figures 2, 3			1.9	ns
Rise/Fall Time	T_{TLH}, t_{THL}	Figures 2, 3	150	220	450	ps
Maximum Input Frequency (Note 9)	f_{MAX}	Figures 2, 3	400			Mbps

Low-Jitter, 10-Port LVDS Repeater

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, R_L = 50Ω ±1%, C_L = 5pF, $|V_{ID}|$ = 0.2V to 1.0V, V_{CM} = $|V_{ID} / 2|$ to 2.4V - $|V_{ID} / 2|$, $\overline{PWRDN}$ = high, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Notes 2–5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Down Time	t_{PD}	Figures 4, 5			100	ns
Power-Up Time	t_{PU}				100	µs

Note 1: Current-into-device pins is defined as positive. Current-out-of-device pins is defined as negative. All voltages are referenced to ground, except V_{TH}, V_{TL}, V_{OD}, and ΔV_{OD}.

Note 2: Guaranteed by design, not production tested.

Note 3: AC parameters are guaranteed by design and characterization.

Note 4: C_L includes scope probe and test jig capacitance.

Note 5: Signal generator conditions, unless otherwise noted: frequency = 200MHz, 50% duty cycle, R_O = 50Ω, t_R = 1ns, and t_F = 1ns (0% to 100%).

Note 6: Signal generator conditions for t_{JPP}: V_{OD} = 200mV, V_{OS} = 1.2V, frequency = 200MHz, 50% duty cycle, R_O = 50Ω, t_R = 1ns, and t_F = 1ns (0% to 100%. t_{JPP} includes pulse (duty cycle) skew.

Note 7: t_{SKOO} is the magnitude difference in differential propagation delay between outputs for a same-edge transition.

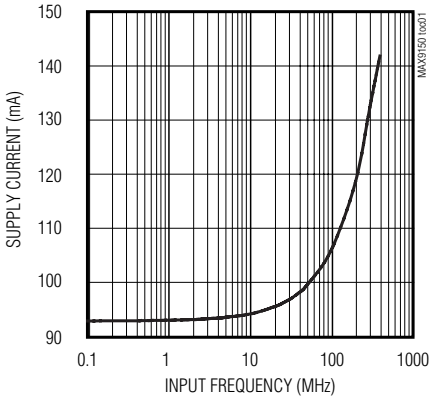
Note 8: t_{SKPP} is the |MAX - MIN| differential propagation delay.

Note 9: Device meets V_{OD} and AC specifications while operating at f_{MAX}.

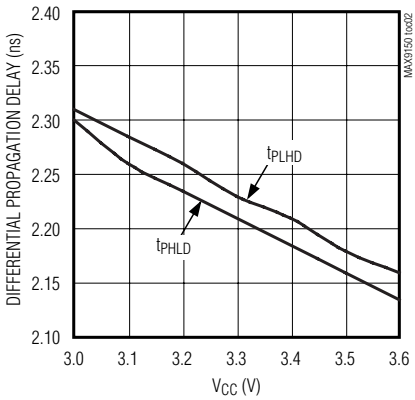
Typical Operating Characteristics

(Figure 2, V_{CC} = +3.3V, R_L = 50Ω, C_L = 5pF, $|V_{ID}|$ = 200mV, V_{CM} = 1.2V, f_{IN} = 50MHz, T_A = +25°C, unless otherwise noted.)

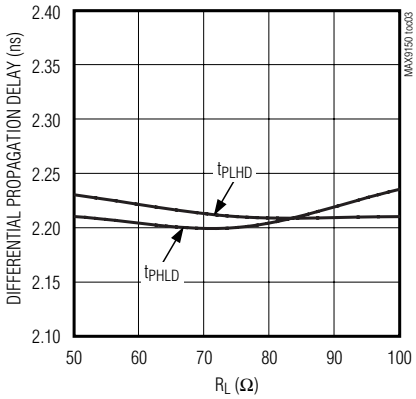
SUPPLY CURRENT vs. FREQUENCY



DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE



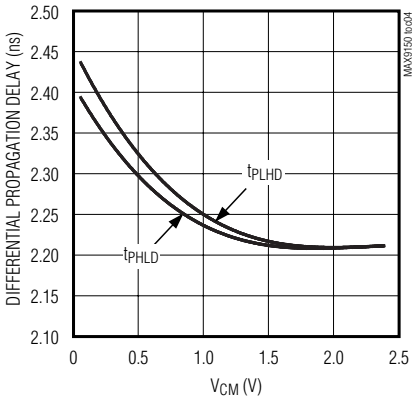
DIFFERENTIAL PROPAGATION DELAY vs. OUTPUT LOAD



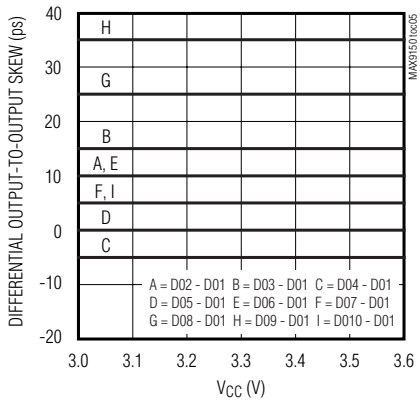
Typical Operating Characteristics (continued)

(Figure 2, V_{CC} = +3.3V, R_L = 50Ω, C_L = 5pF, $|V_{ID}|$ = 200 mV, V_{CM} = 1.2V, f_{IN} = 50MHz, T_A = +25°C, unless otherwise noted.)

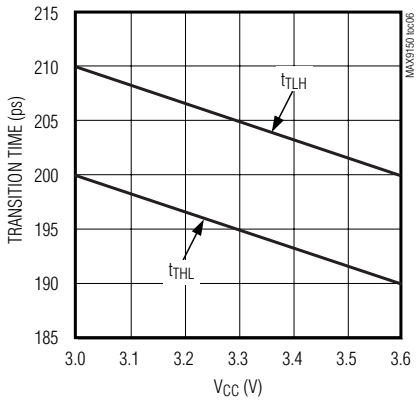
DIFFERENTIAL PROPAGATION DELAY vs. COMMON-MODE VOLTAGE



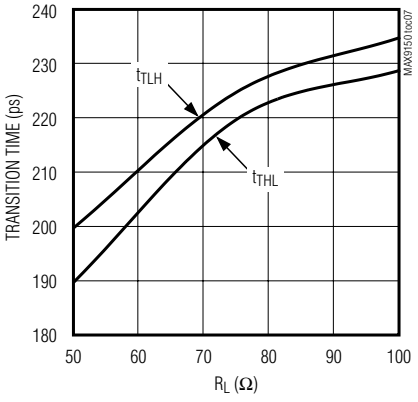
DIFFERENTIAL OUTPUT-TO-OUTPUT SKEW vs. SUPPLY VOLTAGE



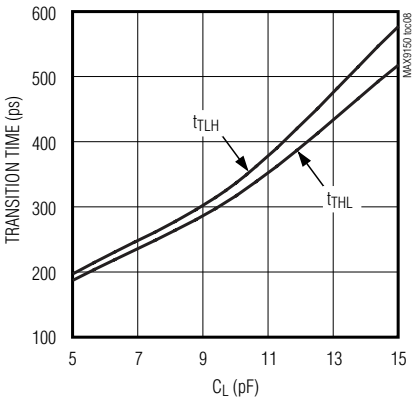
TRANSITION TIME vs. SUPPLY VOLTAGE



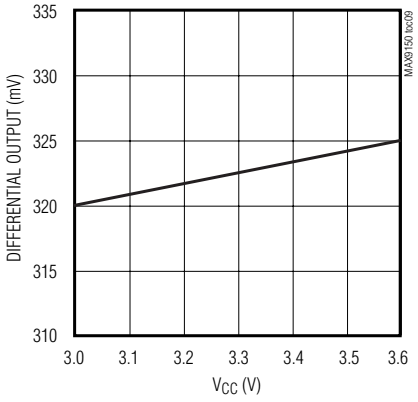
TRANSITION TIME vs. OUTPUT LOAD



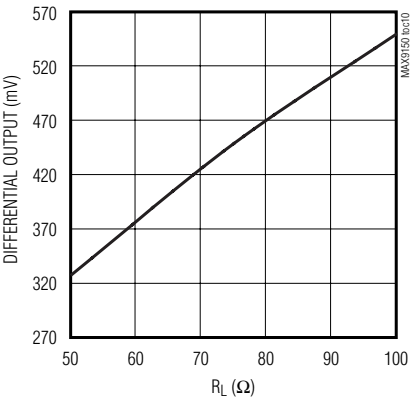
TRANSITION TIME vs. CAPACITANCE



DIFFERENTIAL OUTPUT vs. SUPPLY VOLTAGE



DIFFERENTIAL OUTPUT vs. OUTPUT LOAD



Low-Jitter, 10-Port LVDS Repeater

Pin Description

PIN	NAME	FUNCTION
1, 3, 11, 13, 16, 18, 20, 24, 26, 28	DO2+, DO1+, DO10+, DO9+, DO8+, DO7+, DO6+, DO5+, DO4+, DO3+	Differential LVDS Outputs. Connect a 100Ω resistor across each of the output pairs (DO_+ and DO_-) adjacent to the IC, and connect a 100Ω resistor at the input of the receiving circuit.
2, 4, 12, 14, 15, 17, 19, 23, 25, 27	DO2-, DO1-, DO10-, DO9-, DO8-, DO7-, DO6-, DO5-, DO4-, DO3-	
5	$\overline{PWRDN}$	Power Down. Drive $\overline{PWRDN}$ low to disable all outputs and reduce supply current to 60µA. Drive $\overline{PWRDN}$ high for normal operation.
6, 9, 21	GND	Ground
10, 22	V_{CC}	Power. Bypass each V_{CC} pin to GND with 0.1µF and 1nF ceramic capacitors.
7	RIN+	LVDS Receiver Inputs. RIN+ and RIN- are high-impedance inputs. Connect a resistor from RIN+ to RIN- to terminate the input signal.
8	RIN-	

Detailed Description

The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled impedance medium, as defined by the ANSI/TIA/EIA-644 and IEEE 1596.3 standards. The LVDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

The MAX9150 is a 400Mbps, 10-port LVDS repeater intended for high-speed, point-to-point, low-power applications. This device accepts an LVDS input and repeats it on 10 LVDS outputs. The device is capable of detecting differential signals as low as 100mV and as high as 1V within a 0 to 2.4V input voltage range. The LVDS standard specifies an input voltage range of 0 to 2.4V referenced to ground.

The MAX9150 outputs use a current-steering configuration to generate a 5mA to 9mA output current. This current-steering approach induces less ground bounce and no shoot-through current, enhancing noise margin and system speed performance. The driver outputs are short-circuit current limited, and are high impedance (to ground) when $\overline{PWRDN}$ = low or the device is not powered. The outputs have a typical differential resistance of 240Ω.

The MAX9150 current-steering architecture requires a resistive load to terminate the signal and complete the transmission loop. Because the device switches the direction of current flow and not voltage levels, the output voltage swing is determined by the total value of the termination resistors multiplied by the output current. With a typical 6.4mA output current, the MAX9150 produces a 320mV output voltage when driving a transmission line terminated at each end with a 100Ω termination resistor (6.4mA x 50Ω = 320mV). Logic states are determined by the direction of current flow through the termination resistors.

Fail-Safe

Fail-safe is a receiver feature that puts the output in a known logic state (high) under certain fault conditions. The MAX9150 outputs are differential high when the inputs are undriven and open, terminated, or shorted (Table 1).

Table 1. Input/Output Function Table

INPUT, V_{ID}		OUTPUTS, V_{OD}
+100mV		High
-100mV		Low
Open		High
Short	Undriven	High
Terminated		High

Note: *V_{ID} = RIN+ - RIN-, V_{OD} = DO_+ - DO_-*
High = 450mV > V_{OD} > 250mV
Low = -250mV > V_{OD} > -450mV

Applications Information

Supply Bypassing

Bypass each of the V_{CC} pins with high-frequency surface-mount ceramic 0.1µF and 1nF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to the V_{CC} pins.

Differential Traces

Output trace characteristics affect the performance of the MAX9150. Use controlled impedance traces to match trace impedance to both the transmission medium impedance and termination resistor. Ensure that noise couples as common mode by running the differential traces close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

Maintain the distance between the differential traces to avoid discontinuities in differential impedance. Avoid 90° turns and minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

Transmission media should have a controlled differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Avoid the use of unbalanced cables, such as ribbon or simple coaxial cable. Balanced cables, such as twisted pair, offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

Termination

Termination resistors should match the differential characteristic impedance of the transmission line. Since the MAX9150 has current-steering devices, an output voltage will not be generated without a termination resistor. Output voltage levels are dependent upon the value of the total termination resistance. The MAX9150 produces LVDS output levels for point-to-point links that are double terminated (100Ω at each end). With the typical 6.4mA output current, the MAX9150 produces an output voltage of 320mV when driving a transmission line terminated at each end with a 100Ω termination resistor (6.4mA x 50Ω = 320mV). Termination resistance values may range between 90Ω and 150Ω, depending on the characteristic impedance of the transmission medium.

Minimize the distance between the output termination resistor and the corresponding MAX9150 transmitter output. Use ±1% surface-mount resistors.

Minimize the distance between the input termination resistor and the MAX9150 receiver input. Use a ±1% surface-mount resistor.

Chip Information

TRANSISTOR COUNT: 11,117

PROCESS : CMOS

Test Circuits and Timing Diagrams

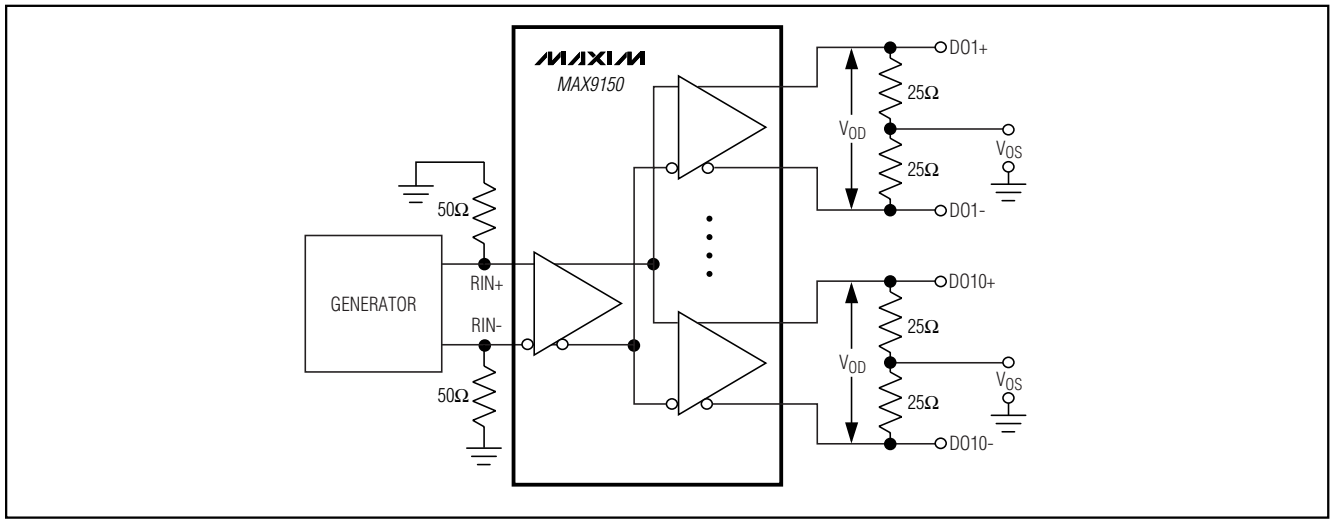


Figure 1. Driver-Load Test Circuit

Low-Jitter, 10-Port LVDS Repeater

Test Circuits and Timing Diagrams (continued)

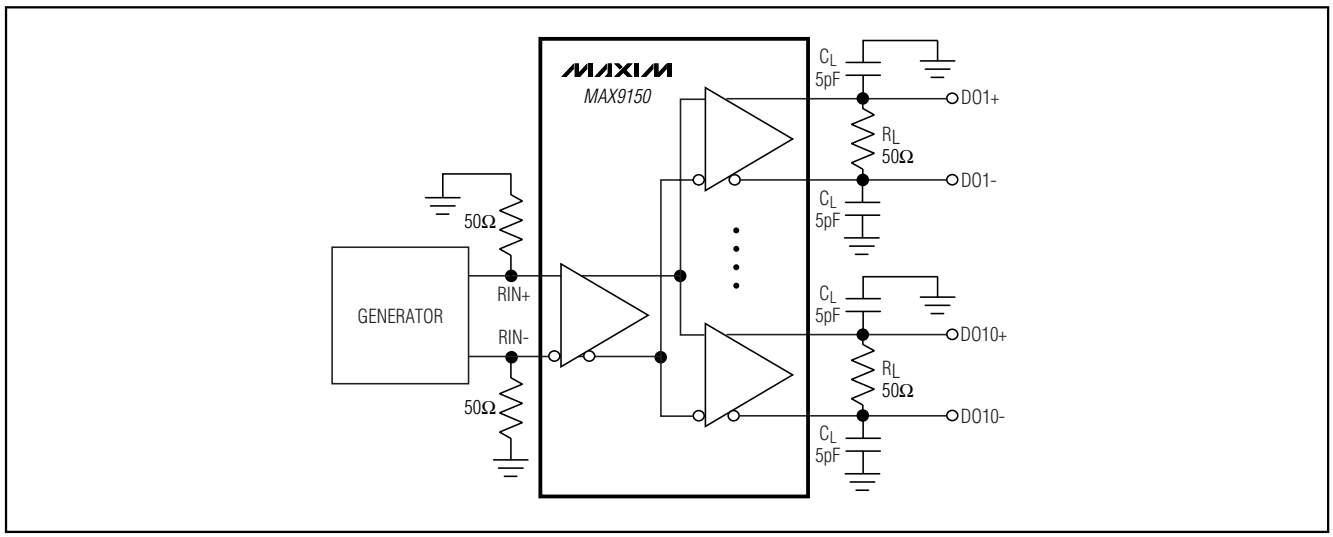


Figure 2. Repeater Propagation Delay and Transition Time Test Circuit

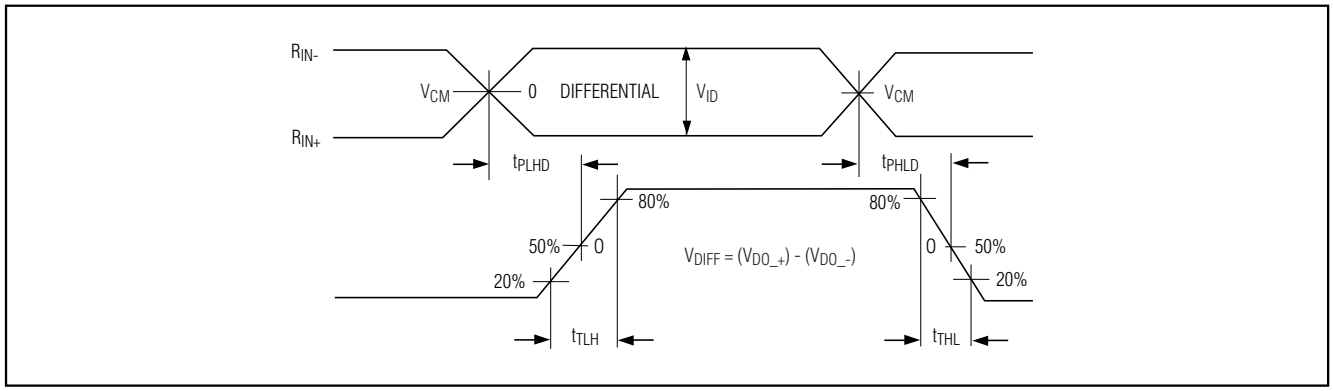


Figure 3. Propagation Delay and Transition Time Waveforms

Test Circuits and Timing Diagrams (continued)

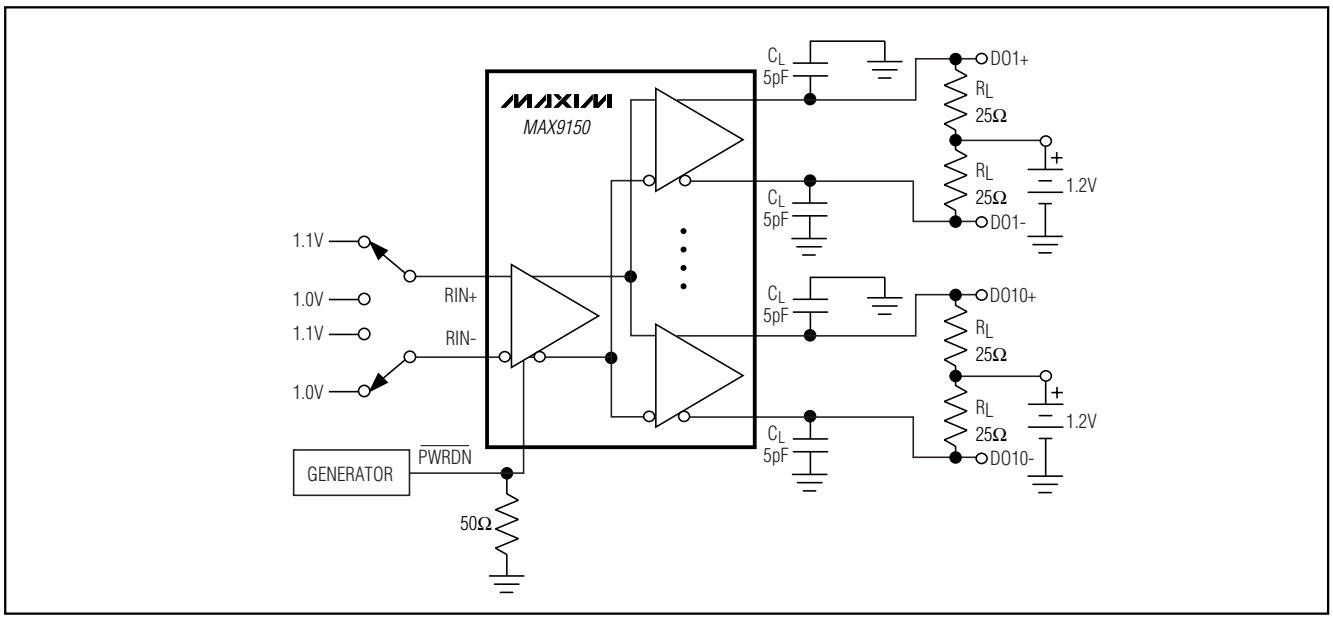


Figure 4. Power-Up/Down Delay Test Circuit

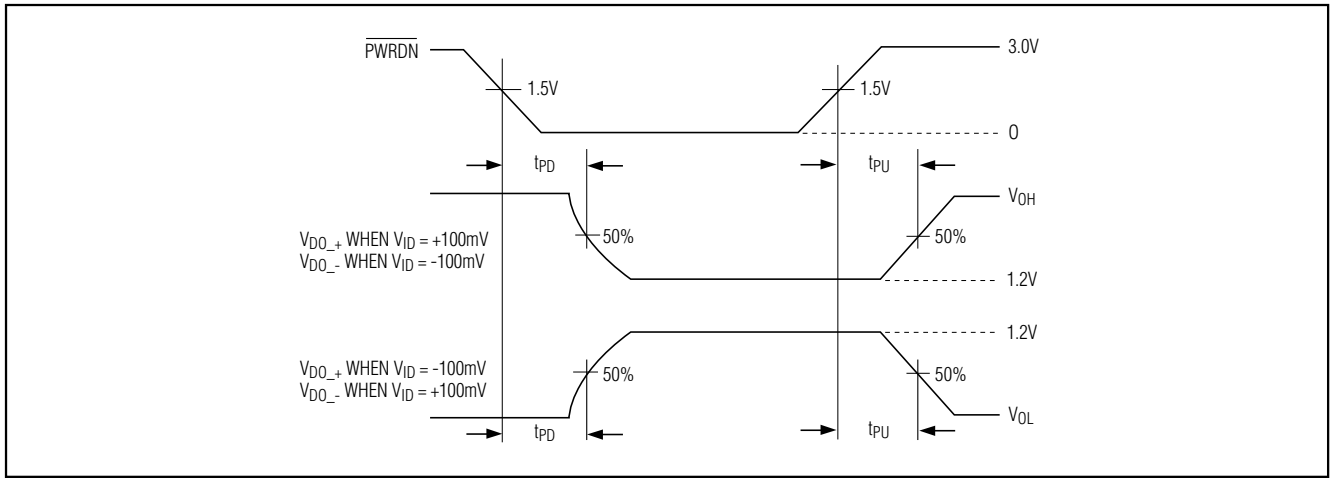
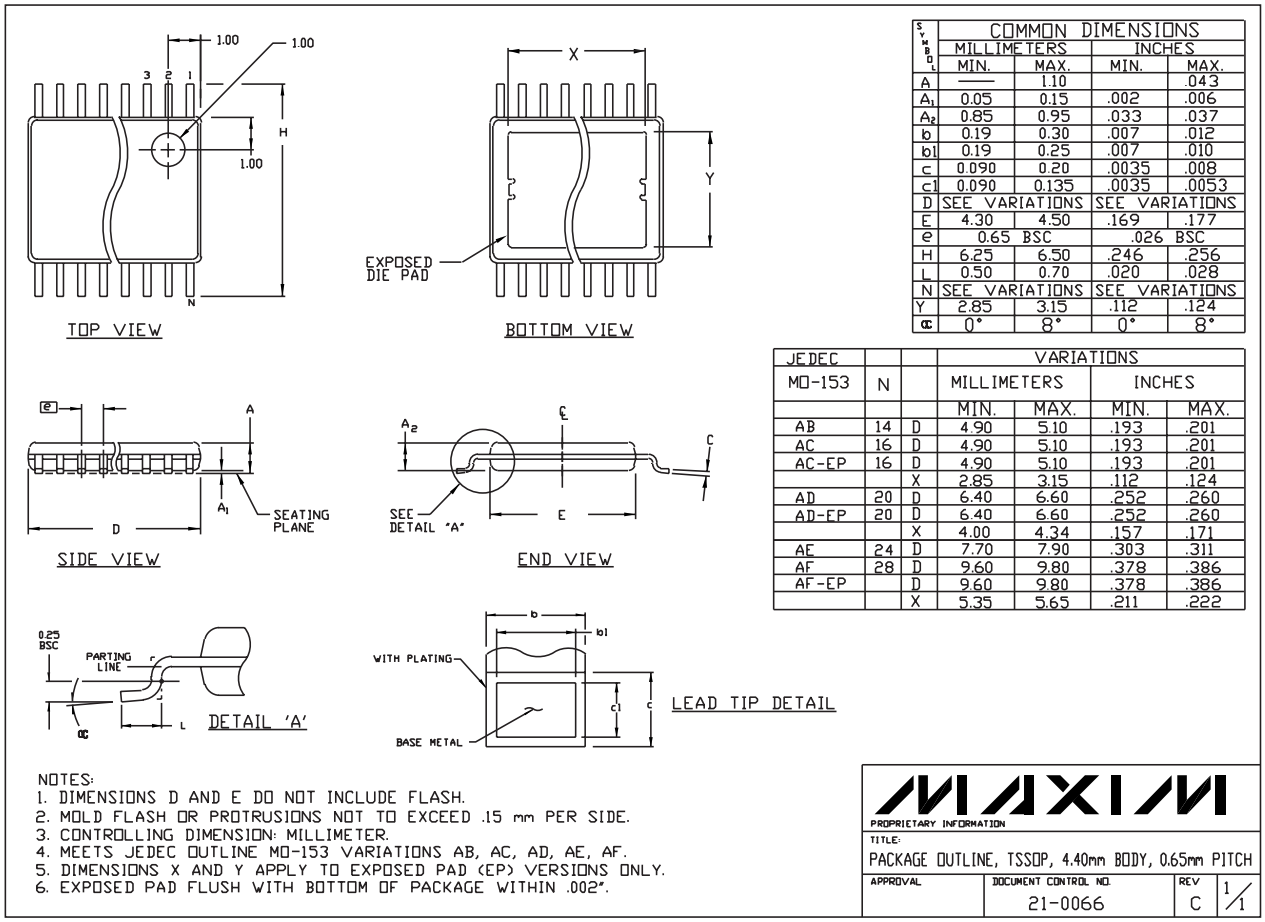


Figure 5. Power-Up/Down Delay Waveform

Low-Jitter, 10-Port LVDS Repeater

Package Information



TSSOP.EPS

SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AC-EP	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
AD	20	D	6.40	6.60	.252	.260
AD-EP	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386
AF-EP		D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC OUTLINE MO-153 VARIATIONS AB, AC, AD, AE, AF.
5. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, TSSOP, 4.40mm BODY, 0.65mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	C	1/1

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