CY2300

Phase-Aligned Clock Multiplier

Features

- 4-multiplier configuration
- Single PLL architecture
- Phase alignment
- Low jitter, high accuracy outputs
- Output enable pin
- 3.3 V operation
- 5 V tolerant input
- Internal loop filter
- 8-pin 150-mil small-outline integrated circuit (SOIC) package
- Commercial temperature

Functional Description

The CY2300 is a 4 output 3.3 V phase-aligned system clock designed to distribute high-speed clocks in PC, workstation, datacom, telecom, and other high-performance applications.

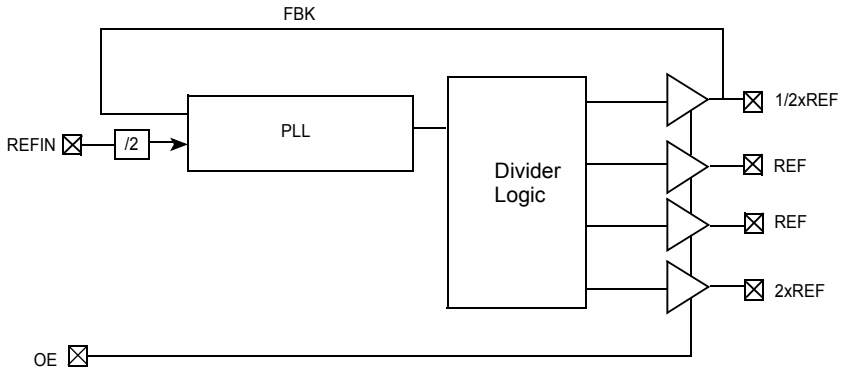
The part allows the user to obtain 1/2x, 1x, $\overline{1x}$ and 2x REFIN output frequencies on respective output pins.

The part has an on-chip PLL which locks to an input clock presented on the REFIN pin. The input-to-output skew is guaranteed to be less than ±200 ps, and output-to-output skew is guaranteed to be less than 200 ps.

Multiple CY2300 devices can accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is guaranteed to be less than 400 ps.

The CY2300 is available in commercial temperature range.

Logic Block Diagram



Pinouts

Figure 1. CY2300 – 8-pin SOIC - Top View

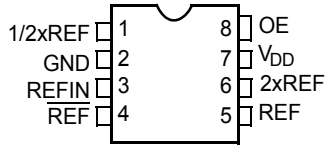


Table 1. Pin Definitions

Pin	Signal[1]	Description
1	1/2xREF	Clock output, 1/2x reference
2	GND	Ground
3	REFIN	Input reference frequency, 5 V tolerant input
4	$\overline{\text{REF}}$	Clock output reference
5	REF	Clock output reference
6	2xREF	Clock output, 2x reference
7	V_{DD}	3.3 V Supply
8	OE	Output enable (weak pull-up)

Maximum Ratings

Supply voltage to ground potential .....–0.5 V to +7.0 V

DC input voltage (except ref).....–0.5 V to V_{DD} + 0.5 V

DC input voltage REF .....–0.5 V to 7 V

Storage temperature ..... –65 °C to +150 °C

Junction temperature..... 150 °C

Static discharge voltage
(per MIL-STD-883, method 3015) ..... > 2000 V

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
T_A	Operating temperature (ambient temperature)	0	70	°C
C_L	Load capacitance, 10 MHz < F_{OUT} < 133.33 MHz	–	18	pF
	Load capacitance,133.33 MHz < F_{OUT} < 166.67 MHz	–	12	pF
C_{IN}	Input capacitance	–	7	pF
t_{PU}	Power-up time for all V_{DD}'s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Note
1. Weak pull-down on all outputs.

[+] Feedback

Electrical Characteristics

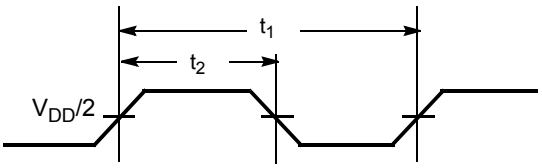
Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW voltage		–	0.8	V
V_{IH}	Input HIGH voltage		2.0	–	V
I_{IL}	Input LOW current	V_{IN} = 0 V	–	100	µA
I_{IH}	Input HIGH current	V_{IN} = V_{DD}	–	50	µA
V_{OL}	Output LOW voltage[2]	I_{OL} = 8 mA	–	0.4	V
V_{OH}	Output HIGH voltage[2]	I_{OH} = –8 mA	2.4	–	V
I_{DD}	Supply current	Unloaded outputs, REFIN = 66 MHz	–	45	mA
		Unloaded outputs, REFIN = 33 MHz	–	32	mA
		Unloaded outputs, REFIN = 20 MHz	–	18	mA

Switching Characteristics

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
$1/t_1$	Output frequency	18-pF load	10	–	133.33	MHz
		12-pF load	–	–	166.67	MHz
	Duty cycle[3] = $t_2 \div t_1$	Measured at $V_{DD}/2$	40	50	60	%
t_3	Rise time[3]	Measured between 0.8 V and 2.0 V	–	–	1.20	ns
t_4	Fall time[3]	Measured between 0.8 V and 2.0 V	–	–	1.20	ns
t_5	Output to output skew on rising edges[3]	All outputs equally loaded Measured at $V_{DD}/2$	–	–	200	ps
t_6	Delay, REFIN rising edge to output rising edge[3]	Measured at $V_{DD}/2$ from REFIN to any output	–	–	±200	ps
t_7	Device to device skew[3]	Measured at $V_{DD}/2$ on the 1/2xREF pin of devices (pin 1)	–	–	400	ps
t_J	Period jitter[3]	Measured at Fout=133.33 MHz, loaded outputs, 18-pF load	–	–	±175	ps
t_{LOCK}	PLL lock time[3]	Stable power supply, valid clocks presented on REFIN	–	–	1.0	ms

Switching Waveforms

Figure 2. Duty Cycle Timing



Notes
2. Parameter is guaranteed by design and characterization. It is not 100% tested in production.
3. All parameters are specified with equally loaded outputs.

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Switching Waveforms (continued)

Figure 3. All Outputs Rise/Fall Time

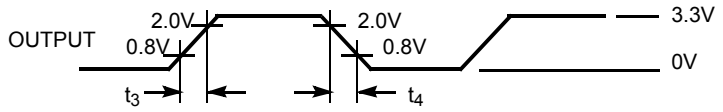


Figure 4. Output to Output Skew

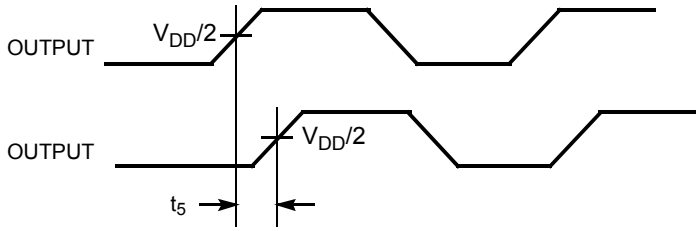


Figure 5. Input to Output Propagation Delay

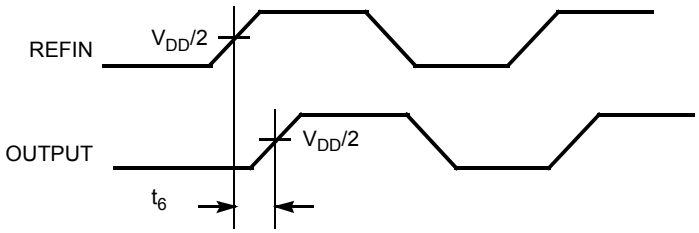
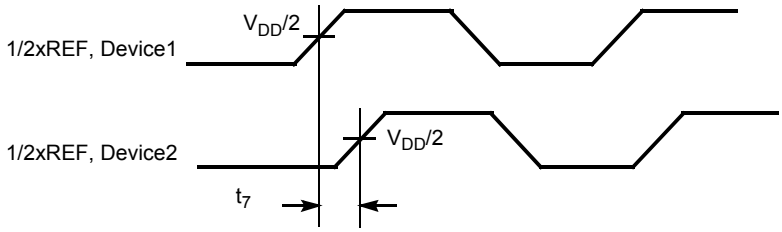
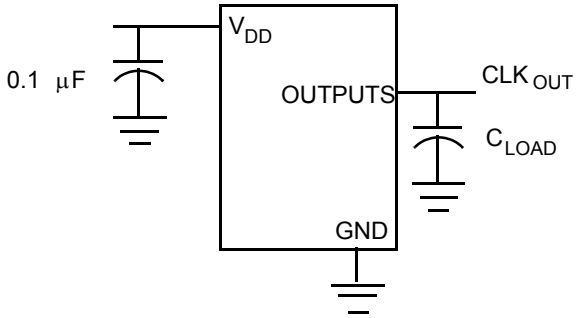


Figure 6. Device to Device Skew



Test Circuits

Figure 7. Test Circuit #1

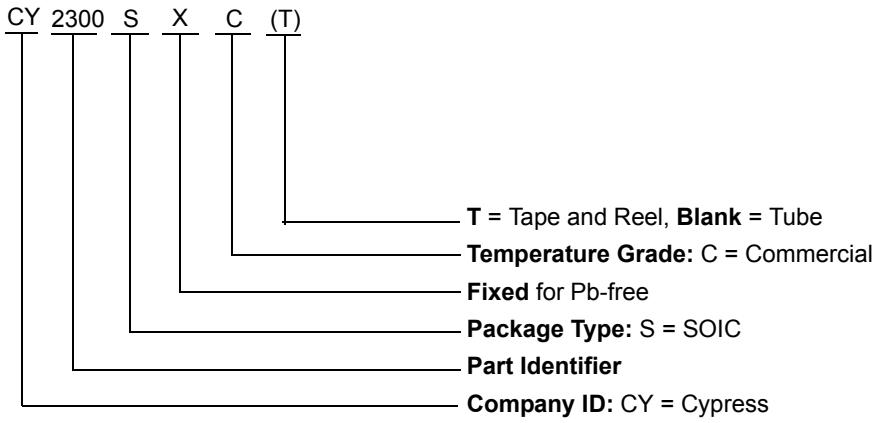


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Ordering Information

Ordering Code	Package Type	Operating Range
Pb-free		
CY2300SXC	8-pin 150-mil SOIC	Commercial (0 to 70 °C)
CY2300SXCT	8-pin 150-mil SOIC - Tape and Reel	Commercial (0 to 70 °C)

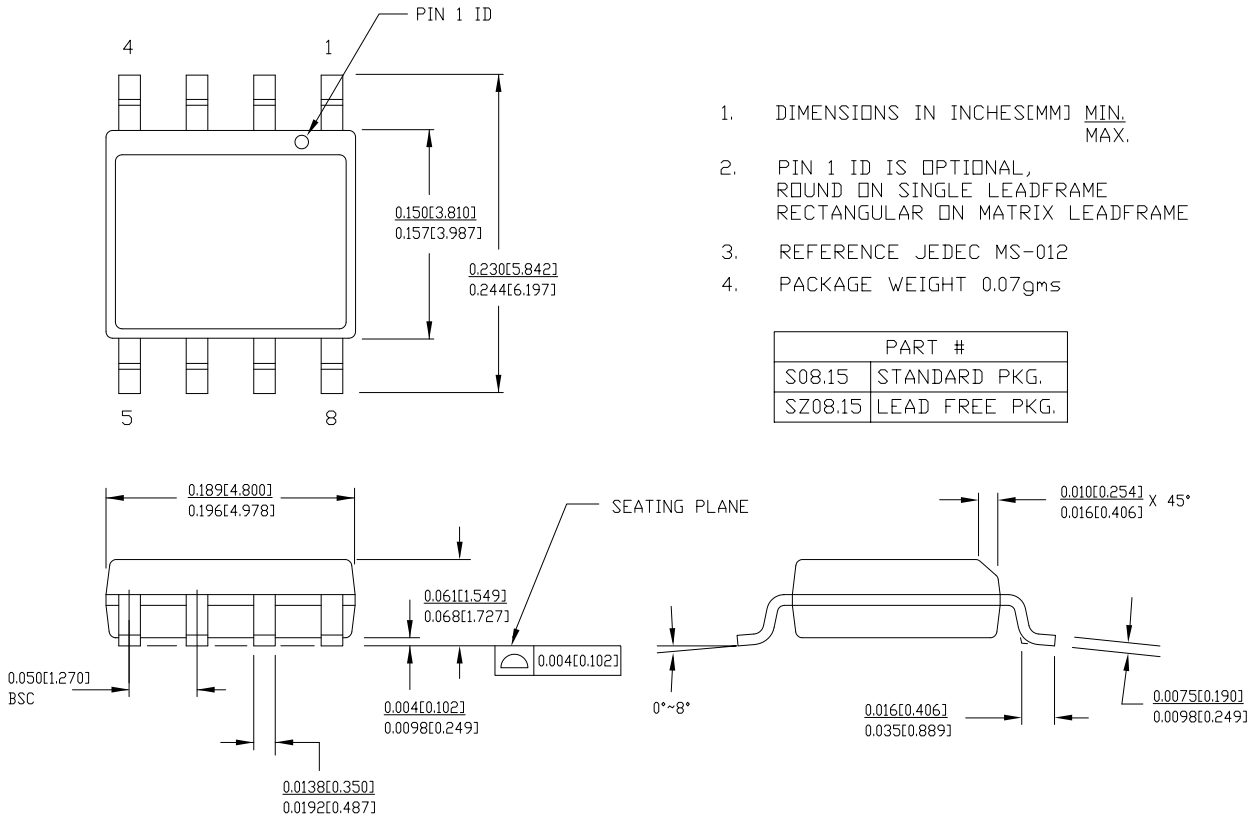
Ordering Code Definitions



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Package Drawing and Dimensions

Figure 7. 8-pin (150-Mil) SOIC S8



51-85066 *D

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Acronyms

Acronym	Description
FBK	Feedback
OE	Output enable
PLL	Phase locked loop
REFIN	Reference input

Reference Documents

Reference documents are available through your local Cypress sales representative. You can also direct your requests to tsbusdev@cypress.com.

Document Number	Document Title	Description
NA	NA	NA

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	Hertz
kHz	kilo Hertz
MHz	Mega Hertz
µA	micro Amperes
µF	micro Farads
µs	micro seconds
µV	micro Volts
mA	milli Amperes
mm	milli meters
ms	milli seconds
mV	milli Volts
ns	nano seconds
pA	pico Amperes
pF	pico Farads
ps	pico seconds
V	Volts

Document History Page

Document Title: CY2300 Phase-Aligned Clock Multiplier Document Number: 38-07252				
REV.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110517	SZV	01/07/02	Change from Spec number: 38-01039 to 38-07252
*A	121854	RBI	12/14/02	Power up requirements added to Operating Conditions Information
*B	246829	RGL	08/02/04	Added Lead Free Devices
*C	2568533	AESA	09/23/08	Updated template. Removed Selector Guide. Removed Operating Conditions for CY2300SI Industrial Temperature Devices. Removed Electrical Characteristics for CY2300SI Industrial Temperature Devices. Removed Switching Characteristics for CY2300SI Industrial Temperature Devices. Removed part number CY2300SC, CY2300SC, CY2300SI, CY2300SI, CY2300SXI and CY2300SXIT.
*D	3026183	BASH	09/01/2010	Removed “Benefits” from page 1. Added lower limit of 10MHz for 18pF load capacitance in Operating Conditions on page 3. Ordering Code Definitions added on page 5. Acronyms, Reference Documents and Document Conventions added on page 7.

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