AN2654
Application note

CCFL backlight half-bridge topology based on L6574 and STD7NS20

Introduction

Cold cathode fluorescent lamps (CCFL) are widely used in the backlighting of television and PC monitor applications due to their low cost and high efficiency. A 12 V or 24 V DC voltage is provided for the backlighting inverter to drive the CCFL. In order to improve the efficiency and performance of the total system both for the AC-DC power supply and inverter, STMicroelectronics has introduced a high-voltage ballast-driver IC L6574 that provides the half-bridge solution for CCFL backlighting. Thanks to BCD™ offline technology, the L6574 can handle high-side voltage rail up to 600 V and consumes less current. Of course, the power loss of the bridge rectifier is reduced.

Figure 1 shows the typical LCD TV power section block diagram. Different supply voltages for backlight applications are available on the market. *Table 1* shows the required backlight power for various sizes of TV display screens. For the same screen size, there are three different types of supply voltages for CCFL backlight and each consumes a different current. Using a high-voltage backlight CCFL solution allows greatly reducing the power losses of the bridge rectifier and the conduction loss of the primary switch.

Figure 1. Typical LCD TV power section block diagram

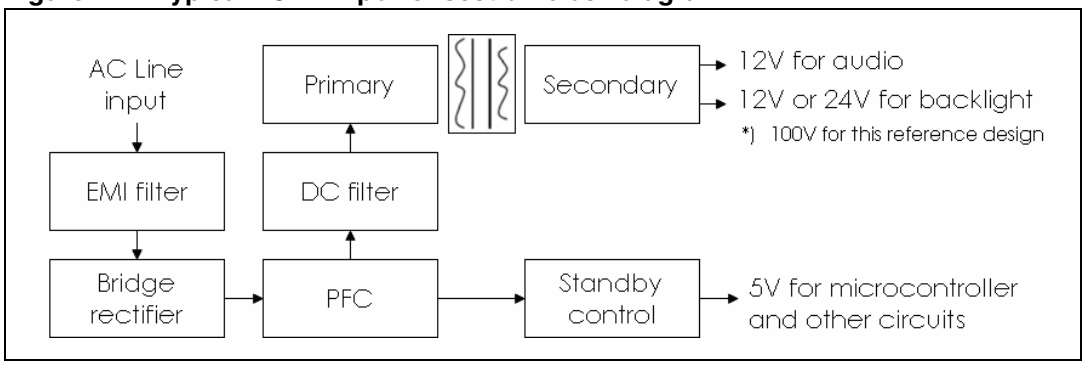


Table 1. Required backlight power and its current consumption vs. supply voltage

TV display screen size (inches)	Backlight power (Watts)	Current consumption vs. supply voltage (V_{lamp})		
		12 V	24 V	100 V
17	24 W	2 A	1 A	0.24 A
19	30 W	2.5 A	1.25 A	0.3 A
27	120 W	-	5 A	1.2 A
32	144 W	-	6 A	1.44 A
42	264 W	-	11 A	2.64 A

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1 Board description

High-voltage half-bridge zero-voltage switching topology has been selected. In order to achieve the best performance, the iteration bench work is nearly inevitable, especially driving with multi-lamps. However, the procedure of transformer design and resonant tank equations are described in *Appendix A* which provides the designer with a feasible approach to start the design work.

1.1 Reference design board and PCB layout

Figure 2. STEVAL-ILC001V1 evaluation board

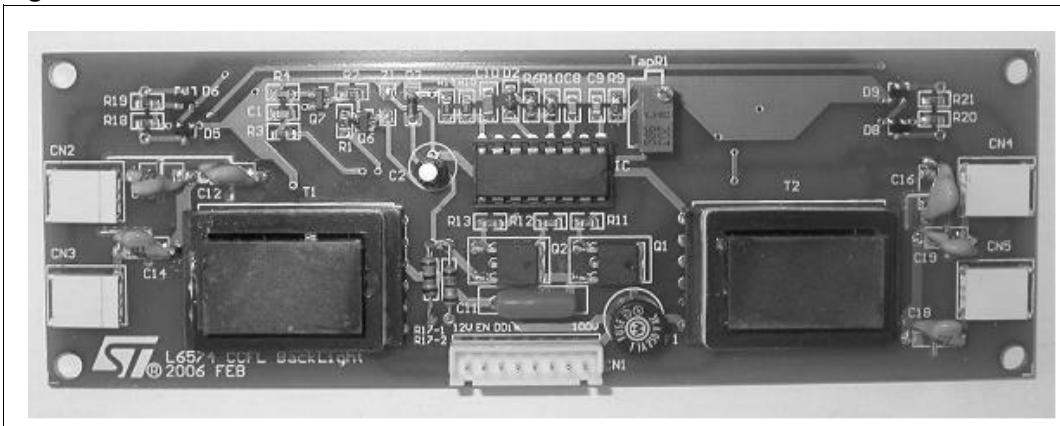


Figure 3. PCB top-side view

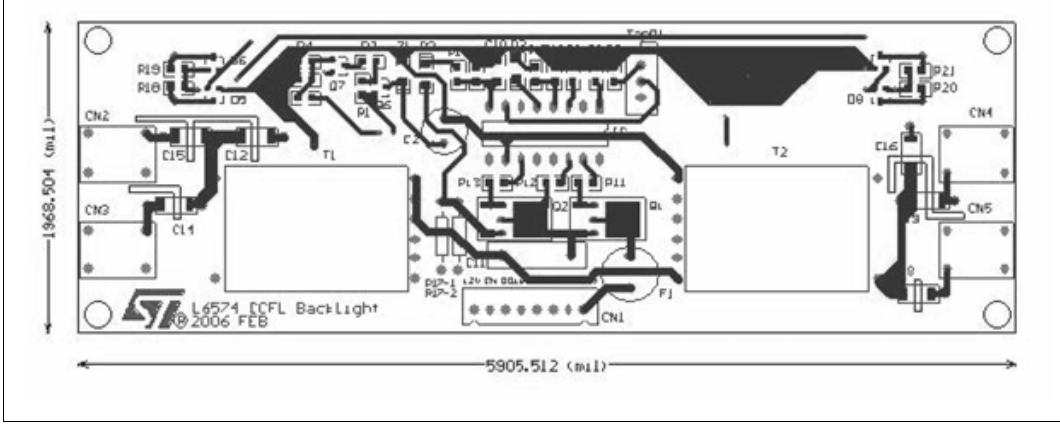
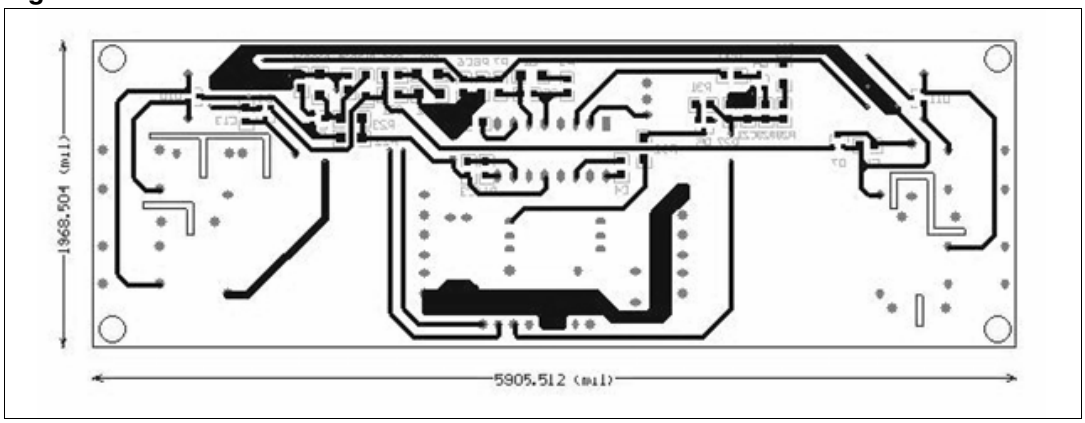


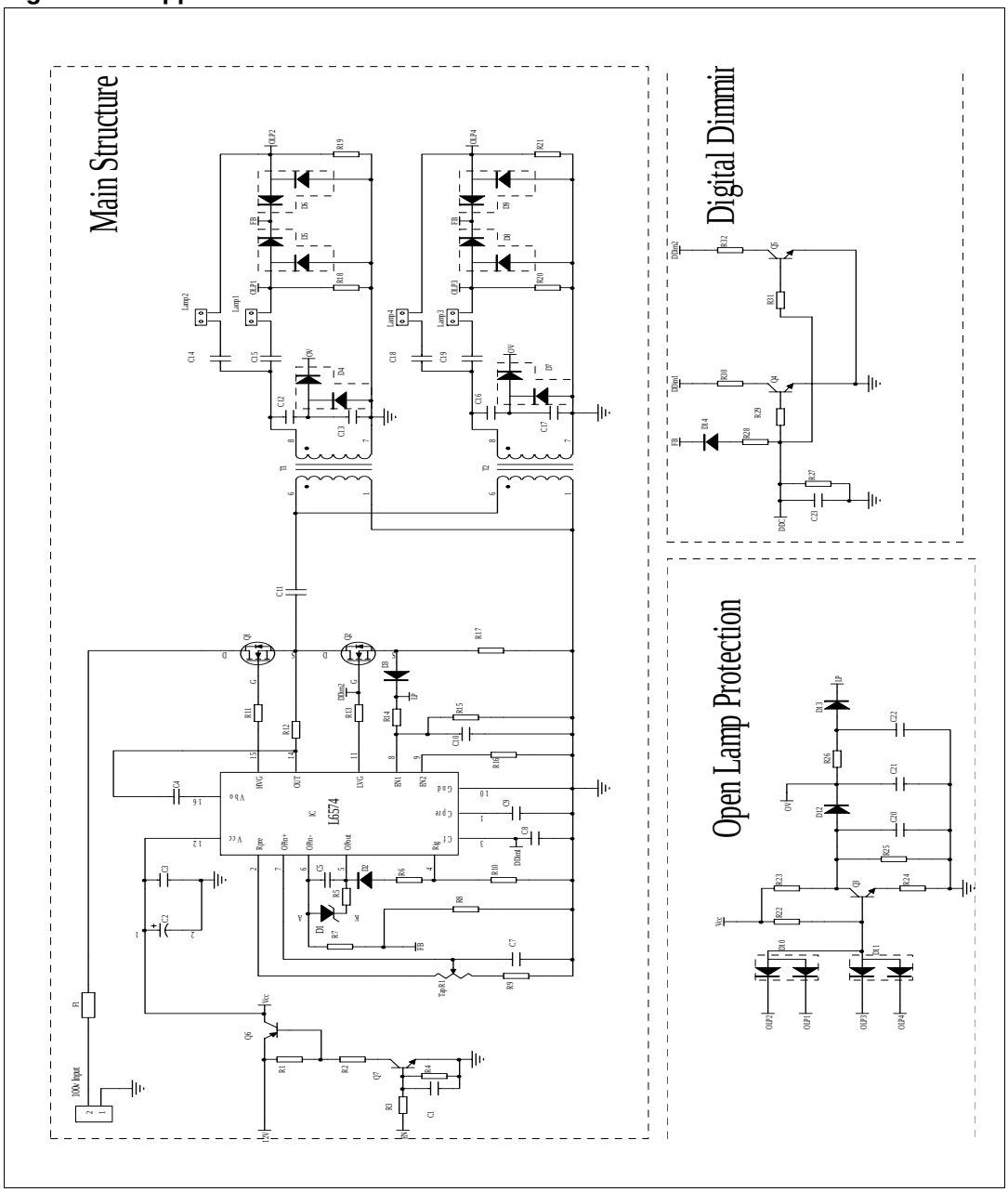
Figure 4. PCB bottom-side view



1.2 Schematic

This CCFL backlighting solution is designed for 17" LCD monitors. This development design board is able to drive 4 tubes of CCFL. During normal conditions, the L6574 provides a current loop that is controlled by varying the switching frequency. The input DC bus voltage has been lifted to 110 V. This reference design provides an open lamp protection, overvoltage protection, soft-start time setting, and analog and digital dimming functions. *Figure 5* shows the application schematic and *Table 2* gives the bill of materials.

Figure 5. Application schematic



1.3 Bill of materials

Table 2. Bill of materials

Symbol	Value	Note	Qty
F1	1 A	Fuse	1
R1, R2, R28	10 kΩ		3
R3, R29, R30, R31	1.1 kΩ		4

Table 2. Bill of materials (continued)

Symbol	Value	Note	Qty
R4	20 kΩ		1
R5, R25, R27	51 kΩ		3
R6	68 kΩ		1
R7	9.1 kΩ		1
R8	22 kΩ		1
R9	15 kΩ		1
R10	75 kΩ	± 1%	1
R11, R13	56		2
R12, R16	0		2
R14	82 kΩ		1
R15	150 kΩ		1
R17-1, R17-2	0.5	± 5%, 0.25 W, through hole	2
R18, R19, R20, R21	240	± 1%	4
R22	43 kΩ		1
R23	100 kΩ		1
R24	330		1
R26	510 kΩ		1
R32	5.6		1
TapR1	20 kΩ	Potential-meter type 3296	1
C1, C3, C7, C23	22 nF	± 10%, 50 V	4
C2	22 nF	± 10%, 25 V, E-Cap	1
C4, C21	100 nF	± 10%, 50 V	2
C5	8.2 nF	± 10%, 25 V	1
C6	nil	nil	0
C8	470 pF	± 10%, 25 V	1
C9, C13, C17	47 nF	± 10%, 50 V	3
C10, C20, C22	2.2 µF	± 10%, 25 V	3
C11	100 nF	± 10%, 400 V, CBB	1
C12, C16	10 pF	± 5%, 3 kV, C4520C0G3F100 F or CC45SL3FD100JYNN, TDK	2
C14, C15, C18, C19	27 pF	± 5%, 3 kV, C4520C0G3F270K or CC45SL3FD270JYNN, TDK	4
D1	2.7 V	0.25 W, Zener diode	1
D2, D3, D12, D13, D14	1N4148	SMD	5
D4, D5, D6, D7, D8, D9	BAT54S	SOT 23, STMicroelectronics	6

Table 2. Bill of materials (continued)

Symbol	Value	Note	Qty
D10, D11	BAT54A	SOT 23, STMicroelectronics	2
Q1, Q2	STD7NS20T4	DPAK, STMicroelectronics	2
Q3, Q4, Q5, Q7	BC817-25	SOT 23 (NPN), STMicroelectronics	4
Q6	BC807-25	SOT 23 (PNP), STMicroelectronics	1
IC	L6574	DIP 16, STMicroelectronics	1
T1, T2	Lpri = 5.8 mH, Lsec = 960 mH, Np=180, Ns=2200	PC40 EE19/28 (core type), NIA19LES-X90H002, TDK	2

2 Electrical function of the design

2.1 Enable

Enable is the function to turn on/off the VCC of the IC (see *Figure 6*). A CMOS or TTL logic signal can be used to drive the L6574 into an on/off state. High enables the chip, low disables it.

Figure 6. Enable function

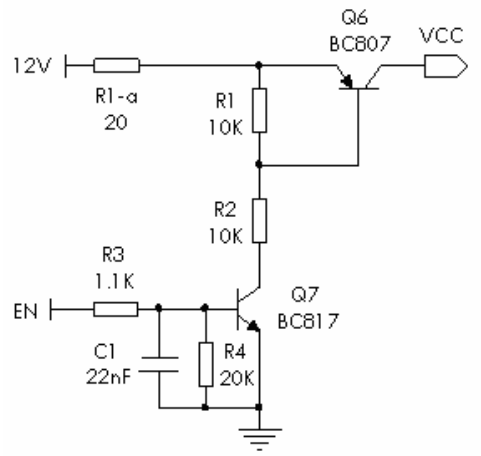
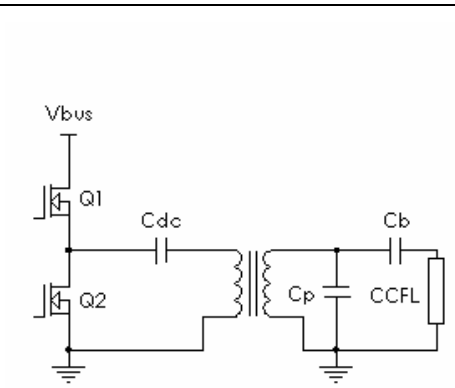


Figure 7. Resonant topology

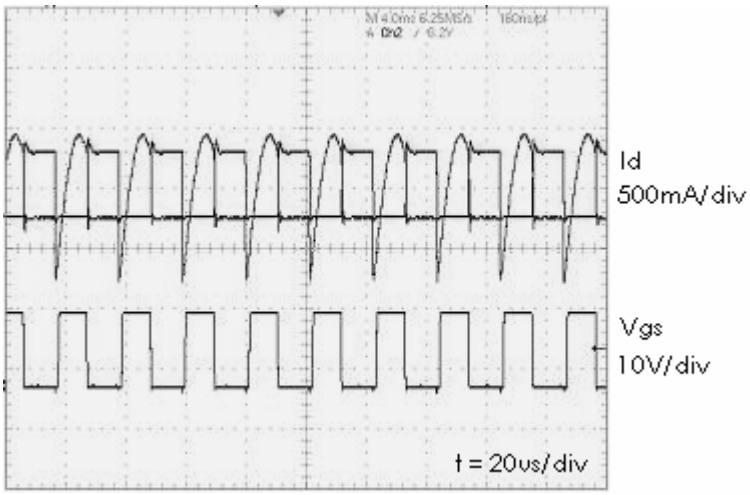


2.2 Operation

In *Figure 7*, Q1 and Q2 are driven by the L6574 in a half-bridge configuration to power the CCFL lamps. In order to provide several kV striking voltage for ignition, one LC tank has been added on the secondary side of the transformer to generate the proper alternative voltage. After power-on, the MOSFET driving frequency starts with a high frequency and decreases to a lower operating point following a descending slope. Ignition is accomplished within this frequency shift. The leakage inductance of the secondary side and the reflected inductance from the primary side consist of the inductance of the LC tank (refer to *Appendix A*). The capacitance is given by the parallel capacitor C_p.

Prior to ignition the LC resonant circuit provides a striking voltage to the lamp. After ignition, impedance of the CCFL and ballast capacitor C_b becomes a portion of the resonant circuit, too. The CCFL becomes an inductive load. This inductive load of half-bridge benefits the MOSFET by making zero-voltage switching (refer to *Figure 8*). Thanks to the high-voltage ZVS topology, the switching and conduction losses are greatly reduced.

Figure 8. Vgs and Id of MOSFET (Q2) in ZVS mode



The IC L6574 builds with a lamp current control loop (refer to *Figure 9*) to regulate the current drain in the CCFL. Pin 6 (the inverting input of the error amplifier integrated in the IC) is the control signal input and the signal is given by the voltage across the resistor named R_{sense}. R_{sense} is connected in series with the lamp at the low voltage terminal. *Figure 10* shows the lamp current related to Q1 and Q2 in zero-voltage switching.

Figure 9. Lamp current control loop

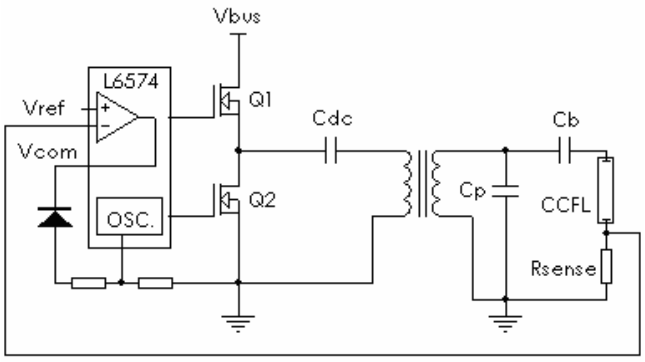
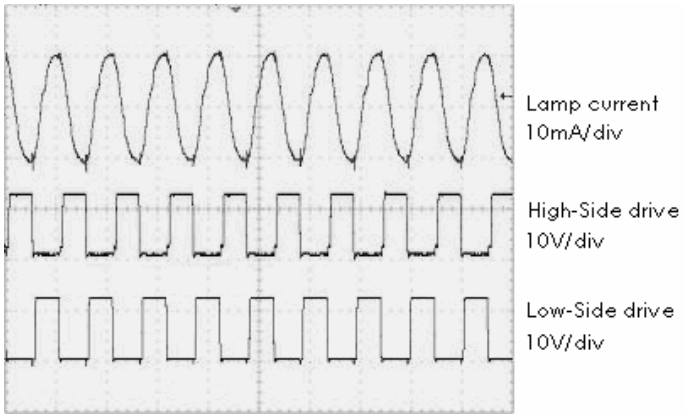


Figure 10. Lamp current during zero-voltage switching

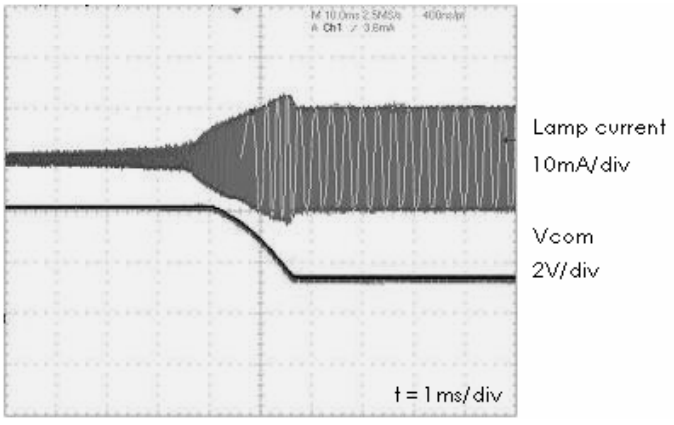


One bypass diode is connected in series with the resistor to save the power loss at the negative half cycle of the lamp current. The feedback signal compares with the voltage level on the non-inverting input. This non-inverting input is set as a reference (V_{REF} = 0.6 ~ 2 V typical). The error voltage Vcom (pin 5) is used to adjust the current coming from pin 4, eventually it changes the working frequency of the two MOSFETs to allow lamp current regulation. Thus L6574 achieves tight current control while Vbus voltage varies. Considering the frequency adjustable range, the immunity range to Vbus variation is 10% (100 V - 120 V).

2.3 Soft-start

At startup, the L6574 driving frequency decreases from maximum to normal working frequency, which automatically gives a smooth soft-start function. In the actual circuit, one Zener diode and a current-limiting resistor have been used to reduce the lamp current spike caused by the response delay (refer to *Figure 11*) of the error amplifier.

Figure 11. Vcom and lamp current in soft-start



2.4 Dimming

The L6574 provides two ways of controlling brightness. One is current amplitude modulated dimming, which is analog dimming. The other way (digital dimming) is to modulate the lamp current with external pulse width, the brightness depends on the PWM duty cycle.

2.4.1 Analog dimming

Tube brightness is in proportion to lamp current. Reducing the lamp current dims the brightness. The voltage level on the non-inverting input of the error amplifier determines the current amplitude of the lamp. Thus analog dimming is easily achieved by setting the voltage on pin 7 by using a potentiometer.

When analog dimming is adopted, the lamp is operating at relatively low current condition, and it may display a "thermometer effect", that is, light intensity is non-uniformly distributed along the lamp length. More light is emitted near the driven electrode which is due to the electrical field imbalance caused by parasitic capacitance. The "thermometer effect" limits the practical lowest illumination level. The recommended analog dimming range of this demonstration board is 100% ~ 60%.

The lamp current at full brightness is shown in *Figure 12*. The lowest lamp current for 60% brightness is shown in *Figure 13*.

Figure 12. 100% of full brightness for analog dimming

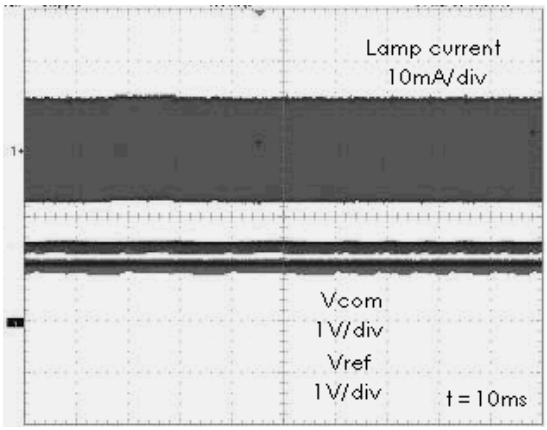
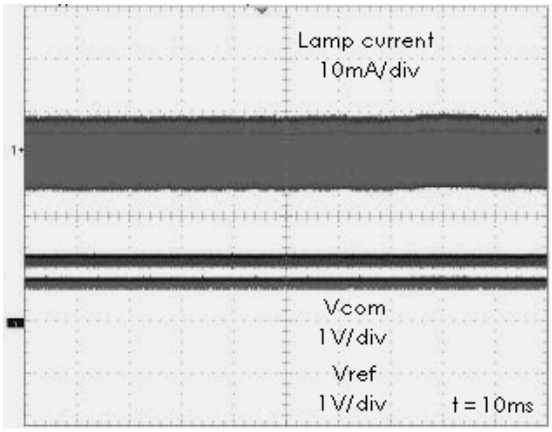


Figure 13. 60% of full brightness for analog dimming



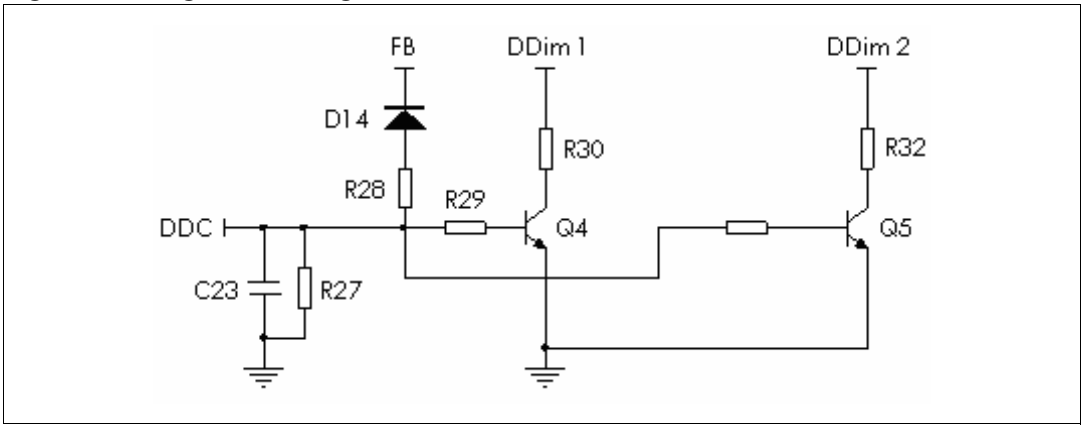
2.4.2 Digital dimming

In digital dimming mode, the lamp current is either fully on or fully off, modulated by the external PWM signal. Of course, the analog dimming is still accessible during digital dimming. The duty cycle determines the brightness of the lamp. The dimming range can be extremely wide compared with analog dimming. However, the external burst repetition rate should be high enough to prevent lamp gas de-ionization and visible flickering. In this case, a 250 Hz/3.3 V square wave should be provided to properly operate this function.

The digital dimming circuit is shown in *Figure 14*. When the PWM signal is high, Q4 is switched on, and it pulls down the voltage DDim1 (the same point on the C_f pin of L6574). If the voltage on C_f remains low, the L6574 stops oscillating by shutting off its high side driver,

while keeping the low side on, until the C_f pin goes back to normal again. In this way, the external PWM signal is able to control the on time of the lamp current.

Figure 14. Digital dimming control circuit



When the oscillator is in the off state, the low side MOSFET (Q2) is always conducting due to the IC internal logic. This creates a path for the resonance between the DC blocking capacitor and the transformer primary leakage inductance, which introduces some undesirable noise in the lamp off state. For this reason another transistor Q5 has been deployed to pull down the gate junction (DDim2) of the low side MOSFET at off state, too. The resistor R30 and R32 are used to limit the discharging current.

As soon as the external PWM signal becomes low, the C_f is charged again and oscillation resumes. Normally an overshoot can be seen on the lamp current, which gives more stress to the lamp and the MOSFET. The L6574 handles this very well by connecting the PWM signal to the feedback pin (FB) through a resistor, and the error amplifier is compensated during off state. In this case, when the oscillation starts again, it begins from high frequency down, producing a lamp current waveform somewhat like a soft-start.

Figure 15. Vgs of low-side MOSFET

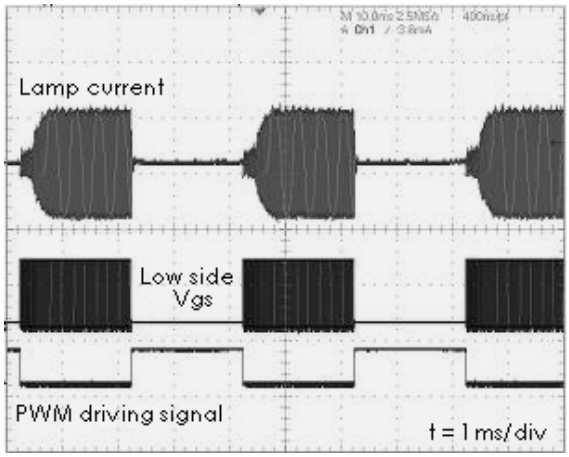


Figure 16. Vcom waveform in digital dimming

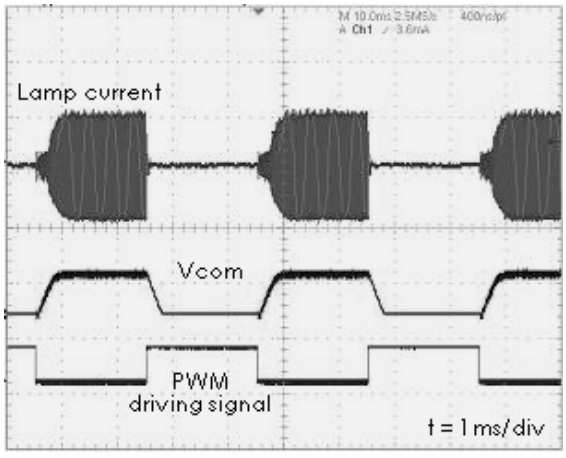


Figure 17. Lamp current at 20% of full brightness

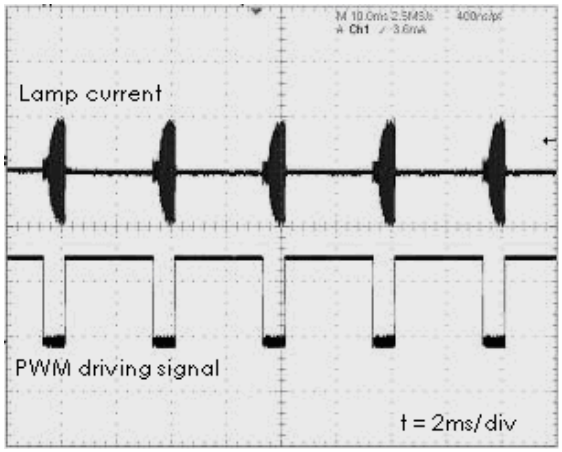
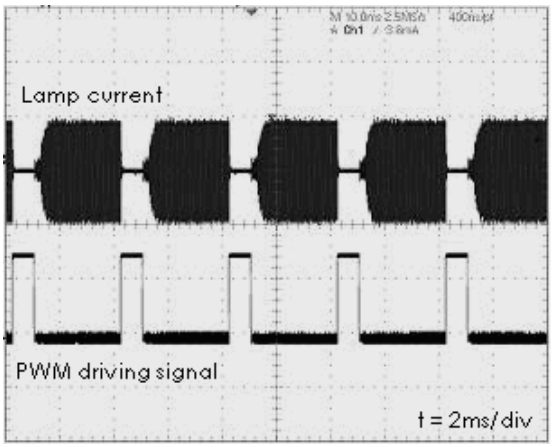


Figure 18. Lamp current at 80% of full brightness

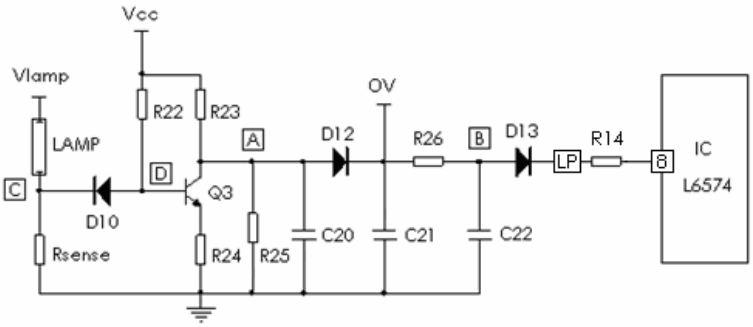


2.5 Protection

2.5.1 Open lamp protection

The protection circuit (refer to *Figure 19*) is constructed upon a signal bipolar transistor Q3 and the L6574 internal latched shutdown protection function (pin 8).

Figure 19. Open lamp protection circuit



After power-on, Q3 is turned on and the voltage at point A nears zero. The lamp current flowing through the sense resistor produces a voltage at point C that is higher than the turn-on threshold voltage of Q3, thus Q3 remains on, and no protection takes place.

Once the lamp is removed, the voltage at point C drops to zero. An additional current flows from Vcc, R22, D10 and R_{sense}. Thanks to the optimized value of R22, the voltage at point D starts going down and falls below the turn-on threshold which eventually turns off Q3.

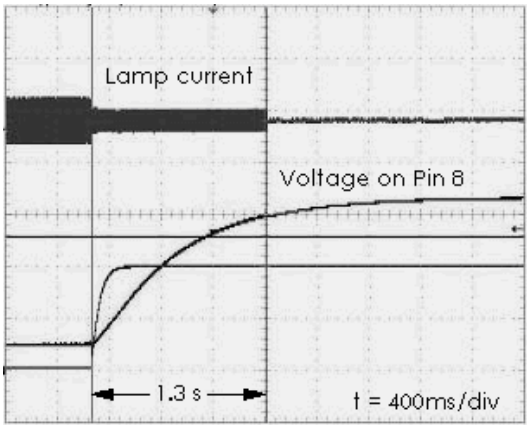
When Q3 is turned off, the voltage at point A approaches Vcc, determined by the proportional ratio of R23 and R25. This voltage charges C20, thus the voltage at point B is rising higher than 0.6 V, eventually triggering the protection.

The open lamp protection circuit is sensitive to this time delay (refer to *Figure 20*). The following considerations should be taken into account:

a) If a low level of digital dimming is required, it means the interval time between two working cycles is relatively long. In this case, the protection must not be falsely triggered. The L6574 uses an RC charging circuit to produce a 1-second delay (R26 / C22).

b) In a multi-lamp situation, even if one lamp goes off, its sense resistor may be affected by the noise from other lamps, which keeps the voltage higher than the bipolar threshold at point C, thus the protection cannot be properly triggered. In this design, one resistor has been added at the emitter of the bipolar to provide some immunity by raising the turn-on threshold.

Figure 20. Open lamp protection time delay

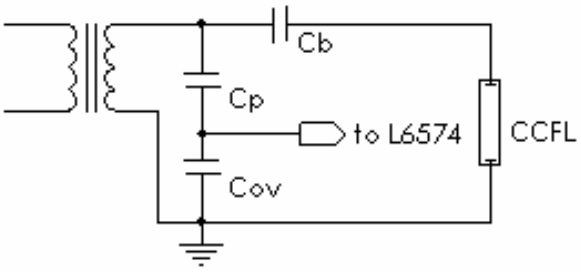


2.5.2 Overvoltage protection

The overvoltage signal (ov) can be detected by the capacitor Cov shown in *Figure 21*. This low voltage capacitor Cov connects in series with the resonance capacitor C_p. With this peak voltage detection circuit, the signal is sent to controller L6574 and the latched shutdown protection function is triggered.

Just a reminder, depending on the lamp condition, the voltage across the secondary winding can be extremely high during the ignition.

Figure 21. Overvoltage detection



2.5.3 Overcurrent protection

The primary current has been monitored for the safety of the MOSFET. A current which is higher than the preset value shuts down the whole circuit to protect the MOSFET. The resistor connected at the low-side MOSFET source junction accomplishes this protection. The resistance should be selected carefully according to the required protection level. However some power loss is introduced if this resistor is used.

3 Description of the half-bridge driver

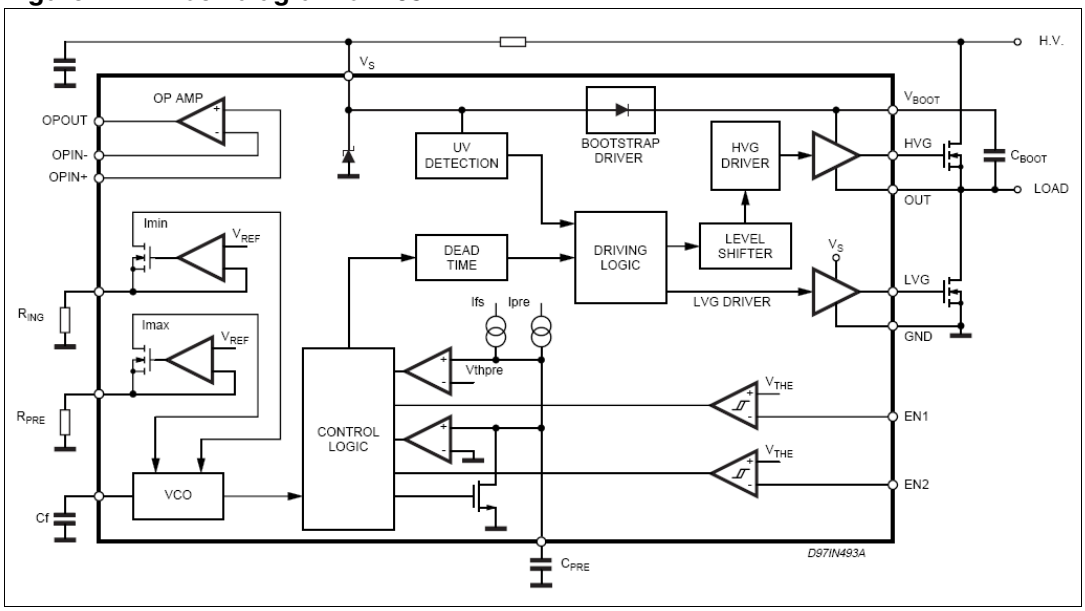
3.1 Functions and block diagram of the IC

The L6574 is the CFL/TL ballast IC intended to drive two N-channel MOSFETs in half-bridge topology thanks to the following inherent versatile features:

- High voltage rail up to 600 V
- High dV/dt immunity ±50 V/ns in full temperature range
- Driver current capability (250 mA source and 450 mA sink)
- CMOS shutdown input
- Undervoltage lockout
- Soft-start frequency shifting timing
- Sense OP AMP for closed-loop control or protection features
- High-accuracy current-controlled oscillator
- Clamping on Vs

The L6574 not only works well in electronic ballast, but can also implement all functions needed in CCFL backlighting applications due to its versatile features. The compromise between cost and performance is the motivation to exploit the aptitude of L6574 to act as the CCFL driver. See *Figure 22* for the block diagram of the L6574.

Figure 22. Block diagram of L6574



3.2 IC pin description in this reference design

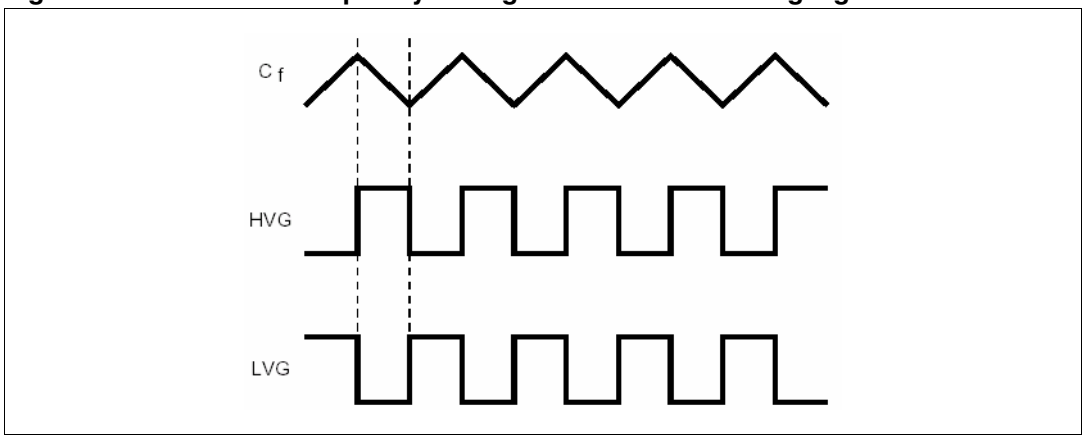
Table 3. IC pin description

Pin number	Pin designate	Description
1	C_{PRE} (C_{SS})	Soft-start timing capacitor. This capacitor sets the soft-start time. This feature is implemented by charging this capacitor with current generated by internal current source and a resistor connected to pin2.
2	R_{PRE}	Soft-start frequency setting resistor. This resistor with C_f and R_{IGN} fixes the difference between maximum frequency and minimum frequency value.
3	C_f	Oscillator frequency setting capacitor. The capacitor along with R_{PRE} and R_{IGN} sets the working frequency. In normal condition, this pin shows a triangular waveform.
4	R_{IGN}	Minimum oscillation frequency setting resistor. This resistor sets the minimum working frequency.
5	OP_{OUT}	Sense OP AMP output. This pin can implement a feedback control loop.
6	OP_{IN-}	Sense OP AMP inverting input
7	OP_{IN+}	Sense OP AMP non-inverting input
8	EN1	Half-bridge latched enable. This pin (active high), forces the device in a latched shutdown state (like in the undervoltage conditions). There are two ways to resume normal operation. The first is to reduce the supply voltage below the undervoltage threshold and then increase it again until the valid supply is recognized. The second is activating EN2 input. The enable 1 is especially designed for strong fault (e.g. in case of lamp disconnection).
9	EN2	Half-bridge unlatched enable. EN2 input (active high) restarts the startup procedure.
10	GND	Ground
11	LVG	Low side driver output
12	VS	Supply voltage with internal Zener clamp
13	N.C.	Not connected
14	OUT	High-side driver reference. This pin must be connected close to the source of the high-side MOS
15	HVG	High-side driver output
16	V_{BOOT}	Bootstrapped supply voltage. The bootstrap capacitor must be connected between this pin and V_S . A patented integrated circuitry replaces the external bootstrap diode, by means of a high-voltage DMOS, synchronously driven with the low-side power MOSFET.

3.3 HVG driver, LVG driver and oscillator frequency

A high and low side driving provide the proper driving signal (*Figure 23*) to the external power MOSFET. The high sink/source driving current (450/250 mA typ.) gives fast switching time performance. The internal logic ensures a minimum deadtime to avoid cross-conduction to the power MOSFET.

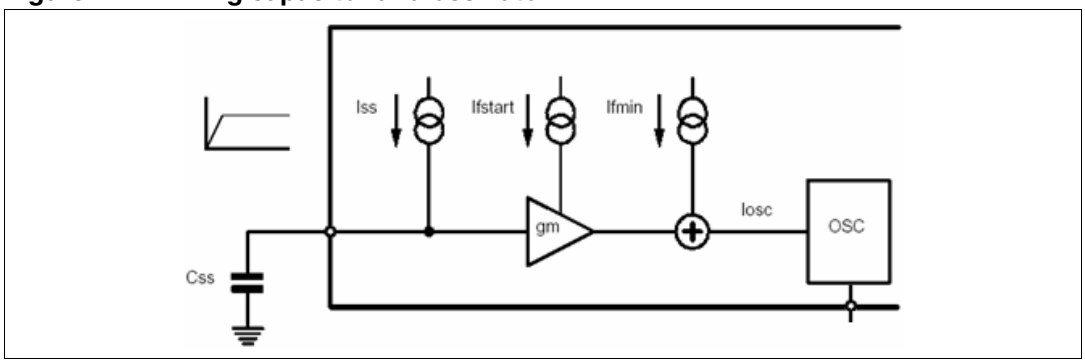
Figure 23. Oscillation frequency vs. high side/low side driving signal



3.4 Timing capacitor, oscillator frequency and equations

The timing capacitor C_{SS} is charged by internal current source (I_{SS}).

Figure 24. Timing capacitor and oscillator



During the soft-start, voltage across C_{SS} generates a voltage ramp and feeds to a transconductance amplifier. In *Figure 24*, I_{SS} is converted in a growing current which is subtracted from I_{fstart}. Therefore the current which drives the oscillator to set the frequency during the soft-start is equal to:

Equation 1

$$I_{OSC} = I_{fmin} + (I_{fstart} - g_m V_{CSS}(t)) = I_{fmin} + \left(I_{fstart} - \frac{g_m I_{SS}}{C_{SS}} t\right)$$

where

Equation 2

$$I_{fmin} = \frac{V_{REF}}{R_{fmin}} \qquad I_{fstart} = \frac{V_{REF}}{R_{fstart}} \qquad V_{REF} = 2\ V$$

At startup (t = 0) the oscillator frequency is set by:

Equation 3

$$I_{OSC}(0) = I_{fmin} + I_{fstart} = V_{REF}\left(\frac{1}{R_{fmin}} + \frac{1}{R_{fstart}}\right)$$

At the end of the soft-start ($t = T_{SS}$) the second term of *Equation 1* decreases to zero and the switching frequency is set only by I_{min} (i.e. R_{fmin}):

Equation 4

$$I_{OSC}(T_{SS}) = I_{fmin} = \frac{V_{REF}}{R_{fmin}}$$

Since the second term of *Equation 1* is equal to zero, we have:

Equation 5

$$I_{fstart} - \frac{g_m I_{SS}}{C_{SS}} T_{SS} = 0 \rightarrow T_{SS} = \frac{C_{SS} I_{fstart}}{g_m I_{SS}}$$

Note that there is not a fixed threshold of voltage across C_{SS} in which the soft-start finishes (i.e. the end of the frequency shifting), and T_{SS} depends on C_{SS}, I_{fstart}, g_m, and I_{SS} (*Equation 5*). Making T_{SS} independent of I_{fstart}, the I_{SS} current has been designed to be a fraction of I_{fstart}, so:

Equation 6

$$I_{SS} = \frac{I_{fstart}}{K} \rightarrow T_{SS} = \frac{C_{SS} I_{fstart}}{g_m I_{fstart} K} \rightarrow T_{SS} = \frac{C_{SS}}{g_m K} \rightarrow T_{SS} - k_{SS} C_{SS}$$

In this way the soft-start time depends only on the capacitor C_{SS}. Here the typical value of k_{SS} constant (soft-start timing constant) is 0.15 s/µF.

The current I_{osc} is fed to the oscillator as shown in *Figure 24*. It is twice mirrored (x4 and x8) generating the triangular wave on the oscillator capacitor C_f. Referring to the internal structure of the oscillator (*Figure 24*), a good relationship to compute an approximate value of the oscillator frequency in normal operation is:

Equation 7

$$f_{min} = \frac{1.41}{R_{fmin} C_f}$$

The degree of approximation depends on the frequency value, but it remains very good in the range from 30 kHz to 100 kHz.

3.5 Figures for F_{min}, R_{min} and F_{start}

When $C_f = 470$ pF has been selected, plots in *Figure 25* help us to find proper value of R_{fmin} based on required minimum operation frequency (fmin).

The operating frequency between F_{start} and fmin is called Δf. According to target Δf and given R_{fmin}, the R_{start} can be well defined. Of course, the R_{start} can be defined in order to obtain a proper Δf. In *Figure 26*, the plot is based on $R_{fmin} = 33$ kΩ. In *Figure 27*, the plot is based on $R_{fmin} = 50$ kΩ and *Figure 28* plot is based on $R_{fmin} = 100$ kΩ.

If C_f is considered below 470 pF, F_{min} is determined in *Figure 29* based on the chosen value of R_f (either by measurement or calculation).

Figure 25. F_{min} vs R_{fmin} at C_f = 470 pF

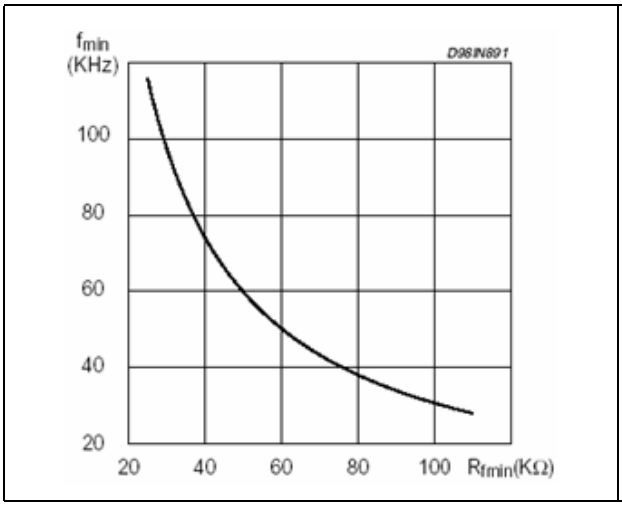


Figure 26. (F_{start} - F_{min}) vs R_{fstart} at C_f = 470 pF

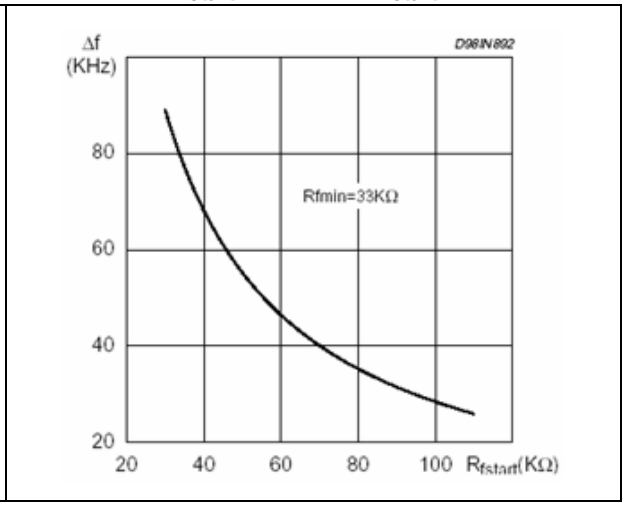


Figure 27. (F_{start} - F_{min}) vs R_{fst} at C_f = 470 pF

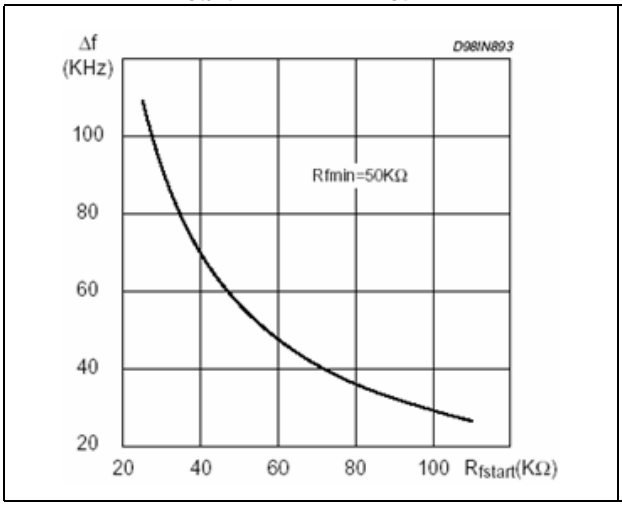


Figure 28. (F_{start} - F_{min}) vs R_{fst} at C_f = 470 pF

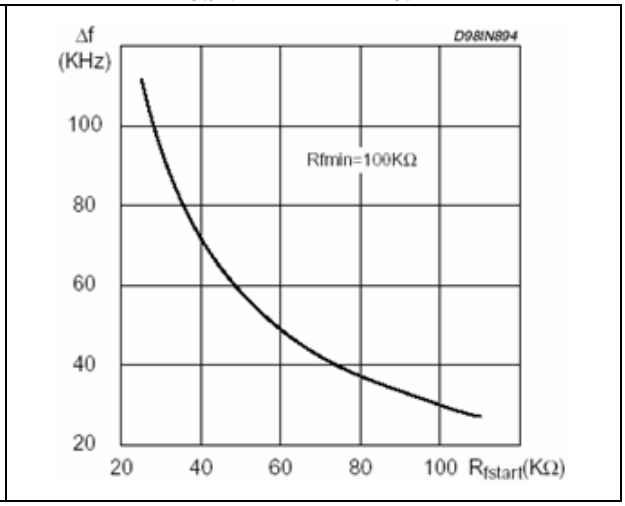
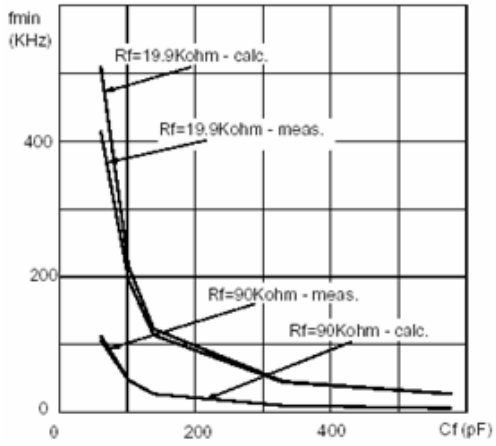


Figure 29. F_{min} at different Rf_{start} vs C_f

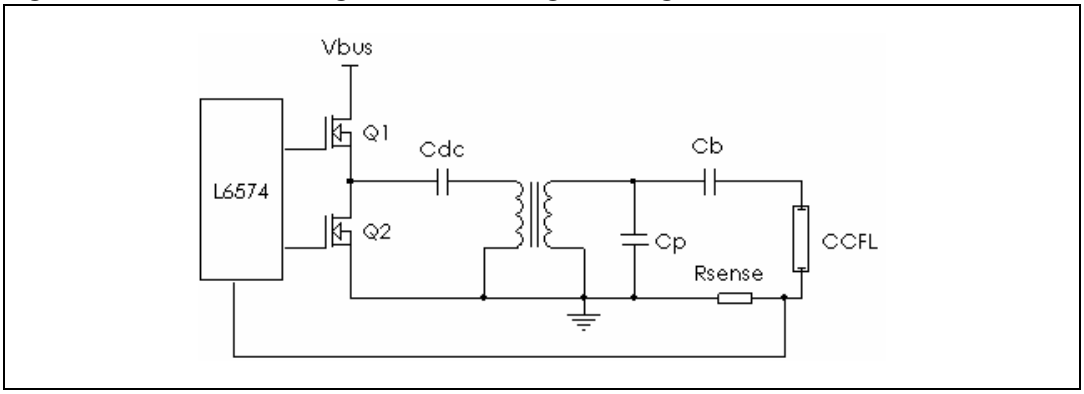


Appendix A Resonant tank design

The transformer and the resonance tank is the most important and difficult section in a CCFL design process. To achieve the best performance, the iteration work is nearly inevitable, especially in the multi-lamp situation. However, the procedure and equations described in this section gives the designer a feasible approach to start the design work.

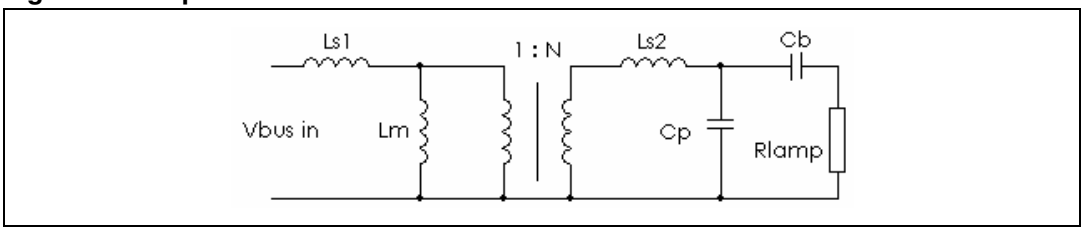
Figure 30 shows a common schematic of a half-bridge CCFL drive circuit. The Cdc is only used to block the DC-component of the input voltage. And normally, compared with C_p and C_b, its value is high enough to be ignored in designing the LC resonant tank.

Figure 30. Schematic diagram of half-bridge backlight inverter



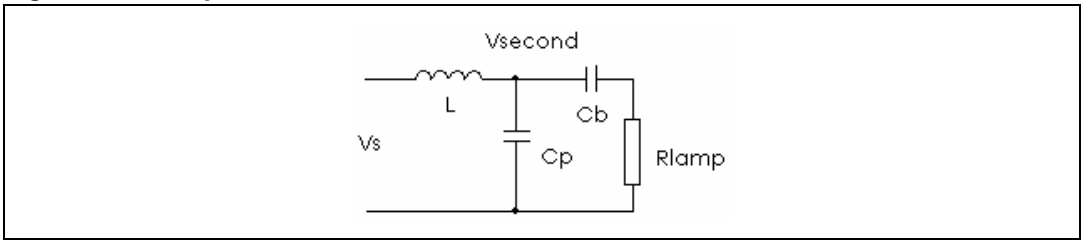
The resonant tank makes use of the leakage inductance of the transformer, so modeling the LC tank cannot make the transformer be treated as an ideal transformer. The equivalent model could be like *Figure 31*.

Figure 31. Equivalent model of resonant tank



The non-ideal transformer can be split into a magnetizing inductance Lm, the leakage inductance of primary side Ls1 and secondary side Ls2, and its turn ratio N. This model can be further simplified by transferring all primary components to the secondary side, like primary leakage inductance, magnetizing inductance and input voltage. The simplified model is shown in *Figure 32*.

Figure 32. Simplified model of resonant tank



The input voltage Vbus at primary side is transferred with the below equation:

Equation 8

$$Vs = \frac{L_m}{L_{s1} + L_m} N V_{Pri} = kNV_{BUS}$$

Please note that Vs is not the real secondary voltage, but the voltage present at the magnetizing inductance Lm transferred to the secondary side of the ideal transformer, which is frequency independent. The factor k, known as the couple factor, is a normally around 0.5 - 0.7 in this kind of application.

The inductance L, which is the series connection of L_{s2} and the parallel value of the primary inductance transferred to the secondary side, can be described as:

Equation 9

$$L = L_{s2} + \frac{L_{s1} L_m}{L_{s1} + L_m} \cdot N^2 = L_{sec}\ (1 - k) + \frac{L^2_{prim}(k - k^2)}{L_{prim}} \cdot \frac{L_{sec}}{L_{prim}} = L_{sec}\ (1 - k^2)$$

The resonant frequency shifts before and after lamp ignition. Before ignition, the infinite impedance of the lamp makes C_b not influence the resonant frequency. Thus the resonant frequency is determined only by C_p.

Equation 10

$$f_{ig} = \frac{1}{2\pi\sqrt{LC_p}}$$

This circuit displays the characteristic of a parallel-load resonant converter. While in parallel-load resonant operation, the inverter behaves like a voltage source to generate the necessary striking voltage. Theoretically, the output voltage of the resonant circuit increases until the lamp ionizes or overvoltage protection is triggered when the frequency keeps approaching the resonant frequency. The minimum working frequency is set by the L6574 pin 4 which normally is around 50 kHz, and the frequency shift starting frequency is set by pin 2 of L6574. So f_{ig} must be fixed in the shifting range of L6574.

Once the lamp has been ignited, the C_b and lamp resistance R_{lamp} can't be ignored any more. By analyzing the circuit, the following transfer function can be derived:

Equation 11

$$\frac{V_{lamp}}{V_s} = \frac{1}{1 - \omega^2 LC_p + j\left(\omega L \frac{C_p}{C_b R_{lamp}} + \omega L \frac{1}{R_{lamp}} - \frac{1}{\omega C_b R_{lamp}}\right)}$$

Please note that ω in *Equation 4* should be calculated using MOSFET switching frequency f-running, not the resonant frequency.

From *Equation 4* the resonant frequency f_{op} can be deduced as follows:

Equation 12

$$f_{op} = \frac{1}{2\pi\sqrt{L(C_p + C_b)}}$$

Properly setting the f_{op} is very important to the total performance of the solution. As a rule of thumb, the switching frequency should stay close to the resonant frequency f_{op} to get a nice sine-wave lamp current. At the same time, the designer must guarantee that the half-bridge

never operates in the capacitive mode which means f-running should be always higher than f_{op} in any case.

As we know, the CCFL shows negative impedance characteristic during startup. The ballast capacitor C_b is used to compensate this characteristic and stabilize the control loop. The value is normally determined experientially to provide 1.5 times impedance as the lamp impedance at switching frequency, thus C_b is determined with regards to the specification of the lamp.

Once the f_{ig}, f_{op}, f-running and C_b have been fixed, it is possible to obtain the L value and C_p by *Equation 3* and *5*. Then by inputting the value of L and C_p into *Equation 4*, Vs is determined. After that, *Equation 1* gives the turn ratio N of the design.

Unlike the Vs, transformer secondary output voltage is frequency dependent. Considering the simplified model in *Figure 32*, the V_{lamp}/V_{second} transfer function can be written as follows:

Equation 13

$$\frac{V_{lamp}}{V_{second}} = \frac{1}{1 + \frac{1}{j\omega C_b R_{lamp}}}$$

To ensure the ignition of CCFL, the maximum striking voltage must be taken into account. Making $R_{lamp} \rightarrow \infty$ in *Equation 6*, the maximum secondary voltage is equal to lamp striking voltage. Then the secondary number of turns N_{sec} can be determined by:

Equation 14

$$N_{sec} = \frac{\sqrt{2} \cdot V_{sec_max}}{2\pi \cdot f \cdot B_{sat} \cdot A_e}$$

Revision history

Table 4. Document revision history

Date	Revision	Changes
23-May-2008	1	Initial release

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