Wide Range Input, Dual/Two-Phase, DC-to-DC Synchronous Buck Controller

ADP1850

FEATURES

Wide range input: 2.75 V to 20 V
Power stage input voltage: 1 V to 20 V
Output voltage range: 0.6 V up to 90% V_{IN}
Output current to more than 25 A per channel
Accurate current sharing between channels (interleaved)
Programmable frequency: 200 kHz to 1.5 MHz
180° phase shift between channels for reduced input capacitance
±0.85% reference voltage accuracy from −40°C to +85°C
Integrated boost diodes
Power saving mode (PSM) at light loads
Accurate power good with internal pull-up resistor
Accurate voltage tracking capability
Independent channel precision enable
Overvoltage and overcurrent limit protection
Externally programmable soft start, slope compensation and current sense gain
Synchronization input
Thermal overload protection
Input undervoltage lockout (UVLO)
Available in 32-lead 5 mm × 5 mm LFCSP

APPLICATIONS

High current single and dual output intermediate bus and point of load converters requiring sequencing and tracking capability, including converters for:
- **Point-of-load power supplies**
- **Telecom base station and networking**
- **Consumer**
- **Industrial and instrumentation**
- **Healthcare and medical**

GENERAL DESCRIPTION

The ADP1850 is a configurable dual output or two-phase, single output dc-to-dc synchronous buck controller capable of running from commonly used 3.3 V to 12 V (up to 20 V) voltage inputs. The device operates in current mode for improved transient response and uses valley current sensing for enhanced noise immunity.

The architecture enables accurate current sharing between interleaved phases for high current outputs.

The ADP1850 is ideal in system applications requiring multiple output voltages: the ADP1850 includes a synchronization feature to eliminate beat frequencies between switching devices; provides accurate tracking capability between supplies and includes precision enable for simple, robust sequencing.

The ADP1850 provides high speed, high peak current drive capability with dead-time optimization to enable energy efficient power conversion. For low load operation, the device can be configured to operate in power saving mode (PSM) by skipping pulses and reducing switching losses to improve the energy efficiency at light load and standby conditions.

The accurate current limit (±6%) allows the power architect to design within a narrower range of tolerances and can reduce overall converter size and cost.

The ADP1850 provides a configurable architecture capable of wide range input operation to provide the designer with maximum re-use opportunities and improved time to market. Additional flexibility is provided by external programmability of loop compensation, soft start, frequency setting, power saving mode, current limit and current sense gain can all be programmed using external components.

The ADP1850 includes a high level of integration in a small size package. The start-up linear regulator and the boot-strap diode for the high side drive are included. Protection features include: undervoltage lock-out, overvoltage, overcurrent/short-circuit and over temperature. The ADP1850 is available in a compact 32-lead LFCSP 5 mm × 5 mm thermally enhanced package.

TYPICAL OPERATION CIRCUIT

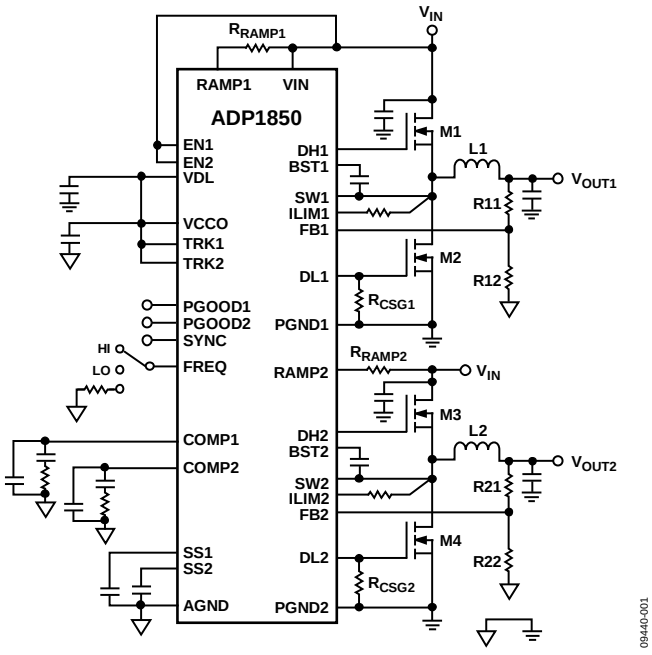


Figure 1. Single Phase Circuit

Rev. 0

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **©2010 Analog Devices, Inc. All rights reserved.**

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REVISION HISTORY

11/10—Revision 0: Initial Version

SPECIFICATIONS

All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). V_{IN} = 12 V. The specifications are valid for T_J = −40°C to +125°C, unless otherwise specified. Typical values are at T_A = 25°C.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
Input Voltage	V_{IN}		2.75		20	V
Undervoltage Lockout Threshold	IN_{UVLO}	V_{IN} rising	2.45	2.6	2.75	V
		V_{IN} falling	2.4	2.5	2.6	
Undervoltage Lockout Hysteresis				0.1		V
Quiescent Current	I_{IN}	EN1 = EN2 = V_{IN} = 12 V, V_{FB} = V_{CCO} in PWM mode (no switching)		4.5	5.8	mA
		EN1 = EN2 = V_{IN} = 12 V, V_{FB} = V_{CCO} in PSM mode		2.8		mA
Shutdown Current	I_{IN_SD}	EN1 = EN2 = GND, V_{IN} = 5.5 V or 20 V		100	200	µA
ERROR AMPLIFIER						
FBx Input Bias Current	I_{FB}		−100	+1	+100	nA
Transconductance	G_m	Sink or source 1 µA	385	550	715	µS
TRK1, TRK2 Input Bias Current	I_{TRK}	0 V ≤ V_{TRK1}/V_{TRK2} ≤ 5 V	−100	+1	+100	nA
CURRENT SENSE AMPLIFIER GAIN	A_{CS}	Gain resistor connected to DLx, R_{CSG} = 47 kΩ ± 5%	2.4	3	3.6	V/V
		Gain resistor connected to DLx, R_{CSG} = 22 kΩ ± 5%	5.2	6	6.9	V/V
		Default setting, R_{CSG} = open	10.5	12	13.5	V/V
		Gain resistor connected to DLx, R_{CSG} = 100 kΩ ± 5%	20.5	24	26.5	V/V
OUTPUT CHARACTERICTISTICS						
Feedback Accuracy Voltage	V_{FB}	T_J = −40°C to +85°C, V_{FB} = 0.6 V	−0.85%	+0.6	+0.85%	V
		T_J = −40°C to +125°C, V_{FB} = 0.6 V	−1.5%	+0.6	+1.5%	V
Line Regulation of PWM	$\Delta V_{FB}/\Delta V_{IN}$			±0.015		%/V
Load Regulation of PWM	$\Delta V_{FB}/\Delta V_{COMP}$	V_{COMP} range = 0.9 V to 2.2 V		±0.3		%
OSCILLATOR						
Frequency	f_{SW}	R_{FREQ} = 340 kΩ to AGND	170	200	235	kHz
		R_{FREQ} = 78.7 kΩ to AGND	720	800	880	kHz
		R_{FREQ} = 39.2 kΩ to AGND	1275	1500	1725	kHz
		FREQ to AGND	235	300	345	kHz
		FREQ to VCCO	475	600	690	kHz
SYNC Input Frequency Range	f_{SYNC}	f_{SYNC} = 2 × f_{SW}	400		3000	kHz
SYNC Input Pulse Width	$t_{SYNCMIN}$		100			ns
SYNC Pin Capacitance to GND	C_{SYNC}			5		pF
LINEAR REGULATOR						
VCCO Output Voltage		I_{VCCO} = 100 mA	4.7	5.0	5.3	V
VCCO Load Regulation		I_{VCCO} = 0 mA to 100 mA,		35		mV
VCCO Line Regulation		V_{IN} = 5.5 V to 20 V, I_{VCCO} = 20 mA		10		mV
VCCO Current Limit[1]		VCCO drops to 4 V from 5 V		350		mA
VCCO Short-Circuit Current[1]		VCCO < 0.5 V		370	400	mA
VIN to VCCO Dropout Voltage[2]	$V_{DROPOUT}$	I_{VCCO} = 100 mA, V_{IN} ≤ 5 V		0.33		V
LOGIC INPUTS						
EN1, EN2		EN1/EN2 rising	0.57	0.63	0.68	V
EN1, EN2 Hysteresis				0.03		V
EN1, EN2 Input Leakage Current	I_{EN}	V_{IN} = 2.75 V to 20 V		1	200	nA
SYNC Logic Input Low					1.3	V
SYNC Logic Input High			1.9			V
SYNC Input Pull-Down Resistance	R_{SYNC}			1		MΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GATE DRIVERS						
DHx Rise Time		C_{DH} = 3 nF, $V_{BST} - V_{SW}$ = 5 V		16		ns
DHx Fall Time		C_{DH} = 3 nF, $V_{BST} - V_{SW}$ = 5 V		14		ns
DLx Rise Time		C_{DL} = 3 nF		16		ns
DLx Fall Time		C_{DL} = 3 nF		14		ns
DHx to DLx Dead Time		External 3 nF is connected to DHx and DLx		25		ns
DHx or DLx Driver R_{ON}, Sourcing Current[1]	R_{ON_SOURCE}	Sourcing 2 A with a 100 ns pulse		2		Ω
		Sourcing 1 A with a 100 ns pulse, V_{IN} = 3 V		2.3		Ω
DHx or DLx Driver R_{ON}, Tempco	TC_{RON}	V_{IN} = 3 V or 12 V		0.3		%/°C
DHx or DLx Driver R_{ON}, Sinking Current[1]	R_{ON_SINK}	Sinking 2 A with a 100 ns pulse		1.5		Ω
		Sinking 1 A with a 100 ns pulse, V_{IN} = 3 V		2		Ω
DHx Maximum Duty Cycle		f_{SW} = 300 kHz	90			%
DHx Maximum Duty Cycle		f_{SW} = 1500 kHz	50			%
Minimum DHx On Time		f_{SW} = 200 kHz to 1500 kHz			135	ns
Minimum DHx Off Time		f_{SW} = 200 kHz to 1500 kHz			335	ns
Minimum DLx On Time		f_{SW} = 200 kHz to 1500 kHz			285	ns
COMPx VOLTAGE RANGE						
COMPx Pulse Skip Threshold	$V_{COMP,THRES}$	In pulse skip mode		0.9		V
COMPx Clamp High Voltage	$V_{COMP,HIGH}$		2.25			V
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{TMSD}			155		°C
Thermal Shutdown Hysteresis				20		°C
OVERVOLTAGE AND POWER GOOD THRESHOLDS						
FBx Overvoltage Threshold	V_{OV}	V_{FB} rising	0.635	0.65	0.665	V
FBx Overvoltage Hysteresis				30		mV
FBx Undervoltage Threshold	V_{UV}	V_{FB} falling	0.525	0.55	0.578	V
FBx Undervoltage Hysteresis				30		mV
TRKx INPUT VOLTAGE RANGE			0		5	V
FBx TO TRKx OFFSET VOLTAGE		TRKx = 0.1 V to 0.57 V, offset = $V_{FB} - V_{TRK}$	−10	0	+10	mV
SOFT START						
SSx Output Current	I_{SS}	During start-up	4.6	6.5	8.4	µA
SSx Pull-Down Resistor		During a fault condition		3		kΩ
FBx to SSx Offset		V_{SS} = 0.1 V to 0.6 V, offset = $V_{FB} - V_{SS}$	−10		+10	mV
PGOODx						
PGOODx Pull-up Resistor	R_{PGOOD}	Internal pull-up resistor to VCCO		12.5		kΩ
PGOODx Delay				12		µs
Over Voltage or Under Voltage Minimum Duration		This is the minimum duration required to trip the PGOOD signal		10		µs
ILIM1, ILIM2 Threshold Voltage[1]		Relative to PGNDx	−5	0	+5	mV
ILIM1, ILIM2 Output Current		ILIMx = PGNDx	47	50	53	µA
Current Sense Blanking Period		After DLx goes high, current limit is not sensed during this period		100		ns
INTEGRATED RECTIFIER (BOOST DIODE) RESISTANCE		At 20 mA forward current		16		Ω
ZERO CURRENT CROSS OFFSET (SWx TO PGNDx)[1]		In pulse skip mode only, f_{SW} = 600 kHz	0	2	4	mV

[1] Guaranteed by design.
[2] Connect V_{IN} to VCCO when 2.75 V < V_{IN} < 5.5 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, EN1/EN2, RAMP1/RAMP2	21 V
FB1/FB2, COMP1/COMP2, SS1/SS2, TRK1/TRK2, FREQ, SYNC, VCCO, VDL, PGOOD1/PGOOD2	−0.3 V to +6 V
ILIM1/ILIM2, SW1/SW2 to PGND1/PGND2	−0.3 V to +21 V
BST1/BST2, DH1/DH2 to PGND1/PGND2	−0.3 V to +28 V
DL1/DL2 to PGND1/PGND2	−0.3V to VCCO + 0.3 V
BST1/BST2 to SW1/SW2	−0.3 V to +6 V
BST1/BST2 to PGND1/PGND2 20 ns Transients	32 V
SW1/SW2 to PGND1/PGND2 20 ns Transients	25 V
DL1/DL2, SW1/SW2, ILIM1/ILIM2 to PGND1/PGND2 20 ns Negative Transients	−8 V
PGND1/PGND2 to AGND	−0.3 V to +0.3 V
PGND1/PGND2 to AGND 20 ns Transients	−8 V to +4 V
θ_{JA} on Multilayer PCB (Natural Convection)[1, 2]	32.6°C/W
Operating Junction Temperature Range[3]	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Soldering Lead Temperature	260°C

[1] Measured with exposed pad attached to PCB.
[2] Junction-to-ambient thermal resistance (θ_{JA}) of the package was calculated or simulated on multilayer PCB.
[3] The junction temperature, T_J, of the device is dependent on the ambient temperature, T_A, the power dissipation of the device, P_D, and the junction-to-ambient thermal resistance of the package, θ_{JA}. Maximum junction temperature is calculated from the ambient temperature and power dissipation using the formula: $T_J = T_A + P_D \times \theta_{JA}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

SIMPLIFIED BLOCK DIAGRAM

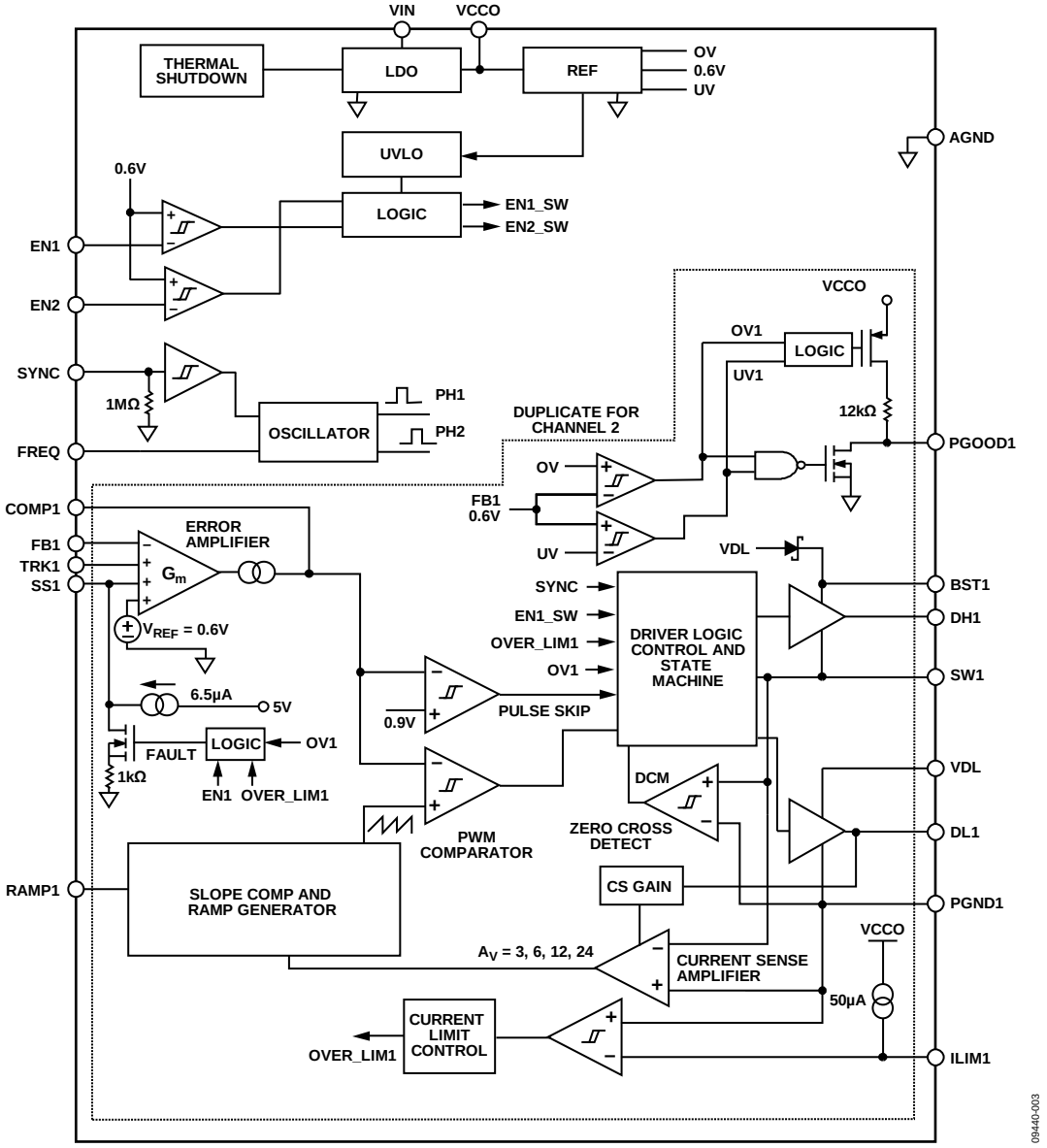


Figure 2.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

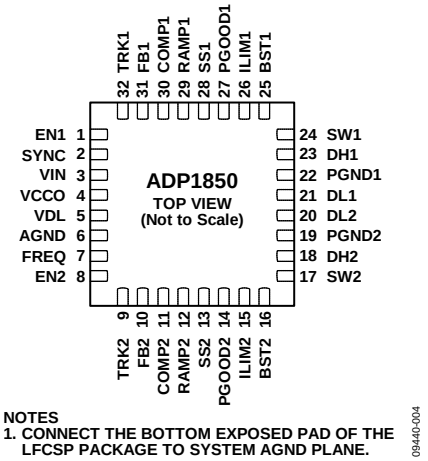


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN1	Enable Input for Channel 1. Drive EN1 high to turn on the Channel 1 controller, and drive EN1 low to turn off the Channel 1 controller. Tie EN1 to VIN for automatic startup. For a precision UVLO, put an appropriately sized resistor divider from VIN to AGND and tie the midpoint to this pin.
2	SYNC	Frequency Synchronization Input. Accepts an external signal between 1× and 2.3× of the internal oscillator frequency, f_{SW}, set by the FREQ pin. The controller operates in forced PWM when a signal is detected at SYNC or when SYNC is high. The resulting switching frequency is ½ of the SYNC frequency. When SYNC is low or left floating, the controller operates in pulse skip mode. For dual-phase operation, connect SYNC to a logic high or an external clock.
3	VIN	Connect to Main Power Supply. Bypass with a 1 µF or larger ceramic capacitor connected as close to this pin as possible and PGNDx.
4	VCCO	Output of the Internal Low Dropout Regulator (LDO). Bypass VCCO to AGND with a 1 µF or larger ceramic capacitor. The VCCO output remains active even when EN1 and EN2 are low. For operation with VIN below 5 V, VIN may be shorted to VCCO. Do not use the LDO to power other auxiliary system loads.
5	VDL	Power Supply for the Low-Side Driver. Bypass VDL to PGNDx with a 1 µF or greater ceramic capacitor. Connect VCCO to VDL.
6	AGND	Analog Ground.
7	FREQ	Sets the desired operating frequency between 200 kHz and 1.5 MHz with one resistor between FREQ and AGND. Connect FREQ to AGND for a preprogrammed 300 kHz or FREQ to VCCO for 600 kHz operating frequency.
8	EN2	Enable Input for Channel 2. Drive EN2 high to turn on the Channel 2 controller, and drive EN2 low to turn off the Channel 2 controller. Tie EN2 to VIN for automatic startup. For a precision UVLO, put an appropriately sized resistor divider from VIN to AGND, and tie the midpoint to this pin.
9	TRK2	Tracking Input for Channel 2. Connect TRK2 to VCCO if tracking is not used.
10	FB2	Output Voltage Feedback for Channel 2. Connect to Output 2 via a resistor divider.
11	COMP2	Compensation Node for Channel 2. Output of Channel 2 error amplifier. Connect a series resistor-capacitor network from COMP2 to AGND to compensate the regulation control loop.
12	RAMP2	Connect a resistor from RAMP2 to VIN to set up a ramp current for slope compensation in Channel 2. The voltage at RAMP2 is 0.2 V. This pin is high impedance when the channel is disabled.
13	SS2	Soft Start Input for Channel 2. Connect a capacitor from SS2 to AGND to set the soft start period. The node is internally pulled up to 5 V with a 6.5 µA current source.
14	PGOOD2	Power Good. Open-drain power-good indicator logic output with an internal 12 kΩ resistor connected between PGOOD2 and VCCO. PGOOD2 is pulled to ground when the Channel 2 output is outside the regulation window. An external pull-up resistor is not required.

Pin No.	Mnemonic	Description
15	ILIM2	Current Limit Sense Comparator Inverting Input for Channel 2. Connect a resistor between ILIM2 and SW2 to set the current limit offset. For accurate current limit sensing, connect ILIM2 to a current sense resistor at the source of the low-side MOSFET.
16	BST2	Boot-Strapped Upper Rail of High Side Internal Driver for Channel 2. Connect a multilayer ceramic capacitor (0.1 µF to 0.22 µF) between BST2 and SW2. There is an internal boost rectifier connected between VDL and BST2.
17	SW2	Switch Node for Channel 2. Connect to source of the high-side N-channel MOSFET and the drain of the low-side N-channel MOSFET of Channel 2.
18	DH2	High-Side Switch Gate Driver Output for Channel 2. Capable of driving MOSFETs with total input capacitance up to 20 nF.
19	PGND2	Power Ground for Channel 2. Ground for internal Channel 2 driver. Differential current is sensed between SW2 and PGND2. Use the Kelvin sensing connection technique between PGND2 and source of the low-side MOSFET.
20	DL2	Low-Side Synchronous Rectifier Gate Driver Output for Channel 2. To set the gain of the current sense amplifier, connect a resistor between DL2 and PGND2. Capable of driving MOSFETs with a total input capacitance up to 20 nF.
21	DL1	Low-Side Synchronous Rectifier Gate Driver Output for Channel 1. To set the gain of the current sense amplifier, connect a resistor between DL1 and PGND1. Capable of driving MOSFETs with a total input capacitance up to 20 nF.
22	PGND1	Power Ground for Channel 1. Ground for internal Channel 1 driver. Differential current is sensed between SW1 and PGND1. Use the Kelvin sensing connection technique between PGND1 and source of the low-side MOSFET.
23	DH1	High-Side Switch Gate Driver Output for Channel 1. Capable of driving MOSFETs with a total input capacitance up to 20 nF.
24	SW1	Power Switch Node for Channel 1. Connect to source of the high-side N-channel MOSFET and the drain of the low-side N-channel MOSFET of Channel 1.
25	BST1	Boot-Strapped Upper Rail of High Side Internal Driver for Channel 1. Connect a multilayer ceramic capacitor (0.1 µF to 0.22 µF) between BST1 and SW1. There is an internal boost diode or rectifier connected between VDL and BST1.
26	ILIM1	Current Limit Sense Comparator Inverting Input for Channel 1. Connect a resistor between ILIM1 and SW1 to set the current limit offset. For accurate current limit sensing, connect ILIM1 to a current sense resistor at the source of the low-side MOSFET.
27	PGOOD1	Power Good. Open-drain power-good indicator logic output with an internal 12 kΩ resistor connected between PGOOD1 and VCCO. PGOOD1 is pulled to ground when the Channel 1 output is outside the regulation window. An external pull-up resistor is not required.
28	SS1	Soft Start Input for Channel 1. Connect a capacitor from SS1 to AGND to set the soft start period. This node is internally pulled up to 5 V with a 6.5 µA current source.
29	RAMP1	Connect a resistor from RAMP1 to VIN to set up a ramp current for slope compensation in Channel 1. The voltage at RAMP2 is 0.2 V. This pin is high impedance when the channel is disabled.
30	COMP1	Compensation Node for Channel 1. Output of Channel 1 error amplifier. Connect a series resistor-capacitor network from COMP1 to AGND to compensate the regulation control loop.
31	FB1	Output Voltage Feedback for Channel 1. Connect to Output 1 via a resistor divider.
32	TRK1	Tracking Input for Channel 1. Connect TRK1 to VCCO if tracking is not used.
33 (EPAD)	Exposed Pad (EPAD)	Connect the bottom exposed pad of the LFCSP package to the system AGND plane.

TYPICAL PERFORMANCE CHARACTERISTICS

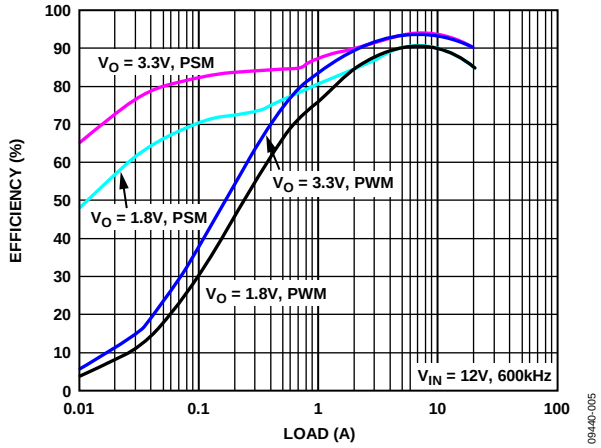


Figure 4. Efficiency Plot of Figure 44

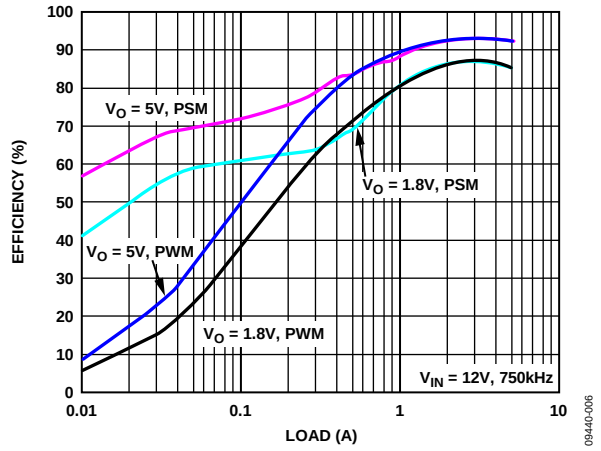


Figure 5. Efficiency Plot of Figure 45

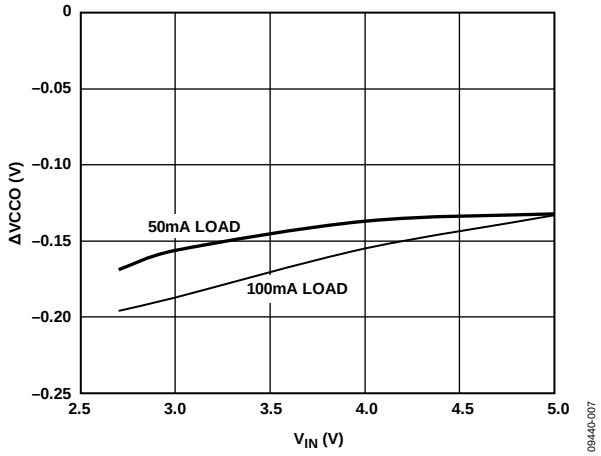


Figure 6. LDO Load Regulation

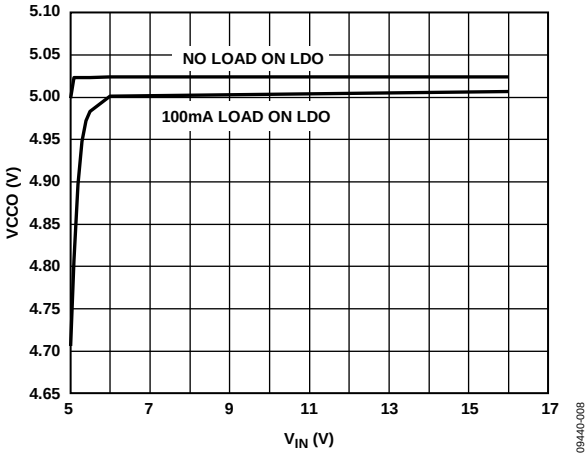


Figure 7. LDO Line Regulation

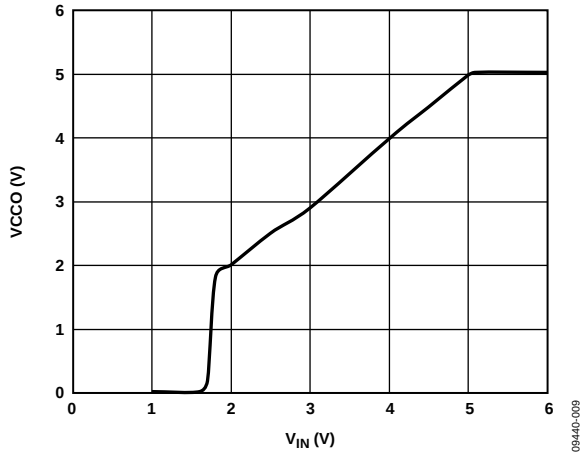


Figure 8. VCCO vs. V_{IN}

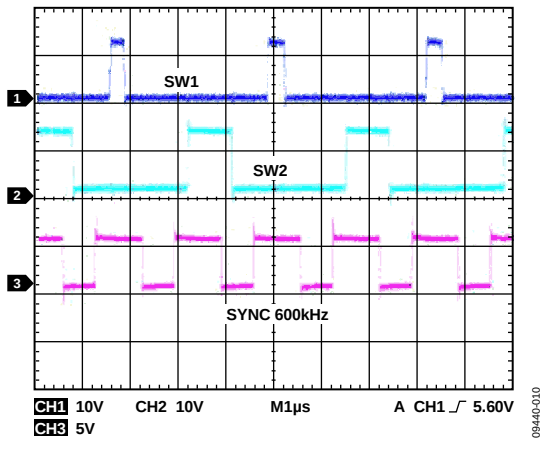


Figure 9. An Example of Synchronization, f_{SYNC} = 600 kHz

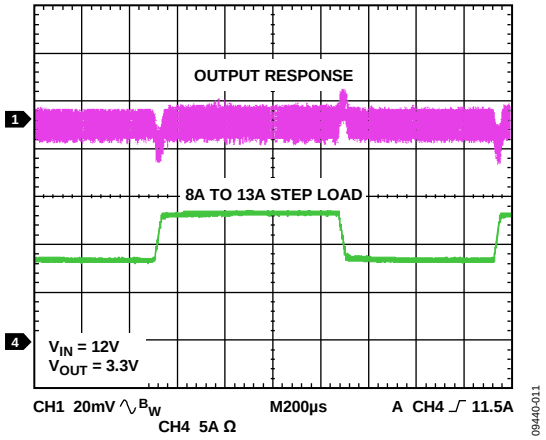


Figure 10. Step Load Transient of Figure 44

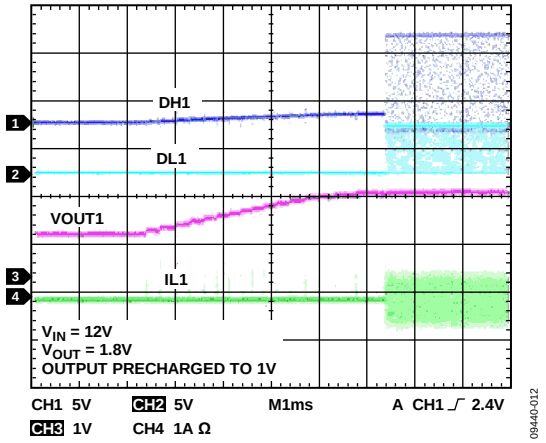


Figure 11. Soft Start into Precharged Output

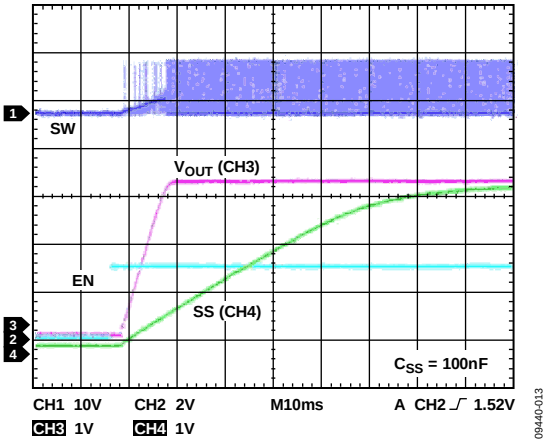


Figure 12. Enable Start-Up Function

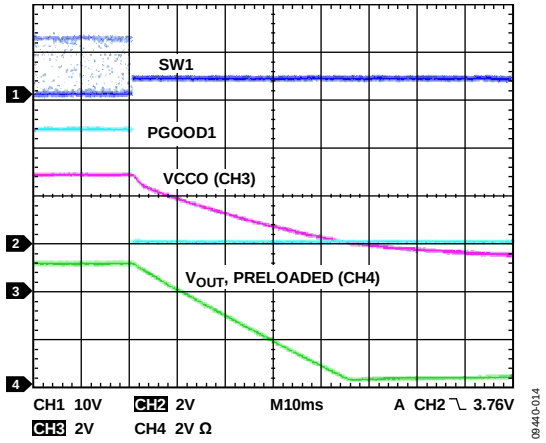


Figure 13. Thermal Shutdown Waveform

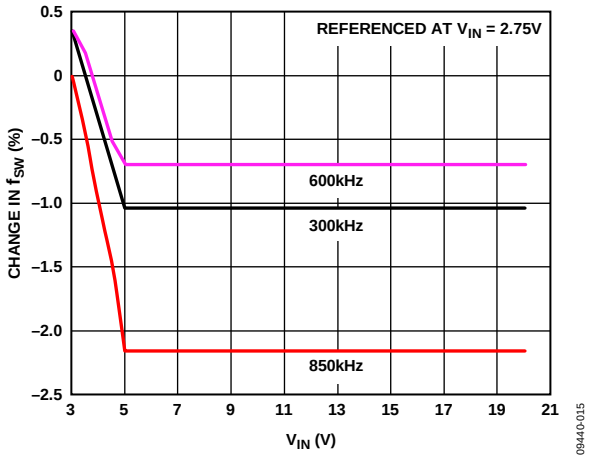


Figure 14. Change in f_{SW} vs. V_{IN}

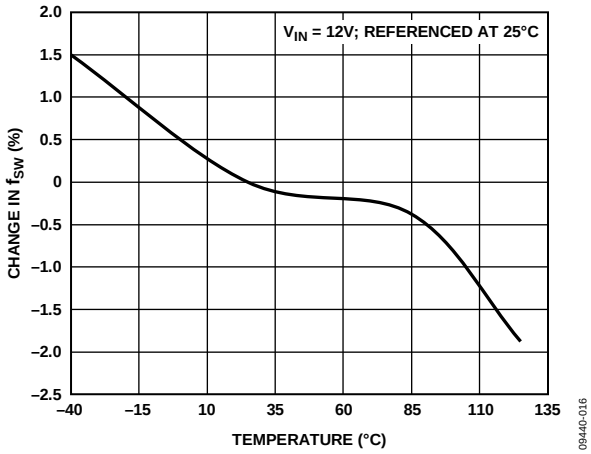


Figure 15. f_{SW} vs. Temperature

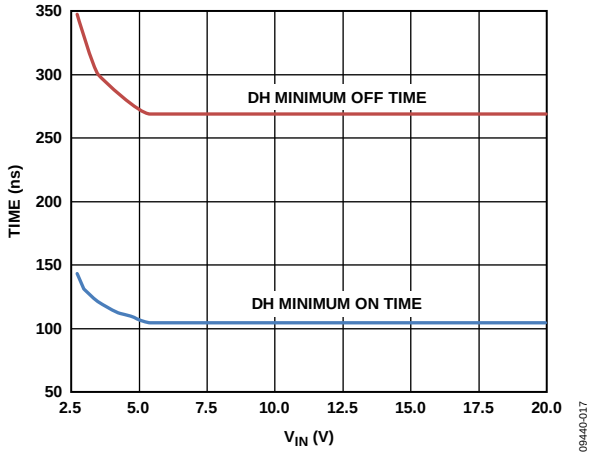


Figure 16. Typical DH Minimum On Time and Off Time

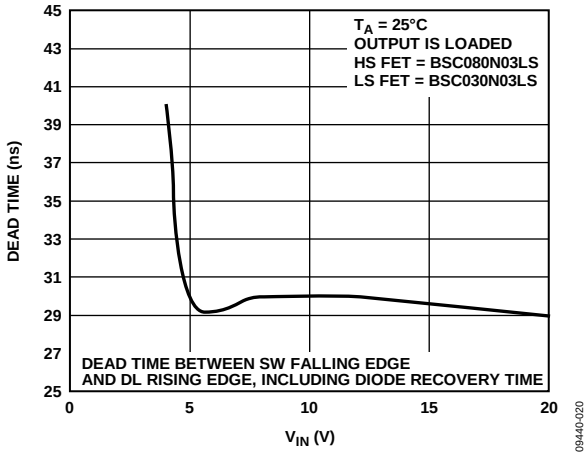


Figure 19. Dead Time vs. V_{IN}

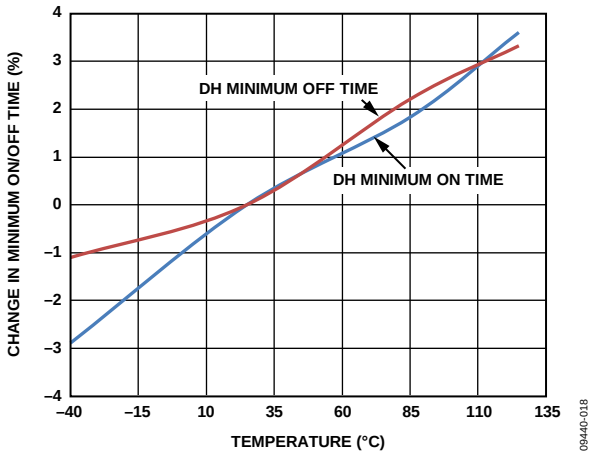


Figure 17. DH Minimum On Time and Off Time Over Temperature

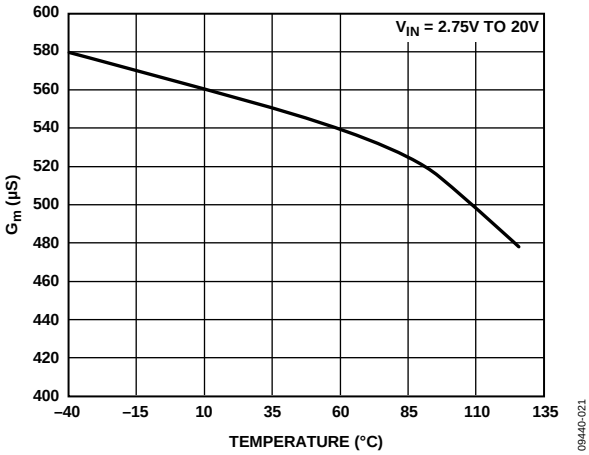


Figure 20. G_m of Error Amplifier vs. Temperature

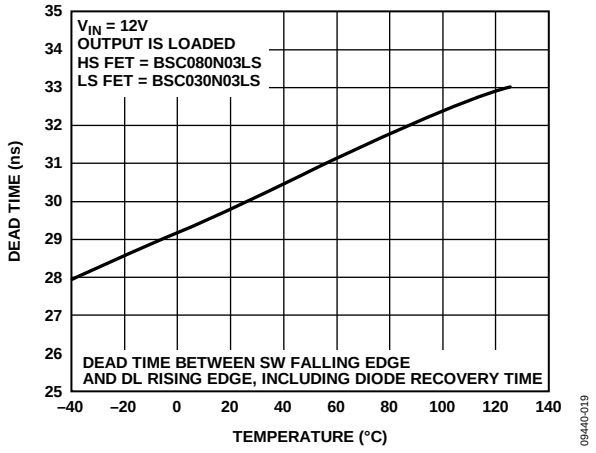


Figure 18. Dead Time vs. Temperature

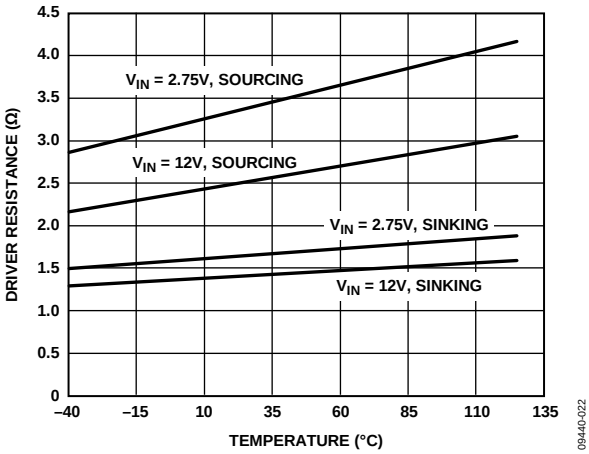


Figure 21. Driver Resistance vs. Temperature

THEORY OF OPERATION

The ADP1850 is a current mode, dual-channel, step-down switching controller with integrated MOSFET drivers for external N-channel synchronous power MOSFETs. The two outputs are phase shifted 180°. This reduces the input RMS ripple current, thus minimizing required input capacitance. In addition, the two outputs can be combined for dual-phase PWM operation that can deliver more than 50 A output current and the two channels are optimized for current sharing.

The ADP1850 can be set to operate in pulse skip high efficiency mode (power saving mode) under light load or in forced PWM. The integrated boost diodes in the ADP1850 reduce the overall system cost and component count. The ADP1850 includes programmable soft start, output overvoltage protection, programmable current limit, power good, and tracking function. The ADP1850 can be set to operate in any switching frequency between 200 kHz and 1.5 MHz with one external resistor.

CONTROL ARCHITECTURE

The ADP1850 is based on a fixed frequency, current mode, PWM control architecture. The inductor current is sensed by the voltage drop measured across the external low-side MOSFET, R_{DSON}, during the off period of the switching cycle (valley inductor current). The current sense signal is further processed by the current sense amplifier. The output of the current sense amplifier is held, and the emulated current ramp is multiplexed and fed into the PWM comparator as shown in Figure 22. The valley current information is captured at the end of the off period, and the emulated current ramp is applied at that point when the next on cycle begins. An error amplifier integrates the error between the feedback voltage and the generated error voltage from the COMPx pin (from error amplifier in Figure 22).

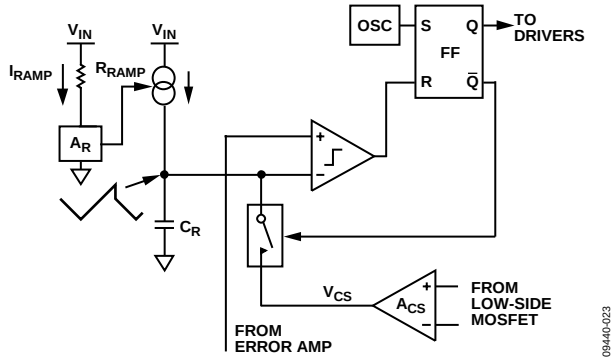


Figure 22. Simplified Control Architecture

As shown in Figure 22, the emulated current ramp is generated inside the IC but offers programmability through the RAMPx pin. Selecting an appropriate value resistor from V_{IN} to the RAMPx pin programs a desired slope compensation value and, at the same time, provides a feed forward feature. The benefits realized by deploying this type of control scheme are that there is no need to worry about the turn-on current spike corrupting the current ramp. Also, the current signal is stable because the current signal is sampled at the end of the turn-off period, which gives time for the switch node ringing to settle. Other benefits of using current mode control scheme still apply, such as simplicity of loop compensation. Control logic enforces antishoot-through operation to limit cross conduction of the internal drivers and external MOSFETs.

OSCILLATOR FREQUENCY

The internal oscillator frequency, which ranges from 200 kHz to 1.5 MHz, is set by an external resistor, R_{FREQ}, at the FREQ pin. Some popular f_{SW} values are shown in Table 4, and a graphical relationship is shown in Figure 23. For instance, a 78.7 kΩ resistor sets the oscillator frequency to 800 kHz. Furthermore, connecting FREQ to AGND or FREQ to VCCO sets the oscillator frequency to 300 kHz or 600 kHz, respectively. For other frequencies that are not listed in Table 4, the values of R_{FREQ} and f_{SW} can be obtained from Figure 23, or use the following empirical formula to calculate these values:

$$R_{FEQ}\,(\text{k}\Omega) = 96568 \times f_{SW}\,(\text{kHz})^{-1.065}$$

Table 4. Setting the Oscillator Frequency

R_{FREQ}	f_{SW} (Typical)
332 kΩ	200 kHz
78.7 kΩ	800 kHz
60.4 kΩ	1000 kHz
51 kΩ	1200 kHz
40.2 kΩ	1500 kHz
FREQ to AGND	300 kHz
FREQ to VCCO	600 kHz

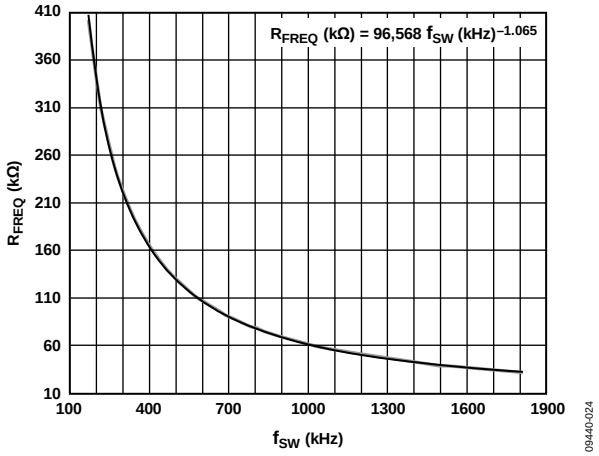


Figure 23. R_{FREQ} vs. f_{SW}

MODES OF OPERATION

The SYNC pin is a multifunctional pin. PWM mode is enabled when SYNC is connected to VCCO or a high logic. With SYNC connected to ground or left floating, the pulse skip mode is enabled. Switching SYNC from low to high or high to low on the fly causes the controller to transition from forced PWM to pulse skip mode or pulse skip mode to forced PWM, respectively, in two clock cycles.

Table 5. Mode of Operation Truth Table

SYNC Pin	Mode of Operation
Low	Pulse skip mode
High	Forced PWM or two-phase operation
No Connect	Pulse skip mode
Clock Signal	Forced PWM or two-phase operation

The ADP1850 has a pulse skip sensing circuitry that allows the controller to skip PWM pulses, thus, reducing the switching frequency at light loads and, therefore, maintaining high efficiency during a light load operation. The switching frequency is a fraction of the natural oscillator frequency and is automatically adjusted to regulate the output voltage. The resulting output ripple is larger than that of the fixed frequency forced PWM. Figure 24 shows that the ADP1850 operates in PSM under a very light load. Pulse skip frequency under light load is dependent on the inductor, output capacitance, output load, and input and output voltages.

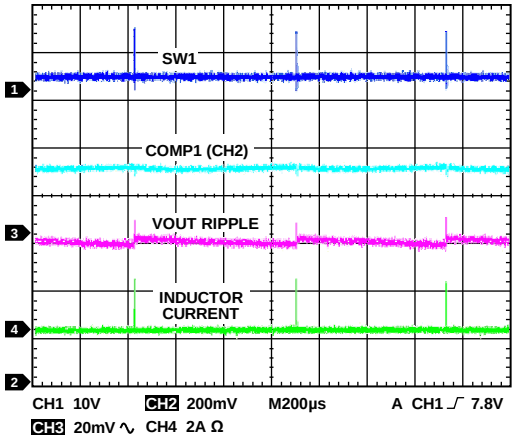


Figure 24. Example of Pulse Skip Mode Under Light Load

When the output load is greater than the pulse skip threshold current, that is, V_{COMP} reaches the threshold of 0.9 V, the ADP1850 exits the pulse skip mode of operation and enters the fixed frequency discontinuous conduction mode (DCM), as shown in Figure 25. When the load increases further, the ADP1850 enters CCM.

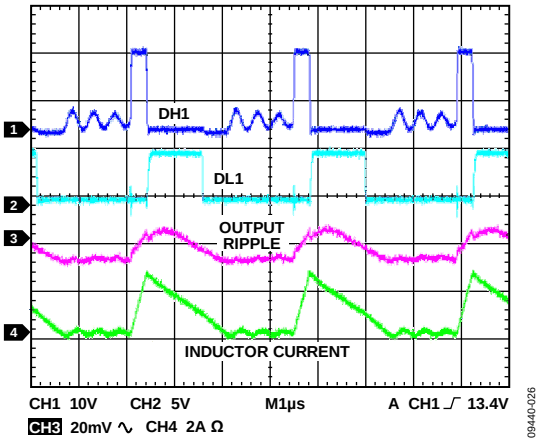


Figure 25. Example of Discontinuous Conduction Mode (DCM) Waveform

In forced PWM, the ADP1850 always operates in CCM at any load. The inductor current is always continuous, thus, efficiency is poor at light loads.

SYNCHRONIZATION

The switching frequency of the ADP1850 can be synchronized to an external clock by connecting SYNC to a clock signal. The external clock should be between 1× and 2.3× of the internal oscillator frequency, f_{SW}. The resulting switching frequency is ½ of the external SYNC frequency because the SYNC input is divided by 2, and the resulting phases are used to clock the two channels alternately. In synchronization, the ADP1850 operates in PWM.

When an external clock is detected at the first SYNC edge, the internal oscillator is reset, and the clock control shifts to SYNC. The SYNC edges then trigger subsequent clocking of the PWM outputs. The DH1/DH2 rising edges appear approximately 100 ns after the corresponding SYNC edge, and the frequency is locked to the external signal. Depending on the start-up conditions of Channel 1 and Channel 2, either Channel 1 or Channel 2 can be the first channel synchronized to the rising edge of the SYNC clock. If the external SYNC signal disappears during operation, the ADP1850 reverts to its internal oscillator. When the SYNC function is used, it is recommended to connect a pull-up resistor from SYNC to VCCO so that when the SYNC signal is lost, the ADP1850 continues to operate in PWM.

SYNCHRONOUS RECTIFIER AND DEAD TIME

The synchronous rectifier (low-side MOSFET) improves efficiency by replacing the Schottky diode that is normally used in an asynchronous buck regulator. In the ADP1850, the antishoot-through circuit monitors the SW and DL nodes and adjusts the low-side and high-side drivers to ensure break-before-make switching which prevents cross-conduction or shoot-through between the high-side and low-side MOSFETs. This break-before-make switching is known as dead time, which is not fixed and depends on how fast the MOSFETs are turned on and off. In a typical application circuit that uses medium sized MOSFETs with input capacitance of approximately 3 nF, the typical dead time is approximately 30 ns. When small and fast MOSFETs with fast diode recovery time are used, the dead time can be as low as 13 ns.

INPUT UNDERVOLTAGE LOCKOUT

When the bias input voltage, V_{IN}, is less than the undervoltage lockout (UVLO) threshold, the switch drivers stay inactive. When V_{IN} exceeds the UVLO threshold, the switchers start switching.

INTERNAL LINEAR REGULATOR

The internal linear regulator is low dropout (LDO) meaning it can regulate its output voltage, VCCO. VCCO powers up the internal control circuitry and provides power for the gate drivers. It is guaranteed to have more than 200 mA of output current capability, which is sufficient to handle the gate drive requirements of typical logic threshold MOSFETs driven at up to 1.5 MHz. VCCO is always active and cannot be shut down by the EN1 and EN2 pins. Bypass VCCO to AGND with a 1 µF or greater capacitor.

Because the LDO supplies the gate drive current, the output of VCCO is subject to sharp transient currents as the drivers switch and the boost capacitors recharge during each switching cycle. The LDO has been optimized to handle these transients without overload faults. Due to the gate drive loading, using the VCCO output for other external auxiliary system loads is not recommended.

The LDO includes a current limit well above the expected maximum gate drive load. This current limit also includes a short-circuit fold back to further limit the VCCO current in the event of a short-circuit fault.

The VDL pin provides power to the low-side driver. Connect VDL to VCCO. Bypass VDL to PGNDx with a 1 µF (minimum) ceramic capacitor, which must be placed close to the VDL pin.

For an input voltage less than 5.5 V, it is recommended to bypass the LDO by connecting VIN to VCCO, as shown in Figure 26, thus eliminating the dropout voltage. However, if the input range is 4 V to 7 V, the LDO cannot be bypassed by shorting VIN to VCCO because the 7 V input has exceeded the maximum voltage rating of the VCCO pin. In this case, use the LDO to drive the internal drivers, but keep in mind that there is a dropout when V_{IN} is less than 5 V.

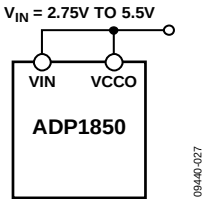


Figure 26. Configuration for V_{IN} < 5.5 V

OVERVOLTAGE PROTECTION

The ADP1850 has a built-in circuit for detecting output overvoltage at the FB node. When the FB voltage, V_{FB}, rises above the overvoltage threshold, the low-side N-channel MOSFET (NMOSFET) is immediately turned on, and the high-side NMOSFET is turned off until the V_{FB} drops below the undervoltage threshold. This action is known as the crowbar overvoltage protection. If the overvoltage condition is not removed, the controller maintains the feedback voltage between the overvoltage and undervoltage thresholds, and the output is regulated to within typically +8% and −8% of the regulation voltage. During an overvoltage event, the SS node discharges toward zero through an internal 3 kΩ pull-down resistor. When the voltage at FBx drops below the undervoltage threshold, the soft start sequence restarts. Figure 27 shows the overvoltage protection scheme in action in PSM.

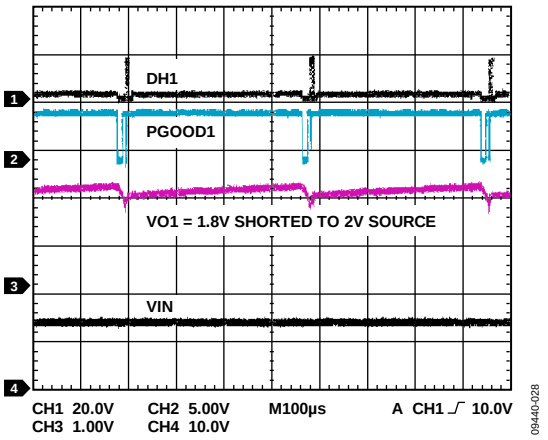


Figure 27. Overvoltage Protection in PSM

POWER GOOD

The PGOODx pin is an open-drain NMOSFET with an internal 12 kΩ pull-up resistor connected between PGOODx and VCCO. PGOODx is internally pulled up to VCCO during normal operation and is active low when tripped. When the feedback voltage, V_{FB}, rises above the overvoltage threshold or drops below the undervoltage threshold, the PGOODx output is pulled to ground after a delay of 12 µs. The overvoltage or undervoltage condition must exist for more than 10 µs for PGOODx to become active. The PGOODx output also becomes active if a thermal overload condition is detected.

SHORT CIRCUIT AND CURRENT LIMIT PROTECTION

When the output is shorted or the output current exceeds the current limit set by the current limit setting resistor (between ILIMx and SWx) for eight consecutive cycles, the ADP1850 shuts off both the high-side and low-side drivers and restarts the soft start sequence every 10 ms, which is known as hiccup mode. The SS node discharges to zero through an internal 1 kΩ resistor during an overcurrent or short-circuit event. Figure 28 shows that the ADP1850 on a high current application circuit is entering current limit hiccup mode when the output is shorted.

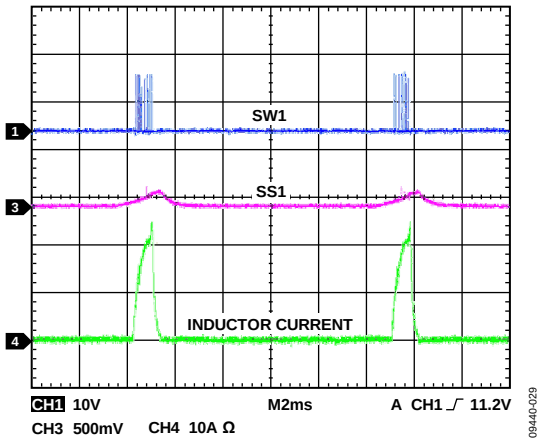


Figure 28. Current Limit Hiccup Mode, 20 A Current Limit

SHUTDOWN CONTROL

The EN1 and EN2 pins are used to enable or disable Channel 1 and Channel 2 of the ADP1850. The precision enable (minimum) threshold for EN1/EN2 is 0.57 V. When the voltage at EN1/EN2 rises above the threshold voltage, the ADP1850 is enabled and starts normal operation after the soft start period. And when the voltage at EN1/EN2 drops typically 30 mV (hysteresis) below the threshold voltage, the switchers and the internal circuits in the ADP1850 are turned off. Note that EN1/EN2 cannot shut down the LDO at VCCO, which is always active.

For the purpose of start-up power sequencing, the startup of the ADP1850 can be programmed by connecting an appropriate resistor divider from the master power supply to the EN1/EN2 pin, as shown in Figure 29. For instance, if the desired start-up voltage from the master power supply is 10 V, R1 and R2 can be set to 156 kΩ and 10 kΩ, respectively.

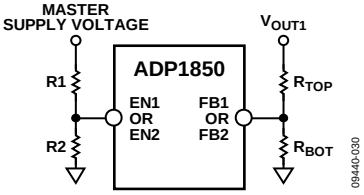


Figure 29. Optional Power-Up Sequencing Circuit

THERMAL OVERLOAD PROTECTION

The ADP1850 has an internal temperature sensor that senses the junction temperature of the chip. When the junction temperature of the ADP1850 reaches approximately 155°C, the ADP1850 goes into thermal shutdown, the converter is turned off, and SS discharges toward zero through an internal 1 kΩ resistor. At the same time, VCCO discharges to zero. When the junction temperature drops below 135°C, the ADP1850 resumes normal operation after the soft start sequence.

APPLICATIONS INFORMATION

SETTING THE OUTPUT VOLTAGE

The output voltage is set using a resistive voltage divider from the output to FB. The voltage divider divides down the output voltage to the 0.6 V FB regulation voltage to set the regulation output voltage. The output voltage can be set to as low as 0.6 V and as high as 90% of the power input voltage.

The maximum input bias current into FB is 100 nA. For a 0.15% degradation in regulation voltage and with 100 nA bias current, the low-side resistor, R_{BOT}, must be less than 9 kΩ, which results in 67 μA of divider current. For R_{BOT}, use a 1 kΩ to 20 kΩ resistor. A larger value resistor can be used but results in a reduction in output voltage accuracy due to the input bias current at the FBx pin, while lower values cause increased quiescent current consumption. Choose R_{TOP} to set the output voltage by using the following equation:

$$R_{TOP} = R_{BOT}\left(\frac{V_{OUT} - V_{FB}}{V_{FB}}\right)$$

where:
R_{TOP} is the high-side voltage divider resistance.
R_{BOT} is the low-side voltage divider resistance.
V_{OUT} is the regulated output voltage.
V_{FB} is the feedback regulation threshold, 0.6 V.

The minimum output voltage is dependent on f_{SW} and minimum DH on time. The maximum output voltage is dependent on f_{SW}, the minimum DH off time, and the IR drop across the high-side NMOSFET and the DCR of the inductor. For example, with f_{SW} of 600 kHz (or 1.67 μs) and a minimum on time of 130 ns, the minimum duty cycle is approximately 7.8% (130 ns/1.67 μs). If V_{IN} is 12 V and the duty cycle is 7.8%, then the lowest output is 0.94 V. As an example for the maximum output voltage, if V_{IN} is 5 V, f_{SW} is 600 kHz, and the minimum DH off time is 395 ns (335 ns DH off time plus approximately 60 ns total dead time), then the maximum duty cycle is 76%. Therefore, the maximum output is approximately 3.8 V. If the IR drop across the high-side NMOSFET and the DCR of the inductor is 0.5 V, then the absolute maximum output is 4.5 V (5 V − 0.5 V), independent of f_{SW} and duty cycle.

SOFT START

The soft start period is set by an external capacitor between SS1/SS2 and AGND. The soft start function limits the input inrush current and prevents output overshoot.

When EN1/EN2 is enabled, a current source of 6.5 μA starts charging the capacitor, and the regulation voltage is reached when the voltage at SS1/SS2 reaches 0.6 V.

The soft start period is approximated by

$$t_{SS} = \frac{0.6\ \text{V}}{6.5\ \mu\text{A}} C_{SS}$$

The SSx pin reaches a final voltage equal to VCCO. If the output voltage is precharged prior to turn-on, the ADP1850 prevents reverse inductor current, which discharges the output capacitor. Once the voltage at SSx exceeds the regulation voltage (typically 0.6 V), the reverse current is reenabled to allow the output voltage regulation to be independent of load current.

Furthermore, in dual-phase operation, where SS1 is shorted to SS2, the current source is doubled to 13 μA during the soft start sequence.

When a controller is disabled, for instance, EN1/EN2 is pulled low or experiences an overcurrent limit condition, the soft start capacitor is discharged through an internal 3 kΩ pull-down resistor.

SETTING THE CURRENT LIMIT

The current limit comparator measures the voltage across the low-side MOSFET to determine the load current.

The current limit is set by an external current limit resistor, R_{ILIM}, between ILIMx and SWx. The current sense pin, ILIMx, sources nominally 50 μA to this external resistor. This creates an offset voltage of R_{ILIM} multiplied by 50 μA. When the drop across the low-side MOSFET, R_{DSON}, is equal to or greater than this offset voltage, the ADP1850 flags a current limit event.

Because the ILIMx current and the MOSFET, R_{DSON}, vary over process and temperature, the minimum current limit should be set to ensure that the system can handle the maximum desired load current. To do this, use the peak current in the inductor, which is the desired output current limit level plus ½ of the ripple current, the maximum R_{DSON} of the MOSFET at its highest expected temperature, and the minimum ILIM current. Keep in mind that the temperature coefficient of the MOSFET, R_{DSON}, is typically 0.4%/°C.

$$R_{ILIM} = \frac{I_{LPK} \times R_{DSON_MAX}}{47\ \mu\text{A}}$$

where:
I_{LPK} is the peak inductor current.

ACCURATE CURRENT LIMIT SENSING

R_{DSON} of the MOSFET can vary by more than 50% over the temperature range. Accurate current limit sensing is achieved by adding a current sense resistor from the source of the low-side MOSFET to PGNDx. Make sure that the power rating of the current sense resistor is adequate for the application. Apply the previous equation and calculate R_{ILIM} by replacing R_{DSON_MAX} with R_{SENSE}. Figure 30 illustrates the implementation of accurate current limit sensing.

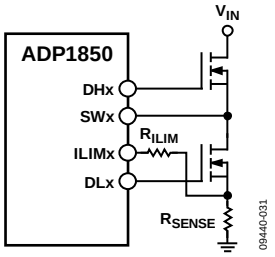


Figure 30. Accurate Current Limit Sensing

SETTING THE SLOPE COMPENSATION

In a current-mode control topology, slope compensation is needed to prevent subharmonic oscillations in the inductor current and to maintain a stable output. The external slope compensation is implemented by summing the amplified sense signal and a scaled voltage at the RAMPx pin. To implement the slope compensation, connect a resistor between RAMPx and the input voltage. The resistor, R_{RAMP}, is calculated by

$$R_{RAMP} = \frac{7 \times 10^9 L}{A_{CS} \times R_{DSON_MAX}}$$

where:
7×10^9 is an internal parameter.
L is the inductance (with units in H) of the inductor.
R_{DSON_MAX} is the low-side MOSFET maximum on resistance.
A_{CS} is the gain, either 3 V/V, 6 V/V, 12 V/V, or 24 V/V, of the current sense amplifier (see the Setting the Current Sense Gain section for more details).

R_{DSON} is temperature dependent and can vary as much as 0.4%/°C. Choose R_{DSON} at the maximum operating temperature. The voltage at RAMPx is fixed at 0.2 V, and the current going into RAMPx should be between 10 µA and 160 µA. Make sure that the following condition is satisfied:

$$10\ \mu A \le \frac{V_{IN} - 0.2\ V}{R_{RAMP}} \le 160\ \mu A$$

For instance, with an input voltage of 12 V, R_{RAMP} should not exceed 1.1 MΩ. If the calculated R_{RAMP} produces less than 10 µA, then select an R_{RAMP} value that produces between 10 µA and 15 µA. Figure 31 illustrates the connection of the slope compensation resistor, R_{RAMP}, and the current sense gain resistor, R_{CSG}.

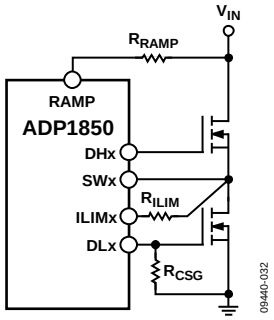


Figure 31. Slope Compensation and CS Gain Connection

SETTING THE CURRENT SENSE GAIN

The voltage drop across the external low-side MOSFET is sensed by a current sense amplifier by multiplying the peak inductor current and the R_{DSON} of the MOSFET. The result is then amplified by a gain factor of either 3 V/V, 6 V/V, 12 V/V, or 24 V/V, which is programmable by an external resistor, R_{CSG}, connected to the DLx pin. This gain is sensed only during power-up and not during normal operation. The amplified voltage is summed with the slope compensation ramp voltage and fed into the PWM controller for a stable regulation voltage.

The voltage range of the internal node, V_{CS}, is between 0.4 V and 2.2 V. Select the current sense gain such that the internal minimum amplified voltage (V_{CSMIN}) is above 0.4 V and the maximum amplified voltage (V_{CSMAX}) is 2.1 V. Note that V_{CSMIN} or V_{CSMAX} is not the same as V_{COMP}, which has a range of 0.85 V to 2.25 V. Make sure that the maximum V_{COMP} ($V_{COMPMAX}$) does not exceed 2.2 V to account for temperature and part-to-part variations. See the following equations for V_{CSMIN}, V_{CSMAX}, and $V_{COMPMAX}$:

$$V_{CSMIN} = 0.75\ V - \frac{1}{2} I_{LPP} \times R_{DSON_MIN} \times A_{CS}$$

$$V_{CSMAX} = 0.75\ V + (I_{LOADMAX} + \frac{1}{2} I_{LPP}) \times R_{DSON_MAX} \times A_{CS}$$

$$V_{COMPMAX} = \frac{(V_{IN} - 0.2\ V) t_{ON}}{100\ pF \times R_{RAMP}} + V_{CSMAX}$$

where:
V_{CSMIN} is the minimum amplified voltage of the internal current sense amplifier at zero output current.
V_{CSMAX} is the maximum amplified voltage of the internal current sense amplifier at maximum output current.
R_{DSON_MIN} is the low-side MOSFET minimum on resistance. The zero-current level voltage of the current sense amplifier is 0.75 V.
I_{LPP} is the peak-to-peak ripple current in the inductor.
$I_{LOADMAX}$ is the maximum output dc load current.
$V_{COMPMAX}$ is the maximum voltage at the COMP pin.
100 pF is an internal parameter.
t_{ON} is the high-side driver (DH) on time.

INPUT CAPACITOR SELECTION

The input current to a buck converter is a pulse waveform. It is zero when the high-side switch is off and approximately equal to the load current when it is on. The input capacitor carries the input ripple current, allowing the input power source to supply only the direct current. The input capacitor needs sufficient ripple current rating to handle the input ripple, as well as an ESR that is low enough to mitigate input voltage ripple. For the usual current ranges for these converters, it is good practice to use two parallel capacitors placed close to the drains of the high-side switch MOSFETs (one bulk capacitor of sufficiently high current rating and a 10 µF ceramic decoupling capacitor, typically).

Select an input bulk capacitor based on its ripple current rating. First, determine the duty cycle of the output.

$$D = \frac{V_{OUT}}{V_{IN}}$$

The input capacitor RMS ripple current is given by

$$I_{RMS} = I_O \sqrt{D(1-D)}$$

where:
I_O is the output current.
D is the duty cycle

The minimum input capacitance required for a particular load is

$$C_{IN,MIN} = \frac{I_O \times D(1-D)}{(V_{PP} - I_O \times DR_{ESR}) f_{SW}}$$

where:
V_{PP} is the desired input ripple voltage.
R_{ESR} is the equivalent series resistance of the capacitor.

If an MLCC capacitor is used, the ESR is near 0, then the equation is simplified to

$$C_{IN,MIN} = I_O \times \frac{D(1-D)}{V_{PP} \times f_{SW}}$$

The capacitance of MLCC is voltage dependent. The actual capacitance of the selected capacitor must be derated according to the manufacturer's specification. In addition, add more bulk capacitance, such as by using electrolytic or polymer capacitors, as necessary for large step load transients. Make sure the current ripple rating of the bulk capacitor exceeds the maximum input current ripple of a particular design.

INPUT FILTER

Normally a 0.1 µF or greater value bypass capacitor from the input pin (VIN) to AGND is sufficient for filtering out any unwanted switching noise. However, depending on the PCB layout, some switching noise can enter the ADP1850 internal circuitry; therefore, it is recommended to have a low pass filter at the VIN pin. Connecting a resistor, between 2 Ω and 5 Ω, in series with VIN and a 1 µF ceramic capacitor between VIN and AGND creates a low pass filter that effectively filters out any unwanted glitches caused by the switching regulator. Keep in mind that the input current could be larger than 100 mA when driving large MOSFETs. A 100 mA across a 5 Ω resistor creates a 0.5 V drop, which is the same voltage drop in VCCO. In this case, a lower resistor value is desirable.

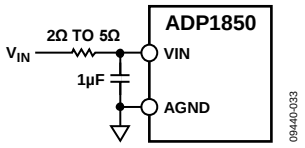


Figure 32. Input Filter Configuration

BOOST CAPACITOR SELECTION

To lower system component count and cost, the ADP1850 has an integrated rectifier (equivalent to the boost diode) between VCCO and BSTx. Choose a boost ceramic capacitor with a value between 0.1 µF and 0.22 µF; this capacitor provides the current for the high-side driver during switching.

INDUCTOR SELECTION

The output LC filter smoothes the switched voltage at SWx. For most applications, choose an inductor value such that the inductor ripple current is between 20% and 40% of the maximum dc output load current. Generally, a larger inductor current ripple generates more power loss in the inductor and larger voltage ripples at the output. Check the inductor data sheet to make sure that the saturation current of the inductor is well above the peak inductor current of a particular design.

Choose the inductor value by the following equation:

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \times \Delta I_L} \times \frac{V_{OUT}}{V_{IN}}$$

where:
L is the inductor value.
f_{SW} is the switching frequency.
V_{OUT} is the output voltage.
V_{IN} is the input voltage.
ΔI_L is the peak-to-peak inductor ripple current.

OUTPUT CAPACITOR SELECTION

Choose the output bulk capacitor to set the desired output voltage ripple. The impedance of the output capacitor at the switching frequency multiplied by the ripple current gives the output voltage ripple. The impedance is made up of the capacitive impedance plus the nonideal parasitic characteristics, the equivalent series resistance (ESR), and the equivalent series inductance (ESL). The output voltage ripple can be approximated by

$$\Delta V_{OUT} \cong \Delta I_L \left(R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}} + 4 f_{SW} \times L_{ESL} \right)$$

where:
ΔV_{OUT} is the output ripple voltage.
ΔI_L is the inductor ripple current.
R_{ESR} is the equivalent series resistance of the output capacitor (or the parallel combination of ESR of all output capacitors).
L_{ESL} is the equivalent series inductance of the output capacitor (or the parallel combination of ESL of all capacitors).

Solving C_{OUT} in the previous equation yields

$$C_{OUT} \cong \frac{\Delta I_L}{8 f_{SW}} \times \frac{1}{\Delta V_{OUT} - \Delta I_L R_{ESR} - 4 \Delta I_L f_{SW} \times L_{ESL}}$$

Usually the capacitor impedance is dominated by ESR. The maximum ESR rating of the capacitor, such as in electrolytic or polymer capacitors, is provided in the manufacturer's data sheet; therefore, output ripple reduces to

$$\Delta V_{OUT} \cong \Delta I_L \times R_{ESR}$$

Electrolytic capacitors also have significant ESL, on the order of 5 nH to 20 nH, depending on type, size, and geometry. PCB traces contribute some ESR and ESL, as well. However, using the maximum ESR rating from the capacitor data sheet usually provides some margin such that measuring the ESL is not usually required.

In the case of output capacitors where the impedance of the ESR and ESL are small at the switching frequency, for instance, where the output capacitor is a bank of parallel MLCC capacitors, the capacitive impedance dominates and the output capacitance equation reduces to

$$C_{OUT} \cong \frac{\Delta I_L}{8 \, \Delta V_{OUT} \times f_{SW}}$$

Make sure that the ripple current rating of the output capacitors is greater than the maximum inductor ripple current.

During a load step transient on the output, for instance, when the load is suddenly increased, the output capacitor supplies the load until the control loop has a chance to ramp the inductor current. This initial output voltage deviation results in a voltage droop or undershoot. The output capacitance, assuming 0 Ω ESR, required to satisfy the voltage droop requirement is approximated by

$$C_{OUT} \cong \frac{\Delta I_{STEP}}{\Delta V_{DROOP} \times f_{SW}}$$

where:
ΔI_{STEP} is the step load.
ΔV_{DROOP} is the voltage droop at the output.

When a load is suddenly removed from the output, the energy stored in the inductor rushes into the capacitor, causing the output to overshoot. The output capacitance required to satisfy the output overshoot requirement can be approximated by

$$C_{OUT} \cong \frac{\Delta I_{STEP}{}^2 L}{(V_{OUT} + \Delta V_{OVERSHOOT})^2 - V_{OUT}{}^2}$$

where:
$\Delta V_{OVERSHOOT}$ is the overshoot voltage during the step load.

Select the largest output capacitance given by any of the previous three equations.

MOSFET SELECTION

The choice of MOSFET directly affects the dc-to-dc converter performance. A MOSFET with low on resistance reduces I^2R losses, and low gate charge reduces transition losses. The MOSFET should have low thermal resistance to ensure that the power dissipated in the MOSFET does not result in excessive MOSFET die temperature.

The high-side MOSFET carries the load current during on time and usually carries most of the transition losses of the converter. Typically, the lower the on resistance of the MOSFET, the higher the gate charge and vice versa. Therefore, it is important to choose a high-side MOSFET that balances the two losses. The conduction loss of the high-side MOSFET is determined by the equation

$$P_C \cong (I_{LOAD})^2 \times R_{DSON} \left(\frac{V_{OUT}}{V_{IN}} \right)$$

where:
R_{DSON} is the MOSFET on resistance.

The gate charging loss is approximated by the equation

$$P_G \cong V_{PV} \times Q_G \times f_{SW}$$

where:
V_{PV} is the gate driver supply voltage.
Q_G is the MOSFET total gate charge.

Note that the gate charging power loss is not dissipated in the MOSFET but rather in the ADP1850 internal drivers. This power loss should be taken into consideration when calculating the overall power efficiency.

The high-side MOSFET transition loss is approximated by the equation

$$P_T \cong \frac{V_{IN} \times I_{LOAD} \times (t_R + t_F) \times f_{SW}}{2}$$

where:
P_T is the high-side MOSFET switching loss power.
t_R is the rise time in charging the high-side MOSFET.
t_F is the fall time in discharging the high-side MOSFET.

t_R and t_F can be estimated by

$$t_R \cong \frac{Q_{GSW}}{I_{DRIVER_RISE}}$$

$$t_F \cong \frac{Q_{GSW}}{I_{DRIVER_FALL}}$$

where:
Q_{GSW} is the gate charge of the MOSFET during switching and is given in the MOSFET data sheet.
I_{DRIVER_RISE} and I_{DRIVER_FALL} are the driver current put out by the ADP1850 internal gate drivers.

If Q_{GSW} is not given in the data sheet, it can be approximated by

$$Q_{GSW} \cong Q_{GD} + \frac{Q_{GS}}{2}$$

where:
Q_{GD} and Q_{GS} are the gate-to-drain and gate-to-source charges given in the MOSFET data sheet.

I_{DRIVER_RISE} and I_{DRIVER_FALL} can be estimated by

$$I_{DRIVER_RISE} \cong \frac{V_{DD} - V_{SP}}{R_{ON_SOURCE} + R_{GATE}}$$

$$I_{DRIVER_FALL} \cong \frac{V_{SP}}{R_{ON_SINK} + R_{GATE}}$$

where:
V_{DD} is the input supply voltage to the driver and is between 2.75 V and 5 V, depending on the input voltage.
V_{SP} is the switching point where the MOSFET fully conducts; this voltage can be estimated by inspecting the gate charge graph given in the MOSFET data sheet.
R_{ON_SOURCE} is the on resistance of the ADP1850 internal driver, given in Table 1 when charging the MOSFET.
R_{ON_SINK} is the on resistance of the ADP1850 internal driver, given in Table 1 when discharging the MOSFET.
R_{GATE} is the on gate resistance of MOSFET given in the MOSFET data sheet. If an external gate resistor is added, add this external resistance to R_{GATE}.

The total power dissipation of the high-side MOSFET is the sum of conduction and transition losses:

$$P_{HS} \cong P_C + P_T$$

The synchronous rectifier, or low-side MOSFET, carries the inductor current when the high-side MOSFET is off. The low-side MOSFET transition loss is small and can be neglected in the calculation. For high input voltage and low output voltage, the low-side MOSFET carries the current most of the time. Therefore, to achieve high efficiency, it is critical to optimize the low-side MOSFET for low on resistance. In cases where the power loss exceeds the MOSFET rating or lower resistance is required than is available in a single MOSFET, connect multiple low-side MOSFETs in parallel. The equation for low-side MOSFET conduction power loss is

$$P_{CLS} \cong (I_{LOAD})^2 \times R_{DSON}\left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

There is also additional power loss during the time, known as dead time, between the turn-off of the high-side switch and the turn-on of the low-side switch, when the body diode of the low-side MOSFET conducts the output current. The power loss in the body diode is given by

$$P_{BODYDIODE} = V_F \times t_D \times f_{SW} \times I_O$$

where:
V_F is the forward voltage drop of the body diode, typically 0.7 V.
t_D is the dead time in the ADP1850, typically 30 ns when driving some medium-size MOSFETs with input capacitance, C_{iss}, of approximately 3 nF. The dead time is not fixed. Its effective value varies with gate drive resistance and C_{iss}, so $P_{BODYDIODE}$ increases in high load current designs and low voltage designs.

Then the power loss in the low-side MOSFET is

$$P_{LS} = P_{CLS} + P_{BODYDIODE}$$

Note that MOSFET, R_{DSON}, increases with increasing temperature with a typical temperature coefficient of 0.4%/°C. The MOSFET junction temperature (T_J) rise over the ambient temperature is

$$T_J = T_A + \theta_{JA} \times P_D$$

where:
θ_{JA} is the thermal resistance of the MOSFET package.
T_A is the ambient temperature.
P_D is the total power dissipated in the MOSFET.

LOOP COMPENSATION (SINGLE PHASE OPERATION)

As with most current mode step-down controller, a transconductance error amplifier is used to stabilize the external voltage loop. Compensating the ADP1850 is fairly easy; an RC compensator is needed between COMPx and AGND. Figure 33 shows the configuration of the compensation components: R_{COMP}, C_{COMP}, and C_{C2}. Because C_{C2} is very small compared to C_{COMP}, to simplify calculation, C_{C2} is ignored for the stability compensation analysis.

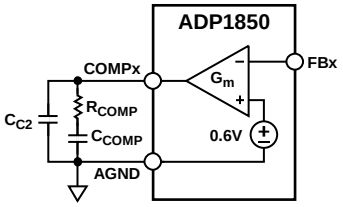


Figure 33. Compensation Components

The open loop gain transfer function at angular frequency, s, is given by

$$H(s) = G_m \times G_{CS} \times \frac{V_{REF}}{V_{OUT}} \times Z_{COMP}(s) \times Z_{FILTER}(s) \quad (1)$$

where:
G_m is the transconductance of the error amplifier, 500 µS.
G_{CS} is the tranconductance of the power stage.
Z_{COMP} is the impedance of the compensation network.
Z_{FILTER} is the impedance of the output filter.
V_{REF} = 0.6 V.

G_{CS} with units of A/V is given by

$$G_{CS} = \frac{1}{A_{CS} \times R_{DSON_MIN}} \quad (2)$$

where:
A_{CS} is the current sense gain of either 3 V/V, 6 V/V, 12 V/V, or 24 V/V set by the gain resistor between DLx and PGNDx.
R_{DSON_MIN} is the low-side MOSFET minimum on resistance.

If a sense resistor, R_S, is added in series with the low-side FET, then G_{CS} becomes

$$G_{CS} = \frac{1}{A_{CS} \times (R_{DSON_MIN} + R_S)}$$

Because the zero produced by the ESR of the output capacitor is not needed to stabilize the control loop, assuming ESR is small the ESR is ignored for analysis. Then Z_{FILTER} is given by

$$Z_{FILTER} = \frac{1}{sC_{OUT}} \quad (3)$$

Because C_{C2} is small relative to C_{COMP}, Z_{COMP} can be simplified to

$$Z_{COMP} = R_{COMP} + \frac{1}{sC_{COMP}} = \frac{1 + sR_{COMP} \times C_{COMP}}{sC_{COMP}} \quad (4)$$

At the crossover frequency, the open-loop transfer function is unity or 0 dB, H (f_{CROSS}) = 1. Combining Equation 1 and Equation 3, Z_{COMP} at the crossover frequency can be written as

$$Z_{COMP}(f_{CROSS}) = \left(\frac{2\pi \times f_{CROSS}}{G_m \times G_{CS}}\right)\left(\frac{C_{OUT} \times V_{OUT}}{V_{REF}}\right) \quad (5)$$

The zero produced by R_{COMP} and C_{COMP} is

$$f_{ZERO} = \frac{1}{2\pi R_{COMP} \times C_{COMP}} \quad (6)$$

At the crossover frequency, Equation 4 can be shown as

$$Z_{COMP}(f_{CROSS}) = R_{COMP} \times \frac{\sqrt{{f_{CROSS}}^2 + {f_{ZERO}}^2}}{f_{CROSS}} \quad (7)$$

Combining Equations 5 and Equation 7 and solving for R_{COMP} gives

$$R_{COMP} = \frac{f_{CROSS}}{\sqrt{{f_{CROSS}}^2 + {f_{ZERO}}^2}} \times \left(\frac{2\pi \times f_{CROSS}}{G_m \times G_{CS}}\right) \times \left(\frac{C_{OUT} \times V_{OUT}}{V_{REF}}\right) \quad (8)$$

Choose the crossover and zero frequencies as follows:

$$f_{CROSS} = \frac{f_{SW}}{12} \quad (9)$$

$$f_{ZERO} = \frac{f_{CROSS}}{4} = \frac{f_{SW}}{48} \quad (10)$$

Substituting Equation 2, Equation 9, and Equation 10 into Equation 8 yields

$$R_{COMP} = 0.97 \times A_{CS} \times R_{DSON}\left(\frac{2\pi \times f_{CROSS}}{G_m}\right) \times \left(\frac{C_{OUT} \times V_{OUT}}{V_{REF}}\right) \quad (11)$$

where:
G_m is the transconductance of the error amplifier, 500 µS.
A_{CS} is the current sense gain of 3 V/V, 6 V/V, 12 V/V, or 24 V/V.
R_{DSON} is on resistance of the low-side MOSFET.
V_{REF} = 0.6 V.

And combining Equation 6 and Equation 10 yields

$$C_{COMP} = \frac{2}{\pi R_{COMP} \times f_{CROSS}} \quad (12)$$

Note that the previous simplified compensation equations for R_{COMP} and C_{COMP} yield reasonable results in f_{CROSS} and phase margin assuming that the compensation ramp current is ideal. Varying the ramp current or deviating the ramp current from ideal can affect f_{CROSS} and phase margin.

And lastly, set C_{C2} to

$$\frac{1}{20} \times C_{COMP} \le C_{C2} \le \frac{1}{10} \times C_{COMP} \quad (13)$$

CONFIGURATION AND LOOP COMPENSATION (DUAL-PHASE OPERATION)

In dual-phase operation, the two outputs of the switching regulators are shorted together and can source more than 50 A of output current depending on the selection of the power components. Internal parameters in the ADP1850 are optimized and trimmed in the factory to minimize the mismatch in output currents between the two channels. See Figure 34 and Figure 47 for a configuration of a typical dual-phase application circuit. Note that FB1 shorts to FB2, SS1 to SS2, and COMP1 to COMP2, where the outputs of the two error amplifiers are shared. Furthermore, the controller needs to be placed in forced PWM operation by connecting SYNC to VCCO or logic high.

The equations for calculating the loop compensation components are identical to the single-phase operation, but the combined value of G_m of the error amplifiers, the modulator gain and the effective f_{SW} are all doubled.

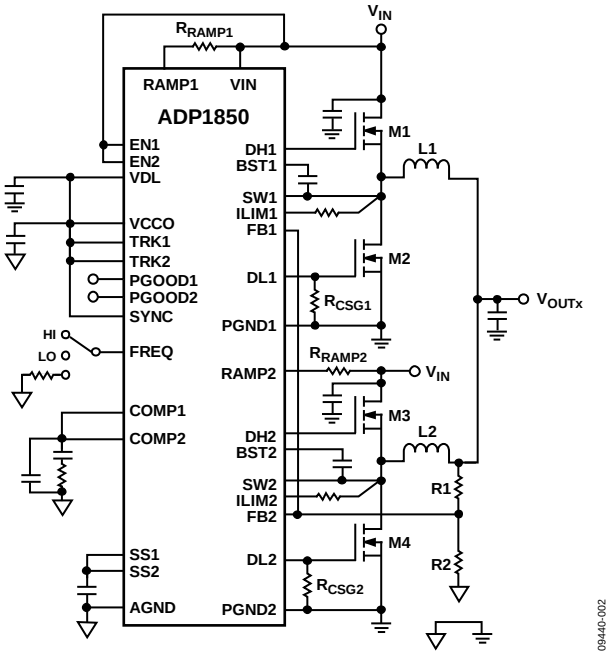


Figure 34. Dual-Phase Circuit

SWITCHING NOISE AND OVERSHOOT REDUCTION

In any high speed step-down regulator, high frequency noise (generally in the range of 50 MHz to 100 MHz) and voltage overshoot are always present at the gate, the switch node (SW), and the drains of the external MOSFETs. The high frequency noise and overshoot are caused by the parasitic capacitance, C_{GD}, of the external MOSFET and the parasitic inductance of the gate trace and the packages of the MOSFETs. When the high current is switched, electromagnetic interference (EMI) is generated, which can affect the operation of the surrounding circuits. To reduce voltage ringing and noise, it is recommended to add an RC snubber between SWx and PGNDx for high current applications, as illustrated in Figure 35.

In most applications, R_{SNUB} is typically 2 Ω to 4 Ω, and C_{SNUB} typically 1.2 nF to 3 nF.

R_{SNUB} can be estimated by

$$R_{SNUB} \cong 2\sqrt{\frac{L_{MOSFET}}{C_{OSS}}}$$

And C_{SNUB} can be estimated by

$$C_{SNUB} \cong C_{OSS}$$

where:
L_{MOSFET} is the total parasitic inductance of the high-side and low-side MOSFETs, typically 3 nH, and is package dependent.
C_{OSS} is the total output capacitance of the high-side and low-side MOSFETs given in the MOSFET data sheet.

The size of the RC snubber components needs to be chosen correctly to handle the power dissipation. The power dissipated in R_{SNUB} is

$$P_{SNUB} = V_{IN}^2 \times C_{SNUB} \times f_{SW}$$

In most applications, a component size 0805 for R_{SNUB} is sufficient. However, the use of an RC snubber reduces the overall efficiency, generally by an amount in the range of 0.1% to 0.5%. The RC snubber does not reduce the voltage overshoot. A resistor, shown as R_{RISE} in Figure 35, at the BSTx pin helps to reduce overshoot and is generally between 2 Ω and 4 Ω. Adding a resistor in series, typically between 2 Ω and 4 Ω, with the gate driver also helps to reduce overshoot. If a gate resistor is added, then R_{RISE} is not needed.

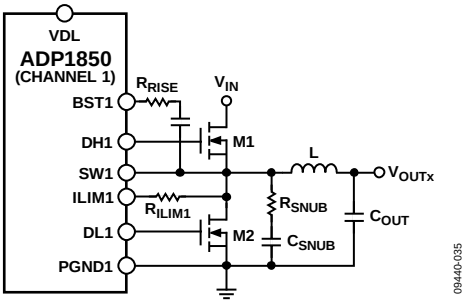


Figure 35. Application Circuit with a Snubber

VOLTAGE TRACKING

The ADP1850 includes a tracking feature that tracks a master voltage. This feature is especially important when the ADP1850 is providing separate power supply voltages to a single integrated circuit, such as the core and I/O voltages of a DSP, FPGA, or microcontroller. In these cases, improper sequencing can cause damage to the load IC.

In all tracking configurations, the output can be set as low as 0.6 V for a given operating condition. The soft start time setting of the master voltage should be longer than the soft start of the slave voltage. This forces the rise time of the master voltage to be imposed on the slave voltage. If the soft start setting of the slave voltage is longer, the slave comes up more slowly, and the tracking relationship is not seen at the output.

Two tracking configurations are possible with the ADP1850: coincident and ratiometric trackings.

Coincident Tracking

The most common application is coincident tracking, used in core vs. I/O voltage sequencing and similar applications. Coincident tracking forces the slave output voltage's ramp rate to be the same as the master's until the slave output reaches its regulation. Connect the slave TRKx input to a resistor divider from the master voltage that is the same as the divider used on the slave FBx pin. This forces the slave voltage to be the same as the master voltage. For coincident tracking, use $R_{TRKT} = R_{TOP}$ and $R_{TRKB} = R_{BOT}$, as shown in Figure 37.

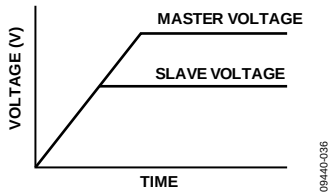


Figure 36. Coincident Tracking

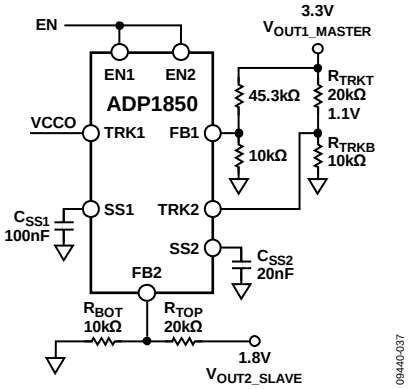


Figure 37. Example of a Coincident Tracking Circuit

The ratio of the slave output voltage to the master voltage is a function of the two dividers.

$$\frac{V_{OUT_SLAVE}}{V_{OUT_MASTER}} = \frac{\left(1+\frac{R_{TOP}}{R_{BOT}}\right)}{\left(1+\frac{R_{TRKT}}{R_{TRKB}}\right)}$$

As the master voltage rises, the slave voltage rises identically. Eventually, the slave voltage reaches its regulation voltage, where the internal reference takes over the regulation while the TRKx input continues to increase and thus removes itself from influencing the output voltage.

To ensure that the output voltage accuracy is not compromised by the TRKx pin being too close in voltage to the reference voltage (V_{FB}, typically 0.6 V), make sure that the final value of the TRKx voltage of the slave channel is at least 30 mV above V_{FB}.

Ratiometric Tracking

Ratiometric tracking limits the output voltage to a fraction of the master voltage, as illustrated in Figure 38 and Figure 39. The final TRKx voltage of the slave channel should be set to at least 30 mV below the FB voltage of the master channel. When the TRKx voltage of the slave channel drops to a level that's below the minimum on-time condition, the slave channel operates in pulse skip mode while keeping the output regulated and tracked to the master channel. Also, when TRKx or FBx drops below the PGOOD undervoltage threshold, the PGOOD signal gets tripped and becomes active low.

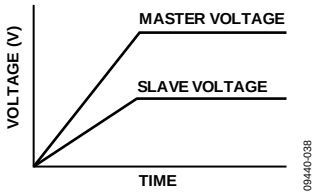


Figure 38. Ratiometric Tracking

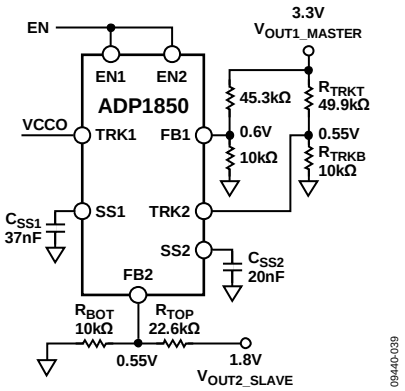


Figure 39. Example of a Ratiometric Tracking Circuit

Another ratiometric tracking configuration is having the slave channel rise more quickly than the master channel, as shown in Figure 40 and Figure 41. The tracking circuits in Figure 39 and Figure 41 are virtually identical with the exception that $R_{TRKB} > R_{TRKT}$ as shown in Figure 41.

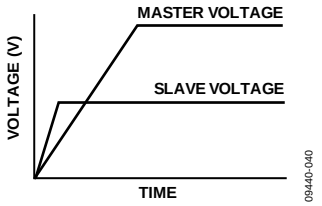


Figure 40. Ratiometric Tracking (Slave Channel Has a Faster Ramp Rate)

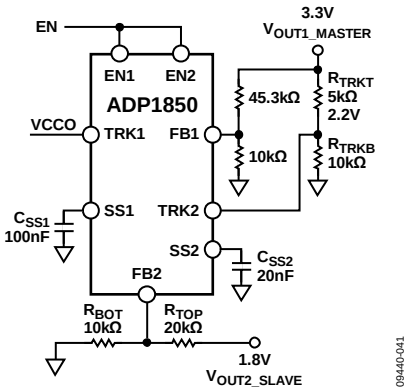


Figure 41. Example of a Ratiometric Tracking Circuit (Slave Channel Has a Faster Ramp Rate)

INDEPDENDENT POWER STAGE INPUT VOLTAGE

In addition to the single power supply configuration, the power stage input voltage of the dc-to-dc converter can come from a different voltage supply, as illustrated in Figure 42. The range of the power stage input voltage (V_{PIN}) is 1 V to 20 V. For instance, the bias input voltage (V_{IN}) is 5 V, V_{PIN} can be as low as 1 V or as high as 20 V. The user needs to make sure that the minimum or the maximum duty cycle is not violated in this operating condition. Furthermore, note that R_{RAMP} is connected to V_{PIN}.

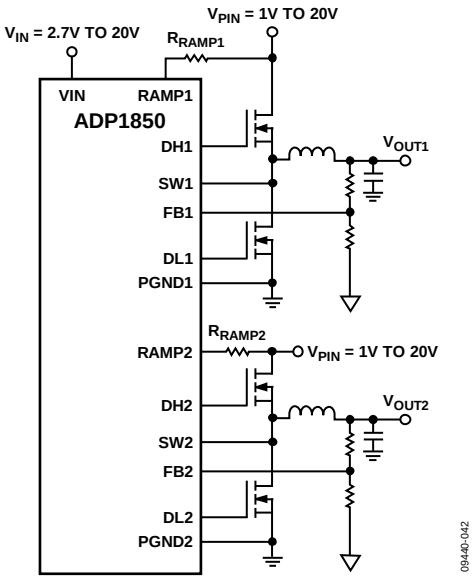


Figure 42. Independent Power Stage Input Voltage (Simplified Schematic)

PCB LAYOUT GUIDELINES

In any switching converter, there are some circuit paths that carry high dI/dt, which can create spikes and noise. Some circuit paths are sensitive to noise, while other circuits carry high dc current and can produce significant IR voltage drops. The key to proper PCB layout of a switching converter is to identify these critical paths and arrange the components and the copper area accordingly. When designing PCB layouts, be sure to keep high current loops small. In addition, keep compensation and feedback components away from the switch nodes and their associated components.

The following is a list of recommended layout practices for the synchronous buck controller, arranged by decreasing order of importance.

MOSFETS, INPUT BULK CAPACITOR, AND BYPASS CAPACITOR

The current waveform in the top and bottom FETs is a pulse with very high dI/dt; therefore, the path to, through, and from each individual FET should be as short as possible, and the two paths should be commoned as much as possible. In designs that use a pair of D-Pak, or a pair of SO-8 FETs, on one side of the PCB, it is best to counter-rotate the two so that the switch node is on one side of the pair. This allows the high-side FET's drain to be bypassed to the low-side FET's source with a suitable ceramic bypass capacitor placed as close as possible to the FETs. Close proximity of the bypass capacitor minimizes the inductance around the loop through the FETs and capacitor. The recommended bypass ceramic capacitor values range from 1 μF to 22 μF, depending on the output current. The ceramic bypass capacitor is usually connected to a larger value bulk filter capacitor and should be grounded to the PGNDx plane.

HIGH CURRENT AND CURRENT SENSE PATHS

Part of the ADP1850 architecture is sensing the current across the low-side FET between the SWx and PGNDx pins. The switching GND currents of one channel creates noise and can be picked up by the other channel. It is essential to have Kelvin sensing connection between SWx and the drain of the respective low-side MOSFET, and between PGNDx and the source of the respective low-side MOSFET, as illustrated in Figure 43. Place these Kelvin connections very close to the FETs to achieve accurate current sensing. Figure 43 illustrates the proper connection technique for the SW1/SW2, PGND1/PGND2, and PGND plane.

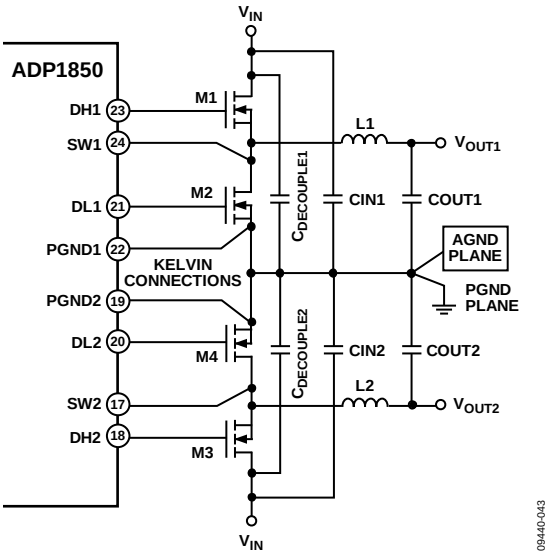


Figure 43. Grounding Technique for Two Channels

SIGNAL PATHS

The negative terminals of VIN bypass, compensation components, soft start capacitor, and the bottom end of the output feedback divider resistors should be tied to a small AGND plane. These connections should attach from their respective pins to the AGND plane and should be as short as possible. No high current or high dI/dt signals should be connected to this AGND plane. The AGND area should be connected through one wide trace to the negative terminal of the output filter capacitors.

PGND PLANE

The PGNDx pin handles a high dI/dt gate drive current returning from the source of the low side MOSFET. The voltage at this pin also establishes the 0 V reference for the overcurrent limit protection function and the ILIMx pin. A PGND plane should connect the PGNDx pin and the VDL bypass capacitor, 1 μF, through a wide and direct path to the source of the low side MOSFET. The placement of CIN is critical for controlling ground bounce. The negative terminal of CIN must be placed very close to the source of the low-side MOSFET.

FEEDBACK AND CURRENT LIMIT SENSE PATHS

Avoid long traces or large copper areas at the FBx and ILIMx pins, which are low-level signal inputs that are sensitive to capacitive and inductive noise pickup. It is best to position any series resistors and capacitors as close as possible to these pins. Avoid running these traces close and/or parallel to high dI/dt traces.

SWITCH NODE

The switch node is the noisiest place in the switcher circuit with large ac and dc voltages and currents. This node should be wide to minimize resistive voltage drop. To minimize capacitively coupled noise, the total area should be small. Place the FETs and inductor close together on a small copper plane to minimize series resistance and keep the copper area small.

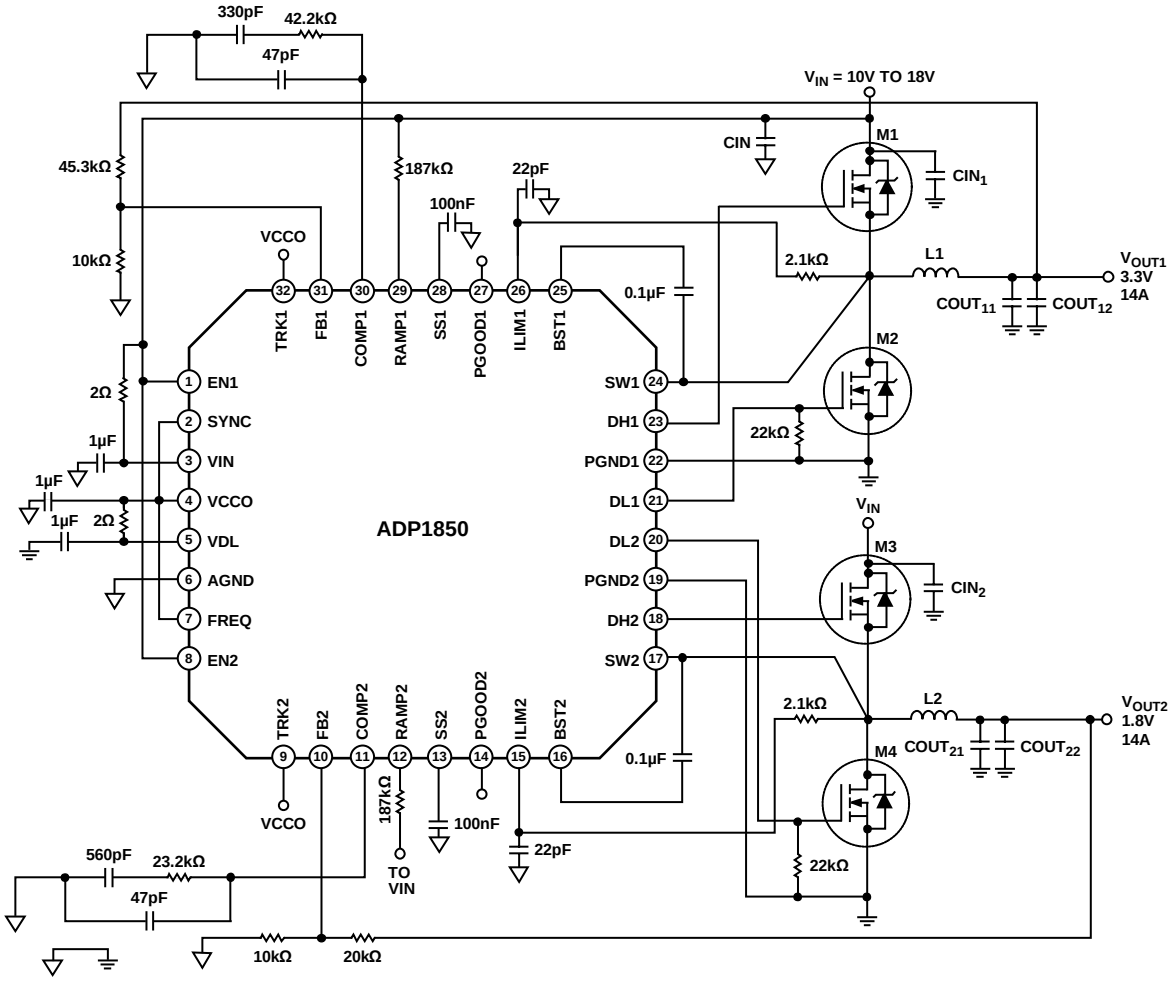
GATE DRIVER PATHS

Gate drive traces (DH and DL) handle high dI/dt and tend to produce noise and ringing. They should be as short and direct as possible. If vias are needed, it is best to use two relatively large ones in parallel to reduce the peak current density and the current in each via. If the overall PCB layout is less than optimal, slowing down the gate drive slightly can be helpful to reduce noise and ringing. It is occasionally helpful to place small value resistors, such as between 2 Ω and 4 Ω, on the DHx and DLx pins. These can be populated with 0 Ω resistors if resistance is not needed. Note that the added gate resistance increases the switching rise and fall times, as well as increasing switching power loss in the MOSFET.

OUTPUT CAPACITORS

The negative terminal of the output filter capacitors should be tied close to the source of the low side FET. Doing this helps to minimize voltage differences between AGND and PGNDx.

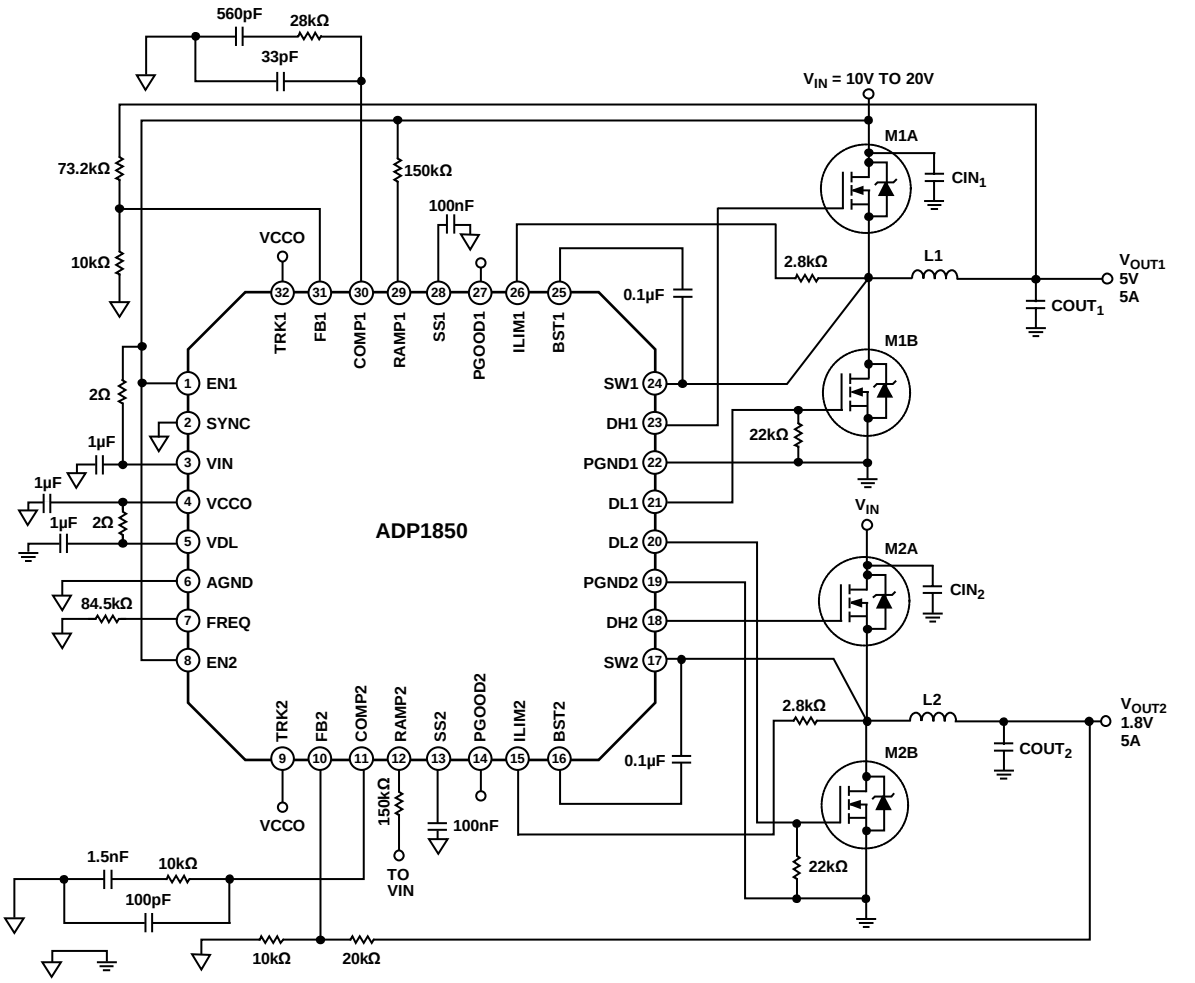
TYPICAL OPERATING CIRCUITS



f_{SW} = 600kHz
CIN: 150µF/20V, OS-CON, 20SEP150M, SANYO
L1, L2: 1.2µH, WURTH ELEKTRONIK, 744325120
M1, M3: BSC080N03LS
M2, M4: BSC030N03LS

CIN_1, CIN_2: 10µF/X7R/25V/1210 × 2, GRM32DR71E106KA12, MURATA
$COUT_{11}$, $COUT_{21}$: 330µF/6.3V/POSCAP × 2, 6TPF330M9L, SANYO
$COUT_{12}$, $COUT_{22}$: 22µF/X5R/0805/6.3V × 3, GRM21BR60J226ME39, MURATA

Figure 44. Typical 14 A Operating Circuit

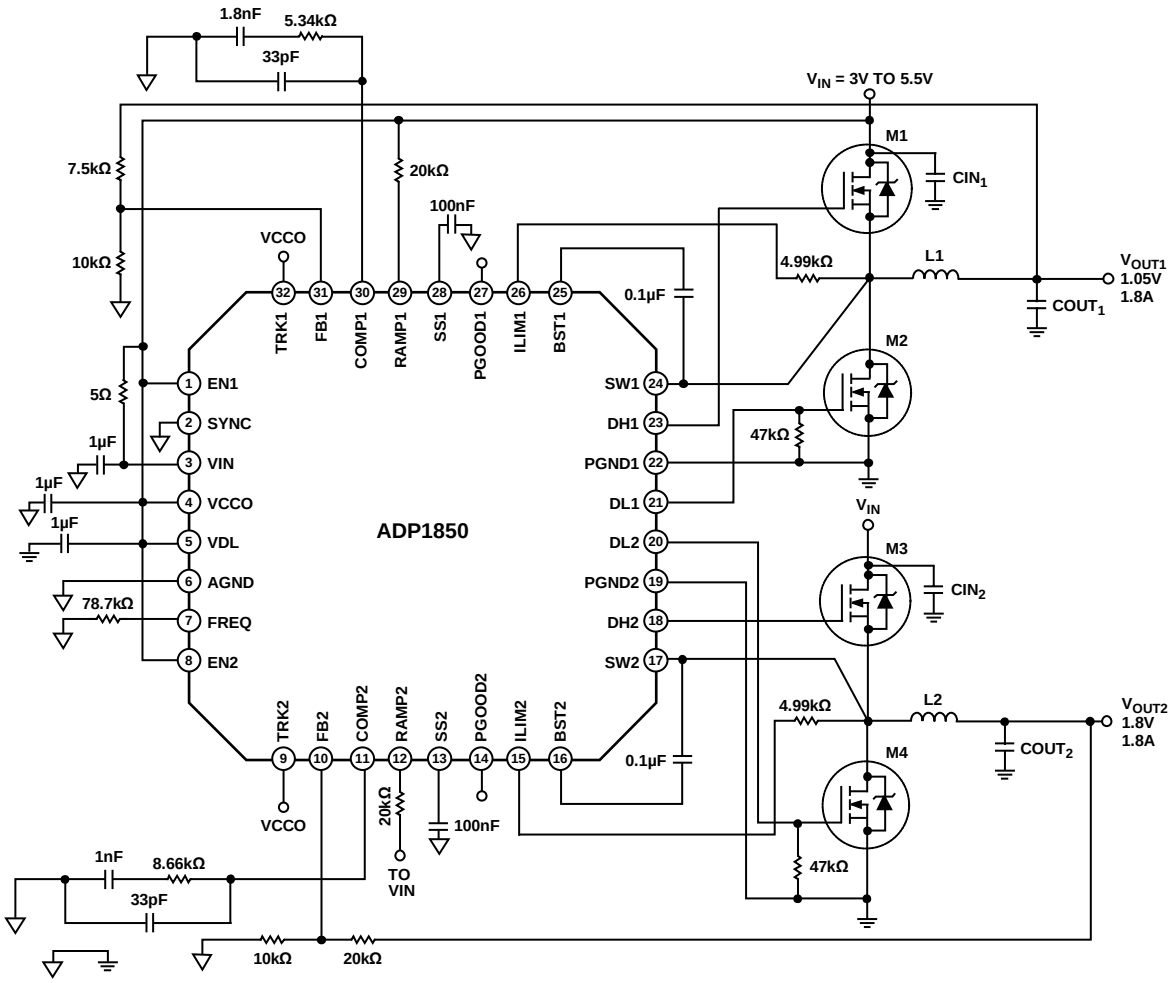


f_{SW} = 750kHz, PULSE SKIP MODE
L1: 2µH, WURTH ELEKTRONIK, 744310200
L2: 1.15µH, WURTH ELEKTRONIK, 744310115

CIN_1, CIN_2: 10µF/X5R/16V/1206 × 2, GRM31CR61C106KA88, MURATA
M1, M2: SI944DY OR BSON03MD
$COUT_1$, $COUT_2$: 22µF/XR5/1210/6.3V × 3, GRM32DR60J226KA01, MURATA

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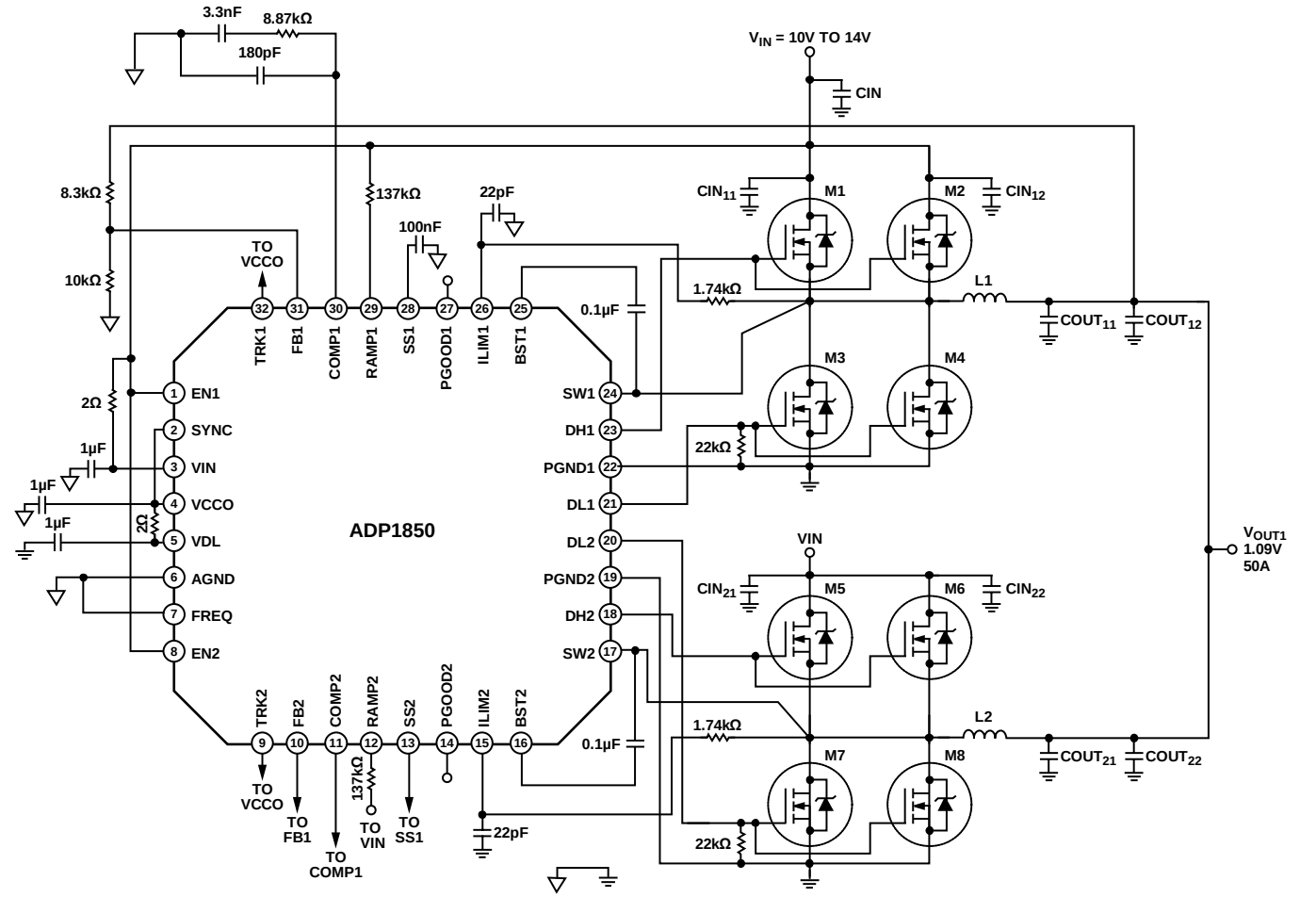
Figure 45. Typical Low Current Operating Circuit



f_{SW} = 800kHz, PULSE SKIP MODE
L1, L2: 1µH, TOKO D62LCB1R0M
M1, M2, M3, M4: SI2302ADS, SOT23

CIN_1, CIN_2: 4.7µF/X5R/16V/0805 × 2, GRM219R60J475KE19, MURATA
$COUT_1$, $COUT_2$: 22µF/XR5/0805/6.3V, GRM21BR60J226ME39, MURATA

Figure 46. Typical Low Current Application with V_{IN} < 5.5 V



f_{SW} = 300kHz
CIN = 180µF/16V × 4, 16SEP180M, OS-CON, SANYO
M1, M2, M5, M6: BSC080N03IS
M3, M4, M7, M8: BSC030N03LS
L1, L2: SER1408-301, 300nH, COILCRAFT; OR 744355147, 0.4µH, WURTH ELECTRONIK

CIN_{11}, CIN_{12}, CIN_{21}, CIN_{22}: 10µF/X7R/25V/1210, MURATA
$COUT_{11}$, $COUT_{21}$, 2SEPC560MZ × 3, 560µF, OSCON, SANYO
$COUT_{12}$, $COUT_{22}$: GRM31CR60J476ME19 × 2, 47µV/1206/6.3V, MURATA

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Figure 47. Dual-Phase Circuit, 50 A Output

OUTLINE DIMENSIONS

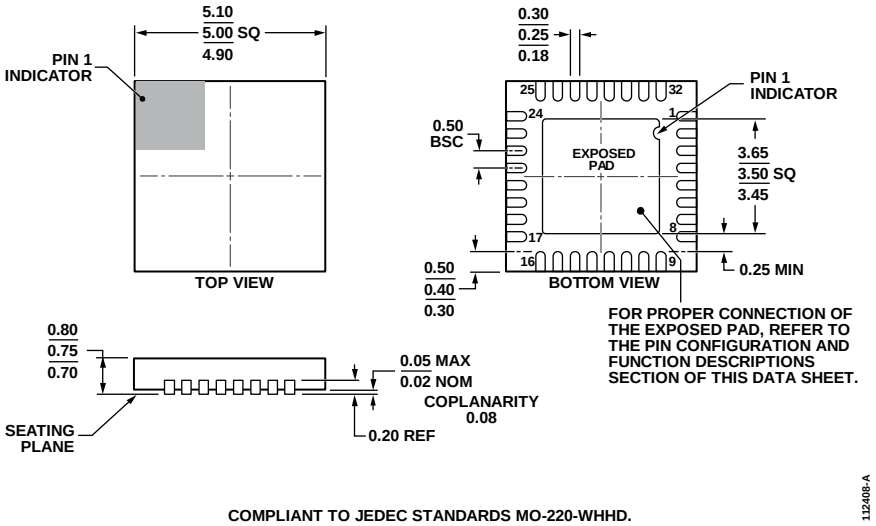


Figure 48. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP1850ACPZ-R7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-11
ADP1850SP-EVALZ		Evaluation Board in Single-Phase Mode with 14 A Output	
ADP1850DP-EVALZ		Evaluation Board in Dual-Phase Mode with 50 A Output	

[1] Z = RoHS Compliant Part.

NOTES

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