PRELIMINARY

ML2731 PA Bias Controller

GENERAL DESCRIPTION

The ML2731 is a power amplifier (PA) bias controller with support circuits for a typical radio transceiver. The IC integrates a PA bias controller, a PA DC switch, a crystal oscillator circuit, a negative voltage generator and two voltage regulators. It can be used with GaAs FETs and silicon bipolar devices.

Micro Linear's ML2731, along with the ML2712 and the ML2713, form a complete transceiver solution for the 2.4 GHz IEEE802.11 communication standard, as well as other wireless ISM communication products.

In addition to supporting Micro Linear's transceiver chip set, the ML2731 can stand alone as:

A compact bias voltage controller

A compact negative voltage generator

A compact crystal oscillator

FEATURES

- Sets PA current and power output using a bias control loop
- Integrates a PA DC supply switch
- Prevents PA power-on if negative voltage is not present
- Integrates all circuits needed for supporting a crystal oscillator with 10MHz to 40MHz frequency range
- Incorporates a fast starting, high switching frequency, negative voltage generator requiring only small ceramic capacitors
- Contains voltage regulators for an oscillator, a negative voltage generator and a 50mA 3.0V LDO output
- Requires less than 1mA of current when powered down
- Supply voltage ranges from 3.3V to 5.5V

APPLICATIONS

- Cellular and Cordless Radios
- WLAN Radios
- Radios with GaAs FET Power Amplifiers
- Fixed and Mobile radio transceivers

SIMPLIFIED BLOCK DIAGRAM

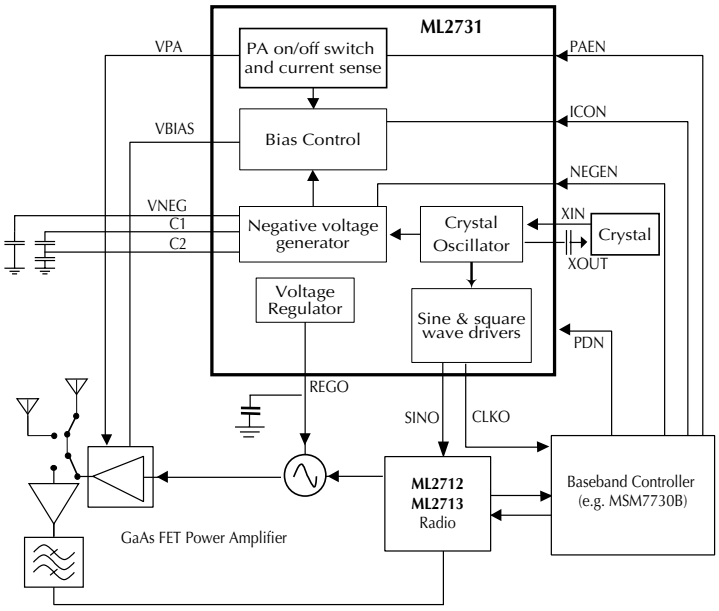


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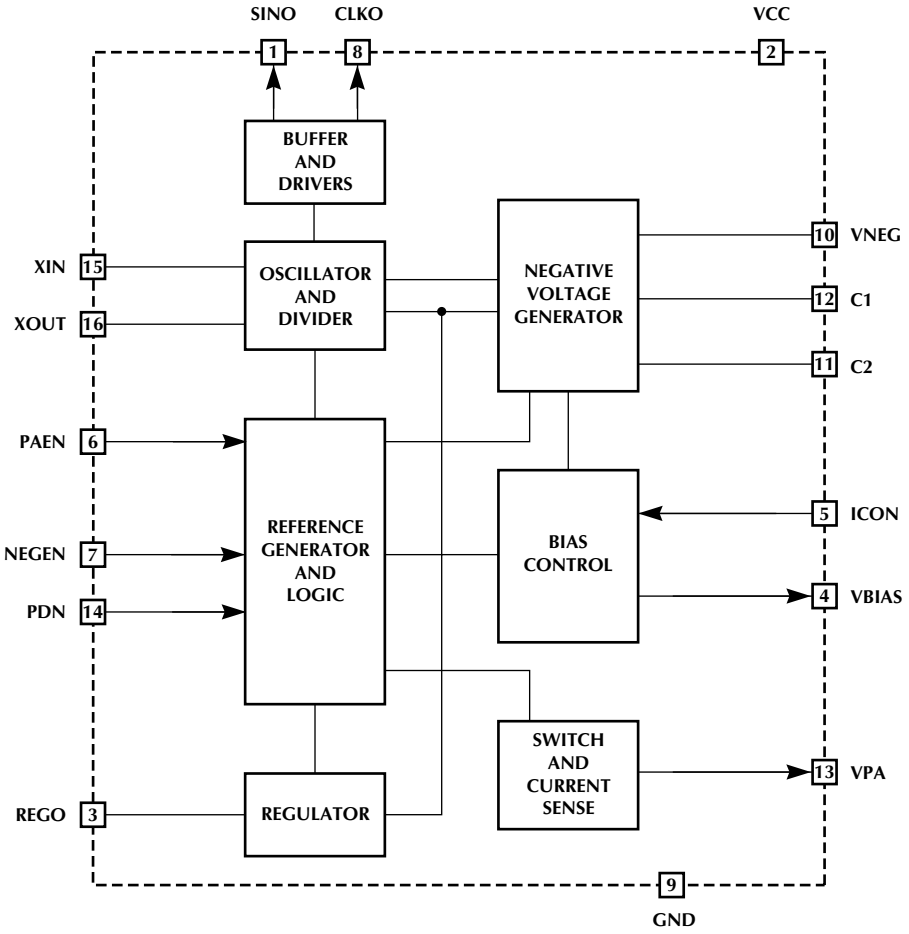
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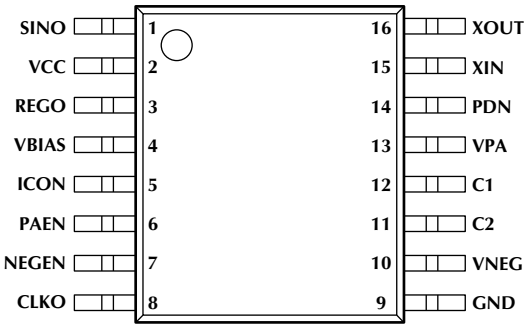
Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; 5,652,479; 5,661,427; 5,663,874; 5,672,959; 5,689,167; 5,714,897; 5,717,798; 5,742,151; 5,747,977; 5,754,012; 5,757,174; 5,767,653; 5,777,514; 5,793,168; 5,798,635; 5,804,950; 5,808,455; 5,811,999; 5,818,207; 5,818,669; 5,825,165; 5,825,223; 5,838,723; 5.844,378; 5,844,941. Japan: 2,598,946; 2,619,299; 2,704,176; 2,821,714. Other patents are pending.

BLOCK DIAGRAM



PIN CONFIGURATION

ML2731
16-Pin TSSOP (T16)



TOP VIEW

PIN DESCRIPTIONS

Pin #	Signal Name	I/O	Description
1	SINO	O (ANLG)	Sine wave output. This pin is a low impedance output capable of driving a 2kΩ load. The signal is sourced with either a crystal interfaced with on-chip components through XOIN (pin 15) and XOUT (pin 16) or with a completely external oscillator through pin 15. Taking PDN (pin 14) high switches off output
2	VCC	O (ANLG)	DC power supply
3	REGO	O (ANLG)	IC regulator output. This is the output from the on IC regulator. It is disabled in the SLEEP mode of operation and enabled in all other modes. The nominal output voltage is 2.9 V and it has a low impedance output which can source up to 50mA
4	VBIAS	O (ANLG)	PA bias voltage output. This output has limited drive capability of 3mA and is intended to drive the gate or bias of the PA
5	ICON	I (ANLG)	Reference current input. Used by the PA bias control loop to set the PA current level. This input appears as a virtual ground
6	PAEN	I (CMOS)	PA Enable. Transitions from high to low on this pin activate the PA current ramp up function, switch the PA voltage supply switch on and enable the PA bias control loop. Transitions from low to high activate the PA current ramp down function and switch the PA voltage supply off
7	NEGEN	I (CMOS)	Negative Voltage Enable. In conjunction with PDN and PAEN, NEGEN controls the operational mode of the IC and enables the negative voltage generator circuits
8	CLKO	I (CMOS)	Clock output. The frequency is set with either a crystal interfaced with on-chip components through XOIN (pin 15) and XOUT (pin 16) or with a completely external oscillator through pin 15. CLKO switches off when device goes into SLEEP mode when PDN is taken high
9	GND	GND	Ground
10	VNEG	O (ANLG)	Negative regulator output. This pin is one of the outputs of the negative switching regulator. A capacitor connected serves as a current reservoir. Typically a 100nF capacitor is connected between pin 10 and GND
11	C2	O (ANLG)	Noise Shunt. Negative voltage generator capacitor connection. This output of the negative switching regulator shunts regulator noise to ground using a 100nF bypass capacitor

PIN DESCRIPTIONS (continued)

Pin #	Signal Name	I/O	Description
12	C1	O (ANLG)	Noise Shunt. Negative voltage generator bypass capacitor connection. Typically a 100nF capacitor is connected between pin C1 and C2
13	VPA	O (ANLG)	PA supply. This is the positive supply for the PA. It is switched by PAEN in conjunction with PDN and NEGEN
14	PDN	I (ANLG)	Power down control. Disables all circuits and reduces power consumption to less than 1mA
15	XIN	I (ANLG)	Crystal or oscillator input. This high input impedance is connected to either an oscillator circuit or to a crystal
16	XOUT	I (ANLG)	Crystal-tank connection. This low impedance output drives the crystal tank circuit

FUNCTIONAL DESCRIPTION

INTRODUCTION

EXTERNAL INTERFACES

The ML2731 has 3 logic inputs: PAEN, NEGEN and PDN. These control lines are used to select the mode of operation to be either SLEEP, STANDBY, PRETX or TRANSMIT. (See Table 1)

PDN	NEGEN	PAEN	Mode
1	X	X	SLEEP
0	1	X	STANDBY
0	0	1	PRETX
0	0	0	TRANSMIT

Table 1. Circuit Enable Logic

MODE CONTROL

Mode Functions
The function of the ML2731 in each mode of operation:

SLEEP

All the circuits are disabled. Current drain is typically less than 1µA.

STANDBY

Oscillator circuits, sine and square wave outputs and 3.0V voltage regulator output are all enabled. VPA output is disabled as well as all other circuits.

PRETX

Oscillator circuits, sine and square wave outputs, 3.0V voltage regulator output, and negative voltage generator are enabled. VBIAS is set to –3.0V. VPA output is disabled and PA bias control loop is inactive.

TRANSMIT

Crystal oscillator circuits, sine and square wave outputs, 3.0V voltage regulator, negative voltage generator, and VPA output are enabled, and VBIAS is voltage controlled so that the VPA current is proportional to the ICON input voltage.

DESCRIPTION OF OPERATION

Voltage Regulator

The ML2731 integrates two low noise voltage regulators. The first regulator internally powers the crystal oscillator support circuit, negative voltage generator support circuit and other on chip circuits.

The second regulator output (REGO) powers external circuits. (See Figure 1) It has a nominal voltage output of 2.9V and sources up to 50mA of current. The low noise output of this regulator makes it suitable for supplying voltage to sensitive components such as final frequency VCO's. The regulator output is disabled in the SLEEP mode and is enabled in all other modes.

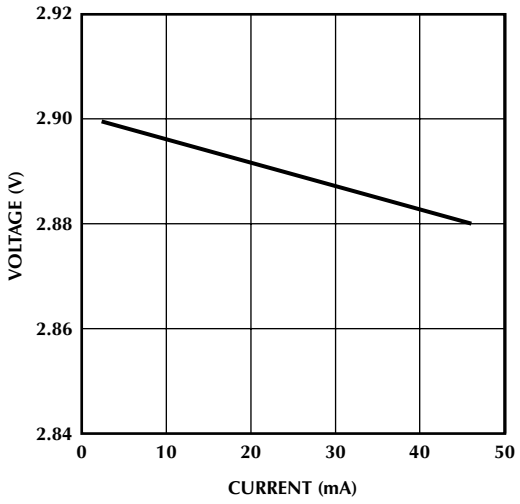


Figure 1. Regulator Ouput Voltage vs. Load Current (REGO)

FUNCTIONAL DESCRIPTION

CRYSTAL OSCILLATOR

The crystal oscillator circuit is powered by an on chip regulator and generates a square wave signal and a sine wave signal. The sine wave is intended for radio PLL circuits, and the square wave clock for the digital circuits.

The frequency range of operation is 10 to 40MHz (determined by the external crystal). The crystal oscillator can also be overdriven by connecting an external oscillator to pin 15 (XIN).

The crystal oscillator square wave and sine wave signal outputs are enabled in STANDBY, PRETX and TRANSMIT modes. (See Figures 2 and 3)

The oscillator circuit is enabled by the PDN logic control pin and turns on and generates stable output signals within 20mS of being enabled.

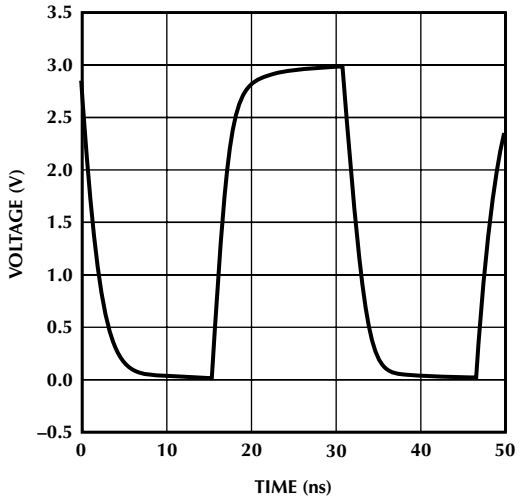


Figure 2: Typical 32 MHz Square wave output signal (1kΩ+10pF load, VCC = 3.3V)

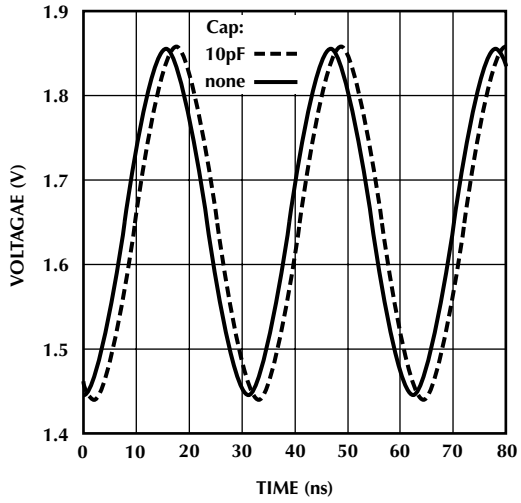


Figure 3: Typical 32 MHz sine wave output signal (1kΩ+0pF load, and 1kΩ+10pF load, VCC = 3.3V)

NEGATIVE VOLTAGE GENERATOR

When driven by a 32 MHz crystal, the charge pump of the ML2731 is clocked with a 2.66 MHz signal. Because the clock frequency is so high, the negative voltage generator requires only small ceramic capacitors on C1 and C2 for operation. (Figure 4) Typically they have values of 100nF. The quick response time (Figure 5), due in part to the small circuit capacitance, allows the charge pump to be disabled when not needed thus reducing power consumption.

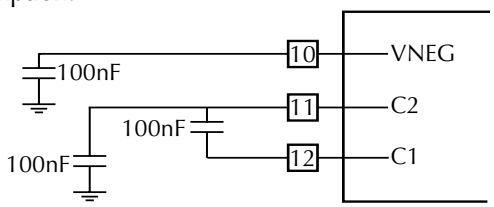


Figure 4: Typical C1 and C2 Noise Shunt Configuration

NEGEN (pin 7) enables the negative voltage generator during the PRETX and TRANSMIT modes of operation.

Output from the negative voltage generator is used internally by the ML2731 to supply the op amp in the PA current control circuit. The resulting voltage is applied to VBIAS for controlling an external PA. The negative voltage generator enables the ML2731 to provide a typical bias voltage in the range of –2.9 V to 0V.

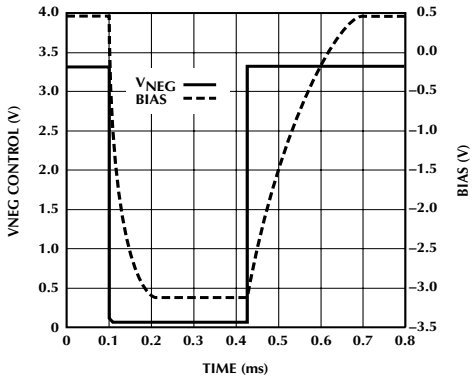


Figure 5: Typical negative voltage generator on and off timing (using 100nF capacitors on pins C1 and C2)

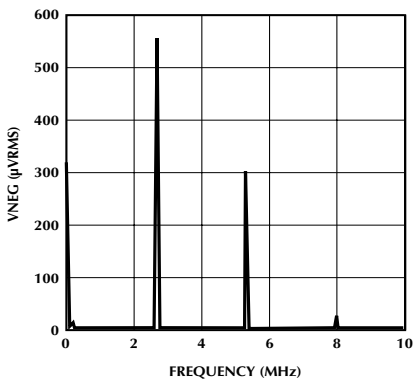


Figure 6: Negative voltage output ripple (µV) (using 100nF bypass and reservoir capacitance)

FUNCTIONAL DESCRIPTION

PA SUPPLY DC SWITCH

The ML2731 includes a DC switch for connecting the supply voltage to an external PA. PAEN activates the DC switch during TRANSMIT mode. To ensure the external PA devices power up correctly, the chip has control circuits preventing the PA supply DC switch from being enabled if the VBIAS voltage is more positive than –3.0V.

Typically, the PA supply DC switch produces a voltage drop of 100mV while conducting a 500mA current. Parameters determining the maximum current capability of the DC switch are the maximum voltage drop that can be tolerated by the external PA and the thermal limitations of the ML2731.

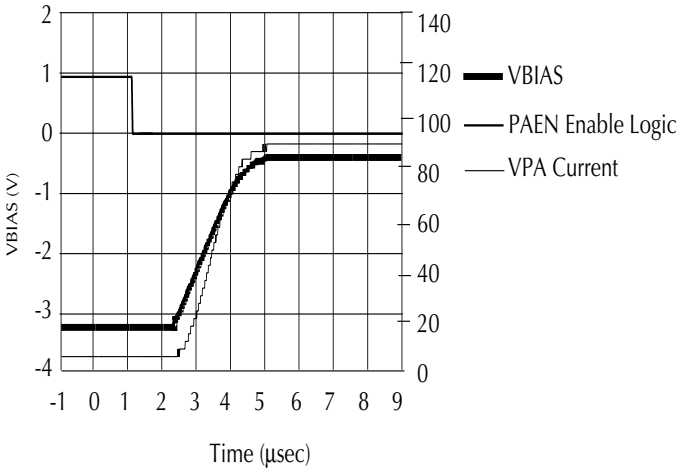


Figure 7: VPA Current ramp following PAEN enable (VBIAS voltage and VPA current values and rise times are determined by PA current control loop component values)

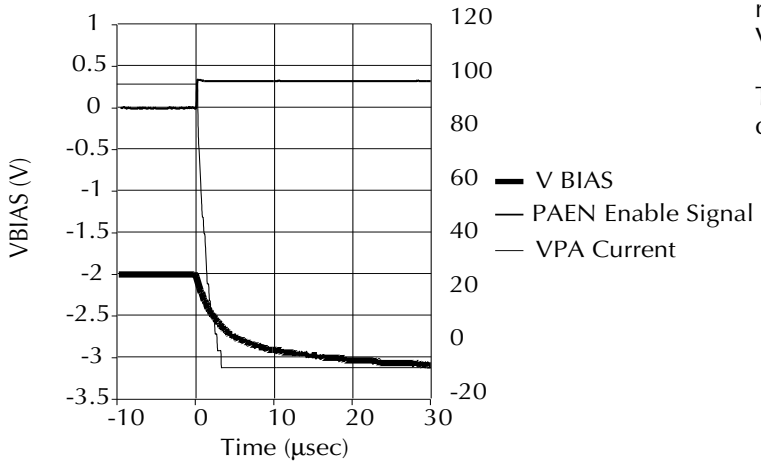


Figure 8: VPA Current ramp following PAEN disable (Vbias voltage and VPA current values and fall times are determined by PA current control loop component values as detailed below)

PA CURRENT CONTROL LOOP

The current control loop allows the PA current to be set by the reference current on the ICON pin. This enables the ML2731 to control PA output power and to compensate for PA current variations due temperature changes. In addition, it removes the need for calibration of PA current in manufacturing because the PA current control loop adjusts the PA bias be proportional to a reference voltage.

The PA current can typically is between 30 to 500mA.

The current control loop is enabled by the PAEN pin.

PA CURRENT CONTROL LOOP AND PA RAMP COMPONENT VALUES

The ICON input pin is at virtual ground. The reference current on the ICON pin is determined by the value of REXT, connected to the ICON input, the voltage reference (VREF), and the voltage source impedance.

For the fixed voltage source in the above circuit, the PA current is determined by the formula:

VPA current = [Vcc(R1/(R2+REXT))*2000] / REXT + Offset

The offset current (minimum PA current) is typically 30mA

A typical REXT resistor value is 12kΩ. Typical reference voltages are in the range 0 to 3.0V to enable the PA current to be controlled over the range of 30mA to 500mA.

For slow PA ramp on/off times (e.g. >10µsec) the PA bias control loop has a sufficiently fast settling time to enable the ramp to be controlled by ramping the ICON voltage input. For fast, e.g. <10µsec PA ramp on/off times, the ramp time is set by the value of the capacitance from VBIAS to ground and VPA to ground.

The typical control loop bandwidths for typical values of capacitance on VBIAS are shown in Figure 13.

FUNCTIONAL DESCRIPTION

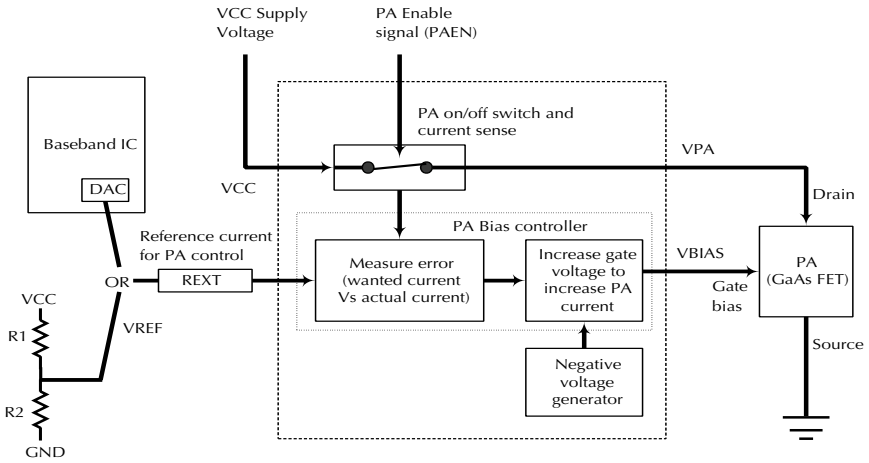


Figure 9: PA Current Control Loop Circuits

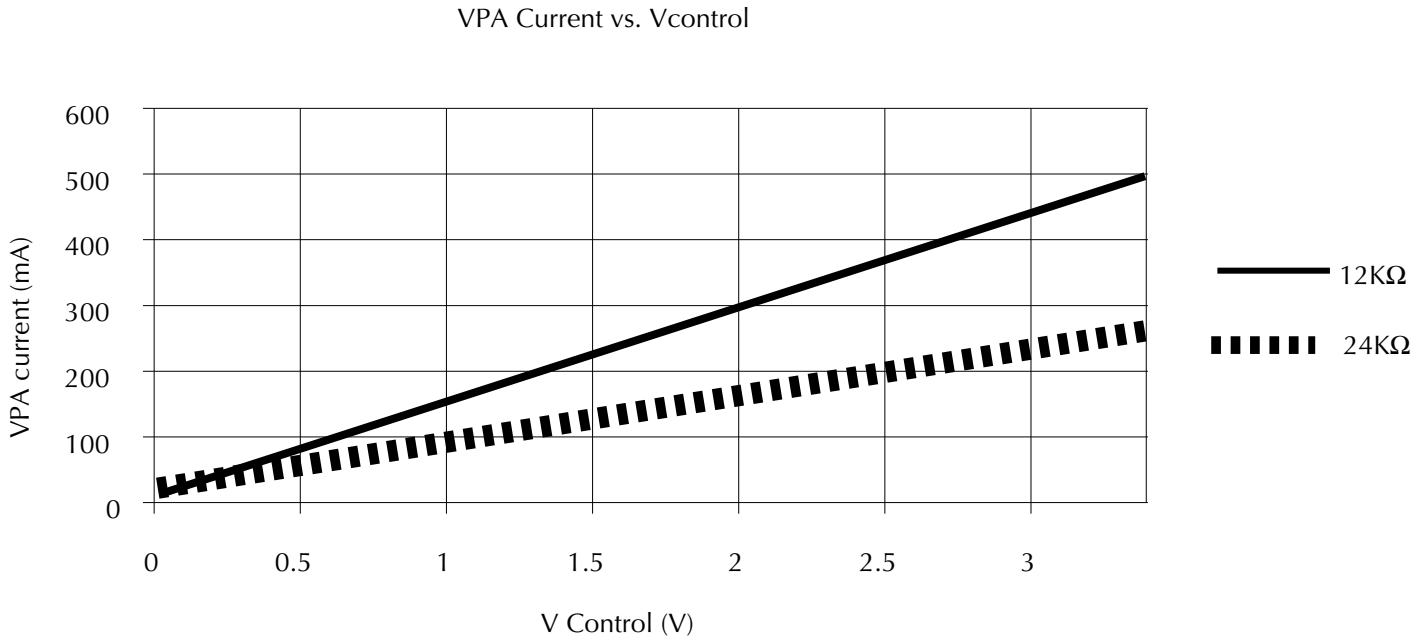


Figure 10: PA Current Control Loop Operation With REXT At 12kΩ and 24kΩ

FUNCTIONAL DESCRIPTION

RECOMMENDED PA BIAS OPERATION

An example of how the PA bias operates is shown in Figure 11. A three-step reference voltage ramp is generated using an external baseband circuit and is applied to the ICON pin via an external resistor. The ML2731 current control loop uses this input as a reference to set the PA current and therefore generates a current ramp output (and hence PA power ramp output.) The rate of change of negative bias and PA current is determined by the capacitance on the VBIAS pin and on the VPA pin. Note sufficient time should be allowed for the negative voltage generator to reach a steady state, prior to enabling the PA.

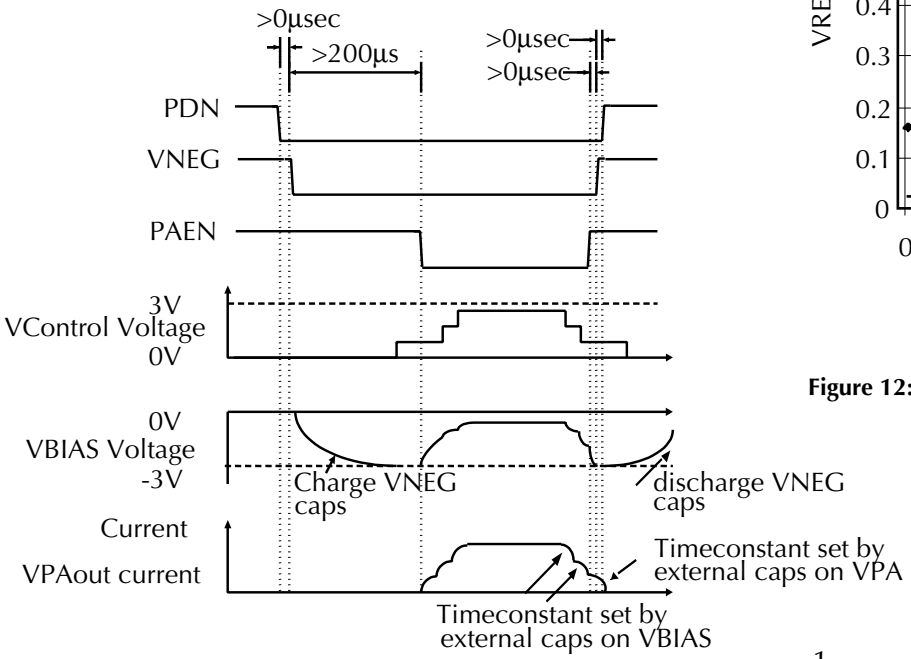


Figure 11: PA Bias Control Loop Operation

Where ICON is a fixed value (i.e. the VPA current is not ramped up and down by changing the value of ICON) then the time taken for the VPA current to ramp up following PAEN being enabled is determined by the capacitor values on VBIAS and VPA. The time taken for the current to ramp down following PAEN being disabled is determined by the capacitance value on VPA only. Example timings are:

1µsec ramp-up for 2nF VBIAS capacitance

4µsec ramp-up for 22nF VBIAS capacitance

An example of a 3 step current ramp up and ramp down, with 3.3nF capacitance on VBIAS, is shown in Figure 12.

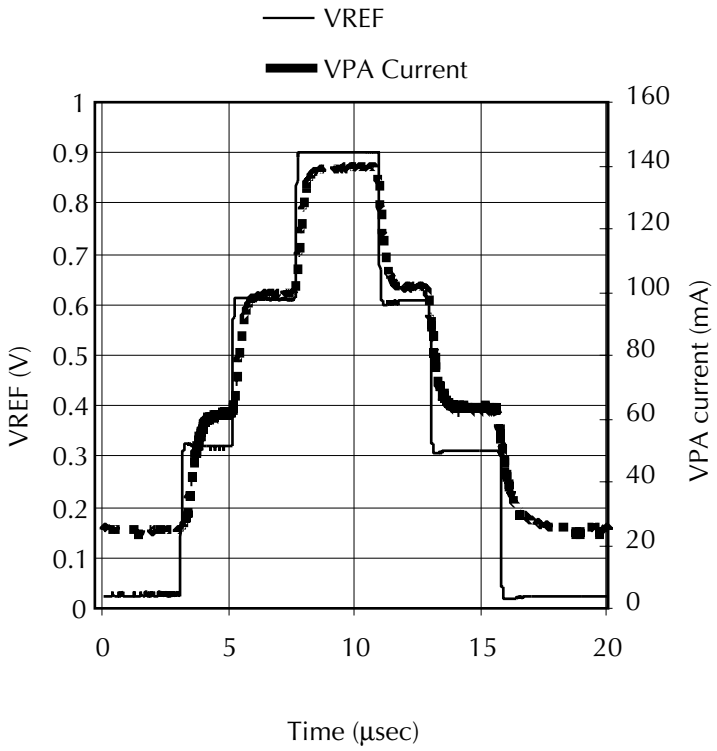


Figure 12: VPA output vs VREF (TRANSMIT mode, REXT = 12kΩ, capacitance on VBIAS = 3.3nF)

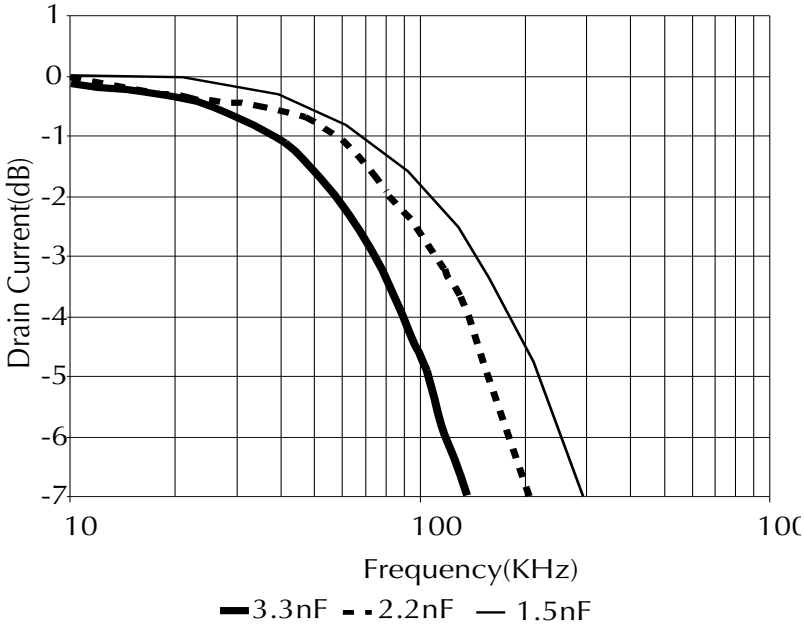


Figure 13: Bandwidth of PA Current control loop for 3.3nF, 2.2nF and 1.5nF VBIAS capacitance

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

VCC 6.0V
All Other Inputs ..... GND –0.3V to VCC + 0.3V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

Commercial Temperature Range ..... 0°C to 70°C
Extended Temperature Range ..... –20°C to 70°C
VCC Range ..... 3.3V to 5.5V
Thermal Resistance (θJA) ..... 100°C/W

ELECTRICAL TABLES

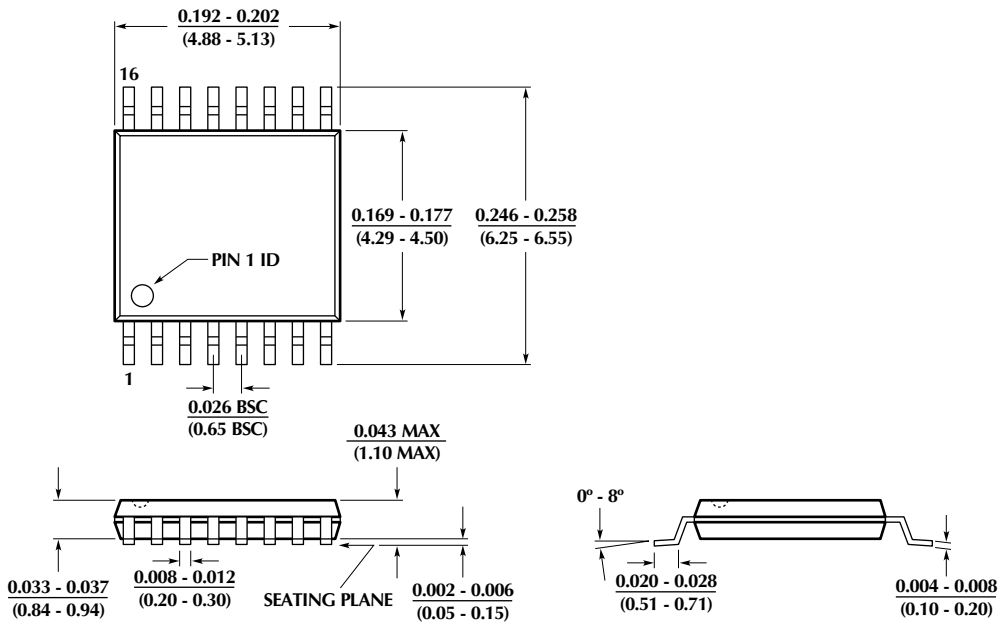
Unless otherwise specified, VCC = 3.3, TA = Operating Temperature Range. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER CONSUMPTION						
	All circuits, supply current, all circuits disabled	DC Connected		1		µA
	Supply current, oscillator enabled, regulator enabled	10pF load on CLKO and SINO 0mA from VREG		5		mA
	Supply current, oscillator and negative voltage generator enabled.	10pF load on CLKO and SINO <1mA current on VBIAS		6		mA
	Supply current, all circuits enabled			9		mA
NEGATIVE VOLTAGE GENERATION						
	Negative Bias Voltage	Current <3mA	–2.9		0	V
	Maximum current, VBIAS			3		mA
	Turn on time, to –3V on VBIAS	Clock 10MHz. PA DISABLED	100			µs
VCONTROL VOLTAGE INPUT						
	Input control voltage range		2.9		0	V
VOLTAGE REGULATOR OUTPUT						
	Output voltage			3.0		V
	Output current				50	mA
OSCILLATOR AND OUTPUTS						
	Frequency Range		10		40	MHz
	Turn on time			5		ms
	SINO voltage range, Peak-to-Peak			450		mV
	CLKO, low			0.4		V
	CLKO, high			VCC – 0.4		V
	Capacitive Load on CLKO	2k shunt R to ground in parallel			15	pF
	Capacitive Load on SINO	2k shunt R to ground in parallel			10	pF
PA SUPPLY VOLTAGE						
	Voltage		VCC – 0.1		VCC	V
	Current		0		500	mA

Note 1: Limis are guaranteed by 100% testing, sampling, or correlation with worst case test condidtions.

PHYSICAL DIMENSIONS

Package: T16
16-Pin TSSOP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML2731CT	0°C to 70°C	TSSOP
ML2731ET	-20°C to 70°C	TSSOP

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