Integrating SMT Synthesizer Solutions into Wireless Designs

Rev. V2

Introduction

Today's high performance, low-cost, SMT solutions for frequency generation greatly simplify the designer's task in developing wireless products. Properly interfacing these devices into the circuit is however essential to achieving maximum performance. This application note highlights some primary areas of concern, some analysis methodologies and suggests possible solutions.

Power Supplies

Clean sources of regulated DC power are essential in minimizing spurious signals from synthesizers. You can calculate the quality of the supply necessary by the following formula:

$$\text{Volts (rms)} \le \frac{\sqrt{2\,(F_s)\,(10)^{\,dBc/20}}}{\text{Pushing Figure}}$$

Where:
Fs = Spur Frequency
dBc = Desired Spur specification in dBc
Pushing Figure = Pushing Figure in Hz/Volt

For example, with a spur frequency of 1 kHz, a spur specification of –80 dBc and a pushing figure of 3MHz/volt, the ripple voltage on the supply must be no greater than 47nV rms. It is good design practice to allow for a margin in the spur specification. For this example, we use –70dBc plus a 10 dB margin for -80 dBc.

Utilizing low-noise regulator designs is critical in achieving the phase noise specifications of these devices. Many DC regulators have their noise output specified in a bandwidth. For example, the LT1761 is specified as 20 V rms typical in 10Hz to 100kHz. Using the previous formula, the maximum allowable noise voltage density at a given offset can be estimated.

$$\text{Noise Voltage Density} \le \frac{\sqrt{2\,(F_s)\,(10)^{\,(dBc/Hz)/20}}}{\text{Pushing Figure}} \text{Volts}\,\sqrt{(Hz)}$$

Relating the noise density to a regulator manufacturer's specification is difficult unless the amplitude/frequency distribution is known. A first order assessment can be made, however if the distribution is assumed flat.

To prevent noise from the digital circuitry in the synthesizer from adversely affecting the VCO, the PLL and VCO supply rails must be adequately decoupled and filtered from each other. In order to facilitate this, M/A-COM synthesizers typically utilize separate VCO and PLL supply pins on the package. A suitable circuit is shown in Figure 1. Component values should be selected that will optimize attenuation of the PLL operating frequency. (step size).

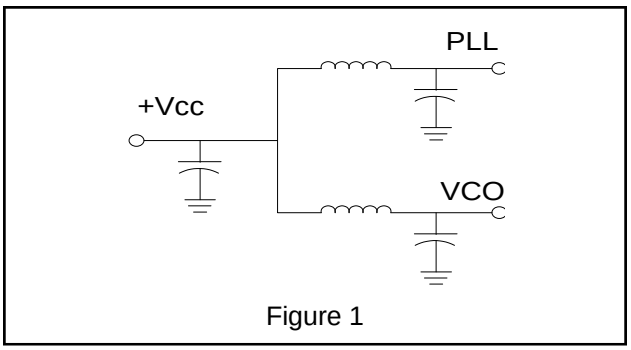


Figure 1

Note: Some synthesizers, such as the MASYVS0060-XXXX series, have a single supply pin, and incorporate an on-board regulator and decoupling between the VCO and PLL. This greatly reduces their sensitivity to power supply noise and ripple.

Synthesizers must be mounted directly on a ground plane and all DC ground returns should be brought to it.

Output Load

It is imperative that the designer understands the load that will be presented to the device. M/A-COM synthesizers are designed for 50 ohm nominal output impedance. Severe mismatches can increase the VCO's phase noise or pull a VCO to the point where it will not oscillate into that load. When it is known that the VSWR of the load will be poor i.e. >2.0:1 any phase angle, a buffered output synthesizer should be specified. Alternatively, the designer can provide the buffer. The best form of load consists of a resistive pad followed by an amplification stage to restore the output power. A representative circuit is shown in Figure 2.

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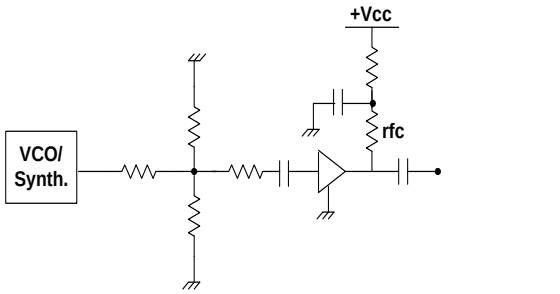


Figure 2

External Reference

The external reference for the synthesizer should not be chosen arbitrarily. Consideration must be made for the waveform and the level. M/A-COM synthesizers are specified for a 1V pk-pk low-pass-filtered square wave, which is internally ac coupled into the PLL IC input. While an unfiltered TTL / CMOS reference signal can be used, there is a potential for spurious products if N x F_{ref} falls into the synthesizer output band, so care should be taken to ensure that harmonics do not fall into the operational band. The internal PLL chip will function with a wide range of reference input levels, but the noise will be degraded if the slew rate is insufficient. For this reason, low frequency / low level sine waves are not recommended.

Noise and spurious on the reference signal also need to be considered, as they will be increased by 20 log(F_{out} / F_{ref}) if they occur within the synthesizer loop bandwidth.

Lock Detector Circuit

In digital mode (where applicable), the Lock Detect output is a CMOS 'high' when the loop is locked and 'low' when it is out of lock.

In analog open-drain mode, when the loop is locked, Lock Detect is 'high' with narrow 'low' pulses at the phase comparison frequency. When the loop is out of lock, Lock Detect alternates between 'high' and 'low', at a rate dependent on the frequency error. An external filter is needed, to turn these conditions into stable 'high' or 'low' states.

Figure 3 shows a typical filter circuit. The component values can be determined after assessing the qualifications for an in-lock condition. This can be specified as being a particular number (N) of consecutive reference cycles of duration (D) during which the phase comparator phase error is some factor less than the reference period. For example, if the phase comparison frequency is 10kHz, one might select the threshold for in-lock as being when 5 consecutive phase comparisons have elapsed where the phase errors are 1000 times shorter than the reference period, i.e. 100ns. Here, N=5 and F=1000.

For the filter shown, when used in conjunction with an open-drain output, the resistor value for R2 would be chosen to be a factor of F x R1. Thus if R1 were pulled low for only 1/1000 of the phase comparison period, its 'effective' resistance would be similar to R2. The two resistors for that duty cycle appear on average to be two 1000 x R1 resistors connected across the supply voltage with their common node voltage (V_c) at V_{cc}/2. Phase errors larger than 1/1000 of the phase comparison period would drag the average voltage of node V_c below V_{cc}/2, indicating an out-of-lock condition. If the time constant R2 x C1 is calculated to be N x the phase comparison period, i.e. 500µs, then the voltage of node V_c would fall below V_{cc}/2 only after 5 consecutive phase errors whose average pulse width was >100ns.

Owing to the possibility of digital noise being present on the Lock Detect line, it should be decoupled as closely to the pin as possible. Additionally, the trace leading to this pin should be isolated as far as possible from the RF output trace.

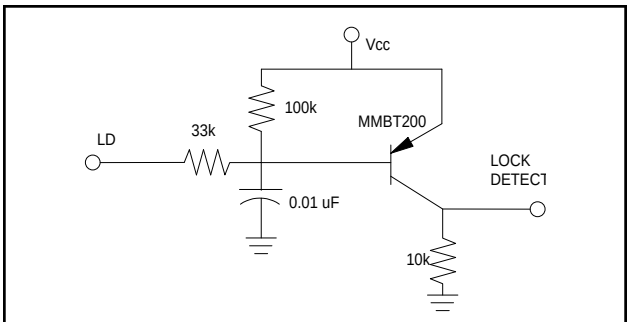


Figure 3

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Clock, Data and Load Enable Inputs

The Clock, Data and Load Enable Inputs are all high impedance CMOS and should be fed with square waves with level of VHIGH ³ 0.8 Vcc and VLOW £ 0.2 Vcc. An external termination resistor can be added externally if desired. Refer to the specific device datasheet for the proper programming information. Consideration needs to be taken when choosing the command word for programming the dividers. While the PLL will allow for a variety of steps to be programmed, the step size specific to the synthesizer design should be used. The internal loop filter is optimized for a given step size and the use of another could result in greater than specified phase noise or spurious outputs.

Noise Contributors

Understanding the key contributors to single sideband phase noise is paramount to achieving optimum performance. Often, the noise profile can be adjusted to obtain dynamic properties of the synthesizer. Careful consideration of the noise profile required at spot frequencies, integrated or both will lead to a superior system design. Phase noise is measured in units of dBc/Hz at a given offset from the carrier. It is the difference between the level of the carrier and the noise level at a given offset normalized to a 1Hz bandwidth.

Assuming power supply contribution is negligible, the three key contributors are:

- Phase Comparator Noise
- Reference Noise
- VCO Noise

The phase comparator noise affects the noise floor within the loop. The phase noise is multiplied up to the VCO output frequency by 20log (F_{out}/F_{step}). Another effect that is often ignored is that the noise floor is related to the step size by approximately 10dB/decade. This is particularly important as the step size is increased because the noise floor degrades by 10log ($F_{step}/F_{step(comp)}$). $F_{step(comp)}$ is the frequency at which the noise floor is measured.

For example consider a PLL IC which has a noise floor of approximately –165 dBc/Hz at a phase comparison frequency of 30 kHz. If the frequency output of the synthesizer is 1 GHz with a step size of 200 kHz the noise floor within the loop is:

= -165 + 10 log (200 kHz/30 kHz)
+ 20 log (1 GHz/200 kHz) = -82.78 dBc/Hz

With respect to the effect of the reference noise, the reference frequency is multiplied up to the VCO output frequency within the PLL IC. The noise side bands of the reference oscillator are increased by the ratio given by 20log(FVCO/Fref).

For example, a synthesizer with a 15 MHz reference is divided down to 30 kHz has an output frequency of 1GHz. If the 15 MHz reference noise is –115 dBc/Hz at 100 Hz offset, then the reference noise at the output frequency would be:

-115 +20 log (1 GHz / 15 MHz) = -78.5 dBc/Hz

Finally the effect of the VCO noise should be considered. Within the loop bandwidth, the VCO noise is suppressed at a rate of –40 dB/decade. Near the loop bandwidth, the suppression is not so great and some of the VCO noise will add to the loop noise floor. Spurious signals that are at or within the loop bandwidth will undergo similar suppression characteristics to phase noise. Figure 4 gives a good representation of this effect when trying to assess design risks.

Ultimately the VCO design is part of the integrated package so outside the scope of changes to the synthesizer interfaces but as noise that appears on the power supplies modulates the VCO this will directly effect the performance of the synthesizer. The same principles as described earlier should be applied to reduce power supply noise.

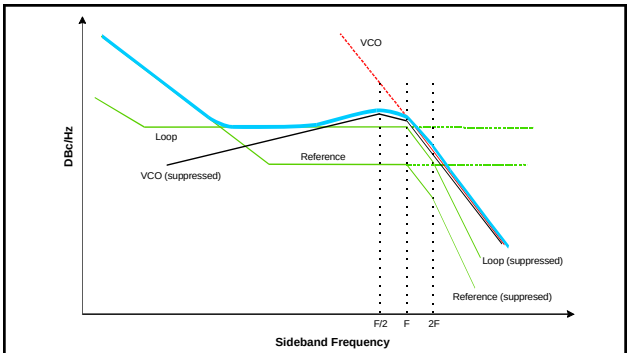


Figure 4

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