ADS7834



SBAS098A – JANUARY 1998 – REVISED SEPTEMBER 2003

12-Bit High-Speed, Low-Power Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 500kHz THROUGHPUT RATE
- 2.5V INTERNAL REFERENCE
- LOW POWER: 11mW
- SINGLE-SUPPLY +5V OPERATION
- DIFFERENTIAL INPUT
- SERIAL INTERFACE
- 12-BITS NO MISSING CODES
- MINI-DIP-8 AND MSOP-8
- 0V TO V_{REF} INPUT RANGE

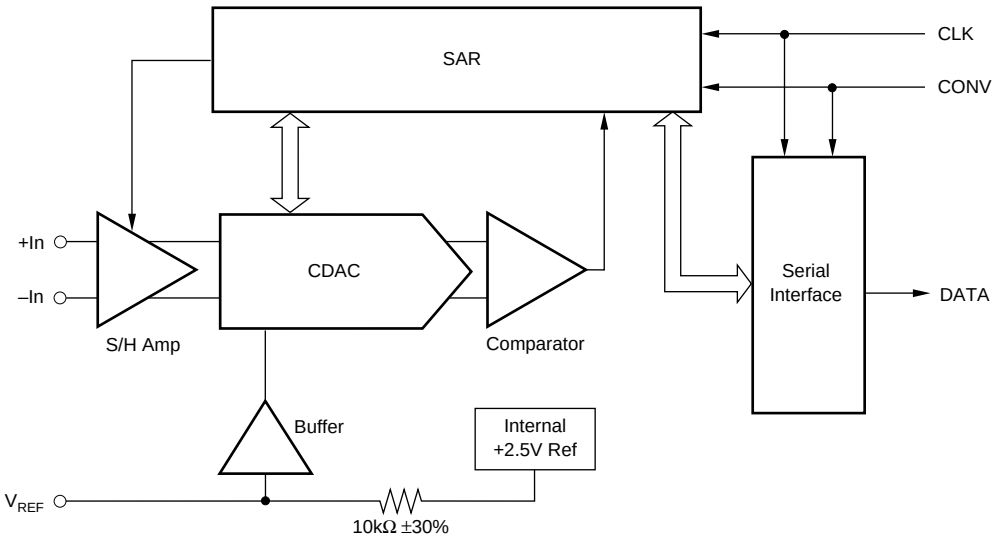
APPLICATIONS

- BATTERY-OPERATED SYSTEMS
- DIGITAL SIGNAL PROCESSING
- HIGH-SPEED DATA ACQUISITION
- WIRELESS COMMUNICATION SYSTEMS

DESCRIPTION

The ADS7834 is a 12-bit sampling analog-to-digital converter (A/D) complete with sample/hold, internal 2.5V reference, and synchronous serial interface. Typical power dissipation is 11mW at a 500kHz throughput rate. The device can be placed into a power-down mode that reduces dissipation to just 2.5mW. The input range is zero to the reference voltage, and the internal reference can be overdriven by an external voltage.

Low power, small size, and high speed make the ADS7834 ideal for battery-operated systems such as wireless communication devices, portable multi-channel data loggers, and spectrum analyzers. The serial interface also provides low-cost isolation for remote data acquisition. The ADS7834 is available in a plastic mini-DIP-8 or an MSOP-8 package and is ensured over the –40°C to +85°C temperature range.



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PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL LINEARITY ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING(2)	ORDERING NUMBER(3)	TRANSPORT MEDIA, QUANTITY
ADS7834E	±2	N/S(3)	MSOP-8	DGK	–40°C to +85°C	C34	ADS7834E/250	Tape and Reel, 250
ADS7834E	"	"	"	"	"	"	ADS7834E/2K5	Tape and Reel, 2500
ADS7834EB	±1	±1	MSOP-8	DGK	–40°C to +85°C	C34	ADS7834EB/250	Tape and Reel, 250
ADS7834EB	"	"	"	"	"	"	ADS7834EB/2K5	Tape and Reel, 2500
ADS7834P	±2	N/S(3)	Plastic DIP-8	P	–40°C to +85°C	ADS7834P	ADS7834P	Rails
ADS7834PB	±1	±1	"	"	"	ADS7834PB	ADS7834PB	Rails

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com. (2) Performance Grade information is marked on the reel. (3) N/S = Not Specified, typical only. However, 12-Bits no missing codes is ensured over temperature.

ABSOLUTE MAXIMUM RATINGS(1)

$+V_{CC}$ to GND	–0.3V to 6V
Analog Inputs to GND	–0.3V to (V_{CC} + 0.3V)
Digital Inputs to GND	–0.3V to (V_{CC} + 0.3V)
Power Dissipation	325mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

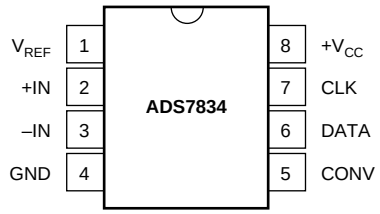
ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Texas Instruments recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

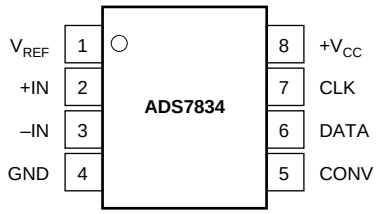
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION

Top View



Plastic Mini-DIP-8



MSOP-8

PIN ASSIGNMENTS

PIN	NAME	DESCRIPTION
1	V_{REF}	Reference Output. Decouple to ground with a 0.1µF ceramic capacitor and a 2.2µF tantalum capacitor.
2	+IN	Noninverting Input.
3	–IN	Inverting Input. Connect to ground or to remote ground sense point.
4	GND	Ground.
5	CONV	Convert Input. Controls the sample/hold mode, start of conversion, start of serial data transfer, type of serial transfer, and power down mode. See the Digital Interface section for more information.
6	DATA	Serial Data Output. The 12-bit conversion result is serially transmitted most significant bit first with each bit valid on the rising edge of CLK. By properly controlling the CONV input, it is possibly to have the data transmitted least significant bit first. See the Digital Interface section for more information.
7	CLK	Clock Input. Synchronizes the serial data transfer and determines conversion speed.
8	$+V_{CC}$	Power Supply. Decouple to ground with a 0.1µF ceramic capacitor and a 10µF tantalum capacitor.

SPECIFICATIONS

At T_A = –40°C to +85°C, $+V_{CC}$ = +5V, f_{SAMPLE} = 500kHz, f_{CLK} = 16 • f_{SAMPLE}, internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7834P, E			ADS7834PB, EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT								
Full-Scale Input Span[1]	+IN – (–IN)	0		V_{REF}	*		*	V
Absolute Input Range	+IN	–0.2		V_{REF} +0.2	*		*	V
	–IN	–0.2		+0.2	*		*	V
Capacitance			25			*		pF
Leakage Current			1			*		µA
SYSTEM PERFORMANCE								
Resolution			12			*		Bits
No Missing Codes		12			*			Bits
Integral Linearity Error			±1	±2		±0.5	±1	LSB[2]
Differential Linearity Error			±0.8			±0.5	±1	LSB
Offset Error			±2	±5		±1	*	LSB
Gain Error[3]	25°C		±12	±30		±7	±15	LSB
	–40°C to +85°C			±50			±35	LSB
Common-Mode Rejection	DC, 0.2Vp-p		70			*		dB
	1MHz, 0.2Vp-p		50			*		dB
Noise			60			*		µVrms
Power Supply Rejection	Worst Case Δ, $+V_{CC}$ = 5V ±5%		1.2			*		LSB
SAMPLING DYNAMICS								
Conversion Time		1.625			*			µs
Acquisition Time		0.350			*			µs
Throughput Rate				500			*	kHz
Aperture Delay			5			*		ns
Aperture Jitter			30			*		ps
Step Response			350			*		ns
DYNAMIC CHARACTERISTICS								
Signal-to-Noise Ratio	V_{IN} = 5Vp-p at 10kHz		72			*		dB
Total Harmonic Distortion[4]	V_{IN} = 5Vp-p at 10kHz		–78	–72		–82	–75	dB
Signal-to-(Noise+Distortion)	V_{IN} = 5Vp-p at 10kHz	68	70		70	72		dB
Spurious Free Dynamic Range	V_{IN} = 5Vp-p at 10kHz	72	78		75	82		dB
Usable Bandwidth	SNR > 68dB		350			*		kHz
REFERENCE OUTPUT								
Voltage	I_{OUT} = 0	2.475	2.50	2.525	2.48	*	2.52	V
Source Current[5]	Static Load			50			*	µA
Drift	I_{OUT} = 0		20			*		ppm/°C
Line Regulation	4.75V ≤ V_{CC} ≤ 5.25V		0.6			*		mV
REFERENCE INPUT								
Range		2.0		2.55	*		*	V
Resistance[6]	to Internal Reference Voltage		10		*	*	*	kΩ
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels:								
V_{IH}	$\|I_{IH}\| \leq +5\mu A$	3.0		V_{CC} +0.3	*		*	V
V_{IL}	$\|I_{IL}\| \leq +5\mu A$	–0.3		0.8	*		*	V
V_{OH}	I_{OH} = –500µA	3.5			*		*	V
V_{OL}	I_{OL} = 500µA			0.4	*		*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENT								
$+V_{CC}$	Specified Performance	4.75		5.25	*		*	V
Quiescent Current	f_{SAMPLE} = 500kHz		2.2			*		mA
	Power-Down		0.5			*		mA
Power Dissipation	f_{SAMPLE} = 500kHz		11	20		*	*	mW
	Power-Down		2.5			*		mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

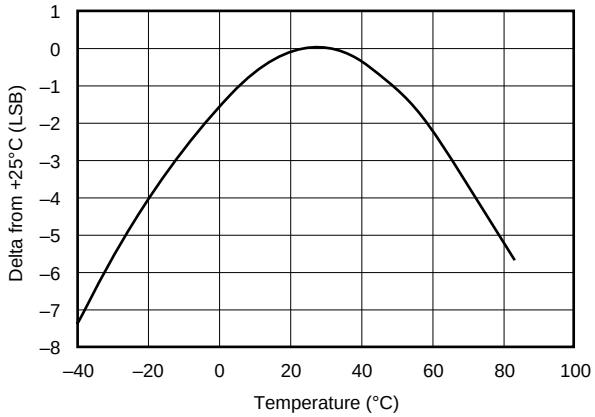
* Specifications same as ADS7834P,E.

NOTES: (1) Ideal input span, does not include gain or offset error. (2) LSB means Least Significant Bit, with V_{REF} equal to +2.5V, one LSB is 610µV. (3) Measured relative to an ideal, full-scale input (+IN – (–IN)) of 2.499V. Thus, gain error includes the error of the internal voltage reference. (4) Calculated on the first nine harmonics of the input frequency. (5) If the internal reference is required to source current to an external load, the reference voltage will change due to the internal 10kΩ resistor. (6) Can vary ±30%.

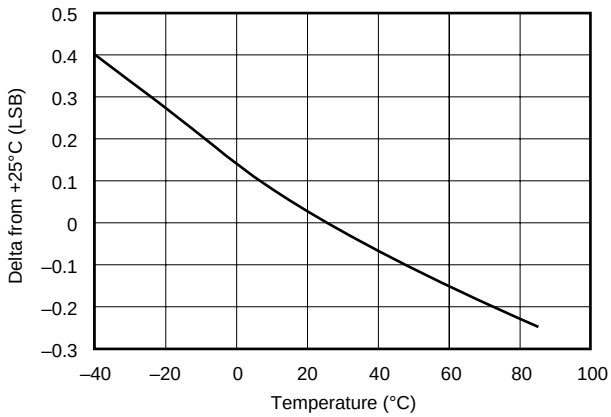
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{CC} = +5V, f_{SAMPLE} = 500kHz, f_{CLK} = 16 • f_{SAMPLE}, and internal +2.5V reference, unless otherwise specified.

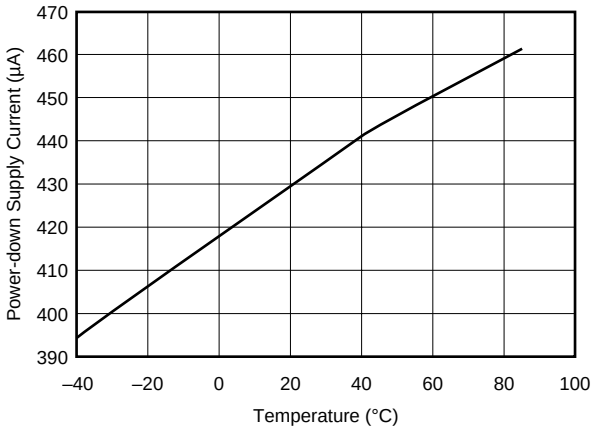
FULL-SCALE ERROR vs TEMPERATURE



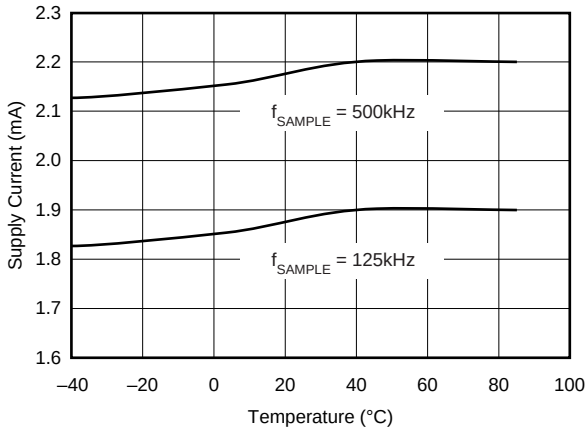
OFFSET VOLTAGE vs TEMPERATURE



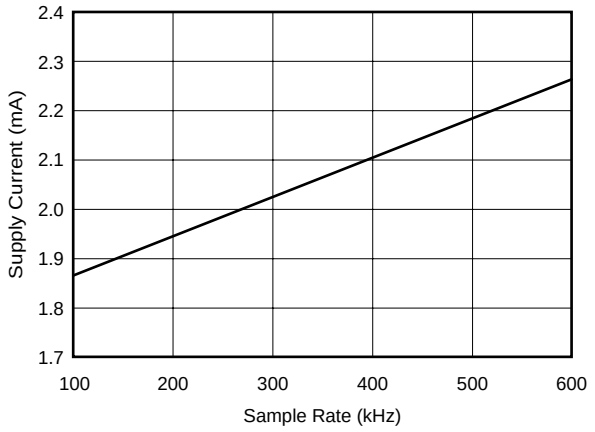
POWER-DOWN SUPPLY CURRENT vs TEMPERATURE



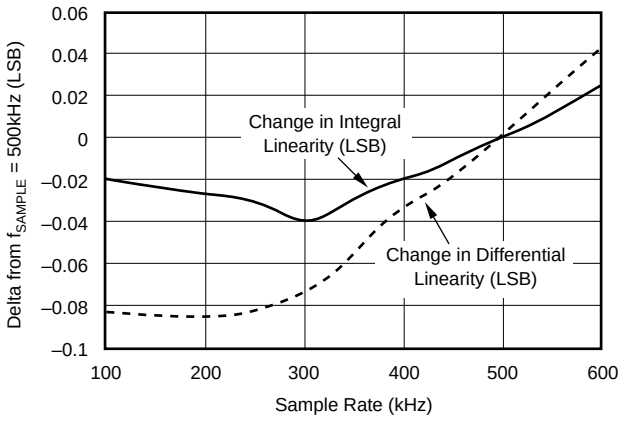
SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs SAMPLE RATE



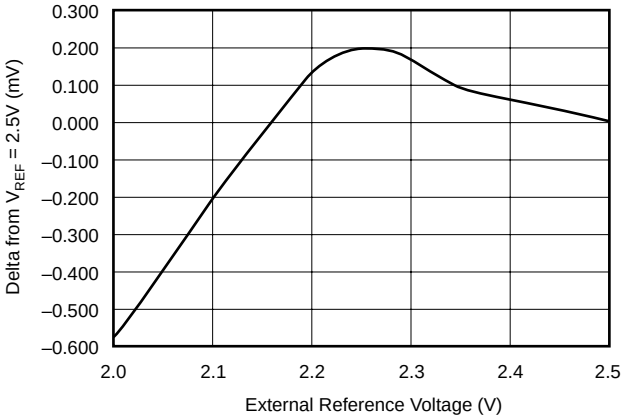
INTEGRAL LINEARITY and DIFFERENTIAL LINEARITY vs SAMPLE RATE



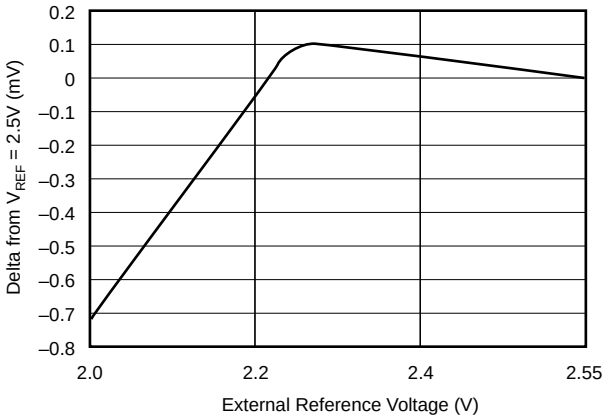
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_{CC} = +5V, f_{SAMPLE} = 500kHz, f_{CLK} = 16 • f_{SAMPLE}, and internal +2.5V reference, unless otherwise specified.

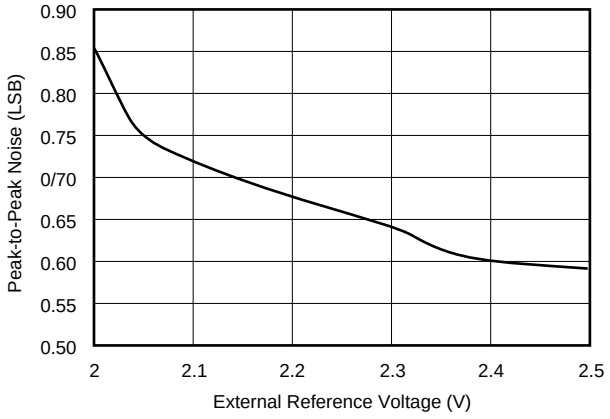
FULL-SCALE ERROR
vs EXTERNAL REFERENCE VOLTAGE



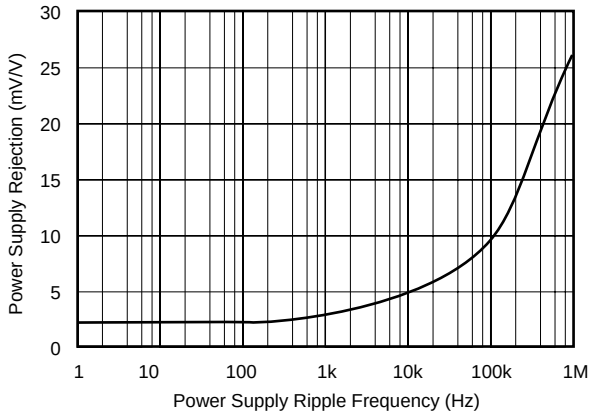
OFFSET VOLTAGE vs EXTERNAL
REFERENCE VOLTAGE



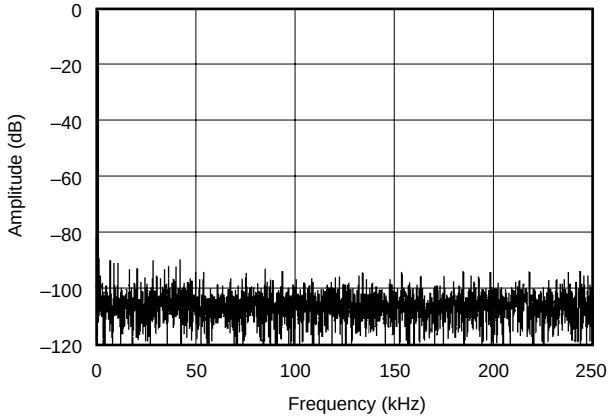
PEAK-TO-PEAK NOISE
vs EXTERNAL REFERENCE VOLTAGE



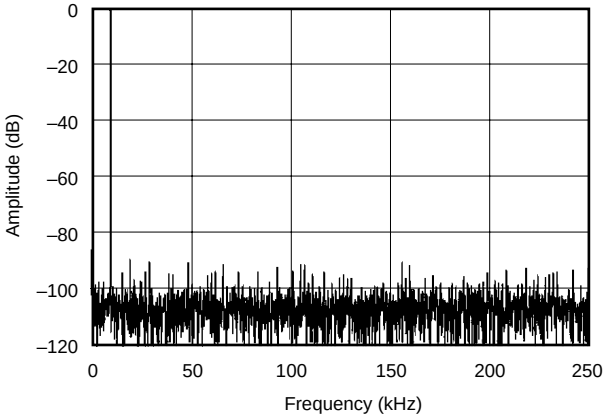
POWER SUPPLY REJECTION
vs POWER SUPPLY RIPPLE FREQUENCY



FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 977Hz, –0.2dB)



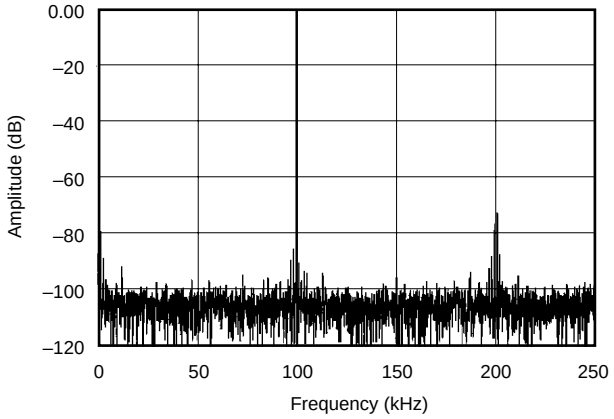
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 9.77kHz, –0.2dB)



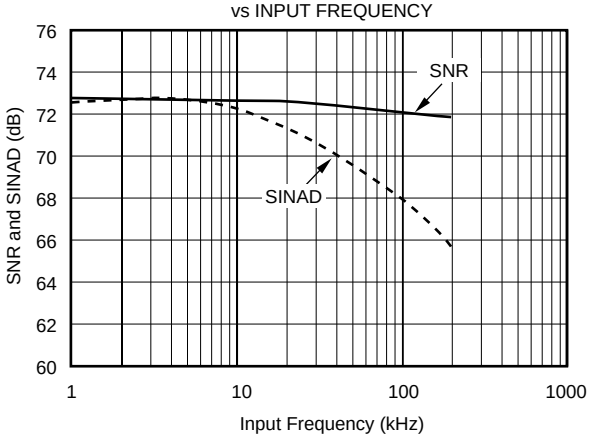
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_{CC} = +5V, f_{SAMPLE} = 500kHz, f_{CLK} = 16 • f_{SAMPLE}, and internal +2.5V reference, unless otherwise specified.

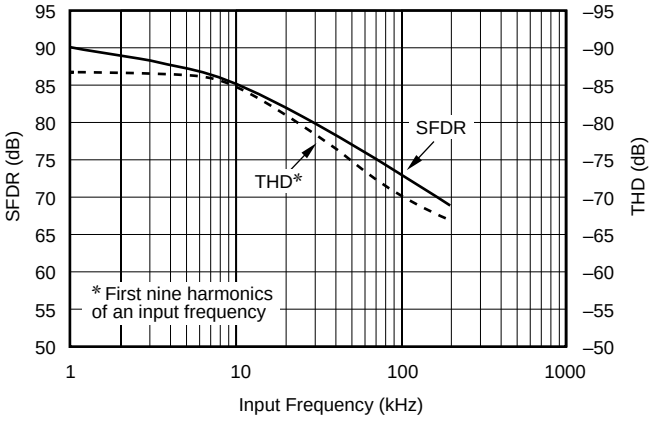
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 99.7kHz, –0.2dB)



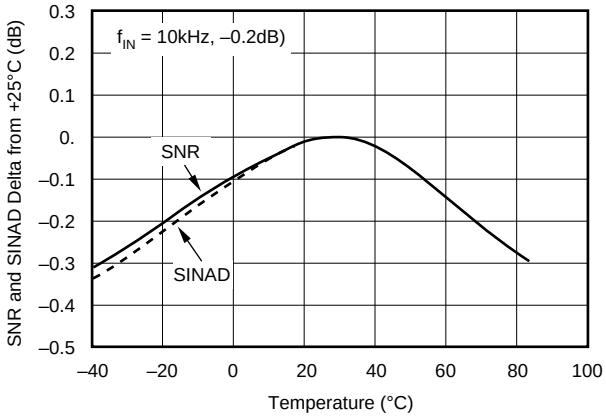
SIGNAL-TO-NOISE RATIO and
SIGNAL-TO-(NOISE+DISTORTION)
vs INPUT FREQUENCY



SPURIOUS FREE DYNAMIC RANGE
and TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY



SIGNAL-TO-NOISE and
SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



THEORY OF OPERATION

The ADS7834 is a high-speed. successive approximation register (SAR) analog-to-digital converter (A/D) with an internal 2.5V bandgap reference. The architecture is based on capacitive redistribution which inherently includes a sample/hold function. The converter is fabricated on a 0.6µ CMOS process. See Figure 1 for the basic operating circuit for the ADS7834.

The ADS7834 requires an external clock to run the conversion process. This clock can vary between 200kHz (12.5kHz throughput) and 8MHz (500kHz throughput). The duty cycle of the clock is unimportant as long as the minimum HIGH and LOW times are at least 50ns and the clock period is at least 125ns. The minimum clock frequency is set by the leakage on the capacitors internal to the ADS7834.

The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

The range of the analog input is set by the voltage on the V_{REF} pin. With the internal 2.5V reference, the input range is 0V to 2.5V. An external reference voltage can be placed on V_{REF}, overdriving the internal voltage. The range for the external voltage is 2.0V to 2.55V, giving an input voltage range of 2.0V to 2.55V.

The digital result of the conversion is provided in a serial manner, synchronous to the CLK input. The result is provided most significant bit first and represents the result of the conversion currently in progress—there is no pipeline delay. By properly controlling the CONV and CLK inputs, it is possible to obtain the digital result least significant bit first.

ANALOG INPUT

The +IN and –IN input pins allow for a differential input signal to be captured on the internal hold capacitor when the converter enters the hold mode. The voltage range on the –IN input is limited to –0.2V to 0.2V. Because of this, the differential input can be used to reject only small signals that are common to both inputs. Thus, the –IN input is best used to sense a remote ground point near the source of the +IN signal. If the source driving the +IN signal is nearby, the –IN should be connected directly to ground.

The input current into the analog input depends on input voltage and sample rate. Essentially, the current into the device must charge the internal hold capacitor (typically 20pF) during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance to a 12-bit settling level within the sample period—which can be as little as 350ns in some operating modes. While the converter is in the hold mode or after the sampling capacitor has been fully charged, the input impedance of the analog input is greater than 1GΩ.

Care must be taken regarding the input voltage on the +IN and –IN pins. To maintain the linearity of the converter, the +IN input should remain within the range of GND – 200mV to V_{REF} + 200mV. The –IN input should not drop below GND – 200mV or exceed GND + 200mV. Outside of these ranges, the converter's linearity may not meet specifications.

REFERENCE

The reference voltage on the V_{REF} pin directly sets the full-scale range of the analog input. The ADS7834 can operate with a reference in the range of 2.0V to 2.55V, for a full-scale range of 2.0V to 2.55V.

The voltage at the V_{REF} pin is internally buffered and this buffer drives the capacitor DAC portion of the converter. This is important because the buffer greatly reduces the dynamic load placed on the reference source. However, the voltage at V_{REF} will still contain some noise and glitches from the SAR conversion process. These can be reduced by carefully bypassing the V_{REF} pin to ground as outlined in the sections that follow.

INTERNAL REFERENCE

The ADS7834 contains an onboard 2.5V reference, resulting in a 0V to 2.5V input range on the analog input. The specification table gives the various specifications for the

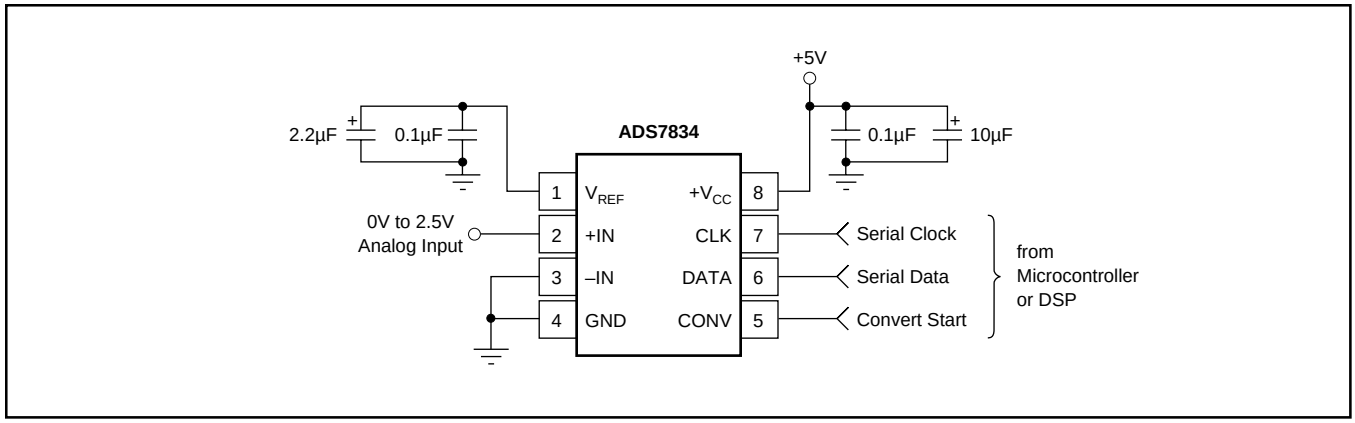


FIGURE 1. Basic Operation of the ADS7834.

internal reference. This reference can be used to supply a small amount of source current to an external load, but the load should be static. Due to the internal 10kΩ resistor, a dynamic load will cause variations in the reference voltage, and will dramatically affect the conversion result. Note that even a static load will reduce the internal reference voltage seen at the buffer input. The amount of reduction depends on the load and the actual value of the internal "10kΩ" resistor. The value of this resistor can vary by ±30%.

The V_{REF} pin should be bypassed with a 0.1µF capacitor placed as close as possible to the ADS7834 package. In addition, a 2.2µF tantalum capacitor should be used in parallel with the ceramic capacitor. Placement of this capacitor, while not critical to performance, should be placed as close to the package as possible.

EXTERNAL REFERENCE

The internal reference is connected to the V_{REF} pin and to the internal buffer via a 10kΩ series resistor. Thus, the reference voltage can easily be overdriven by an external reference voltage. The voltage range for the external voltage is 2.0V to 2.55V, corresponding to an analog input range of 2.0V to 2.55V.

While the external reference will not source significant current into the V_{REF} pin, it does have to drive the series 10kΩ resistor that is terminated into the 2.5V internal reference (the exact value of the resistor will vary up to ±30% from part to part). In addition, the V_{REF} pin should still be bypassed to ground with at least a 0.1µF ceramic capacitor (placed as close to the ADS7834 as possible). The reference will have to be stable with this capacitive load. Depending on the particular reference and A/D conversion speed, additional bypass capacitance may be required, such as the 2.2µF tantalum capacitor shown in Figure 1.

Reasons for choosing an external reference over the internal reference vary, but there are two main reasons. One is to achieve a given input range. For example, a 2.048V reference provides for a 0V to 2.048V input range—or 500µV per LSB. The other is to provide greater stability over temperature. (The internal reference is typically 20ppm/°C which translates into a full-scale drift of roughly 1 output code for every 12°C. This does not take into account other sources of full-scale drift). If greater stability over temperature is needed, then an external reference with lower temperature drift will be required.

DIGITAL INTERFACE

Figure 2 shows the serial data timing and Figure 3 shows the basic conversion timing for the ADS7834. The specific timing numbers are listed in Table I. There are several important items in Figure 3 which give the converter additional capabilities over typical 8-pin converters. First, the transition from sample mode to hold mode is synchronous to the falling edge of CONV and is not dependent on CLK. Second, the CLK input is not required to be continuous during the sample mode. After the conversion is complete, the CLK may be kept LOW or HIGH.

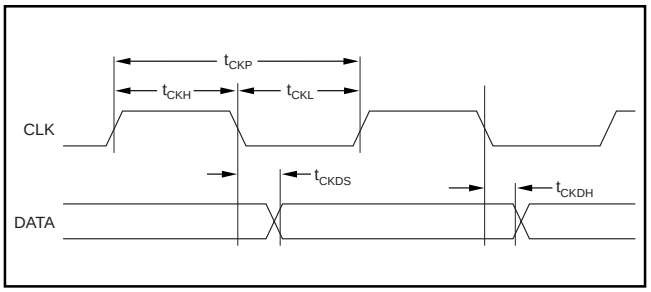


FIGURE 2. Serial Data and Clock Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	350			ns
t_{CONV}	Conversion Time	1.625			µs
t_{CKP}	Clock Period	125		5000	ns
t_{CKL}	Clock LOW	50			ns
t_{CKH}	Clock HIGH	50			ns
t_{CKDH}	Clock Falling to Current Data Bit No Longer Valid	5	15		ns
t_{CKDS}	Clock Falling to Next Data Valid		30	50	ns
t_{CVL}	CONV LOW	40			ns
t_{CVH}	CONV HIGH	40			ns
t_{CKCH}	CONV Hold after Clock Falls(1)	10			ns
t_{CKCS}	CONV Setup to Clock Falling(1)	10			ns
t_{CKDE}	Clock Falling to DATA Enabled		20	50	ns
t_{CKDD}	Clock Falling to DATA High Impedance		70	100	ns
t_{CKSP}	Clock Falling to Sample Mode		5		ns
t_{CKPD}	Clock Falling to Power-Down Mode		50		ns
t_{CVHD}	CONV Falling to Hold Mode (Aperture Delay)		5		ns
t_{CVSP}	CONV Rising to Sample Mode		5		ns
t_{CVPU}	CONV Rising to Full Power-up		50		ns
t_{CVDD}	CONV Changing State to DATA High Impedance		70	100	ns
t_{CVPD}	CONV Changing State to Power-Down Mode		50		ns
t_{DRP}	CONV Falling to Start of CLK (for hold droop < 0.1 LSB)			5	µs

Note: (1) This timing is not required under some situations. See text for more information.

TABLE I. Timing Specifications (T_A = –40°C to +85°C, C_{LOAD} = 30pF).

The asynchronous nature of CONV to CLK raises some interesting possibilities, but also some design considerations. Figure 3 shows that CONV has timing restraints in relation to CLK (t_{CKCH} and t_{CKCS}). However, if these times are violated (which could happen if CONV is completely asynchronous to CLK), the converter will perform a conversion correctly, but the exact timing of the conversion is indeterminate. Since the setup and hold time between CONV and CLK has been violated in this example, the start of conversion could vary by one clock cycle. (Note that the start of conversion can be detected by using a pull-up resistor on DATA. When DATA drops out of high-impedance and goes LOW, the conversion has started and that clock cycle is the first of the conversion.)

In addition if CONV is completely asynchronous to CLK and CLK is continuous, then there is the possibility that CLK will transition just prior to CONV going LOW. If this

occurs faster than the 10ns indicated by t_{CKCH}, then there is a chance that some digital feedthrough may be coupled onto the hold capacitor. This could cause a small offset error for that particular conversion.

Thus, there are two basic ways to operate the ADS7834. CONV can be synchronous to CLK and CLK can be continuous. This would be the typical situation when interfacing the converter to a digital signal processor. The second method involves having CONV asynchronous to CLK and gating the operation of CLK (a non-continuous clock). This method would be more typical of an SPI-like interface on a microcontroller. This method would also allow CONV to be generated by a trigger circuit and to initiate (after some delay) the start of CLK. These two methods are covered under DSP Interfacing and SPI Interfacing.

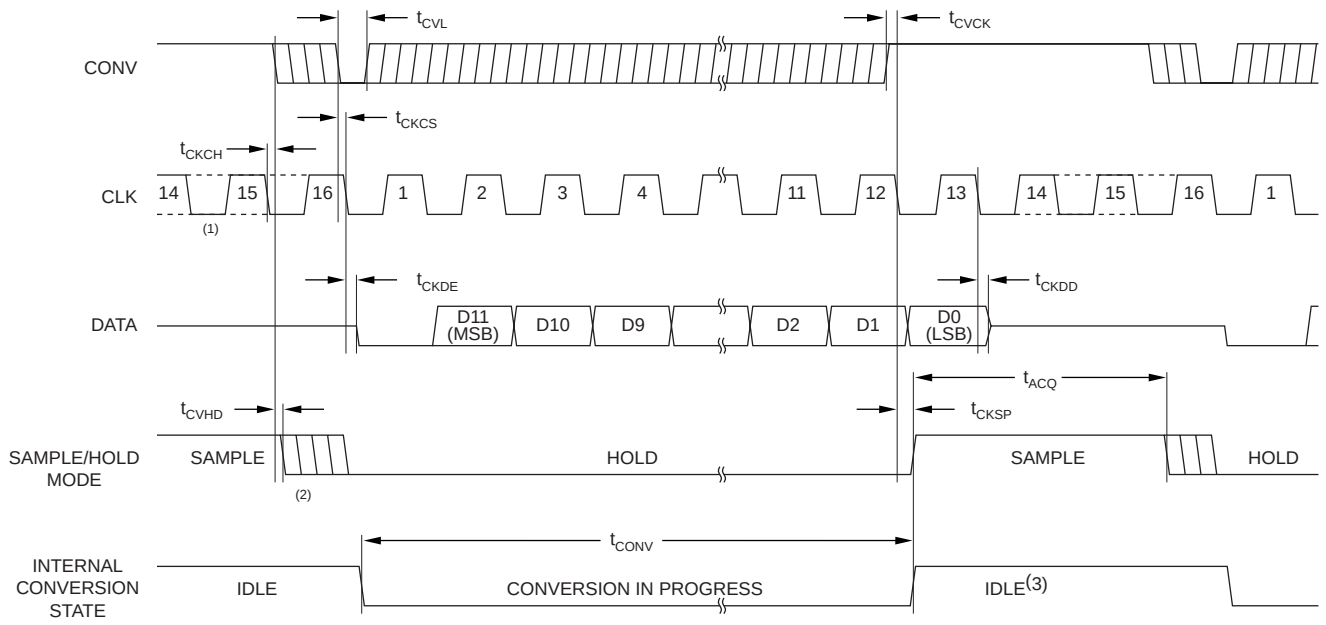
POWER-DOWN TIMING

The conversion timing shown in Figure 3 does not result in the ADS7834 going into the power-down mode. If the conversion rate of the device is high (approaching 500kHz), then there is very little power that can be saved by using the power-down mode. However, since the power-down mode incurs no conversion penalty (the very first conversion is valid), at lower sample rates, significant power can be saved by allowing the device to go into power-down mode between conversions.

Figure 4 shows the typical method for placing the A/D into the power-down mode. If CONV is kept LOW during the conversion and is LOW at the start of the 13 clock cycle, then the device enters the power-down mode. It remains in this mode until the rising edge of CONV. Note that CONV must be HIGH for at least t_{ACQ} in order to sample the signal properly as well as to power-up the internal nodes.

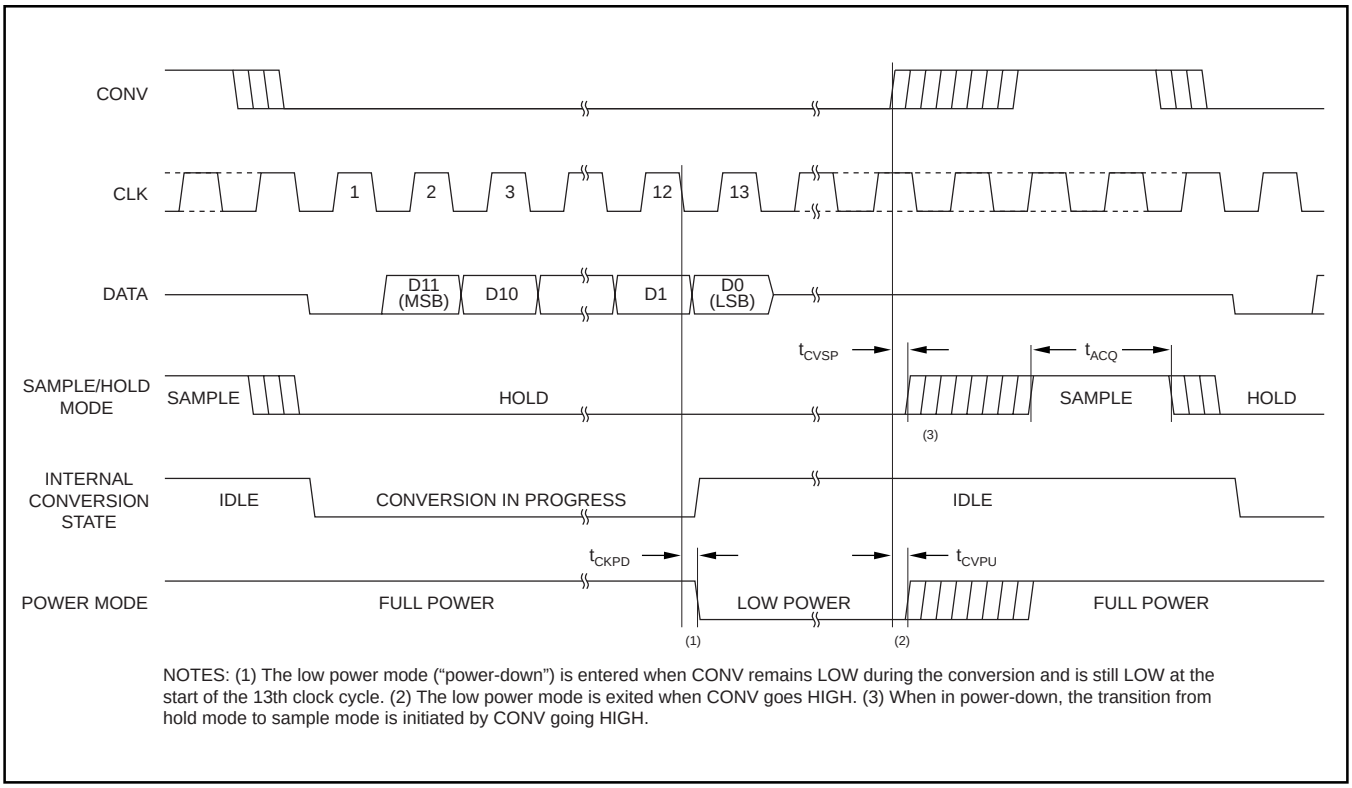
There are two different methods for clocking the ADS7834. The first involves scaling the CLK input in relation to the conversion rate. For example, an 8MHz input clock and the timing shown in Figure 3 results in a 500kHz conversion rate. Likewise, a 1.6MHz clock would result in a 100kHz conversion rate. The second method involves keeping the clock input as close to the maximum clock rate as possible and starting conversions as needed. This timing is similar to that shown in Figure 4. As an example, a 50kHz conversion rate would require 160 clock periods per conversion instead of the 16 clock periods used at 500kHz.

The main distinction between the two is the amount of time that the ADS7834 remains in power-down. In the first mode, the converter only remains in power-down for a small number of clock periods (depending on how many clock periods there are per each conversion). As the conversion rate scales, the converter always spends the same percentage of time in power-down. Since less power is drawn by the digital logic, there is a small decrease in power consumption, but it is very slight. This effect can be seen in the typical performance curve “Supply Current vs Sample Rate.”



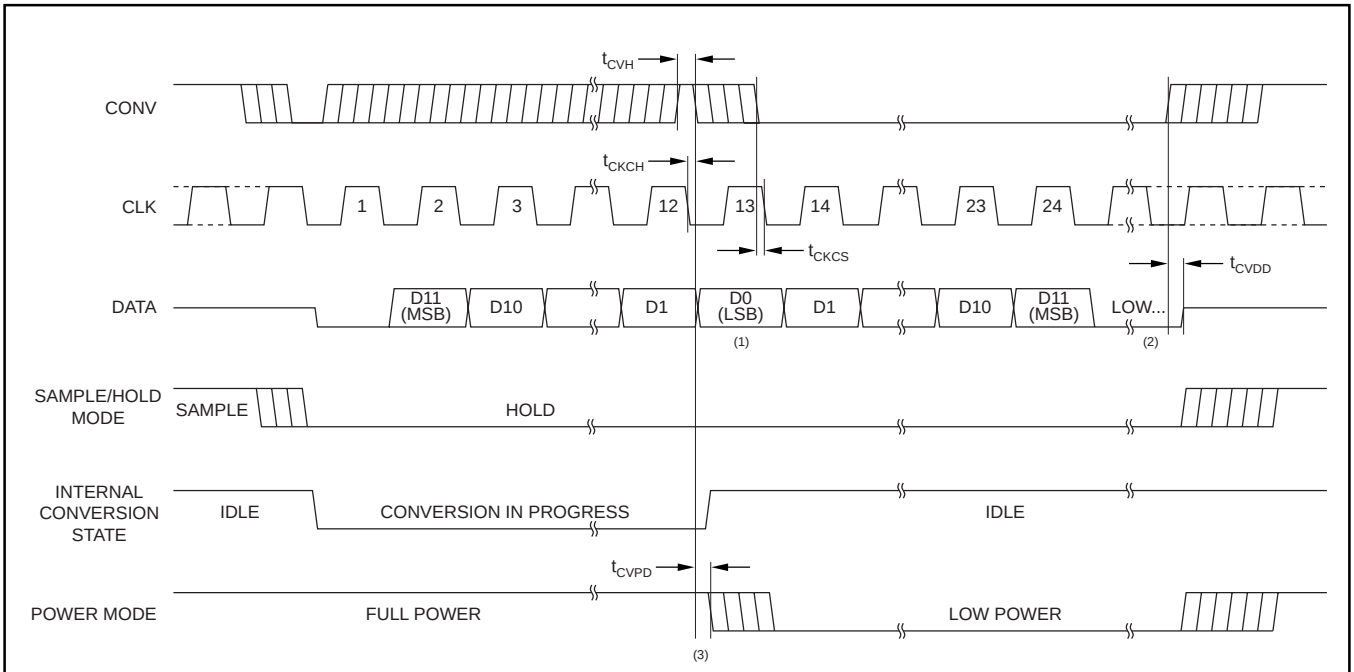
NOTES: (1) Clock periods 14 and 15 are shown for clarity, but are not required for proper operation of the ADS7834, provided that the minimum t_{ACQ} time is met. The CLK input may remain HIGH or LOW during this period. (2) The transition from sample mode to hold mode occurs on the falling edge of CONV. This transition is not dependent on CLK. (3) The device remains fully powered when operated as shown. If the sample time is longer than 3 clock periods, power consumption can be reduced by allowing the device to enter a power-down mode. See the power-down timing for more information.

FIGURE 3. Basic Conversion Timing.



NOTES: (1) The low power mode ("power-down") is entered when CONV remains LOW during the conversion and is still LOW at the start of the 13th clock cycle. (2) The low power mode is exited when CONV goes HIGH. (3) When in power-down, the transition from hold mode to sample mode is initiated by CONV going HIGH.

FIGURE 4. Power-down Timing.



NOTES: (1) The serial data can be transmitted LSB first by pulling CONV LOW during the 13th clock cycle. (2) After the MSB has been transmitted, the DATA output pin will remain LOW until CONV goes HIGH. (3) When CONV is taken LOW to initiate the LSB first transfer, the converter enters the power-down mode.

FIGURE 5. Serial Data "LSB-First" Timing.

In contrast, the second method (clocking at a fixed rate) means that each conversion takes X clock cycles. As the time between conversions get longer, the converter remains in power-down an increasing percentage of time. This reduces total power consumption by a considerable amount. For example, a 50kHz conversion rate results in roughly 1/10 of the power (minus the reference) that is used at a 500kHz conversion rate.

Table II offers a look at the two different modes of operation and the difference in power consumption.

f_{SAMPLE}	POWER WITH CLK = 16 • f_{SAMPLE}	POWER WITH CLK = 8MHz
500kHz	11mW	11mW
250kHz	10mW	7mW
100kHz	9mW	4mW

TABLE II. Power Consumption versus CLK Input.

LSB FIRST DATA TIMING

Figure 5 shows a method to transmit the digital result in a least-significant bit (LSB) format. This mode is entered when CONV is pulled HIGH during the conversion (before the end of the 12th clock) and then pulled LOW during the 13th clock (when D0, the LSB, is being transmitted). The next 11 clocks then repeat the serial data, but in an LSB first format. The converter enters the power-down mode during the 13th clock and resumes normal operation when CONV goes HIGH.

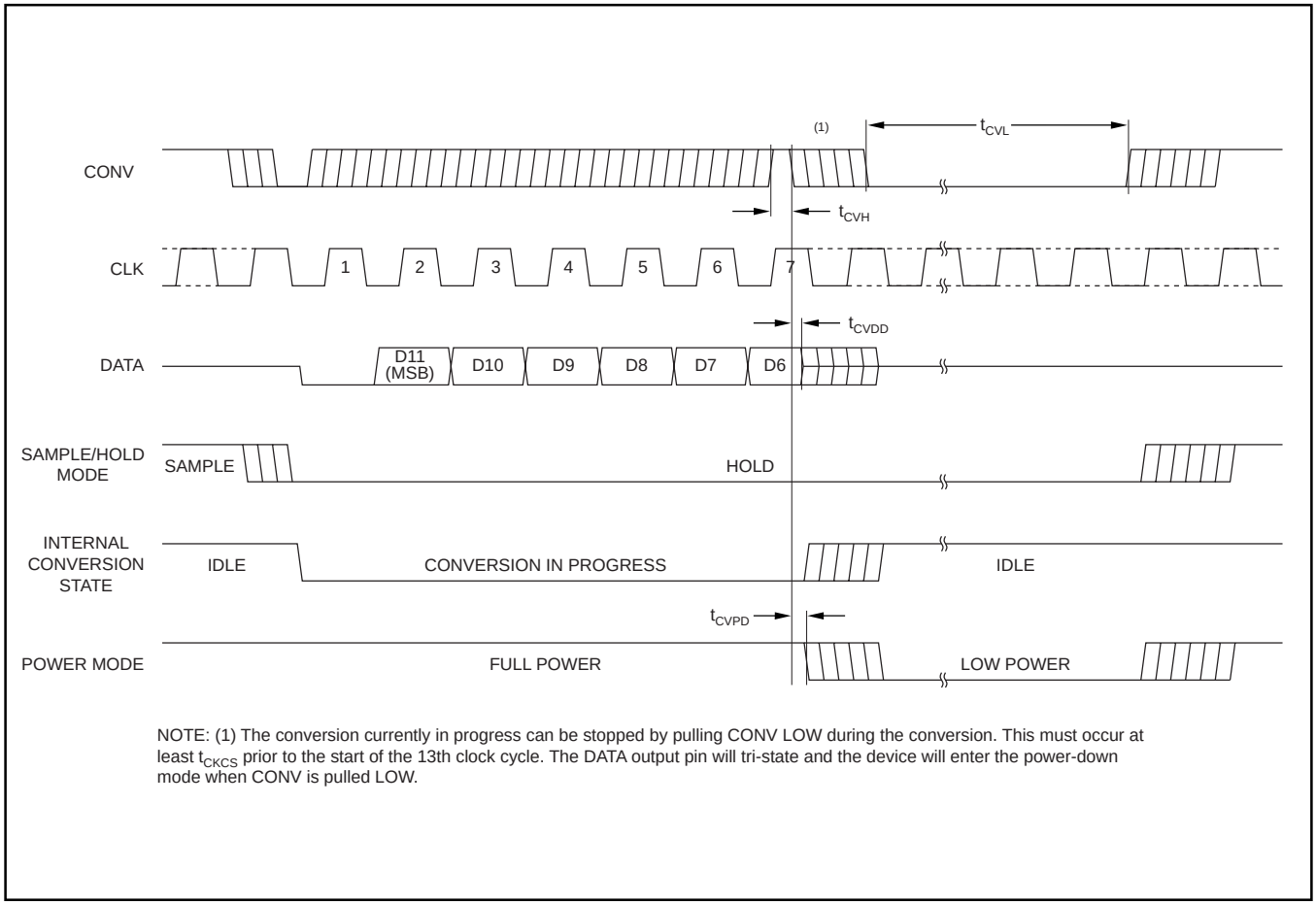
SHORT-CYCLE TIMING

The conversion currently in progress can be "short-cycled" with the technique shown in Figure 6. This term means that the conversion will terminate immediately, before all 12 bits have been decided. This can be a very useful feature when a resolution of 12 bits is not needed. An example would be when the converter is being used to monitor an input voltage until some condition is met. At that time, the full resolution of the converter would then be used. Short-cycling the conversion can result in a faster conversion rate or lower power dissipation.

There are several very important items shown in Figure 6. The conversion currently in progress is terminated when CONV is taken HIGH during the conversion and then taken LOW prior to t_{CKCH} before the start of the 13th clock cycle. Note that if CONV goes LOW during the 13th clock cycle, then the LSB-first mode will be entered (Figure 5). Also, when CONV goes LOW, the DATA output immediately transitions to high impedance. If the output bit that is present during that clock period is needed, CONV must not go LOW until the bit has been properly latched into the receiving logic.

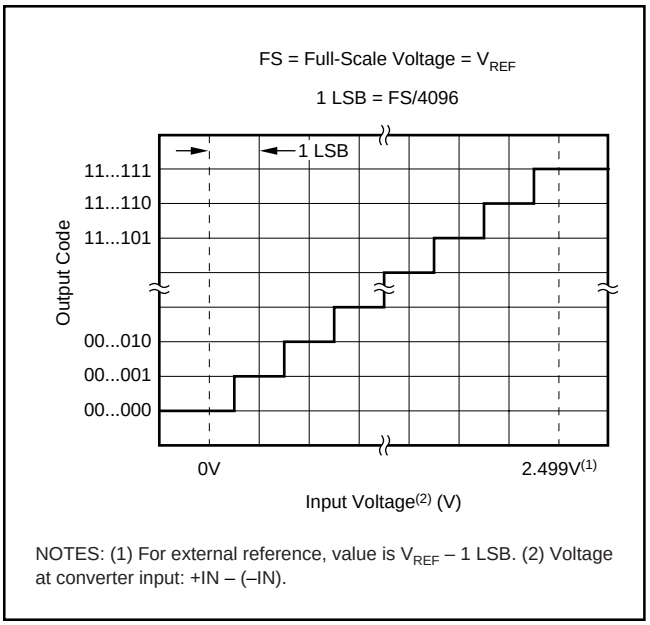
DATA FORMAT

The ADS7834 output data is in straight binary format as shown in Figure 7. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.



NOTE: (1) The conversion currently in progress can be stopped by pulling CONV LOW during the conversion. This must occur at least t_{CKCS} prior to the start of the 13th clock cycle. The DATA output pin will tri-state and the device will enter the power-down mode when CONV is pulled LOW.

FIGURE 6. Short-cycle Timing.



NOTES: (1) For external reference, value is V_{REF} – 1 LSB. (2) Voltage at converter input: +IN – (–IN).

FIGURE 7. Ideal Input Voltages and Output Codes.

DSP INTERFACING

Figure 8 shows a timing diagram that might be used with a typical digital signal processor such as a TI DSP. For the buffered serial port (BSP) on the TMS320C54X family, CONV would tied to BFSX, CLK would be tied to BCLKX, and DATA would be tied to BDR.

SPI/QSPI INTERFACING

Figure 9 shows the timing diagram for a typical serial peripheral interface (SPI) or queued serial peripheral interface (QSPI). Such interfaces are found on a number of microcontrollers form various manufacturers. CONV would be tied to a general purpose I/O pin (SPI) or to a PCX pin (QSPI), CLK would be tied to the serial clock, and DATA would be tied to the serial input data pin such as MISO (master in slave out).

Note the time t_{DRP} shown in Figure 9. This represents the maximum amount of time between CONV going LOW and the start of the conversion clock. Since CONV going LOW places the sample and hold in the hold mode and because the hold capacitor loses charge over time, there is a requirement that time t_{DRP} be met as well as the maximum clock period (t_{CKP}).

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7834 circuitry. This is particularly true if the CLK input is approaching the maximum input rate.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the CLK input.

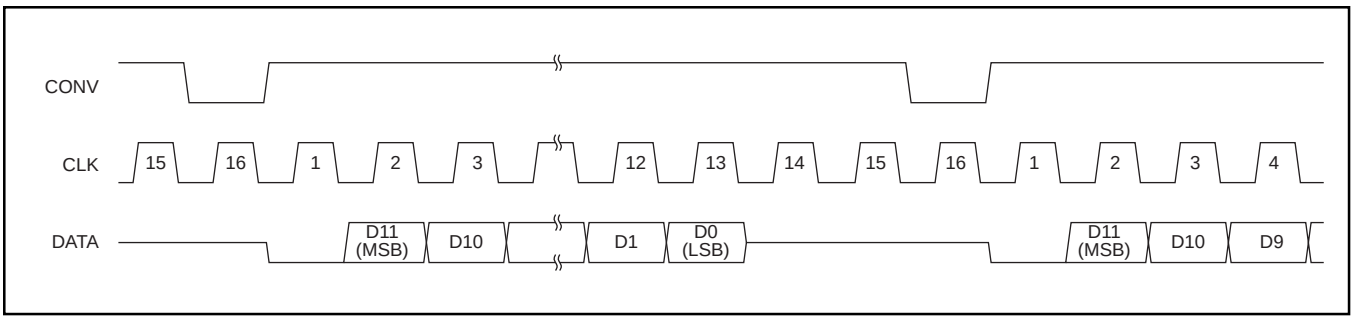


FIGURE 8. Typical DSP Interface Timing.

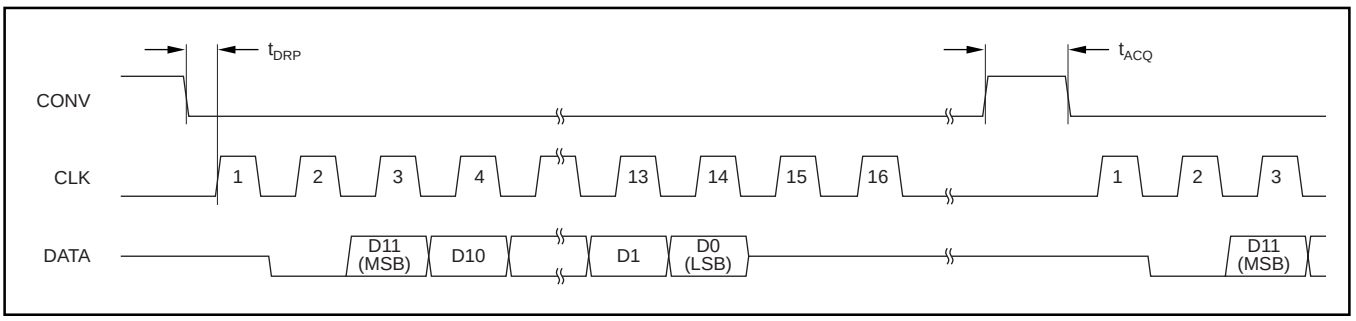


FIGURE 9. Typical SPI/QSPI Interface Timing.

With this in mind, power to the ADS7834 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor is recommended. If needed, an even larger capacitor and a 5Ω or 10Ω series resistor my be used to lowpass filter a noisy supply.

The ADS7834 draws very little current from an external reference on average as the reference voltage is internally buffered. However, glitches from the conversion process appear at the V_{REF} input and the reference source must be able to handle this. Whether the reference is internal or external, the V_{REF} pin should be bypassed with a 0.1µF capacitor. An additional larger capacitor may also be used, if desired. If the reference voltage is external and originates from an op-amp, make sure that it can drive the bypass capacitor or capacitors without oscillation.

The GND pin should be connected to a clean ground point. In many cases, this will be the "analog" ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ADS7834E/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C34	Samples
ADS7834E/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C34	Samples
ADS7834E/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C34	Samples
ADS7834E/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C34	Samples
ADS7834EB/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C34	Samples
ADS7834EB/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C34	Samples
ADS7834EB/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C34	Samples
ADS7834EB/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	C34	Samples
ADS7834P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
ADS7834PB	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

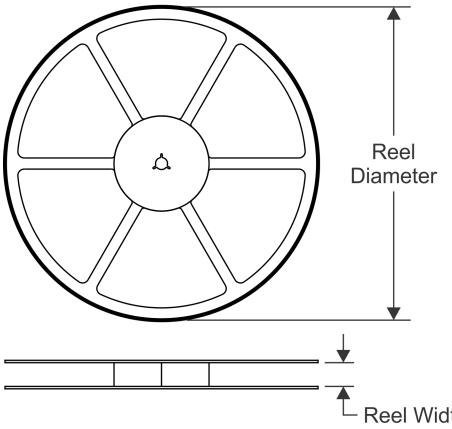
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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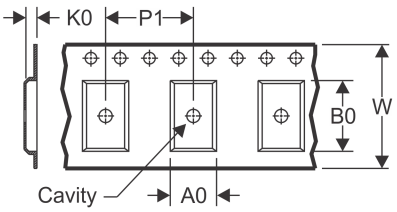
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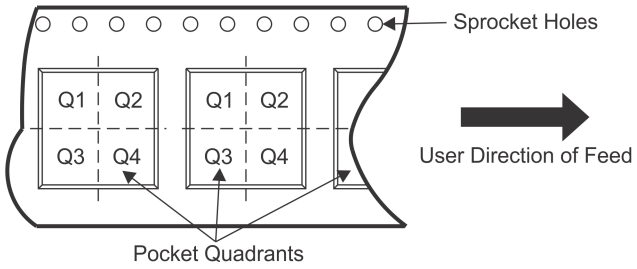


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

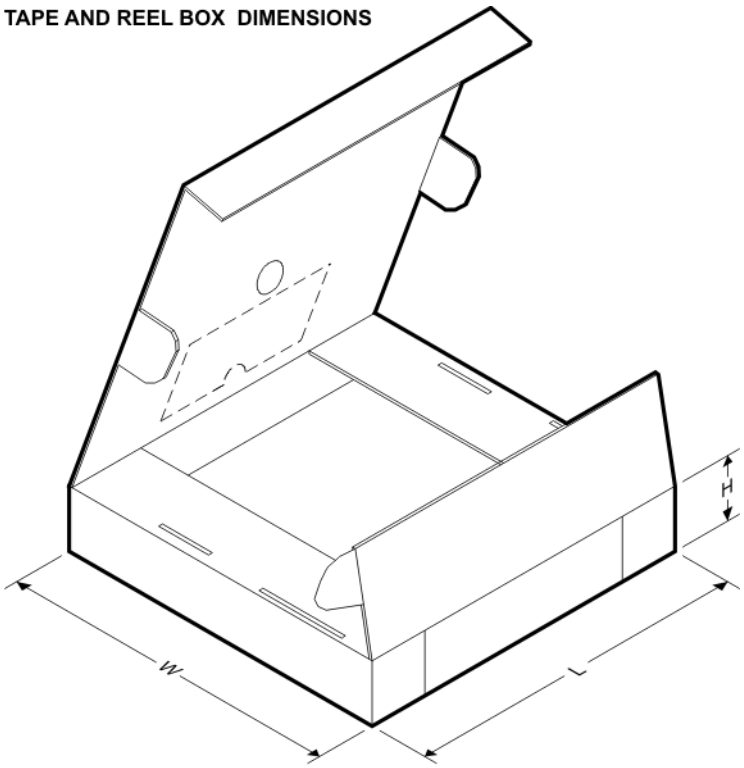
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7834E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7834EB/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS7834EB/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

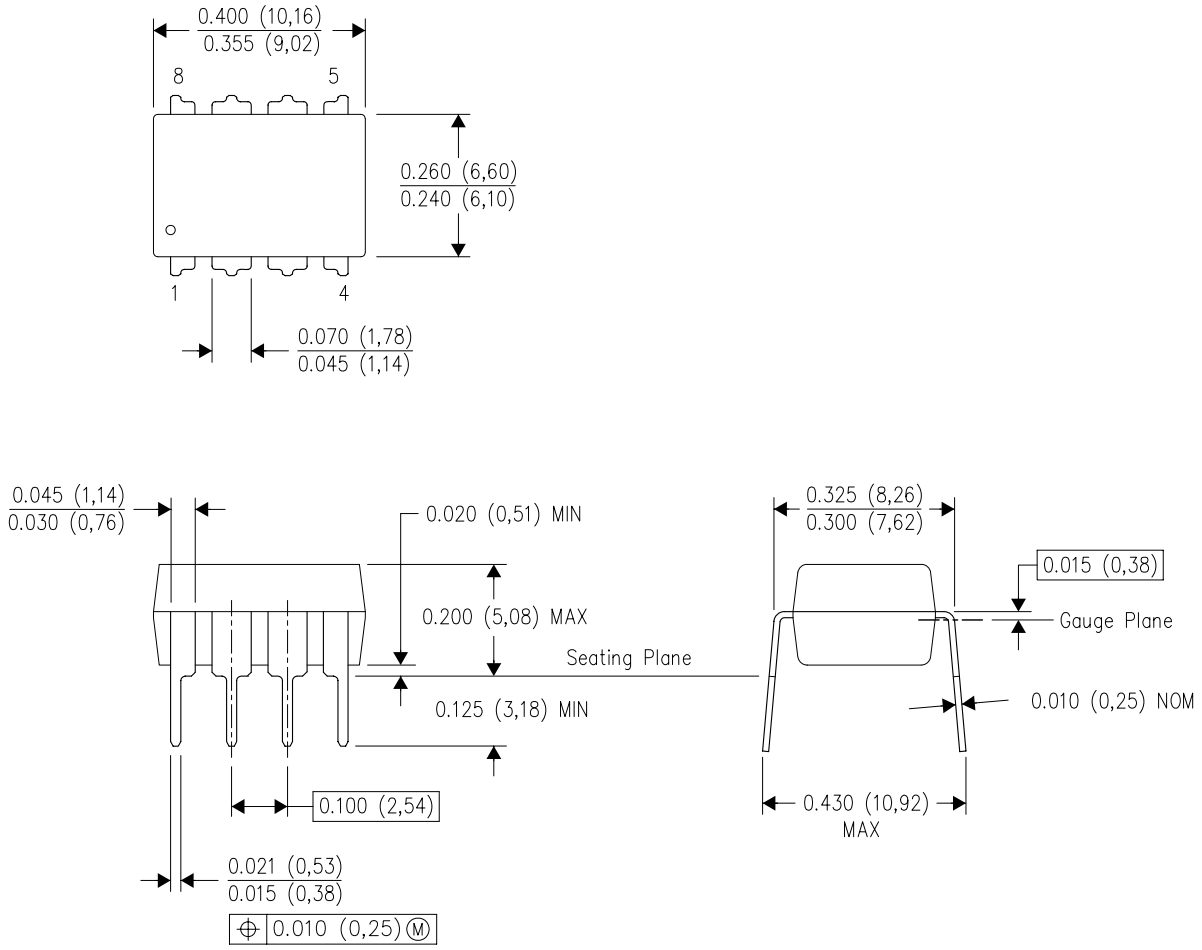
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

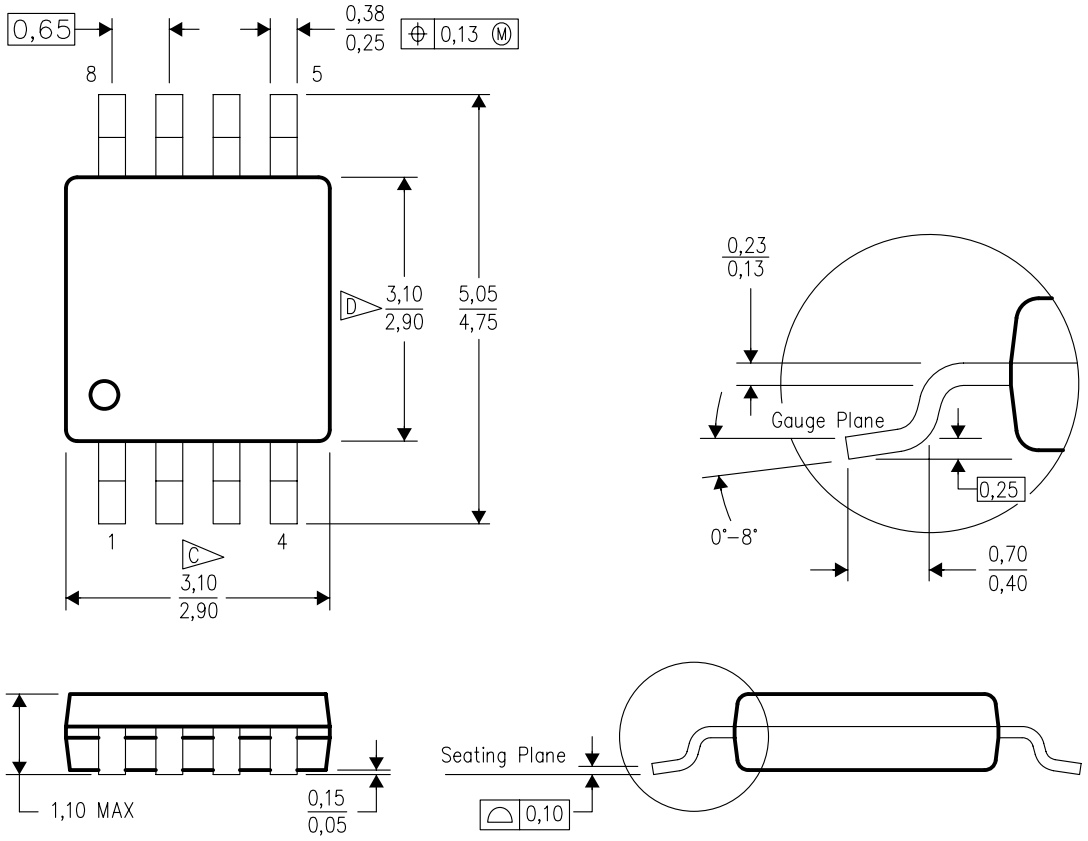
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7834E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
ADS7834EB/250	VSSOP	DGK	8	250	210.0	185.0	35.0
ADS7834EB/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

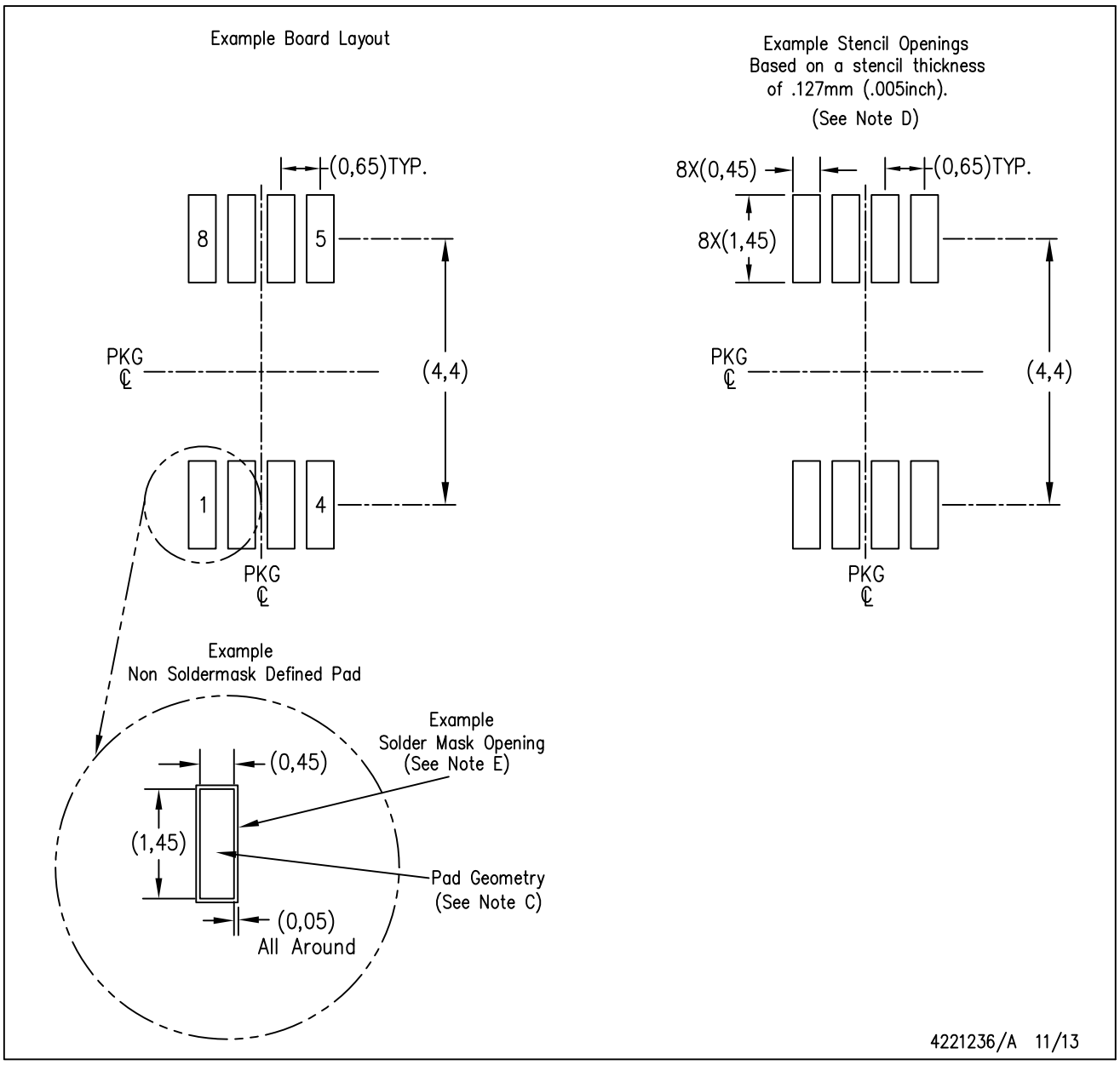
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
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C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
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