DIP 22

The SDA 2120 contains the complete digital section (reference oscillator, 20-bit shift register with memory, programmable divider, band select outputs as well as a phase detector, two charge pumps, one current multiplier, and two amplifiers) for tuning an AM/FM receiver by PLL frequency synthesis.

A serial interface facilitates connection to a microprocessor. The microprocessor will load the divider, the band select outputs, and the current multiplier with the suitable information.

Features

- Integrated prescaler
- Switch-selectable from AM to FM
- High frequency resolution FM = 12.5 kHz, AM = 0.5 kHz

Maximum ratings

Supply voltage	V_S	7.5	V
Tuning supply voltage	V_{SAM}/V_{SFM}	32	V
IFO, PLE, CPL	V_{iH}	5.5	V
Band select: UKW, SW, MW, LW	V_{BS}	18	V
AM, FM	$V_{AM/FM}$	5.5	V
F	V_F	5.5	V
Input current amplifier	I_{iV}	500	µA
Output current amplifier	$I_{DAM/FM}$	7	mA
Junction temperature	T_j	140	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	65	K/W

Operating range

Supply voltage	V_S	4.5 to 5.5	V
Ambient temperature range	T_{amb}	−25 to 85	°C
Resistance for charge pump current[1])	R_I	>100	kΩ
Input frequency input AM	f_{iAM}	10	MHz
Input frequency input FM	f_{iFM}	120	MHz
Prescaler factor LW/MW	$N_{LW/MW}$	2 / 16383	
Prescaler factor SW/UKW	$N_{SW/UKW}$	4097 / 16383	

1) Multiplication factor $M = 15$

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Characteristics ($V_S = 5$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Supply current	I_S		60		mA
L tuning voltage V_{tunAM}/V_{tunFM} ($I_{DL} = 2.5$ mA)	V_{DL}			0.5	V
H tuning voltage V_{tunAM} ($V_{S2} = 32$ V)	V_{tunHAM}	30			V
H tuning voltage V_{tunFM} ($V_{S2} = 32$ V)	V_{tunHFM}	30			V
Sensitivity input AM ($f = 10$ MHz)	V_{iAMrms}		10		mV
Sensitivity input FM ($f = 120$ MHz)	V_{iFMrms}		20		mV
Input resistance input AM ($f = 10$ MHz; $V_{IAMrms} = 100$ mV)	R_{iAM}		1		kΩ
Input resistance input FM ($f = 120$ MHz; $V_{IFMrms} = 100$ mV)	R_{iFM}		0.5		kΩ
Input capacitance, input AM/FM	C_i		4		pF
Inputs IFO, PLE, CPL					
Upper threshold voltage	V_{Su}	2.0[1]			V
Lower threshold voltage	V_{Sl}			0.8[1]	V
H input current	I_{iH}			8	μA
L input current	I_{iL}			−50	μA
BS outputs: UKW, SW, MW, LW					
($V_{pp} = 15$ V)	I_{qH}			10	μA
(0.5 V ≦ $V_{pp} = 15$ V)	I_{qL}	0.8	1.2	3.0	mA
Oscillator output F					
($I_{FH} = -100$ μA)	V_{qFH}	4.5			V
($I_{FL} = 100$ μA)	V_{qFL}			0.7	V
Residual ripple of the tuning voltage ($f = 0$–1 kHz, test bandwidth 10 Hz)	V_{tunAM}		5		μV
($f = 1$–50 kHz, test bandwidth 100 Hz)	V_{tunFM}		1		μV
Charge pump output current AM/FM ($R_I = 130$ kΩ, $M = 15$,	I_{qAI}		±500		μA
I_{qAI} tested against 2.5 V) tristate			±5		nA
Switching times					
IFO, PLE					
Set-up time for enable	t_{SE}	0.3			μs
Set-up time for data	t_{SD}	0.4			μs
Hold time for enable	t_{HE}	3			μs
Hold time for data	t_{HD}	3			μs
CPL					
H pulse width	t_{CH}	2			μs
L pulse width	t_{CL}	2			μs
F					
H pulse width	t_{FH}	200			ns
L pulse width	t_{FL}			300	ns
H/L transition time ($C_{L2} = 10$ pF)	t_{FHL}			20	ns
L/H transition time ($C_{L2} = 10$ pF)	t_{FLH}			50	ns

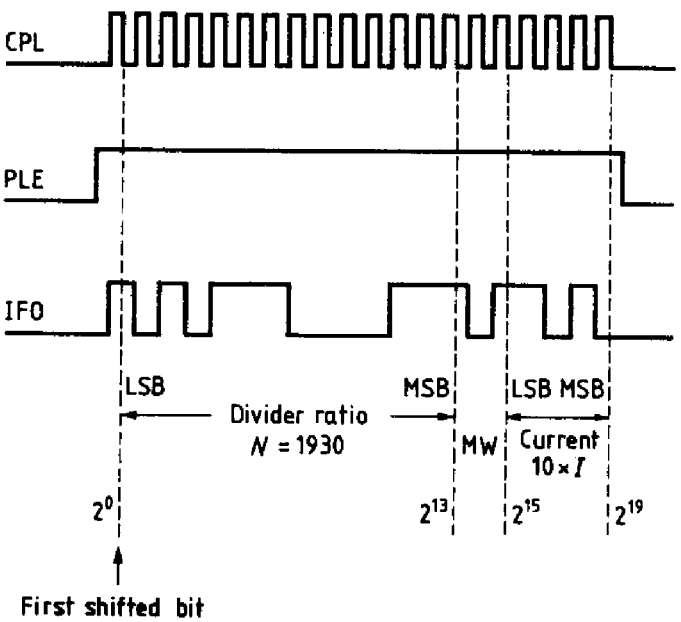
1) Values apply throughout the operational range.

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Truth table

Function	"IFO" bit 2^{14}	bit 2^{15}	Band select outputs LW	MW	SW	UKW	f_{ref}/kHz	Active input	Active output
LW	L	L	H	H	H	H	0.5	AM	AI AM
MW	L	H	H	L	H	H	0.5	AM	AI AM
SW	H	L	H	H	L	H	0.5	AM	AI AM
UKW	H	H	H	H	H	L	12.5	FM	AI FM

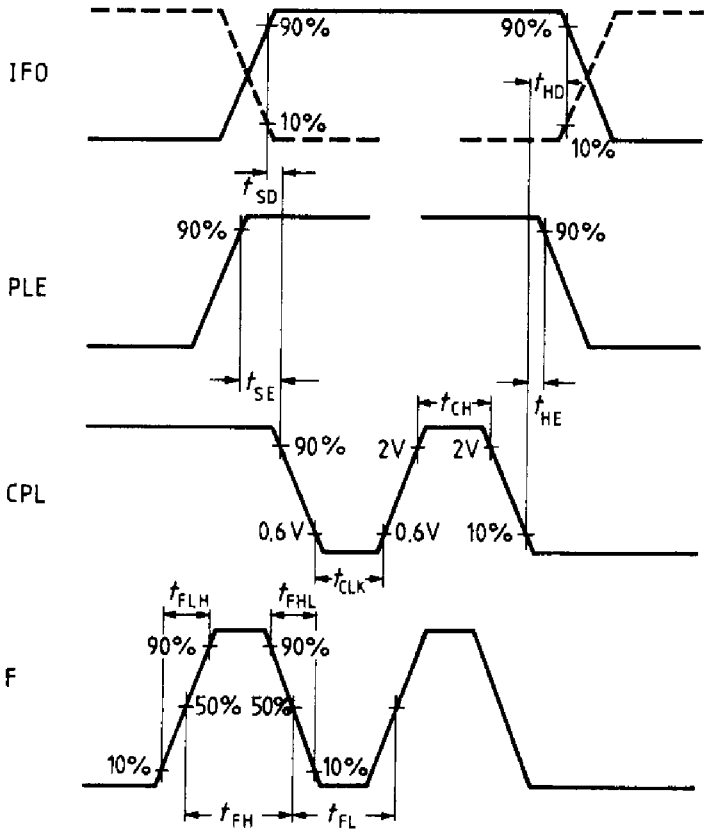
Pulse diagram



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Pulse diagram

Set-up and hold times



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Circuit description

The component contains a 14 bit programmable synchronous divider (% P, % M, % S), which divides the frequency of a signal pending at input AM, or FM resp. by the factor N=2...16383 (LW/MW), or N = 4097...16383 (SW/VHF). The buffered inputs AM and FM can be directly connected to the VCO via capacitors due to their own prevoltage generation.

The input sensitivity of the inputs is 10 mV_{rms} (AM) or 20 V_{rms} (FM). The frequency divider input can be switched optionally to AM or FM per software switch. While the LW/MW signal is divided into a pure synchronous divider, the SW/VHF signal is divided into a modulo two divider followed by a synchronous divider. The shift register with latch, with a depth of 20 bits, is divided into 14 bits to store the divider ratio N of the synchronous divider; 2 bits to control the four band select outputs (VHF, SW, MW, LW); 4 bits for the current multiplier to select the optimum current for the charge pump.

The divider ratio N, the band selection, as well as the information for the current multiplier are loaded into the 20 bit shift register via the serial data input IFO. First, the complement of the divider ratio, beginning with the least significant bit, is loaded in a binary encoded form. This is followed by the band select control bits SB0 und SB1 (refer to table), finished by the information bits for the current multiplier. During FM operation, they are loaded in binary encoded form beginning with the LSB, during which the bit sequence 0000 is not permissible. During AM operation, the complement of the information bit is loaded in binary encoded form beginning with the LSB, during which the bit sequence 1111 is not permissible. The information is loaded with the HL slope of the shift pulse CPL. Acceptance of the data at the IFO input can only take place during the H state of the enable input PLE. The 20 bit latch accepts the data from the shift register during the L state of the enable input PLE. The component is equipped with its own crystal-controlled 4 MHz pulse oscillator.

A square-wave signal of 2 MHz derived from the pulse oscillator is available at output F, which can be used for the synchronization of peripheral devices (e.g. microprocessor). The output F is to be connected to ground in order to provide a high signal-to-noise ratio. The oscillator output signal (f_{OSC} = 4 MHz) is divided down to 0.5 kHz or 12.5 kHz respectively, by a switch-selectable reference divider (reference signal). The reference divider is switched by the same signal that also switches the inputs. The divided input signal is compared with the reference signal in a digital phase detector. If the falling edge of the divided input signal appears prior to the falling edge of the reference signal, the DOWN output of the phase detector goes into the H state for the duration of the phase difference. In the opposite case, the output UP goes into the L state. If both signals are in phase, the DOWN output remains in the L state and output UP in the H state.

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The outputs UP/DOWN control the two current sources I^+ and I^- (charge pump). If output UP is in the L state, current source I^+ is activated; if output DOWN is in the H state, current source I^- is in effect. If DOWN is in the L state and UP is in the H state, the charge pump output changes into a high-ohmic state (TRI STATE). The current pulses generated by the charge pump are integrated with the aid of an active low pass (external FET op amp with *RC* circuitry). The DC output signal of the low pass is available at the FET op amp output and serves as tuning voltage for the VCO. If there are minor requirements to be met regarding the signal-to-noise ratio, an internal amplifier with a series-connected external darlington transistor can be used instead of the external FET op amp. The output stage of the internal amplifier comprises a transistor with open-collector output. The external collector resistor can then be connected to voltages up to 30 V. The output transistor is dimensioned such that a voltage drop of 0.5 V occurs at a 2.5 mA collector current.

The component contains two separate charge pumps and two separate amplifiers. Only one charge pump is active at a time. The switch-over is achieved by the same signal that also switches the AM/FM inputs. Thus, separate low passes can be set up for AM and FM. The output current of both charge pumps (source current = sink current) is $M \times I$. M is the multiplication factor that is given by the information bits for the current multiplier, M being an integer and $1 \leq M \leq 15$. I is the basic current of the charge pump that is set by means of an external resistor between pin I_{ref} and V_S. As the software monitors the current, a fast transient response of the PLL during band limit peaks and range changes (recharging the low pass) can be achieved, as well as a high signal-to-noise ratio in the steady state. The delay time between phase detector input and charge pump output is typically 20 ns. The phase detector with charge pump gain depends on the selected charge pump output current and is calculated as follows:

$$K_D = \frac{2\,I}{4\,\pi}\left[\frac{\mu A}{rad}\right].$$

The wiring of the charge pump output AI has to ensure that the DC voltage value at the output varies only between 1.2 V and 3.8 V (e.g. by applying a reference voltage of approx. 2.5 V when using the external operational amplifier. The band select outputs contain current drains (I_{qL} = 0.8 to 3.0 mA) with open collectors, in order to be able to switch voltages greater than the supply voltage of the component (5 V). Thus the transistors, operating as band select switches, can be directly driven without current limiting resistors (refer to application circuit).

During operation, pin 2 (N.C.) must be connected to ground.

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Supplements to the circuit description

Relationship between IFO bits of current multiplier and multiplication factor for the output current of the charge pump.

IFO BIT				Multiplication factor *M* FM	Multiplication factor *M* AM
2^{16}	2^{17}	2^{18}	2^{19}		
L	L	L	L	0	15
H	L	L	L	1	14
L	H	L	L	2	13
H	H	L	L	3	12
L	L	H	L	4	11
H	L	H	L	5	10
L	H	H	L	6	9
H	H	H	L	7	8
L	L	L	H	8	7
H	L	L	H	9	6
L	H	L	H	10	5
H	H	L	H	11	4
L	L	H	H	12	3
H	L	H	H	13	2
L	H	H	H	14	1
H	H	H	H	15	0

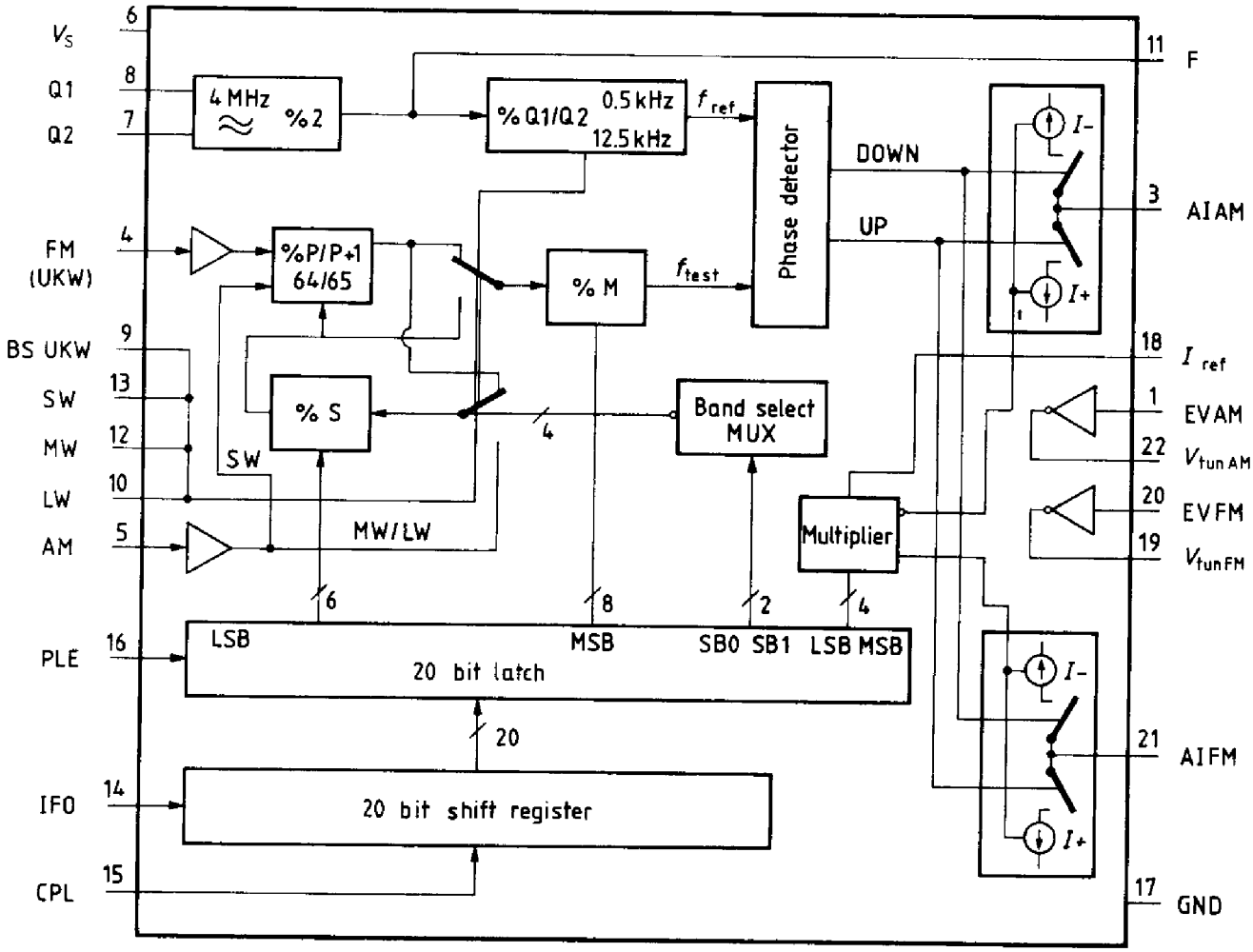
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Pin configuration

Pin No.	Symbol	Function
1	EV AM	Amplifier input AM
2		N.C.
3	AI AM	Charge pump output AM
4	FM	Signal input VHF
5	AM	Signal input SW/MW/LW
6	V_S	Supply voltage
7	Q2	Crystal
8	Q1	Crystal
9	UKW	Band select output VHF
10	LW	Band select output LW
11	F	Oscillator output
12	MW	Band select output MW
13	SW	Band select output SW
14	IFO	Data input
15	CPL	Shift register input
16	PLE	Enable input for shift register
17	GND	Ground
18	I_{ref}	Current adjustment for charge pump
19	$V_{tun\,FM}$	Tuning voltage FM
10	EV FM	Amplifier input FM
21	AI FM	Charge pump output FM
22	$V_{tun\,AM}$	Tuning voltage AM

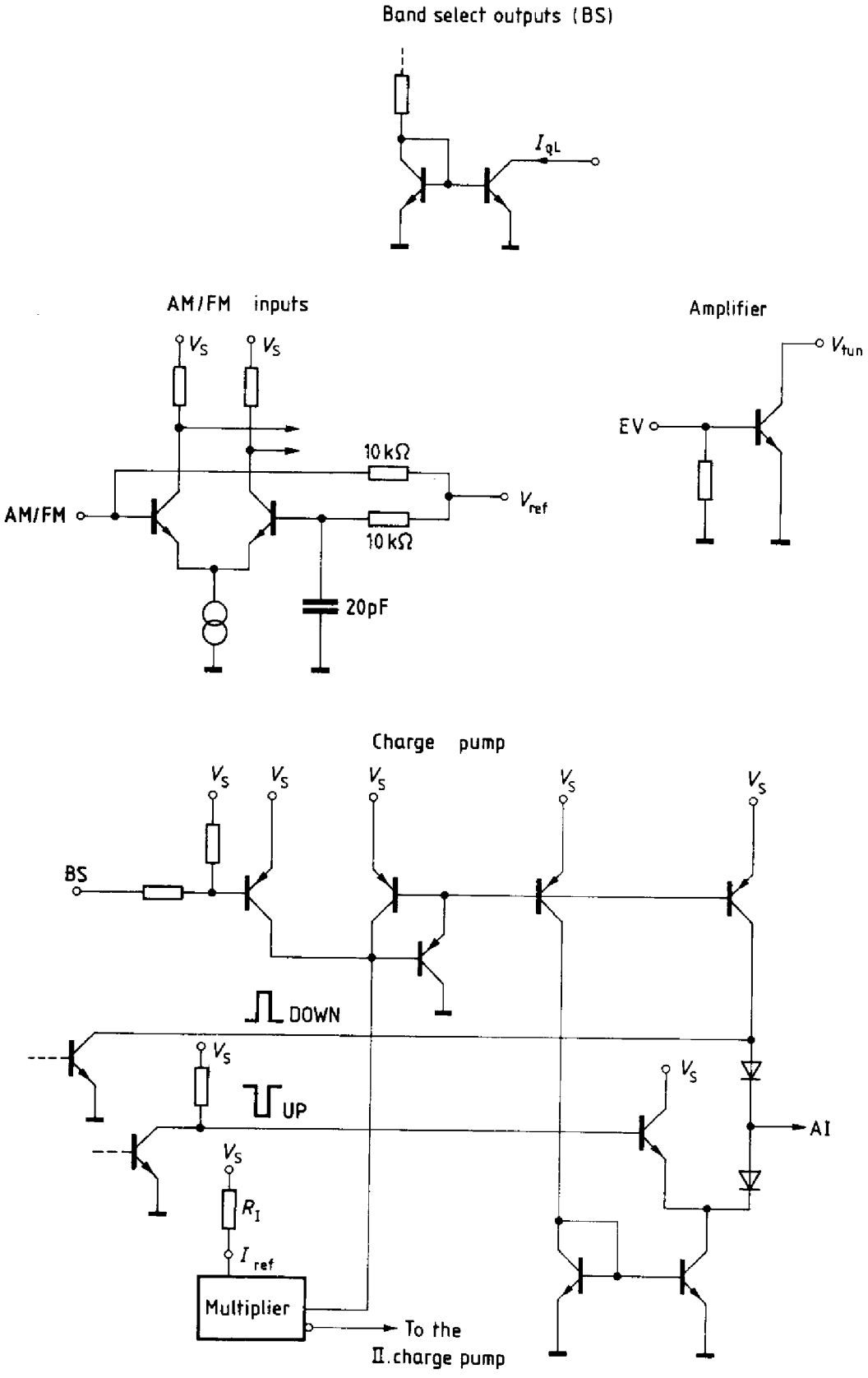
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Block diagram



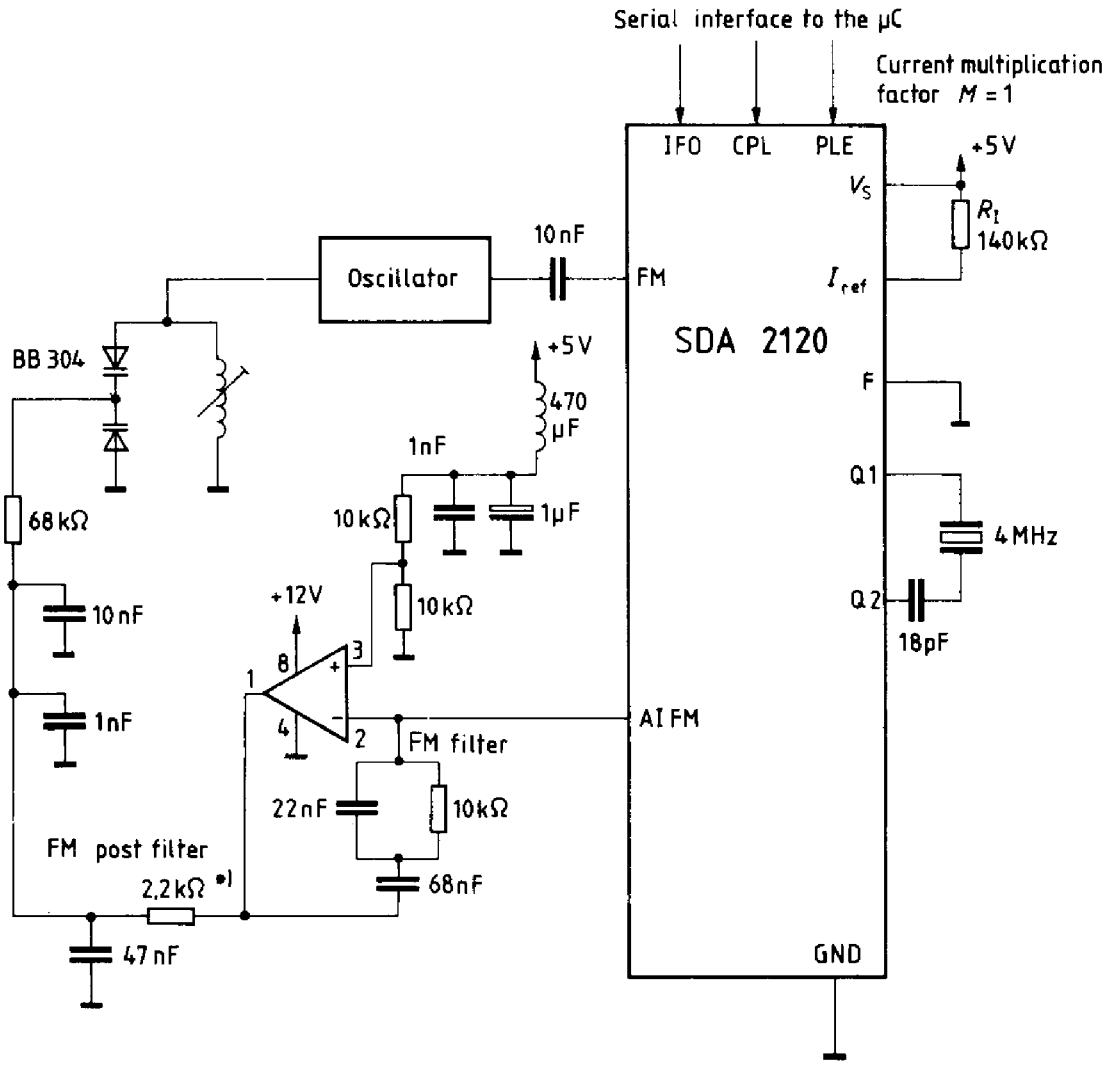
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Circuitry of inputs and outputs (schematic)



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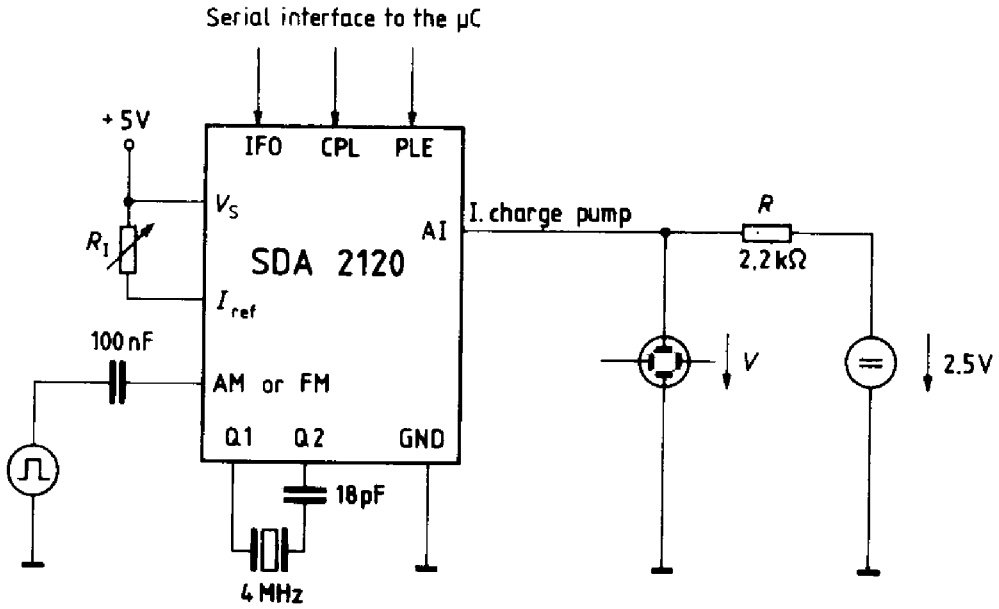
Test circuit for residual ripple of the FM tuning voltage



*) The mentioned filter constants are only approximate values. They have to be matched to the actual tuner by the user.

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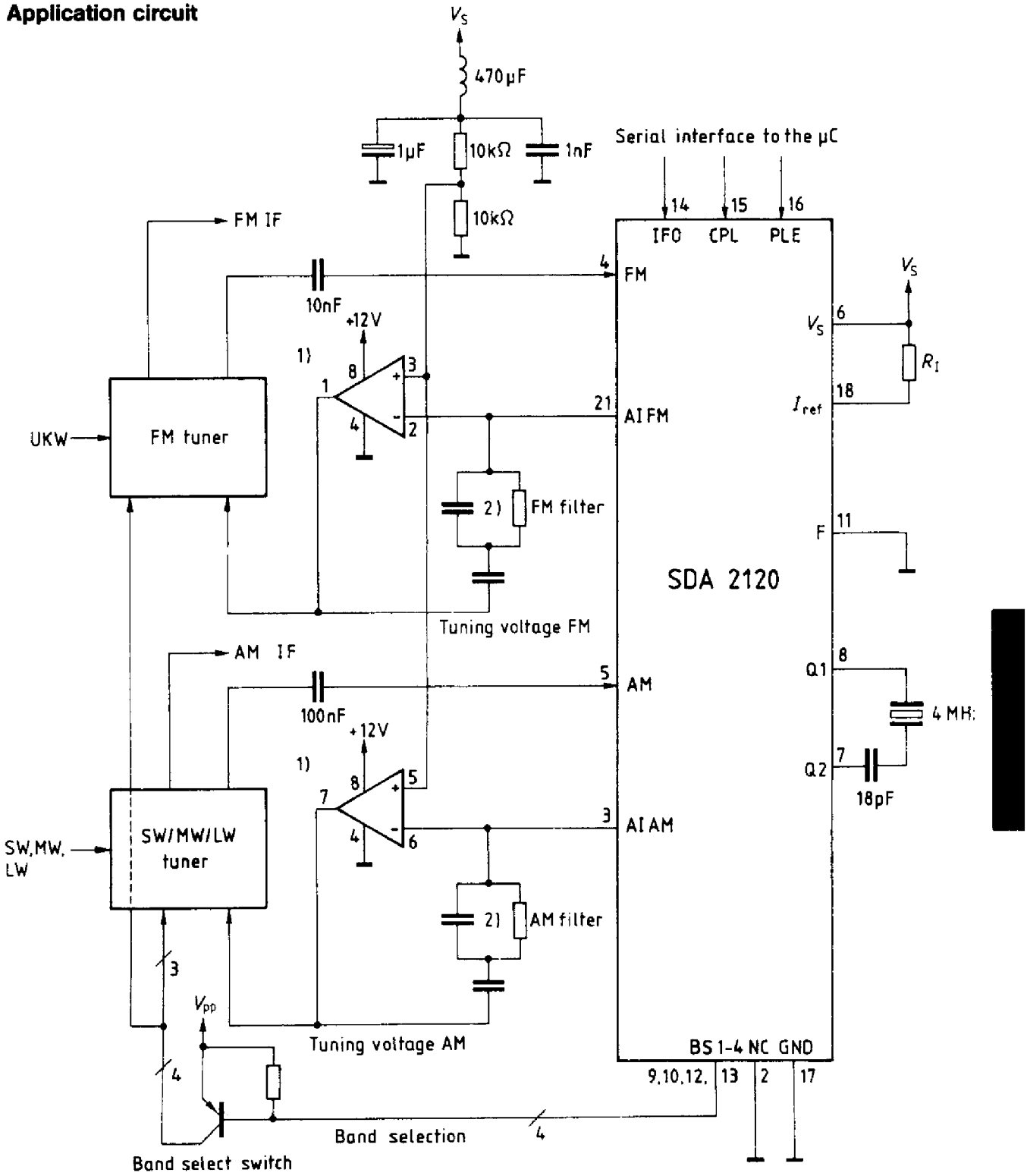
Test circuit for charge pump output current



To activate the "charge pump", there must be a difference between the frequency of the AM/FM inputs and the frequency of the µC.

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Application circuit



1) Double FET operating amplifier: MC 34002, CA 3240, TL 082, LF 353 or similar types.
2) The filter values must be matched to the actual tuner by the user.

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