SONY **CXD1088AQ**

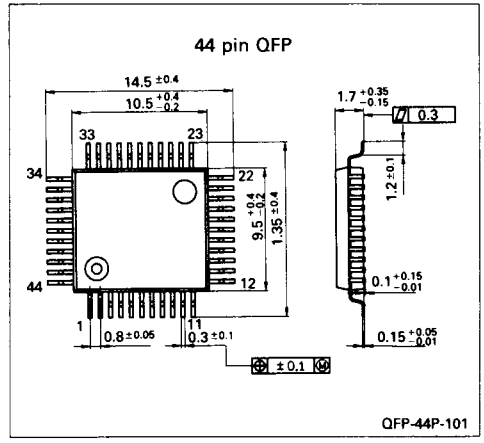
Over Sampling Digital Filter LSI

Description

CXD1088AQ is a digital filter LSI with quadrupled sampling rate, developed for compact disc player.

Package Outline

Unit: mm



Features

- 83rd and 21st order filters linked through cascade connections provide a quadrupled sampling digital filter
- Built-in filters for 2 channels corresponding to L and R
- Variety of functions including soft-muting and offset addition
- 83rd and 21st order filters also have 2 modes of filter coefficients each, to enable the selection of the most suitable filter characteristics, required for usage.

Functions

- Filters for two channels
- Filtering with a quadrupled sampling rate
- Two-stage FIR filters interconnected in cascade (83rd order+21st order)
- 18-bit serial output possible
- Switching between serial and parallel output modes
- ±1% offset addition
- Soft-muting function
- Independent linear error correction for either L or R, up to 8 words
- 2 modes of coefficients provided for both 83rd and 21st orders (refer to "Filter Characteristics")
- Input/output format
  - Input: 2's complement; MSB first (serial)
  - Output: 2's complement; MSB first (serial)
    Offset binary (parallel)

Structure

Silicon gate CMOS IC

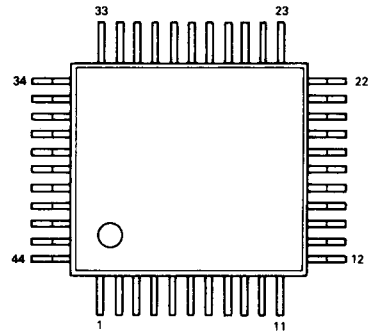
Absolute Maximum Ratings (Ta=−25 to +75°C)

• Supply voltage	V_{DD}	−0.5 to +6.5	V
• Input voltage	V_I	−0.5 to V_{DD} +0.5	V
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	450 (Ta=75°C)	mW

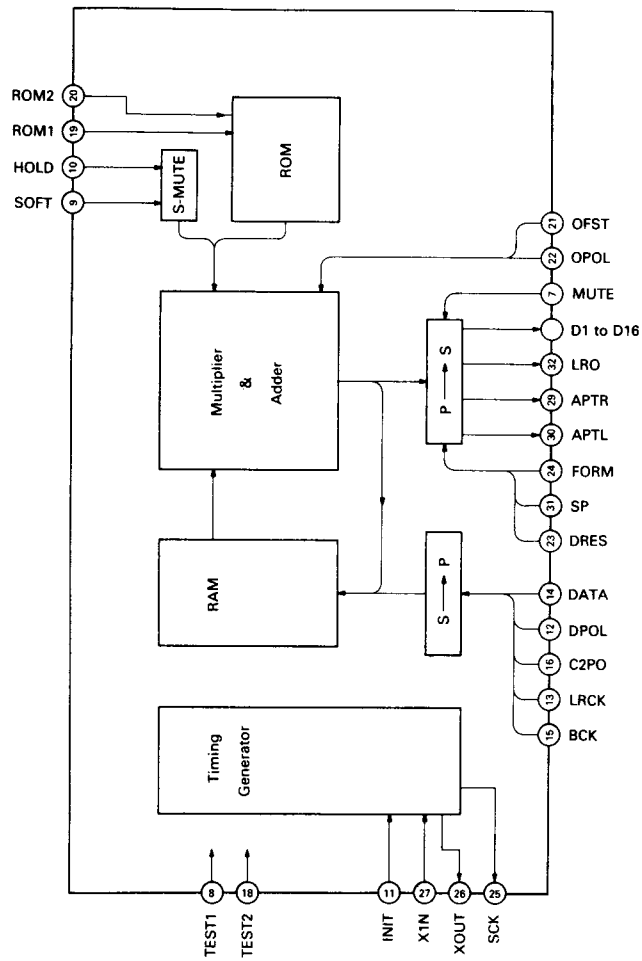
Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr.	−20 to +75	°C
• OSC frequency	fx	10 to 20	MHz

Pin Configuration (Top View)



Block Diagram



Pin Description

No.	Symbol	I/O	Description
1 to 5	D_{12} to D_{16}	O	D_{12} to D_{16} output pins when the parallel output mode is selected; fixed at "L" level when the serial output mode is selected.
6	Vss	–	Negative power supply (0V).
7	MUTE	I	Mutes the output to "0" or an offset value; active at "H" level.
8	TEST1	I	Test pin; normally, fixed at "L" level
9	SOFT	I	Soft muting ON/OFF switch; ON at "H" level
10	HOLD	I	Stops soft muting at "H" level
11	INIT	I	Power-on-Reset input pin; active at "L" level
12	DPOL	I	Reverses the polarity of input data
13	LRCK	I	LRCK input pin
14	DATA	I	"16 bits×2" serial data input pin; 2's complement
15	BCK	I	BCK input pin
16	C2PO	I	Error flag input pin
17	V_{DD}	–	Positive power supply (+5V)
18	TEST2	I	Test pin; normally, fixed at "L" level.
19	ROM1	I	ROM switching for 83rd order (Refer to "Filter Characteristics.")
20	ROM2	I	ROM switching for 21st order (Refer to "Filter Characteristics.")
21	OFST	I	Adds an offset to the output; active at "H" level.
22	OPOL	I	Specifies the polarity of offset values; "H": +1%; "L": −1%
23	DRES	I	Indicates the word length of data for SONY format serial output; "H": 18bits; "L": 16bits.
24	FORM	I	Specifies the output format; "H": I^2S; "L": SONY
25	SCK	O	System clock output for external IC; (384fs)
26	XOUT	O	Output pin of crystal oscillation circuit; (384fs)
27	XIN	I	Input pin of crystal oscillation circuit; (384fs)
28	Vss	–	Negative power supply (0V)
29	APTR	O	Aperture clock for R channel
30	APTL	O	Aperture clock for R channel
31	SP	I	Switches serial/parallel output modes; "H": parallel; "L": serial.
32	LRO	O	LRCK output (4fs)
33	D_1	O	D_1 (MSB) output pin when the parallel output mode is selected; BCK (4fs) output pin when the serial output mode is selected.
34	D_2	O	D_2 output pin when the parallel output mode is selected; DATA (4fs) output pin when the serial output mode is selected.
35	D_3	O	D_3 output pin when the parallel output mode is selected; LRCK (I^2 mode) or WCK (SONY mode) output pin when the serial output mode is selected.
36 to 38	D_4 to D_6	O	D_4 to D_6 output pins when the parallel output mode is selected; fixed at "L" level when the serial output mode is selected.
39	V_{DD}	–	Positive power supply (+5V)
40 to 44	D_7 to D_{11}	O	D_7 to D_{11} output pins when the parallel output mode is selected; fixed at "L" level when the serial output mode is selected.

Electrical Characteristics

DC characteristics

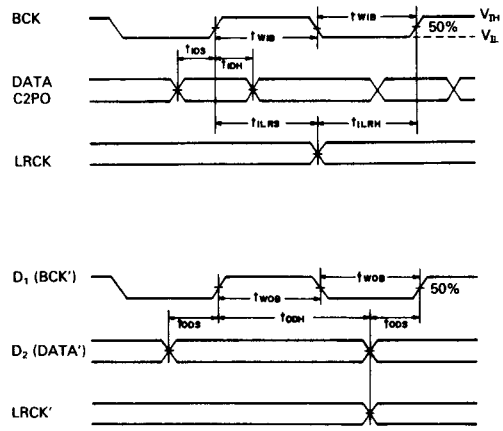
V_{DD}=4.5 to 5.5V, Ta=−20 to +75°C

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
27	Input leak current	I_{LI}	V_I=V_{DD}/0V	–	–	±20	μA
7,9,10 to 16, 19 to 24,31	"H" input voltage	V_{IH}	–	0.76V_{DD}	–	–	V
	"L" input voltage	V_{IL}	–	–	–	0.24V_{DD}	V
	Input leak current	I_{LI}	V_I=V_{DD}/0V	–	–	±5	μA
29,30,32 to 35	"H" output voltage	V_{OH}	I_O=−4mA	V_{DD}−0.5	–	–	V
	"L" output voltage	V_{OL}	I_O=4mA	–	–	0.4	V
2 to 5, 36 to 38, 40, 44	"H" output voltage	V_{OH}	I_O=−1mA	V_{DD}−0.5	–	–	V
	"L" output voltage	V_{OH}	I_O=1mA	–	–	0.4	V
25	"H" output voltage	V_{OH}	I_O=−5mA	V_{DD}−1.0	–	–	V
	"L" output voltage	V_{OL}	I_O=5mA	–	–	1.0	V
	Current consumption	I_{DD}	Under no load: V_I=V_{DD}/0V, fx=16.93MHz	–	–	40	mA

AC characteristics

V_{DD}=4.5 to 5.5V, Ta= −20 to +75°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillating frequency	fxt		–	16.9344	20.0	MHz
Input BCK frequency	f_{BCK}		–	–	3.1	MHz
Input BCK pulse width	t_{WIB}		100	–	–	ns
Input data set-up time	t_{IDS}		20	–	–	ns
Input data hold time	t_{IDH}		20	–	–	ns
Input LRCK set-up time	t_{ILRS}		50	–	–	ns
Input LRCK hold time	t_{ILRH}		50	–	–	ns
Output BCK pulse width	t_{WOB}	I^2S serial output mode f_{XT}=16.9344MHz C_L=50pF	70	–	–	ns
Output data set-up time	t_{ODS}		40	–	–	ns
Output data hold time	t_{ODH}		40	–	–	ns



Functions

Soft muting

Mutes or de-mutes output data within approximately 23ms (1024/fs). The output level can be held during muting operation.

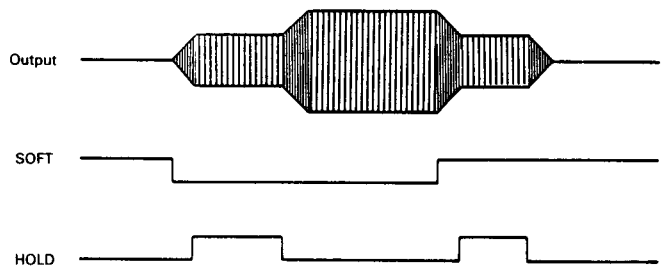


Fig. 1

Offset

Adds an offset to the output data. The offset amount can be positive or negative.

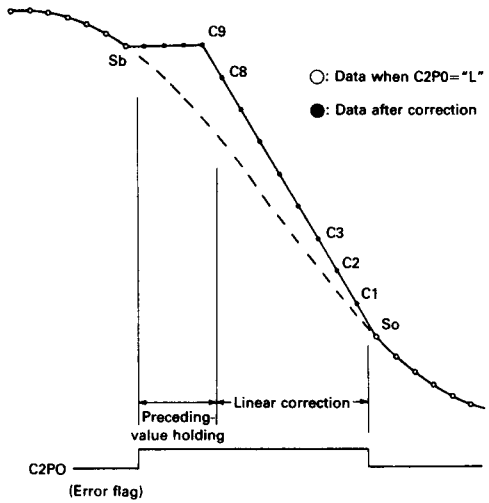
Table 1

OFST	OPOL	Offset amount
L	–	0%
H	L	−1%
H	H	+1%

Muting
When MUTE goes high or INIT goes low, the output is muted. An offset value which has been set following Table 1 above is output.

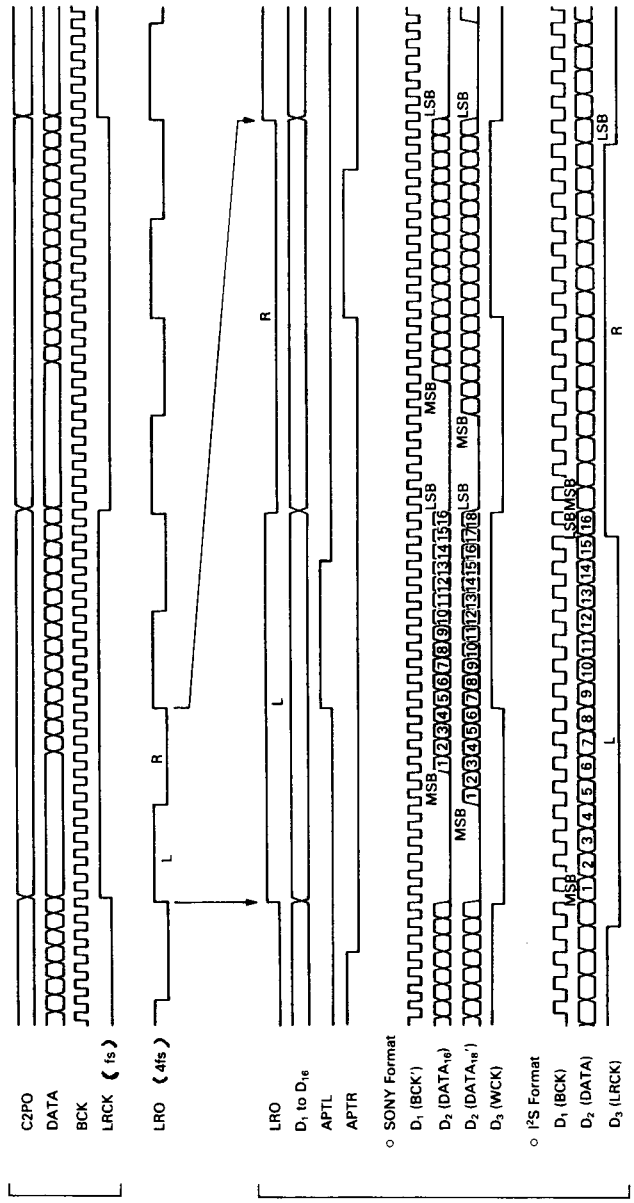
Data polarity
Allows switching between inversion and non-inversion of output data polarity.
When DPOL level is "L": the output data is not inversed with respect to the input data.
When DPOL level is "H": the output data is inversed with respect to the input data.

Error correction
Errors in an input data block consisting of up to eight consecutive data units can be linearly corrected by the two correct data units, the one preceding the erroneous block and the other following it. (This is done separately for L and R.) For errors of more than eight consecutive input data units, only the last eight data are linearly corrected, and all preceding data units are maintained without correction.

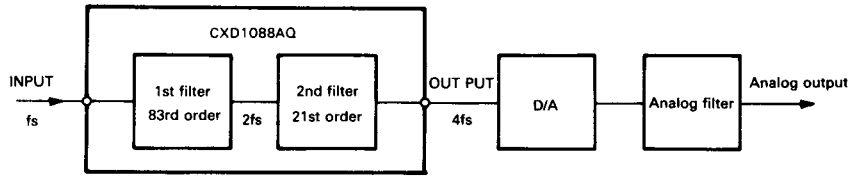


Input and output
1) Input
The changeover point of MSB first serial data (fs) of 2's complement represents the switching of LRCK. Of this data string, only the data of the last 16-bit clock (BCK) are valid.
When INIT="L" (resetting), the input data are invalid and the input is equivalent to ALL "0."
2) Output
SP="L": MSB first serial data (4fs) of 2's complement
SP="H": offset binary parallel data (4fs)
Clock pulses such as LRO and BCK are constantly output as long as the power is on. Data are output only when resetting is canceled (INIT="H") when MUTE="L." Otherwise, muting remains effective.

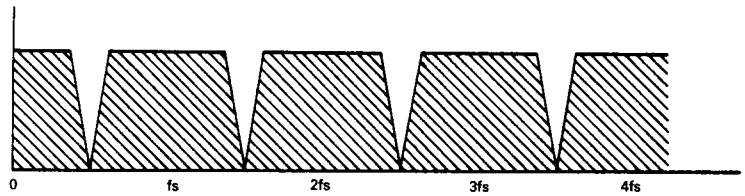
I/O Timing Chart



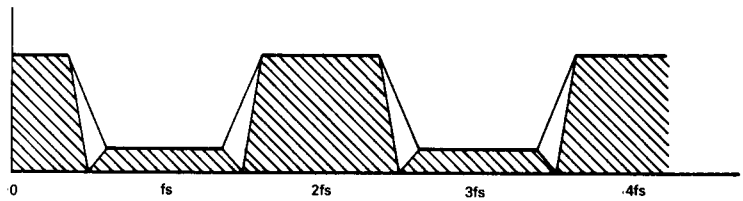
Filter Characteristics



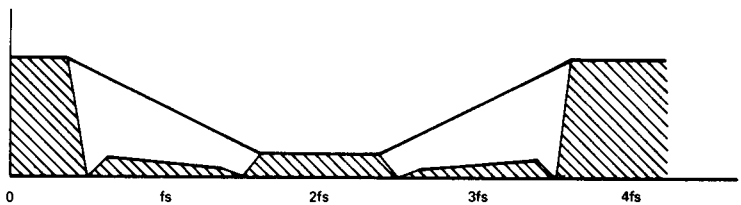
Input spectrum



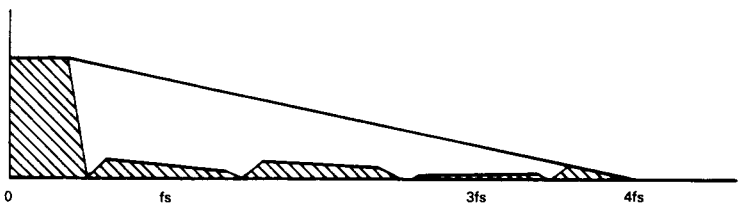
Characteristics of 1st filter



Characteristics of 2nd filter

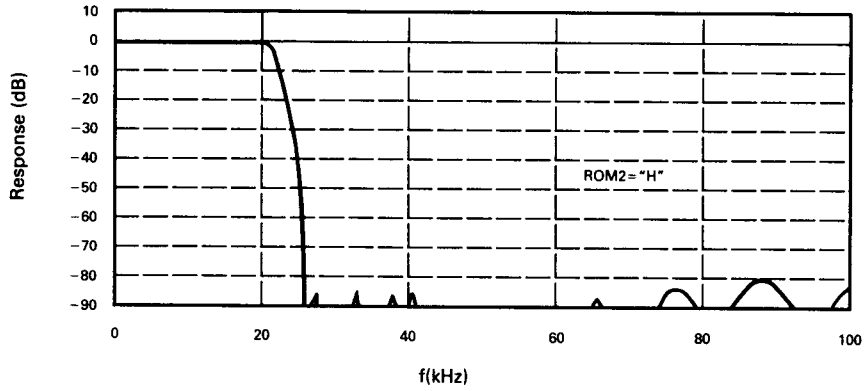


Charcteristics of analog filter

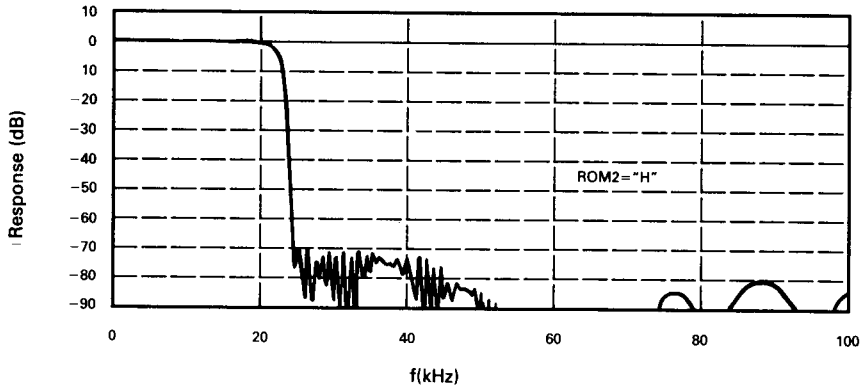


Combined Filter Characteristics (1st filter + 2nd filter)

1) ROM1="H"
Stop band attenuation: 80dB Min. (over 25.7kHz)
Pass band ripple: ±0.001dB Max.



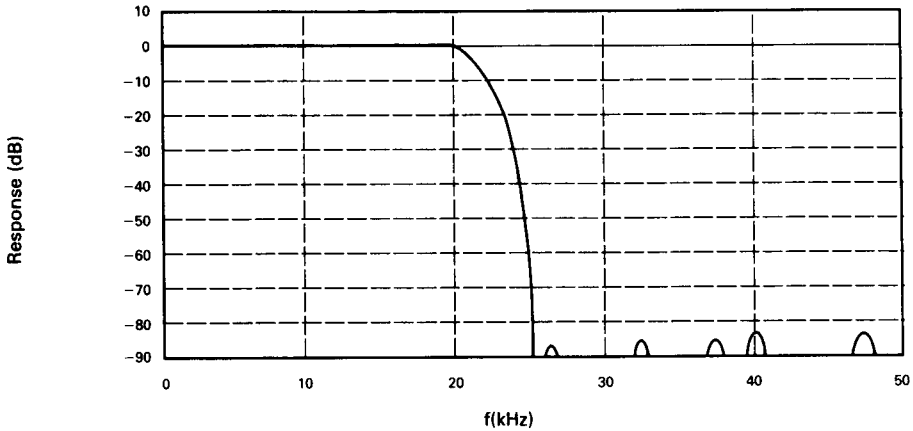
2) ROM1="L"
Stop band attenuation: 60dB Min. (24.1kHz); 65dB Min. (over 24.2kHz)
Pass band ripple: ±0.004dB Max.



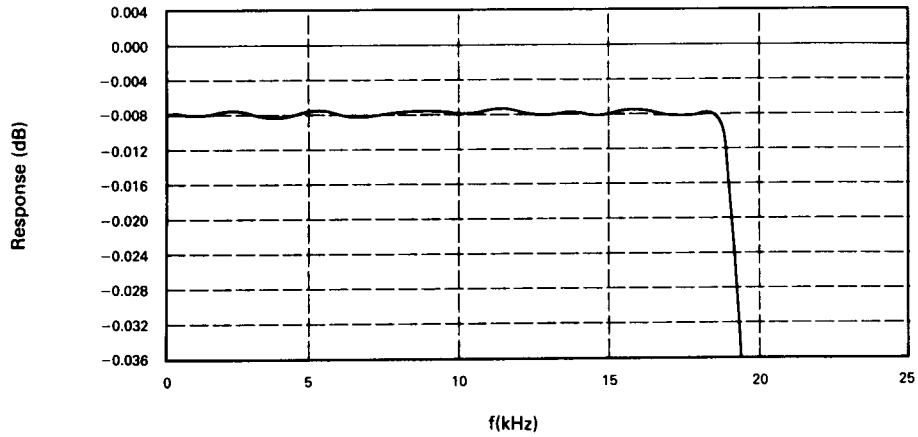
Filter Characteristics-1

1st Filter (83rd order, ROM1="H")

Frequency characteristics of filter



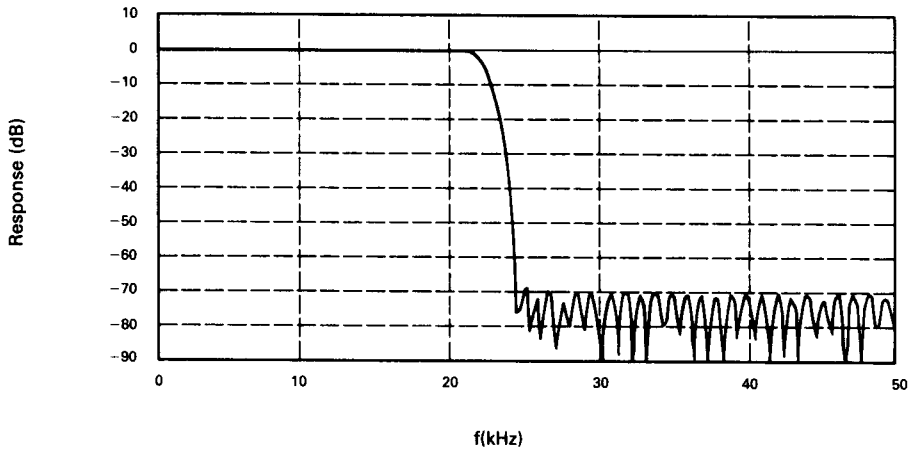
Ripple characteristics in pass band



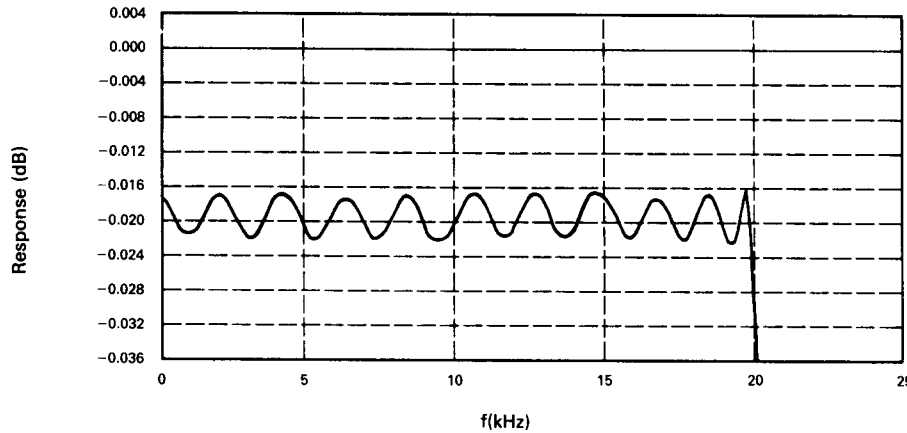
Filter Characteristics-2

1st Filter (83rd order, ROM1="L")

Frequency characteristics of filter



Ripple characteristics in pass band

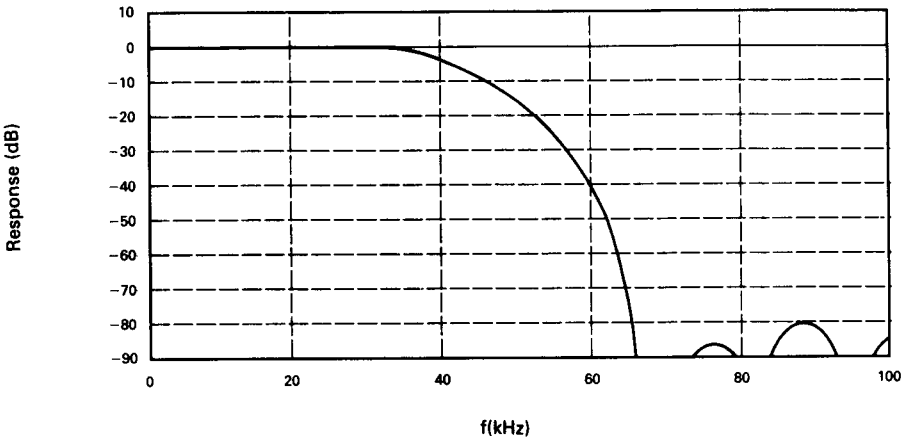


Filter Characteristics-3

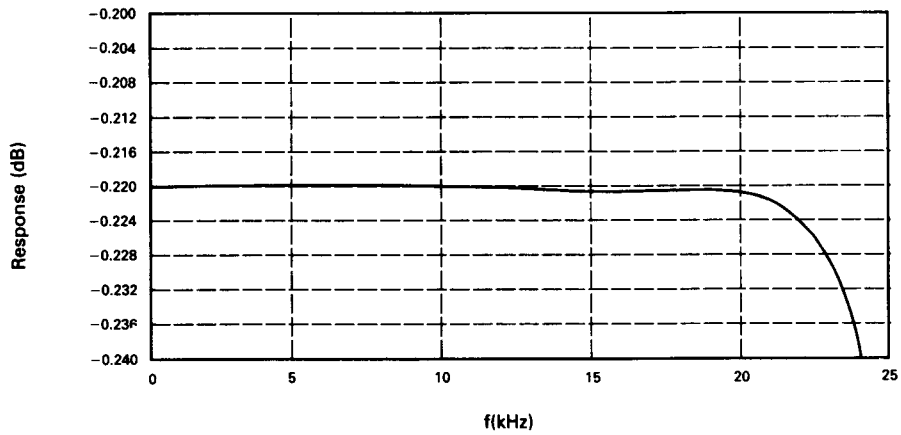
2nd Filter (21st order, ROM2="H")

- Marked flatness in pass band (without frequency characteristics compensation)

Frequency characteristics of filter



Ripple characteristics in pass band

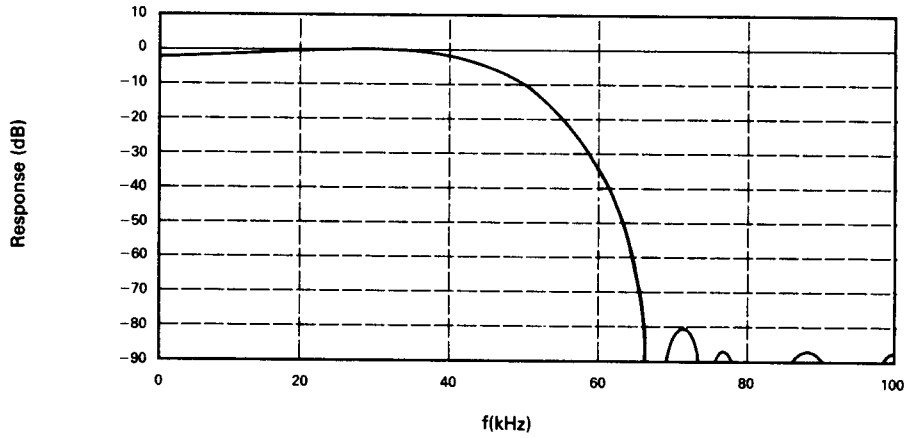


Filter Characteristics-4

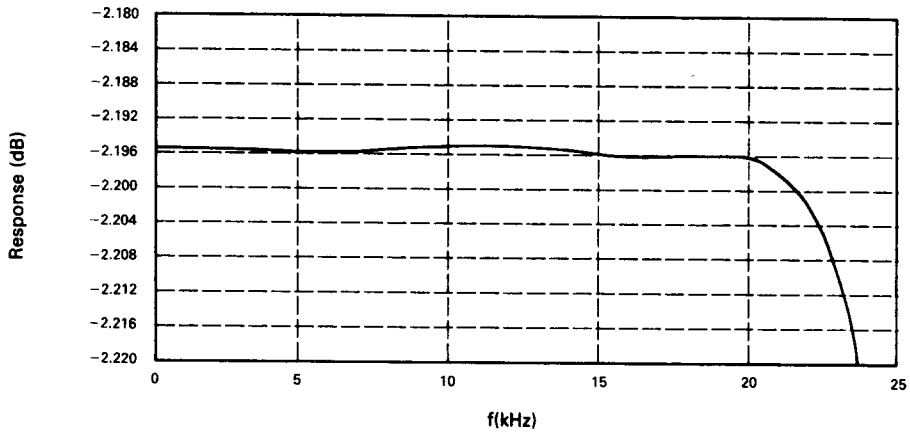
2nd Filter (21st order, ROM2="L")

- Pass band frequency characteristics (compensation of aperture effect of analog third order Bessel filter characteristics)

Frequency characteristics of filter

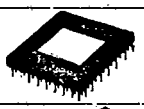
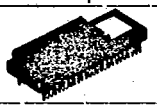


Ripple characteristics in pass band
(Excluding frequency characteristics compensation)



T-90-20

Sony Package Product Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN LINE PACKAGE		P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	4-direction
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT PACKAGE		P	1.0mm 0.8mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull Wing	2-direction
	Standard chip carrier	PLCC	PLASTIC LEADED CHIP CARRIER		P	1.27mm (50MIL)	J-bend	4-direction
		LCC	LEAD LESS CHIP CARRIER		C	1.27mm (50MIL)	Lead less	Package side
	Shrink chip carrier	SPLCC (PLCC)	SHRINK PLASTIC LEADED CHIP CARRIER		P	1.27mm Max. (50MIL Max.)	J-bend	4-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEAD PACKAGE		P	1.27mm (50MIL)	J-bend	2-direction

*P……Plastic, C……Ceramic