Atmel

ATA664151

LIN System Basis Chip with LIN Transceiver, 5V Regulator, Watchdog, 8-channel High Voltage Switch Interface with High Voltage Current Sources, 16-bit SPI

DATASHEET

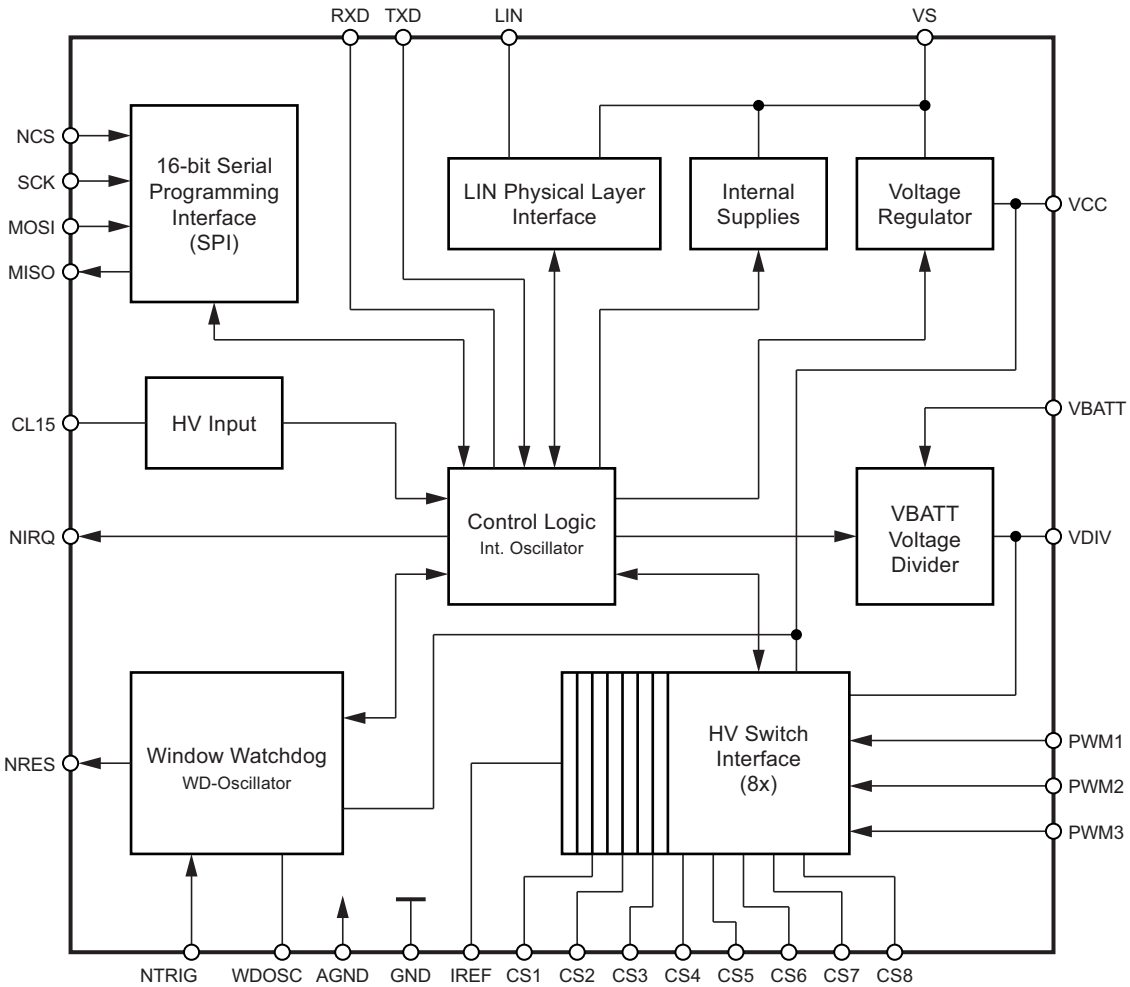
Features

- 8-channel HV switch interface with HV current sources
- Linear low-drop voltage regulator, up to 80mA current capability, V_{CC} = 5.0V ±2%
- Fulfills the OEM “Hardware Requirements for LIN in Automotive Applications Rev.1.3”
- LIN master and slave operation possible
- Supply voltage up to 40V
- Operating voltage V_S = 5V to 27V
- Internal voltage divider for $V_{Battery}$ sensing (±2%)
- 16-bit serial interface (daisy-chain-capable) for configuration and diagnosis
- Typically 8µA supply current during sleep mode
- Typically 35µA supply current in active low-power mode
- VCC-undervoltage detection (4ms reset time) and watchdog reset logical combined at NRES open drain output
- LIN high-speed mode up to 200kBit/s
- Adjustable watchdog timer via external resistor
- Negative trigger input for watchdog
- LIN physical layer complies with LIN 2.1 specification and SAE J2602-2
- Wake-up capability via LIN bus and CL15
- Bus pin is overtemperature and short-circuit protected versus GND and battery
- Advanced EMC and ESD performance
- Package: QFN32 5x5mm

1. Description

The Atmel® ATA664151 is a system basis chip with an eight-channel high voltage switch interface, a LIN 2.1 and SAEJ2602-2-compliant LIN transceiver, low-drop voltage regulator, and an adjustable window watchdog. The Atmel ATA664151 provides 5V output voltage with up to 80mA current capability. This chip combination makes it possible to develop inexpensive, simple, yet powerful slave and master nodes for LIN bus systems. The Atmel ATA664151 is especially designed for LIN switch applications and includes almost the entire LIN node. They are designed to handle low data-rate communication in vehicles (such as in convenience electronics). Improved slope control at the LIN driver ensures secure data communication up to 20kBaud. Sleep Mode and Active Low-power Mode guarantee minimal current consumption even in the case of a floating bus line or a short circuit on the LIN bus to GND.

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning QFN32, 5x5mm

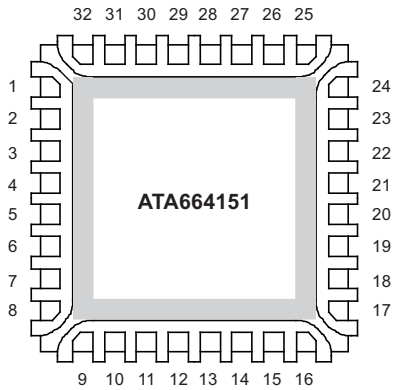


Table 2-1. Pinning

Pin	Name	Function
1	TXD	LIN-bus logic data in from microcontroller
2	RXD	LIN-bus logic data out to microcontroller
3	NRES	Watchdog and VCC undervoltage Reset Output pin (active low, open drain)
4	NIRQ	Interrupt request output to microcontroller (active low, open drain)
5	MISO	SPI Master-In-Slave-Out output pin to microcontroller
6	MOSI	SPI Master-Out-Slave-In input pin from microcontroller
7	SCK	SPI clock input from microcontroller
8	NCS	SPI chip select logic input from microcontroller (active low)
9	PWM1	PWM control input port from microcontroller for first CS pin group
10	PWM2	PWM control input port from microcontroller for second CS pin group
11	PWM3	PWM control input port from microcontroller for third CS pin group
12	WDOSC	Connection for external resistor to set watchdog frequency
13	VDIV	Voltage divider output / watchdog disable input pin
14	IREF	Reference current adjustment pin
15	CS1	High-voltage current sink/source and switch I/O pin no. 1
16	CS2	High-voltage current sink/source and switch I/O pin no. 2
17	CS3	High-voltage current sink/source and switch I/O pin no. 3
18	CL15	Wake-up on ignition high-voltage input pin
19	VBATT	Battery voltage input for voltage divider
20	GND	Ground connection
21	LIN	LIN-bus connection

Table 2-1. Pinning (Continued)

Pin	Name	Function
22	GND	Ground connection
23	GND	Ground connection
24	CS4	High-voltage current source and switch I/O pin no. 4
25	CS5	High-voltage current source and switch I/O pin no. 5
26	CS6	High-voltage current source and switch I/O pin no. 6
27	CS7	High-voltage current source and switch I/O pin no. 7
28	CS8	High-voltage current source and switch I/O pin no. 8
29	VS	Supply input pin
30	AGND	Analog reference ground
31	VCC	5V Voltage regulator output pin
32	NTRIG	Watchdog trigger input from microcontroller
Backside	GND	Back Side Heat Slug, internally connected to GND

3. Pin and Functional Description

3.1 Physical Layer Compatibility

Since the LIN physical layer is independent of higher LIN layers (such as the LIN protocol layer), all nodes with a LIN physical layer as per release version 2.1 can be mixed with LIN physical layer nodes found in older versions (i.e., LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3, LIN 2.0), without any restrictions.

3.2 Supply Pin (VS)

The operating voltage is V_S = 5V to 27V. An undervoltage detection is implemented to disable data transmission via the LIN bus and the switch interface if V_{VS} falls below V_{VSth} in order to avoid false bus messages. After switching on VS, the IC starts in active mode (see also Section 4.1 “Active Mode” on page 9), with the VCC voltage regulator and the window watchdog switched on (the latter depends on the VDIV pin, see Section 10. “Watchdog” on page 28).

3.3 Ground Pins GND and AGND

The IC is neutral on the LIN pin in the event of GND disconnection. It can handle a ground shift of up to 11.5% of VS.

Note: Please note that pin AGND is used for internal reference generation. This should be considered when designing the PCB in order to minimize the effect on the voltage thresholds.

3.4 Voltage Regulator Output Pin (VCC)

The internal 5V voltage regulator is capable of driving loads up to 80mA for supplying the microcontroller and other loads on the PCB. It is protected against overloads by means of current limitation and overtemperature shutdown. In addition, the output voltage is monitored and will cause a reset signal at the NRES output pin if it drops below a defined threshold $V_{VCCthun}$.

A safe operating area (SOA) is defined for the voltage regulator, because the power dissipation caused by this block might exceed the system’s thermal budget.

3.5 Bus Pin (LIN)

A low-side driver with internal current limitation, thermal shutdown and an internal pull-up resistor in compliance with the LIN 2.1 specification are implemented. The allowed voltage range is from –30V to +40V. Reverse currents from the LIN bus to VS are suppressed, even in the event of GND shifts or battery disconnection. The LIN receiver thresholds are compatible with the LIN protocol specification. The fall time from recessive to dominant bus state and the rise time from dominant to recessive bus state are slope-controlled.

For higher bit rates the slope control can be switched off by setting the SPI-bit LSME. Then the slope time of the LIN falling edge is < 2µs. The slope time of the rising edge strongly depends on the capacitive load and the pull-up resistance at the LIN-line. To achieve a high bit rate it is recommended to use a small external pull-up resistor (500Ω) and a small capacitor. This allows very fast data transmission up to 200Kbit/s, e.g., for electronic control tests of the ECU, microcontroller programming or data download. In this High-speed Mode a superior EMC performance is not guaranteed.

Note: The internal pull-up resistor is only switched on in active mode and when the LIN transceiver is activated by the LINE-bit (active mode with LIN bus transceiver).

3.6 Bus Logic Level Input Pin (TXD)

The TXD pin is the microcontroller interface for controlling the state of the LIN output. TXD must be pulled to ground in order to keep the LIN bus in the dominant state. If TXD is high or not connected (internal pull-up resistor), the LIN output transistor is turned off and the bus is in recessive state.

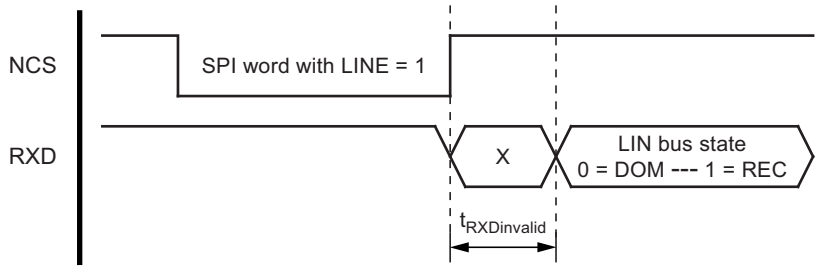
If configured, an internal timer prevents the bus line from being constantly driven in the dominant state. If TXD is forced to low for longer than t_{DOM}, the LIN bus driver is switched back to recessive state. TXD has to be switched to high for at least t_{TOrel} to reactivate the LIN bus driver (by resetting the time-out timer).

As mentioned above, this time-out function can be disabled via the SPI configuration register in order to achieve any long dominant state on the connected line (such as PWM transmission, or low bit rates).

3.7 Bus Logic Level Output Pin (RXD)

This output pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is reported by a high level, LIN low (dominant state) is reported by a low level at RXD. The output has push-pull characteristics meaning no external time defining measures are required. During states of disabled LIN-PHY (configuration bit “LINE” = 0), pin RXD is at high level. Please note that the signal on the RXD pin is not valid for a certain period of time upon activation of the LIN transceiver ($t_{RXDinvalid}$).

Figure 3-1. RXD Timing upon Transceiver Enable



RXD is switched off in sleep- and unpowered mode.

3.8 CL15 Pin

The CL15 pin is a high-voltage input that can be used to wake up the device from sleep mode. It is an edge-sensitive pin (low-to-high transition). Thus, even if CL15 pin is at high voltage ($V_{CL15} > V_{CL15th}$), it is possible to switch into sleep mode. It is usually connected to the ignition for generating a local wake-up in the application if the ignition is switched on. The CL15 pin should be tied directly to ground if not needed. A debounce timer with a value $t_{debCL15}$ of typically 160µs is implemented. The pin state (CL15 ON or OFF) can be read out through the SPI interface.

3.9 Reset Output Pin (NRES)

The reset output pin is an open drain output and switches to low during a VCC undervoltage event or a watchdog timing window failure. Please note the reset hold time of typically 4ms after the undervoltage condition has disappeared.

3.10 Interrupt Request Output Pin (NIRQ)

The interrupt request output pin is an open drain output and switches to low whenever a chip-internal event occurs that is set up to trigger an interrupt. A power-up, a wake-up over LIN bus, a change in a switch state or an overtemperature condition are examples of such events. The pin remains at ground until the end of the next SPI command, where the interrupt source is passed to the SPI master (bits IRQS, see also Section 7. “Serial Programming Interface (SPI)” on page 17).

3.11 WDOSC Output Pin

The WDOSC output pin provides a typical voltage of 1.2V intended to supply an external resistor with values between 34K and 120K. The value of the resistor and with it the pin output current adjusts the watchdog oscillator frequency to provide a certain range of time windows.

If the watchdog is disabled, the output voltage is switched off and the pin can either be tied to VCC or left open.

3.12 NTRIG Input Pin

The NTRIG input pin is the trigger input for the Window Watchdog. A pull-up resistor is implemented. A falling edge triggers the watchdog. The trigger signal (low) must exceed a minimum time $t_{trigmin}$ to generate a watchdog trigger and avoid false triggers caused by transients. The NTRIG pin should be tied directly to VCC if not needed.

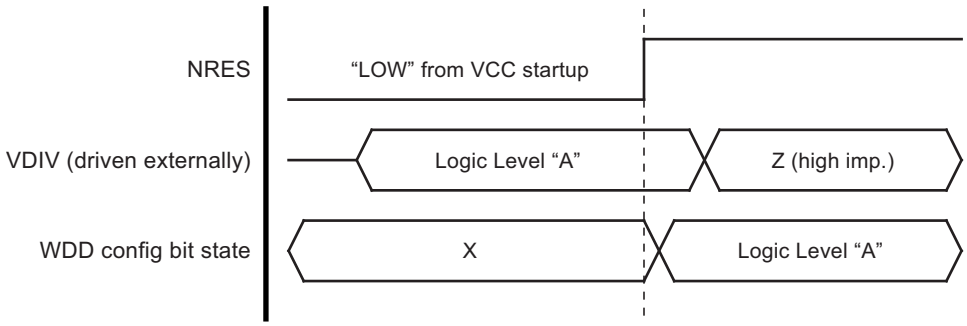
3.13 VBATT Input Pin

The VBATT is a high voltage input pin for measurement purposes by means of a voltage divider. The latter provides a low-voltage signal at the VDIV pin that is linearly dependent on the input voltage. In an application with battery voltage monitoring, this pin is connected to $V_{Battery}$ via a 51Ω resistor in series and a 10nF capacitor to GND. The divider ratio is 1:4. This results in maximum output voltages on pin VDIV when reaching 20V at the input. The VBATT pin can be tied directly to ground or left open if not needed.

3.14 VDIV Input/Output Pin

This pin handles two different functions. During the VCC startup and watchdog reset phase (pin NRES driven to LOW), the pin acts as input and determines the setting of the “WDD” bit within the SPI configuration register (see Figure 3-2). In other words, if the window watchdog operation shall be disabled directly after power-up (e.g., for microcontroller programming or debugging purposes), pin VDIV must be tied to HIGH level until the reset phase ends (pin NRES has a positive slope from LOW to HIGH). In other cases, such as when pin VDIV is not driven actively by the application, the signal is assessed as LOW and the WDD bit (watchdog disable) is thus also low and the window watchdog is operational (see Figure 3-2).

Figure 3-2. WDD Configuration Bit Setup During VCC Startup



During normal operation this pin provides a low-voltage signal for the ADC such as for a microcontroller. It is sourced either by the VBATT pin or one of the switch input pins CS1 to CS8. An external ceramic capacitor is recommended for low-pass filtering of this signal. If selected in the configuration register of the SPI, this pin guarantees a voltage- and temperature-stable output ratio of the selected test input and is available in all modes except sleep mode. Please note that the current consumption values in the active low-power mode of Atmel® ATA664151 given in the electrical characteristics lose their validity if the VDIV output pin is being used in this low-power mode. The voltage on this pin is actively clamped to VCC if the input value would lead to higher values.

3.15 IREF Output Pin

This pin is the connection for an external resistor towards ground. It provides a regulated voltage which will cause a resistor-dependent current used as reference for the current sources in the switch interface I/O ports. The resistor should be placed closely to the pin without any additional capacitor. A fail-safe circuitry detects if the resistor is missing or if there is a short towards ground or VCC on this pin. An internal fail-safe current is generated in this event. Please see also Section 8. “Switch Interface Unit” on page 22 for further details.

3.16 CS1 to CS8 High-voltage Input/Output Pins

These pins are intended for contact monitoring and/or constant current sourcing. A total of eight I/Os (pins CS1 through CS8) are available, of which three (CS1, CS2 and CS3) can be configured either as current sources (such as for switches towards ground) or as current sinks (such as for switches towards battery). The other five pins (CS4 to CS8) have only current sourcing capability. Apart from a high voltage (HV) comparator for simple switches, the I/Os are also equipped with a voltage divider to enable analog voltage measurements on HV pins by using the ADC of the application’s microcontroller (see Section 3.14 “VDIV Input/Output Pin” on page 7 for further details). Also, each input can trigger an interrupt upon state change even during Active Low-power Mode. If one or more CSx pins are not needed, can be left open or directly connected to VS.

Note: Unused CSx-pins should be connected directly to VS.

3.17 PWM1..3 Input Pins

These pins can be used to control the switch interface current sources directly, such as for pulse width-modulated load control or for pulsed switch scanning. They accept logic level signals from the microcontroller and are equipped with pull-down structures so in case of an open connection, the input is well defined. For more information see Section 8. “Switch Interface Unit” on page 22.

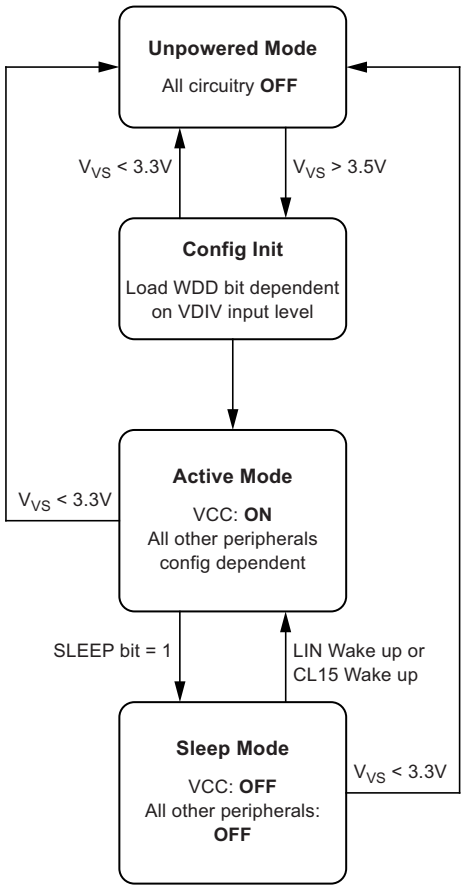
The assignment of the current sources to the three PWM input pins is described in Section 8.1 “Current Sources” on page 22.

4. Operating Modes

There are two primary modes of operation available with the Atmel® ATA664151.

- Active mode:
  In this mode the VCC voltage regulator is active and the SPI is ready for operation. In addition, all other peripherals can be enabled or disabled by configuration via SPI. After power-up the watchdog is enabled (dependent on the VDIV pin only, see Section 3.14 “VDIV Input/Output Pin” on page 7), whereas the LIN transceiver and the switch interface unit are switched off.
- Sleep mode:
  All peripherals are switched off (including the VCC voltage regulator), a wake-up is only possible via the LIN bus or the CL15 pin. In this mode the IC has the lowest possible current consumption.

Figure 4-1. State Diagram



4.1 Active Mode

If sufficient voltage is applied to the IC at the VS pin, the configuration register is initialized and the chip changes to active mode. In this mode different states of power consumption are possible, depending on the configuration selected for the chip and activity on the SPI. The following table lists all power states (except unpowered) for the Atmel® ATA664151.

Table 4-1. State and Current Consumption vs. Enabled Periphery

State and VS Pin Current Consumption	LIN bus Transceiver	Voltage Divider	VCC Voltage Regulator	Watchdog	SPI Data Comm.	Current Sources
Sleep $I_{VS} = I_{VSsleep}$	Off	Off	Off	Off	Off	Off
Active low-power $I_{VS} = I_{VSact_lp}$	Off (LINE=0)	Off (VDIVE=0)	On	Off (WDD=1)	Off (NCS=1)	Off or standby (CSEx=X and CSCx=0 and PWMy=0)
Active SPI comm. $I_{VS} = I_{VSact_spi}$	Off (LINE=0)	Off (VDIVE=0)	On	Off (WDD=1)	On (NCS=0)	Off (CSEx=0)
Active with watchdog $I_{VS} = I_{VSact_wd}$	Off (LINE=0)	Off (VDIVE=0)	On	On (WDD=0)	do not care	Off (CSEx=0)
Active with LIN-bus transceiver $I_{VS} = I_{VSact_lin}$	On (LINE=1)	Off (VDIVE=0)	On	Off (WDD=1)	do not care	Off (CSEx=0)
Active with current sources $I_{VS} = I_{VSact_cs}$	Off (LINE=0)	Off (VDIVE=0)	On	Off (WDD=1)	do not care	On (CSEx=1 and (CSCx=1 or PWMy=1))
Active with voltage divider $I_{VS} = I_{act_vdiv}$	Off (LINE=0)	On (VDIVE=1)	On	Off (WDD=1)	do not care	Off (CSEx=0)

Note: Legend:
0 = bit is programmed 0
1 = bit is programmed 1,
X = Disregards

The descriptions in brackets below the peripherals refer to the configuration register of Atmel ATA664151, accessible via SPI.

Please note that the table above only lists the active mode states with just one extra peripheral enabled. Except for active low-power, any combination of the states above and thus also the current consumption is possible - for example, the parallel operation of the LIN bus transceiver and the current sources. The required supply current is then at least the sum of the values given above.

4.2 Sleep Mode

This mode must be initialized via the SPI configuration register. All peripherals, i.e., the LIN transceiver, the watchdog, the voltage dividers, the switch interface Unit and the VCC voltage regulator are switched off. The overall supply current on pin VS is then reduced to a minimum.

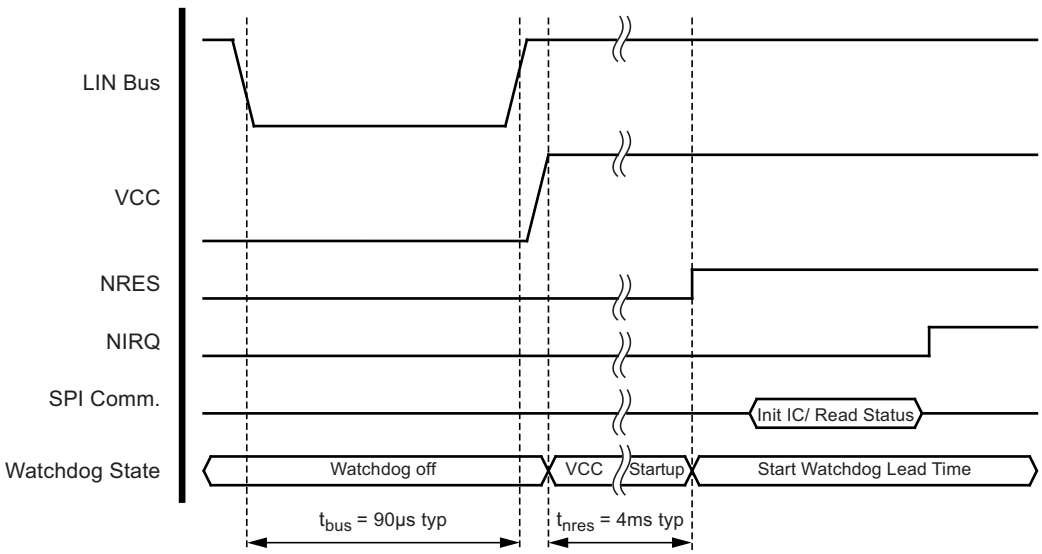
Two wake-up mechanisms are possible to leave sleep mode again: wake-up via LIN and wake-up via CL15.

4.2.1 Wake-up from Sleep Mode via LIN

A voltage below the LIN pre-wake threshold on the LIN pin activates a wake-up detection phase.

A falling edge at the LIN pin followed by a dominant bus level maintained for a time period of at least t_{bus} and the following rising edge at the LIN pin (see Figure 4-2) results in a remote wake-up request. The device switches from sleep mode to active-low power mode (VCC regulator enabled), but the LIN transceiver is still deactivated. Only the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at the NIRQ pin to interrupt the microcontroller (see Figure 4-2). In addition, the wake-up source is stated in the chip status register which can be read out via SPI. Configuring the chip via SPI must be used to enable the LIN transceiver and allow data to be send and/or transmitted via the LIN bus. Note that this can only be done after the LOW level at the NRES pin has been eliminated (after VCC ramp-up and the stabilization phase).

Figure 4-2. LIN Wake-up from Sleep Mode



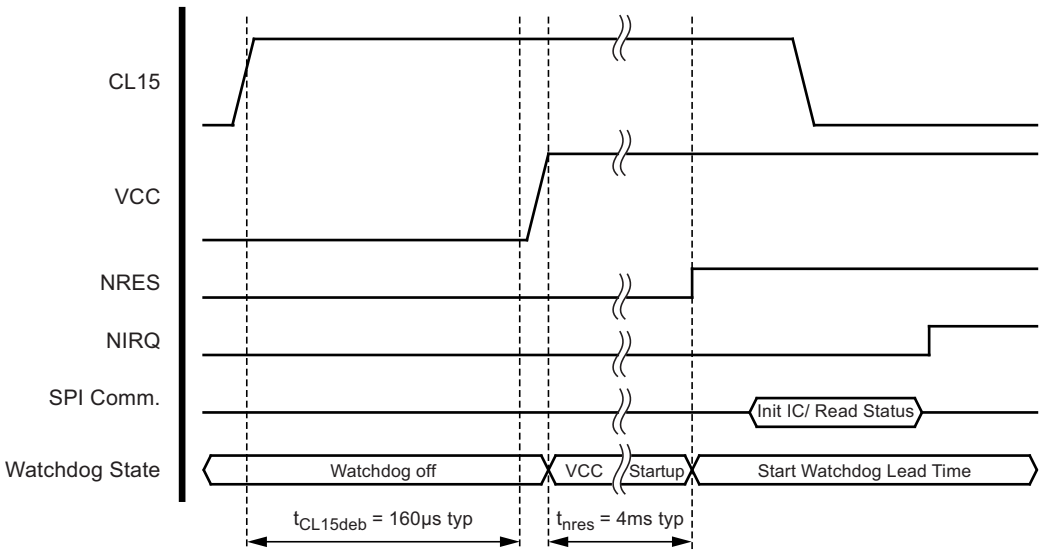
With the initialization of the configuration register by the microcontroller, the status word of Atmel® ATA664151 is transmitted back, including the wake-up source. In other words, the two status bits “IRQS1” and “IRQS0” both read back as '1'. For more information see Section 7. “Serial Programming Interface (SPI)” on page 17.

4.2.2 Wake-up from Sleep Mode via CL15

Voltage above V_{CL15H} at pin CL15 activates a CL15 wake-up detection phase. This state must persist for at least t_{CLdeb} in order to detect a wake-up. If the pulse is too short, the IC remains in Sleep Mode.

When leaving sleep mode first the VCC voltage regulator is activated to enable the microcontroller supply. Then as soon as the VCC level reaches valid levels, the VCC startup timer is started. During this time, the NRES pin is kept low in order to keep the microcontroller from running. This ensures a proper voltage supply and signal stabilization in the application. With the rising edge at NRES, the SPI is ready for communication and the Atmel® ATA664151 can be initialized.

Figure 4-3. CL15 Wake-up from Sleep Mode



The wake-up behavior is analogous to a wake-up via the LIN bus as seen above. One difference is that no negative edge is required to start the wake-up procedure as is the case for LIN wake-ups. After the VCC startup time t_{WDnres} has elapsed, NRES is released and therefore pulled up, either by the internal or additional external resistors. The microcontroller can then configure the Atmel ATA664151 and thus be notified about the actual status including the wake-up source. Here, the two status bits “IRQS1” and “IRQS0” read back as '10'.

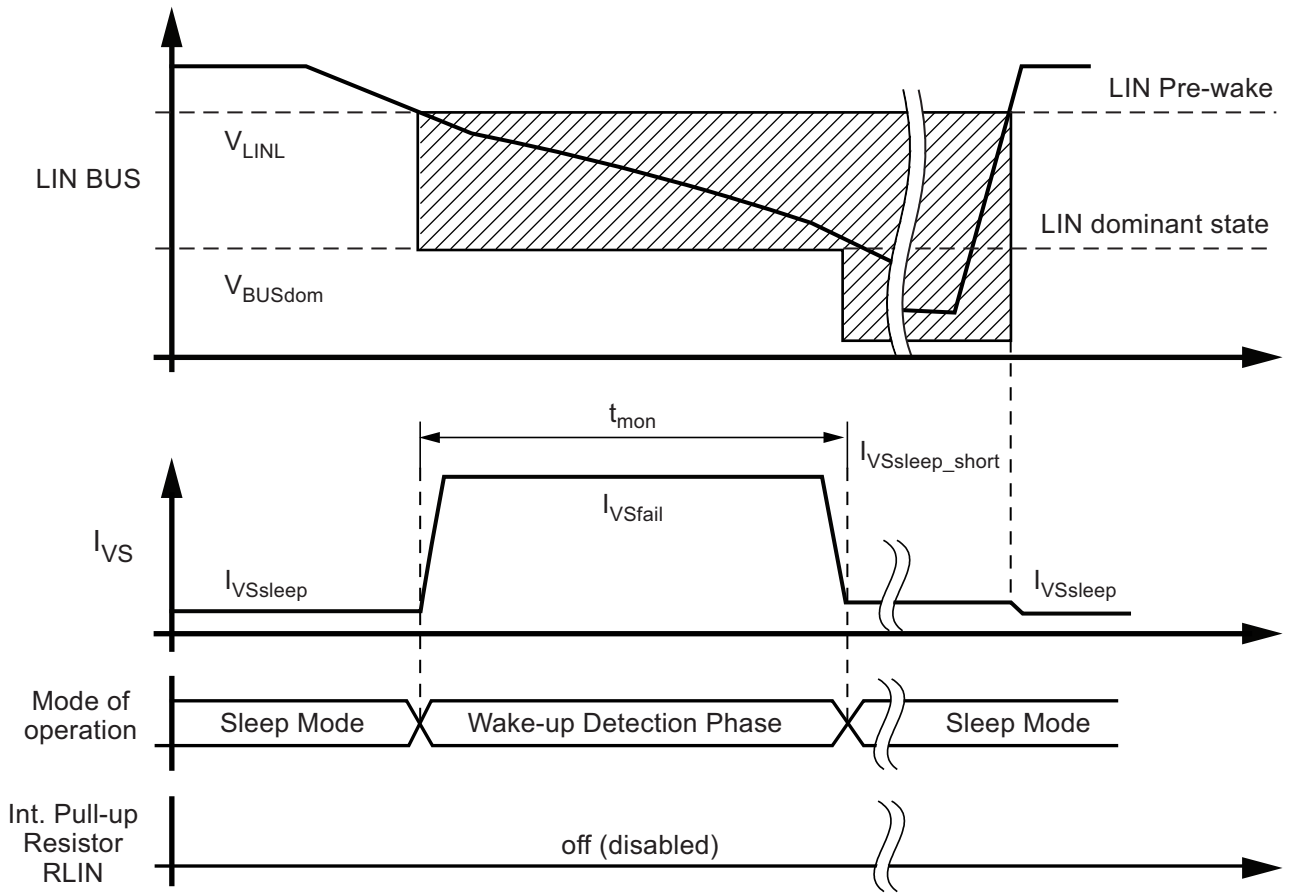
4.2.3 Sleep Mode: Behavior at a Floating LIN bus or a Short-circuited LIN to GND

In sleep mode the device has very low current consumption even during short-circuits or floating conditions on the bus. A floating bus can arise if the master pull-up resistor is missing, such as when it is switched off while the LIN master is in sleep mode or even if the power supply of the master node is switched off.

In order to minimize the current consumption I_{VS} in sleep mode during voltage levels on the LIN pin below the LIN pre-wake threshold, the receiver is activated only for a specific time t_{mon}. If t_{mon} elapses while the voltage at the bus is lower than pre-wake detection low (V_{LINL}) or higher than the LIN dominant level, the receiver is switched off again and the circuit changes back to sleep mode. The current consumption is then $I_{VSsleep_short}$ (typ. 10µA more than $I_{VSsleep}$). If a dominant state is reached on the bus, no wake-up occurs. Even if the voltage rises above the pre-wake detection high (V_{LINH}), the IC will stay in sleep mode.

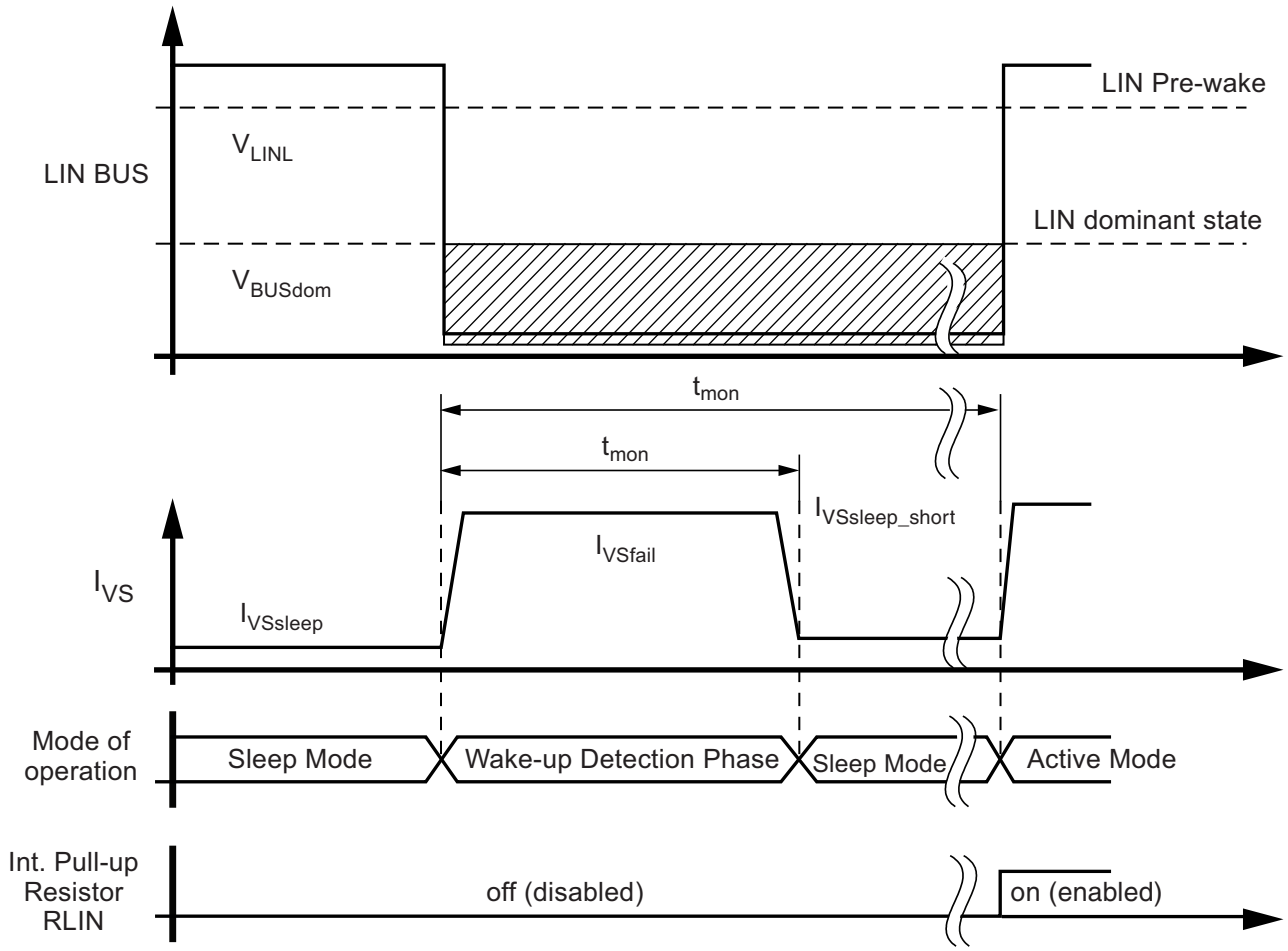
This means the LIN bus must be above the pre-wake detection threshold V_{LINH} for a few microseconds before a new LIN wake-up is possible.

Figure 4-4. Floating LIN Bus During Sleep Mode



If the Atmel® ATA664151 is in Sleep Mode and the voltage level at the LIN bus is in dominant state ($V_{LIN} < V_{BUSdom}$) for a period exceeding t_{mon} (during a short circuit at LIN, for example), the IC switches back to sleep Mode. The V_S current consumption is then $I_{VSsleep_short}$ (typ. 10µA more than $I_{VSsleep}$). After a positive edge at the LIN pin the IC switches directly to active mode.

Figure 4-5. Short Circuit to GND on the LIN Bus During Sleep Mode



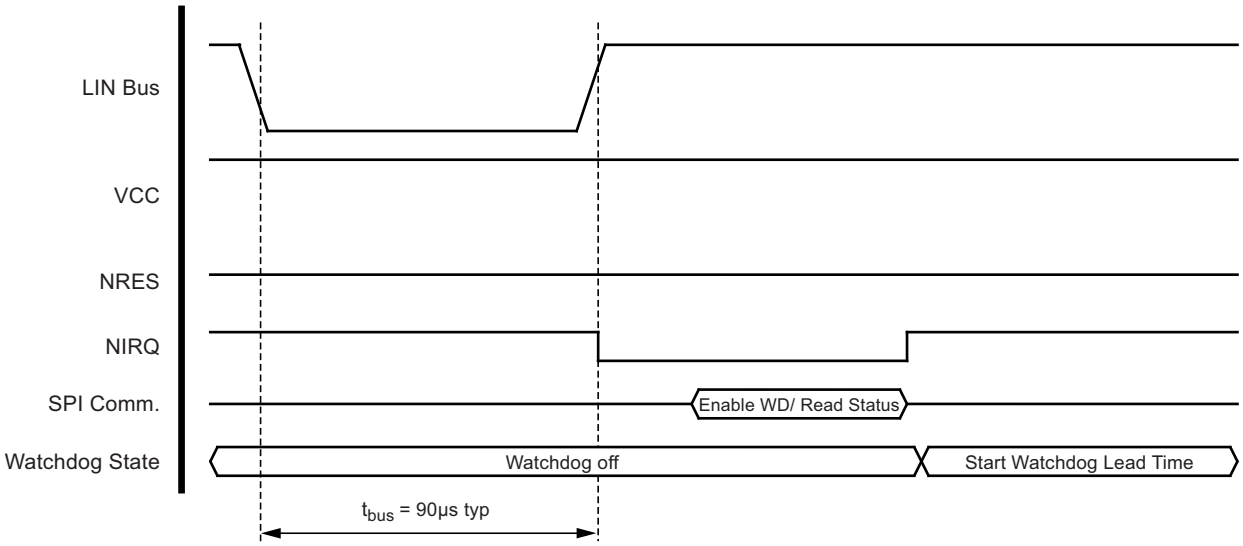
4.3 Active Low-power Mode

In this mode, the VCC voltage regulator is active and can therefore supply the application's microcontroller.

All other functions of the Atmel® ATA664151 are disabled in the configuration register respectively inhibited by the PWM pins for the CSx pin current sources. This reduces the current consumption of the chip itself to a low-power range of typically below 50µA. Note that this is only valid if the chip select input of the SPI, NCS, is also kept at a high level. If it is pulled to ground, SPI communication is enabled, causing a higher current consumption.

If the LIN transceiver is disabled, the bus is monitored for a wake-up event, initialized with a voltage level below the LIN pre-wake threshold at the LIN pin.

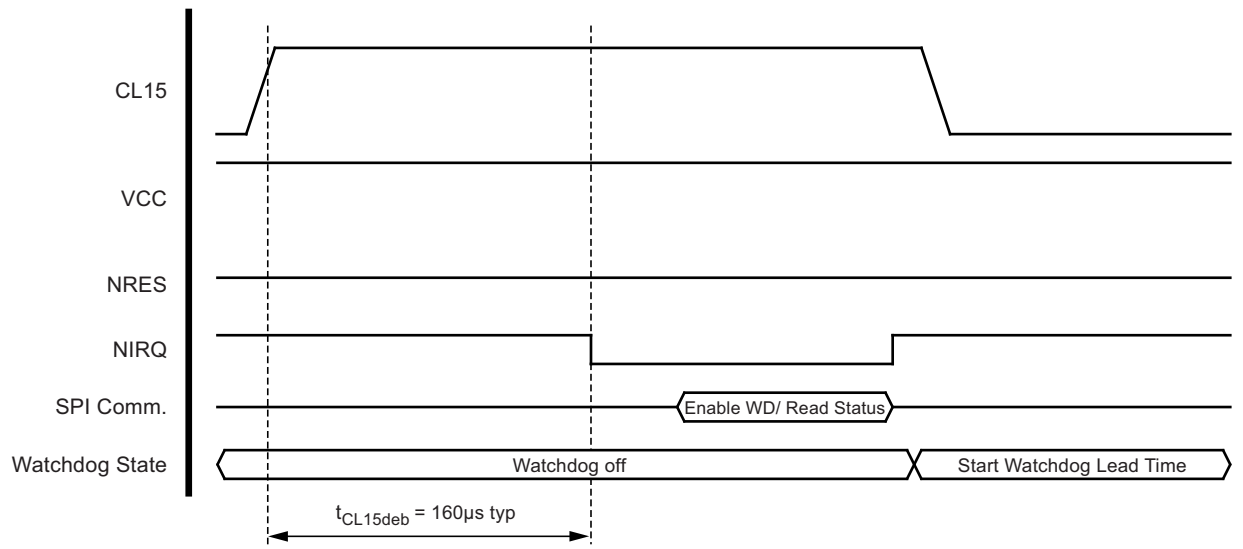
Figure 4-6. LIN Wake-up from Active Low-power Mode



The negative edge on the NIRQ pin indicates a change of conditions, in this case a wake-up request at the LIN bus. The microcontroller can check the IRQ source by assessing the “IRQS1” and “IRQS0” bits in the status register. Note that if a watchdog operation is desired, it must be enabled via the configuration register.

The behavior can be transferred to a wake-up over CL15 pin from active low-power mode.

Figure 4-7. CL15 Wake-up from Active Low-power Mode



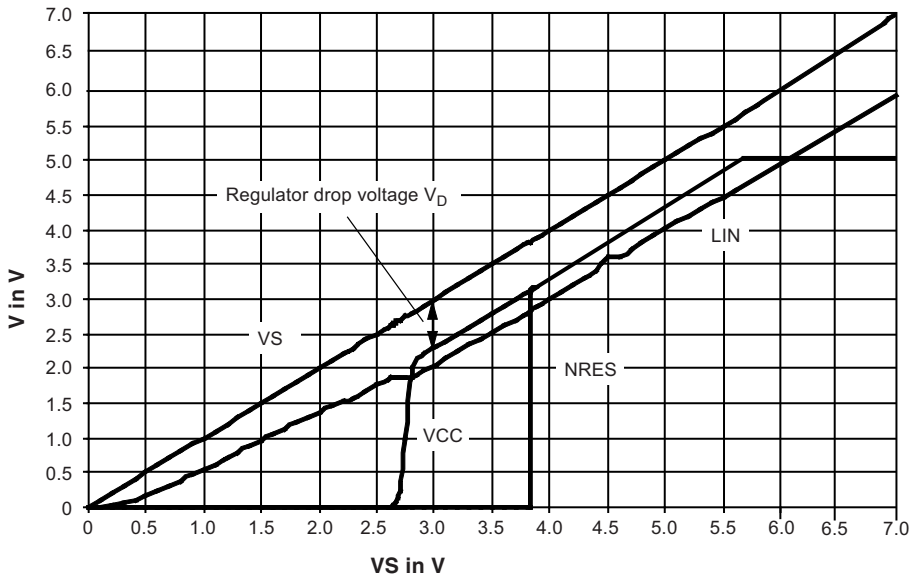
Apart from the LIN transceiver and the CL15 input, the high-voltage I/O ports CS1 to CS8 can also be used to generate interrupts while in active low-power Mode. This can be done by enabling the current sources so that they can generate an interrupt with the corresponding CSEx- and CSIEx bits in the configuration register. As long as the current source is not enabled (CSCx='0' and PWMy low), the IC stays in active low-power mode (if all other conditions are met, such as disabled watchdog). The PWMy pin has to be set to high by the microcontroller, for example, controlled via a PWM timer unit, in order to check the condition of the connected switch. Because the switch interface unit is enabled, current consumption increases drastically. This “switch scanning phase” can be short compared to the interceding idle time so the mean current consumption of the IC remains close to the active low-power Mode current consumption. For more information, see Section 8.1 “Current Sources” on page 22 and Section 8.2 “Switch Inputs” on page 24 for further details.

4.4 Behavior under Low Supply Voltage Conditions

When connected to the car battery, the voltage at the VS pin increases according to the blocking capacitor (see Figure 4-8). As soon as V_{VS} exceeds its undervoltage threshold V_{VSthO}, the Switch Interface Unit and the LIN transceiver can be used. The IC is in active mode after power-up with the VCC voltage regulator and the window watchdog enabled – the latter depends on the state of the pin VDIV. The VCC output voltage reaches its nominal value after t_{VCC}. This time depends on the externally applied VCC capacitor and the load.

The NRES is low for the reset time delay t_{reset}. During this time t_{reset}, no SPI communication and thus no configuration changes or status checks are possible.

Figure 4-8. VCC versus VS



Please note that upper graph is only valid if the VS ramp-up time is much slower than the VCC ramp-up time t_{VCC} and the NRES delay time t_{reset}.

If during active mode the voltage level of VS drops below the undervoltage detection threshold V_{VSthU}, an interrupt is indicated to the microcontroller by means of a low-signal at the NIRQ pin. Furthermore, both the switch interface unit and the LIN transceiver are shut down in order to avoid malfunctions or false bus messages. This shutdown is achieved by simply inhibiting the functions internally. The corresponding bits in the configuration register are not cleared. This means the functionality resumes if enabled after the supply voltage exceeds above V_{VSthO} again.

If during sleep mode the voltage level of VS drops below the undervoltage detection threshold V_{VSthU}, no change of mode or any other activity by the Atmel® ATA664151 occurs as long as the level does not drop below the minimum operation value $V_{VSopmin}$.

5. Wake-up Scenarios from Sleep Mode

5.1 Remote Wake-up via the LIN Bus

A voltage lower than the LIN Pre-wake detection V_{LINL} at the LIN pin activates the internal LIN receiver.

A falling edge at the LIN pin followed by a dominant bus level V_{BUSdom} of at least t_{BUS} and a rising edge at pin LIN results in a remote wake-up request. The device switches from sleep mode to active mode. The VCC voltage regulator is activated and the internal slave termination resistor is switched on. The remote wake-up request is indicated by a low level at the NIRQ pin. this generates an interrupt for the microcontroller and a corresponding flag in the SPI register.

5.2 Local Wake-up via Pin CL15

A positive edge at pin CL15 followed by a high voltage level for a given time period (> $t_{CL15deb}$) results in a local wake-up request. The device switches to active mode. The debouncing time ensures that no transients at CL15 create a wake-up. The local wake-up request is indicated by a low level at the NIRQ pin, generating an interrupt for the microcontroller. During high-level voltage at the CL15 pin, it is possible to switch to sleep mode via an SPI command. In this case the voltage at the CL15 pin has to be switched to low for at least $t_{CL15deb}$ before the positive edge at this pin starts a new local wake-up request. Note that this time can be extended by adapting the external circuitry.

5.3 Wake-up Source Recognition

The device can distinguish between different wake-up sources.

The source for the wake-up event can be read out of the SPI diagnosis register.

6. Wake-up Scenarios from Active Low-power Mode

Generally the active low-power mode is only possible if all clock-dependent peripherals such as the LIN transceiver and the watchdog are disabled. In addition, no SPI communication is allowed to take place to minimize current consumption.

6.1 Wake-up from CSx Pins

The switch input pins can each be used to generate an interrupt request while in active low-power mode. A state change detection circuitry is implemented for this functionality (see Section 8.2 “Switch Inputs” on page 24). For this functionality, the respective current source needs to be configured so that it is controlled via the dedicated PWMy pin. A rising edge on this pin enables the current source, allowing a stable switch readback signal to be delivered at the CSx pin. The switch state is updated with a falling edge at the PWMy pin. If a change of state is monitored, an interrupt request is generated if the CSIE bit of the affected current source is set to '1' in the configuration register. If no wake-up should occur on a certain switch - either because there is no application demand for this or a failure such as a hanging switch or a connection line short-circuit is present - it can be prevented by disabling the current source in the SPI configuration register.

6.2 Wake-up from LIN Bus

If during active low-power mode (i.e., the LIN transceiver is disabled) the LIN bus is tied to ground for at least t_{bus}. This wake-up request is indicated by a negative edge at the NIRQ pin. Please note that the Atmel® ATA664151 stays in active low-power mode for as long as no SPI communication occurs or configuration changes are made. Current consumption is only higher during the LIN bus assessment, in other words as long as the voltage on the LIN bus is below $V_{LIN,preL}$. Regardless of the LIN bus state, this assessment phase ends after t_{LIN_wudet} at the latest. This ensures a low current consumption even during shorts on the LIN bus or when there are floating bus levels.

6.3 Wake-up from CL15

If during active low-power mode the voltage on the CL15 pin exceeds V_{CL15H} for at least $t_{CL15deb}$, an interrupt request is triggered to indicate a change of state at the CL15 pin. Please note that after the $t_{CL15deb}$ has elapsed, the Atmel ATA664151 stays in active low-power mode for as long as no SPI communication occurs or configuration changes are made.

6.4 Wake-up from SPI

If during active low-power mode the chip select input NCS is tied to ground, Atmel® ATA664151 leaves the active low-power mode in order to complete a data communication with the SPI master. The operating mode of the IC is adapted in accordance with the configuration register update. If no change in configuration has taken place – for example, because only the actual status was polled or another bus member connected via daisy chaining was addressed – Atmel ATA664151 goes back to active low-power mode as soon as NCS returns to high level.

7. Serial Programming Interface (SPI)

Most features of the IC are configured via SPI. Diagnostics are carried out using this interface also. It can be used in active mode as long as there is no undervoltage condition at the VCC pin.

The Atmel ATA664151 SPI features both POL = 0 / PHA = 0 and POL = 1 / PHA = 1 operating modes.

Figure 7-1. POL = 0 / PHA = 0 Setup

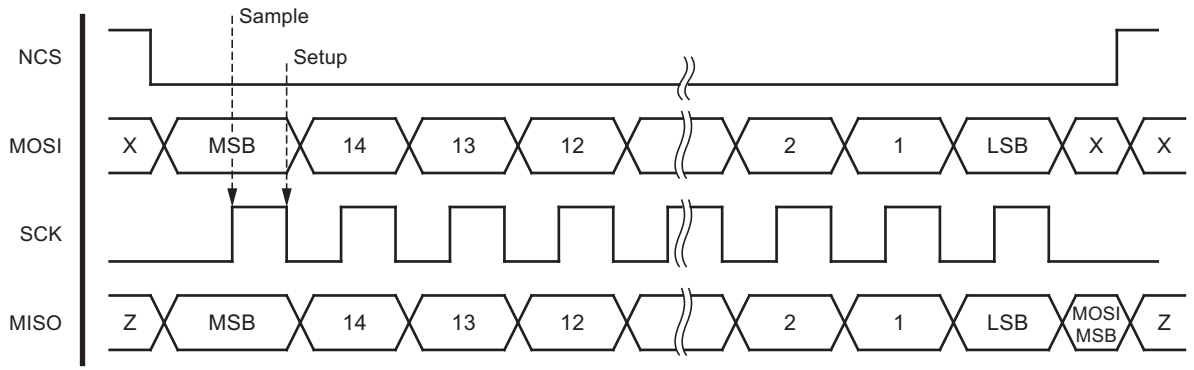
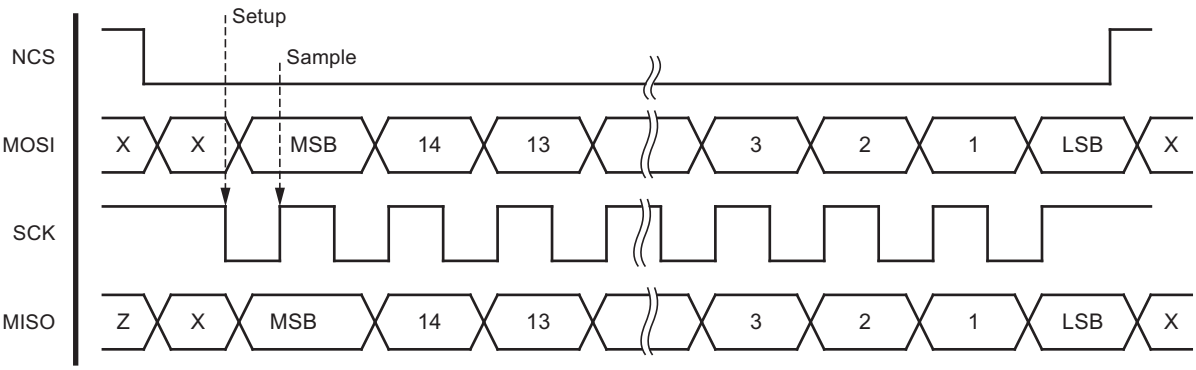


Figure 7-2. POL = 1 / PHA = 1 Setup



The interface contains four pins.

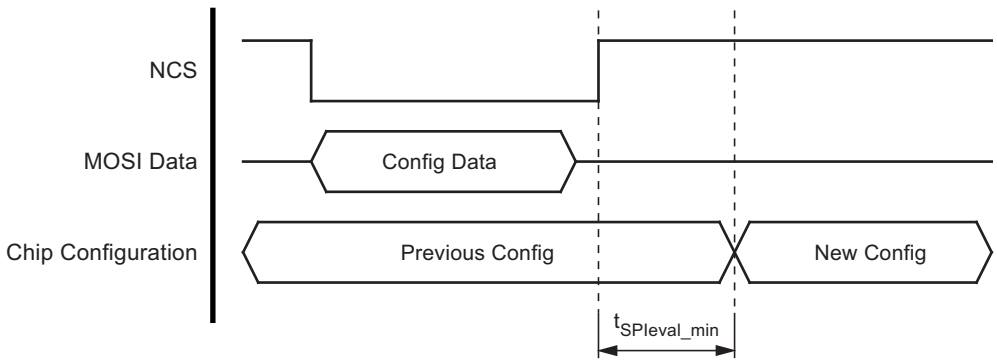
- NCS (chip select pin, active low)
- SCK (serial data clock)
- MOSI (master-out-slave-in serial data port input from master)
- MISO (master-in-slave-out serial data port output from SBC; this pin is tri-state if NCS is high)

No data is loaded from MOSI on SCK edges or provided at MISO if chip select is not active. The output pin MISO is not actively driven (tri-state) during these phases.

The data transfer scheme (bit order) is MSB first, meaning the first bit that is transferred is the most significant bit of the register, with the transfer ending with the least significant bit. These bits are listed on the next pages. The MOSI bits 15 to 0 refer to the configuration register. This means the configuration register is updated with each SPI communication. At the same time the MISO word is built from the status register bits 15 to 0. Note that changes in the configuration are only visible in the next status query. This means, for example, that if you enable the watchdog with an SPI command, the status “Watchdog Active” is not reported in this data transmission but in the next one.

In order to load any data into the chip, the chip select signal must be removed (i.e., set to high) after the 16 SCK clock periods. A minimum data evaluation time $t_{SPIeval,min}$ has to transpire before the next data transfer can start. Please note also that any change in configuration of the IC requires this time to go into effect.

Figure 7-3. SPI Configuration Timing



The following table lists the bits of the configuration register in the Atmel® ATA664151.

Table 7-1. SPI Conflguration Register

#	Bit Name	Description	Default ('0')	Programmed with '1'	Remark
15 MSB	LSME	Enable LIN-bus High-speed mode	Normal	High-speed	See LIN transceiver description
14	TTTD	Disable TxD time-out timer	Enabled	Disabled	See Section 3.6 “Bus Logic Level Input Pin (TXD)” on page 5
13	IMUL	IREF multiplier value	x100	x50	See Section 8. “Switch Interface Unit” on page 22
12	LINE	Enable LIN transceiver	Disabled	Enabled	See LIN transceiver description
11	SLEEP	Go to sleep	Stay in active mode	Enable sleep mode	See Section 4. “Operating Modes” on page 8
10	VDIVE	Enable VDIV as output	VDIV off (high-ohmic)	VDIV on (selected voltage divider active)	See Section 8.2.2 on page 26 and Section 8. “Switch Interface Unit” on page 22
9	VDIVP	Programming VDIV output source	VDIV shows VBATT divider	VDIV shows one CS divider output	See Section 8.2.2 on page 26 and Section 8. “Switch Interface Unit” on page 22

Table 7-1. SPI Conflguration Register (Continued)

#	Bit Name	Description	Default ('0')	Programmed with '1'	Remark
8	CSPE	Enable switch interface unit programming	Disabled	Enabled	See Section 8. “Switch Interface Unit” on page 22
7	CSA2	Address bit 2 (MSB) for switch input	0	1	Used as selector for VDIV and for programming of one current source
6	CSA1	Address bit 1 for switch input	0	1	Used as selector for VDIV and for programming of one current source
5	CSA0	Address bit 0 (LSB) for switch input	0	1	Used as selector for VDIV and for programming of one current source
4	CSE	Enable addressed current source	Disabled	Enabled	See Section 8. “Switch Interface Unit” on page 22
3	CSSSM	Switch between source/sink mode	Source mode selected (highside)	Sink mode selected (lowside)	Sink mode is only possible for switch interfaces 1-3
2	CSC	Control of addressed current source	External (CSE and PWMy)	Internal (CSE only)	See Section 8. “Switch Interface Unit” on page 22
1	CSIE (CSPE=1)	Enable interrupt from addressed switch input	Disabled	Enabled	CSIE will be altered if CSPE of the SPI word is '1'. See Section 8. “Switch Interface Unit” on page 22
	CSSCD (CSPE=0)	CS port current source slope control	Enabled	Disabled	CSSCD will be altered if CSPE of the SPI word is '0'. See Section 8. “Switch Interface Unit” on page 22
0 LSB	WDD	Disable watchdog	Enabled (if pin VDIV on low level)	Disabled	See Section 10. “Watchdog” on page 28

The following table lists the bits of the status register in Atmel® ATA664151.

Figure 7-4. SPI Status Register

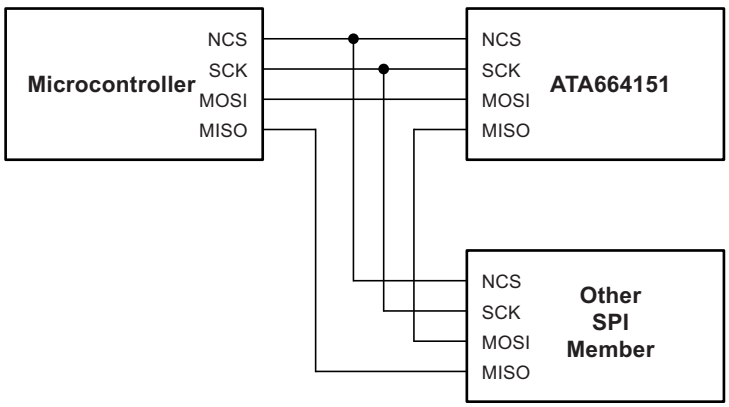
#	Bit Name	Description	Result = "0"	Result = "1"	Remark
15 MSB	OTVCC (VDIVE=0)	Overtemperature prewarning from VCC regulator temp sensor	Temperature not critical	Temperature critical	See Section 9. on page 27; only valid if VDIVE of prev. command was '0'
	MVBATT (VDIVE=1)	VBATT voltage monitor	VBATT not visible on VDIV	VBATT visible on VDIV	Only valid if VDIVE of prev. command was '1'
14	OTLIN (VDIVE=0)	Overtemperature signal from LIN driver temp sensor	no Over-temperature	Over-temperature	See Section 3.5 on page 5; only valid if VDIVE of prev. command was '0'
	MRDIV2 (VDIVE=1)	CS port voltage monitor, address bit 2 (MSB)	MRDIV2..0 indicate the address of the CS port volt. monitor visible on VDIV		This bit is only shown if VDIVE of previous command was '1'
13	OTCS (VDIVE=0)	Overtemperature signal from current sources temp sensor	no Over-temperature	Over-temperature	See Section 8. on page 22; only valid if VDIVE of prev. command was '0'
	MRDIV1 (VDIVE=1)	CS port voltage monitor, address bit 1	MRDIV2..0 indicate the address of the CS port volt. monitor visible on VDIV		This bit is only shown if VDIVE of previous command was '1'
12	CL15S (VDIVE=0)	CL15 pin status	$V_{CL15} < V_{CL15H}$	$V_{CL15} \geq V_{CL15H}$	See Section 11. on page 30; only valid if VDIVE of prev. command was '0'
	MRDIV0 (VDIVE=1)	CS port voltage monitor, address bit 0 (LSB)	MRDIV2..0 indicate the address of the CS port volt. monitor visible on VDIV		This bit is only shown if VDIVE of previous command was '1'
11	WDS	Watchdog status	Watchdog disabled	Watchdog enabled	See Section 10. “Watchdog” on page 28
10	VSS	VS voltage level status	VS voltage OK	VS undervoltage	See Section 4.4 on page 15
9	IRQS1	Interrupt request source	“00” PowerUp “01” CS change “10” CL15 wake-up “11” LIN wake-up		Information will be cleared after status register readout via SPI
8	IRQS0				
7	CS8CS	Switch interface 8 comparator status	$V_{CS8} < V_{CSxth}$	$V_{CS8} > V_{CSxth}$	See Section 8. “Switch Interface Unit” on page 22
6	CS7CS	Switch interface 7 comparator status	$V_{CS7} < V_{CSxth}$	$V_{CS7} > V_{CSxth}$	See Section 8. “Switch Interface Unit” on page 22
5	CS6CS	Switch interface 6 comparator status	$V_{CS6} < V_{CSxth}$	$V_{CS6} > V_{CSxth}$	See Section 8. “Switch Interface Unit” on page 22

Figure 7-4. SPI Status Register

#	Bit Name	Description	Result = "0"	Result = "1"	Remark
4	CS5CS	Switch interface 5 comparator status	$V_{CS5} < V_{CSxth}$	$V_{CS5} > V_{CSxth}$	See Section 8. “Switch Interface Unit” on page 22
3	CS4CS	Switch interface 4 comparator status	$V_{CS4} < V_{CSxth}$	$V_{CS4} > V_{CSxth}$	See Section 8. “Switch Interface Unit” on page 22
2	CS3CS	Switch interface 3 comparator status	$V_{CS3} < V_{CSxth}$	$V_{CS3} > V_{CSxth}$	See Section 8. “Switch Interface Unit” on page 22
1	CS2CS	Switch interface 2 comparator status	$V_{CS2} < V_{CSxth}$	$V_{CS2} > V_{CSxth}$	See Section 8. “Switch Interface Unit” on page 22
0 LSB	CS1CS	Switch interface 1 comparator status	$V_{CS1} < V_{CSxth}$	$V_{CS1} > V_{CSxth}$	See Section 8. “Switch Interface Unit” on page 22

The SPI is capable of daisy chaining as well. In other words, if other ICs with a daisy-chaining-enabled SPI are to be used in the application, they can simply be interconnected one after the other (see Figure 7-5).

Figure 7-5. Daisy Chaining Configuration



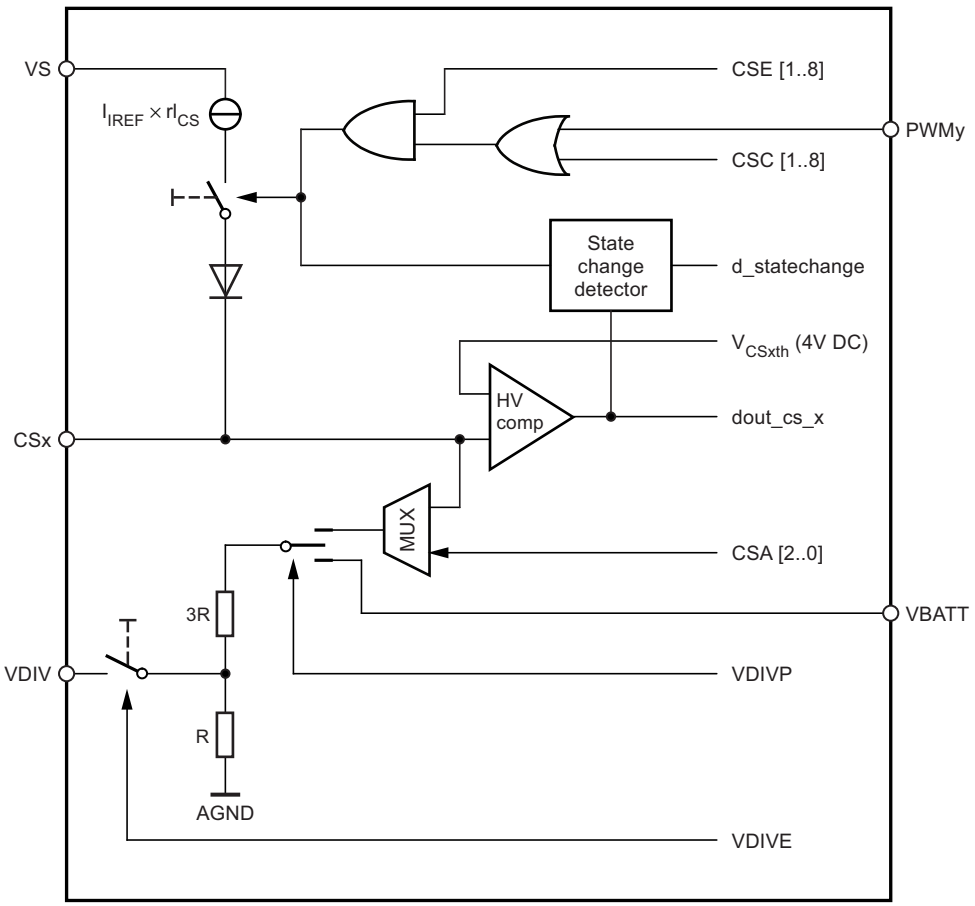
It can be seen that the data output of Atmel® ATA664151 is not connected to the data input of the master but of another SPI member which is also capable of daisy chaining. In order to transmit data, the microcontroller has to send the sum of clock pulses for all bus members. In the example above, if the other SPI member also features 16 bits, the microcontroller has to perform 32 clock cycles with NCS kept low to completely move the data. The first 16 bits of such a transmission are initially fed into the Atmel ATA664151. But when NCS stays low, the data is not loaded into its configuration register but instead shifted out again with the next 16 bits. At the same time the status register of Atmel ATA664151 is first fed into the other SPI bus member which then needs to transfer the data over to the microcontroller with the second 16 bits.

In summary, the daisy chaining is one way to have multiple bus members connected to a single master. Because not all devices support these operating modes, the Atmel ATA664151 still supports the direct addressing mode using the NCS pin. If NCS is not pulled to ground, all data traffic on the SPI is disregarded by the Atmel ATA664151.

8. Switch Interface Unit

A total of eight high-side current sources with high voltage comparators and voltage dividers are available for switch scanning or for example, LED driving purposes. Note that three of them (CS1, CS2, and CS3) can also be switched to low-side current sinks in the configuration register via the SPI. System wake-up from active low-power mode is possible through state change monitoring. Please see Figure 8-1 for an overview of the interface structure.

Figure 8-1. Principle Schematic of a High-Side-Only Switch Interface (CS4 - CS5)



The control signals CSE and CSC are configuration register bits, and unique for each of the eight interfaces. The output signal dout_cs of the comparator can be probed via the SPI status register bit CSxCS.

8.1 Current Sources

The current sources are available in Active Mode. They deliver a current level derived from a reference value measured at the IREF pin. This pin is voltage-stabilized (V_{IREF} = 1.23V typ.) so that the reference current is directly dependent on the externally applied resistor connected between IREF pin and ground. The resulting current at the CSx- pins is $(1.23V/R_{Iref}) \times rI_{CS}$. For example, with a 12K resistor between IREF and GND the value of the current at the CSx-pins is 10mA (assumed IMUL = '0' => rI_{CS_H} = 100). For fail-safe reasons, both a missing and a short-circuited resistor are detected. In this case, an internally generated reference current I_{IREFfs} is used instead to maintain a certain functionality.

The current sources of I/Os 1-3 (CS1..CS3) can be configured either as high-sides (current sources) or low-sides (current sinks). This selection is done by the CSSSM bit of the configuration register. The default value of '0' enables the high-side source whereas a '1' enables the low-side sink.

The output current level can be divided by 2 with the IMUL bit in the configuration register. With the default setting of IMUL = '0', the ratio between the output current I_{CSx} and the reference current I_{IREF} is rI_{CS_H} (typ. 100). If set to '1', the ratio reduces to rI_{CS_L} (typ. 50).

If a current source is enabled by the configuration register (set to ready state, bit CSE = '1'), it supports two different operating modes.

- Directly controlled by the configuration register - bit CSC = '1'
- Externally gated (inhibited with the PWMy pin) - bit CSC = '0' (default)

These modes can be selected independently for each current source via the configuration register. While the current source is permanently on with CSC = '1' it is controlled externally by the logic level input pins PWMy with CSC = '0' for switch scanning or LED driving (external PWM control). The following truth table summarizes all setup variants.

Table 8-1. CS Port Configuration Table

CSEx	CSCx	CSSSM	PWMy	CS1..3	CS4..8	Active Low-power Mode Possible
0	X	X	X	Off	Off	Yes
1	0	X	0	Off	Off	Yes
1	1	0	X	1	1	No
1	1	1	X	0	1	No
1	0	0	1	1	1	No
1	0	1	1	0	1	No

Legend:
0 -> Bit = '0' for CSEx, CSCx and CSSSM; logic low for PWMy; LS current source active for CS1..3
1 -> Bit = '1' for CSEx, CSCx and CSSSM; logic high for PWMy; HS current source active for CS1..8
X -> Do not care for CSEx, CSCx, CSSM and PWMy
Off -> Current source disabled

Please see Table 8-2 for the assignment between the three available PWM control ports PWM1..3 and the eight current source outputs CS1..8.

Table 8-2. Assignment of Current Sources to the PWMy Ports

PWM Port	CS1	CS2	CS3	CS4	CS5	CS6	CS7	CS8
PWM1	X	-	-	-	-	-	X	X
PWM2	-	X	-	-	X	X	-	-
PWM3	-	-	X	X	-	-	-	-

There is one common control bit for all current sources, the bit “CSSCD”. With this bit, the slope control of all eight sources can be disabled. By default, the slope control is activated and all currents are switched on and off smoothly (see also parameter $dU_{CSx,rise}$ and $dU_{CSx,fall}$). When setting this bit to '1', the current sources are enabled and disabled without transition times.

In order to change the configuration of a certain current source via SPI, it must be addressed and the current source programming bit CSPE must be set to '1'. Please see Table 8-3 for the eight available current sources.

Table 8-3. CS Port Addressing Table

Current Source on Pin	Bit CSA0	Bit CSA1	Bit CSA2
CS1, high- or lowside	0	0	0
CS2, high- or lowside	1	0	0
CS3, high- or lowside	0	1	0
CS4, highside only	1	1	0
CS5, highside only	0	0	1
CS6, highside only	1	0	1
CS7, highside only	0	1	1
CS8, highside only	1	1	1

That is, if any of the following configuration bits (CSE, CSSSM, CSIE, and CSC) of a certain I/O port shall be changed, the required data word for the SPI must contain the desired I/O number (bits CSA0..2) and the programming enable bit CSPE must be '1'. Only in this case, the corresponding bits in the SPI data word are loaded into the configuration register of the selected switch interface. For the global current source configuration bit CSSCD (slope control for current sources), the CSPE bit must be '0' in order to be changed via an SPI command. That is, either the four individual configuration bits (CSE, CSSSM, CSIE and CSC) or the global configuration bit (CSSCD) can be changed with one SPI command word.

Dependent on the selected current, the supply voltage, the externally applied load and the number of current sources activated, a not neglectable amount of power will be dissipated in Atmel® ATA664151. In order to protect the IC from damage, the current sources are equipped with thermal monitors. If the temperature in one of the monitors exceeds T_{jsd}, all current sources will be shut down and an interrupt will be generated. Note that the current source enabled bits (CSE) in the configuration register are not cleared by this event. That is, the current sources will be enabled after a certain cooling time.

8.2 Switch Inputs

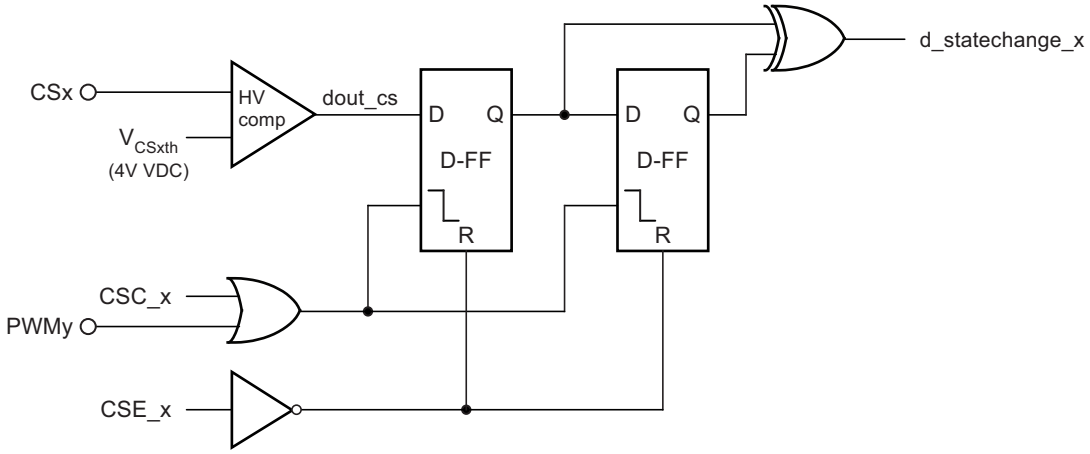
8.2.1 Voltage Comparators

Each switch input has a high voltage comparator, a state-change-detection register for wake-up and interrupt request generation and a voltage divider with a low-voltage output that can be fed through to the measurement pin VDIV.

In sleep mode, the HV comparators and the voltage dividers of each input are switched off. In active mode, the comparator of a channel is activated together with its current source. It has a threshold of V_{CSxth}. The output signal dout_csx of the comparator is debounced with a delay of t_{CSdeb}. A voltage above the threshold will generate a logical '1' in the status register bit CSxCS whereas a voltage below will lead to a '0'.

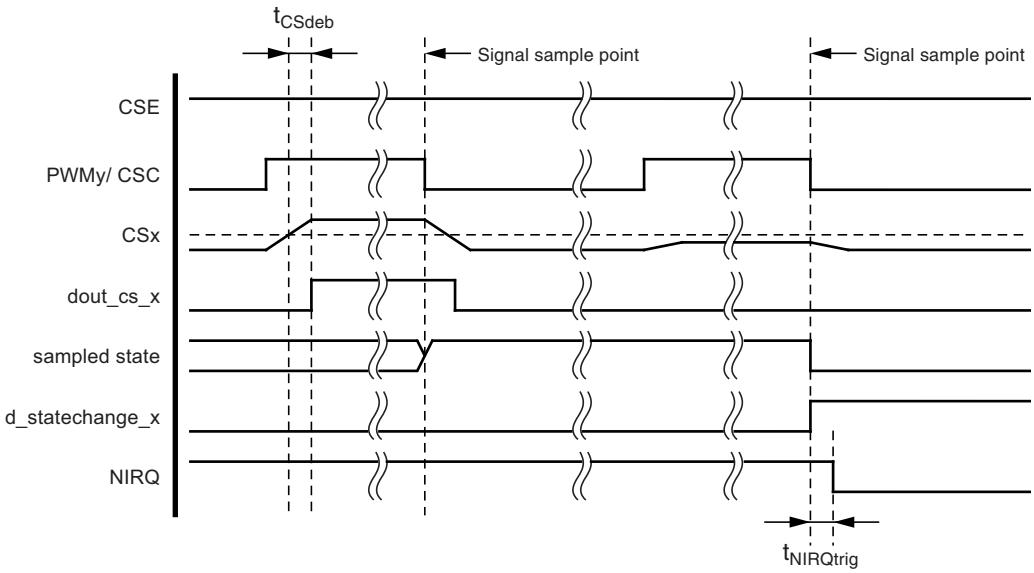
The comparator output signal is also fed into a state change detection logic that can be used to generate wake-up events in form of an interrupt request, signalized on pin NIRQ. Please see Figure 8-2 on page 25 for an overview of the state change detection unit.

Figure 8-2. State Change Detection Circuitry



As can be seen in Figure 8-2, the data from the comparator is latched with the falling edge of either the PWMy pin or the CSC bit. That is, the data is latched in the same moment when the current source is switched off. This ensures that the comparator signal was already stable when its output is evaluated. The output signal d_statechange is evaluated by the main control logic. If the interrupt enable bit CSIE is set in the configuration register and d_statechange is '1', an interrupt is generated and reported by a low level on pin NIRQ. Please see Figure 8-3 for an example of the state change detection system.

Figure 8-3. Interrupt Generation upon State Change



The output state of the HV comparator is sampled with each falling edge of the PWMy or CSC signal. As soon as the sampled state changes, an interrupt request is given.

In order to have minimum power consumption also for switch scanning applications, Atmel® ATA664151 is able to switch to active low-power Mode even if current sources are enabled with the CSEx bit in the configuration register. As long as the current source is inhibited (for example, by having CSCx programmed to 0 and PWMy also at low level), the IC can be in active low-power mode (dependent on the other peripherals, see also Table 4-1 on page 9). The current source is then in a kind of stand-by situation. As soon as the PWMy pin is raised, the IC switches to active mode with the defined current sources on.

8.2.2 Voltage Dividers

A voltage divider (division by 4) is included for each of the eight CS port channels. Please note that the divider is always referred to local ground (pin AGND), regardless of the respective current source/sink configuration. As there is only one output available for all voltage dividers of the chip, only one of them can be active at a time. The SPI data word must contain the following information in order to activate the voltage divider of a certain switch interface.

- The voltage divider enable bit VDIVE must be '1'.
- The VDIV programming source bit VDIVP must be '1'.
- The desired channel must be coded in the three address bits CSA0..2.

Please see Table 8-4 for a list of all voltage divider programming inputs and their corresponding VDIV output state.

Table 8-4. Voltage Divider Addressing Table

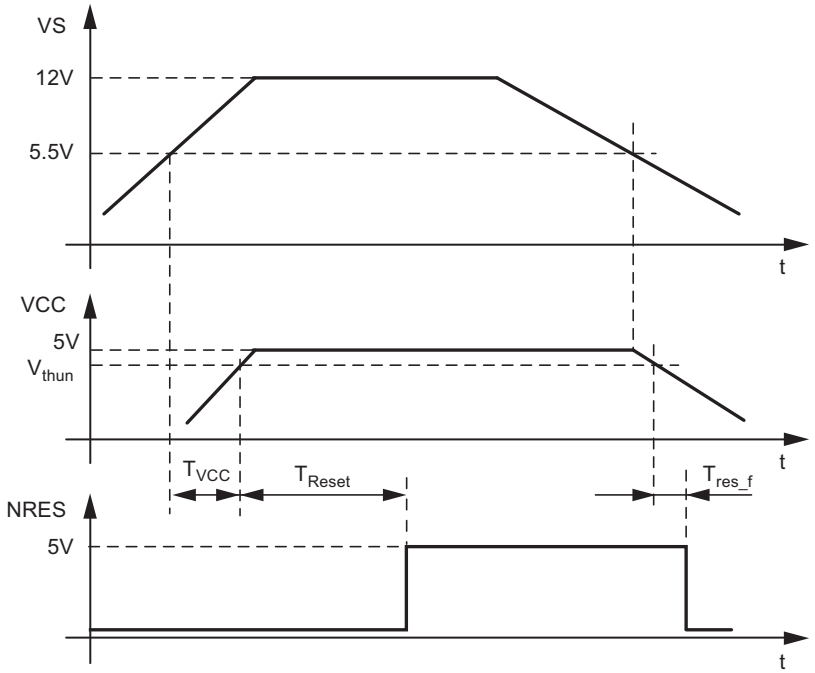
VDIVE	VDIVP	CSA2	CSA1	CSA0	VDIV
0	X	X	X	X	Off
1	0	X	X	X	VBATT / 4
1	1	0	0	0	CS1 / 4
1	1	0	0	1	CS2 / 4
1	1	0	1	0	CS3 / 4
1	1	0	1	1	CS4 / 4
1	1	1	0	0	CS5 / 4
1	1	1	0	1	CS6 / 4
1	1	1	1	0	CS7 / 4
1	1	1	1	1	CS8 / 4

Legend:
0 -> Bit = '0'
1 -> Bit = '1'
X -> Do not care

9. Voltage Regulator

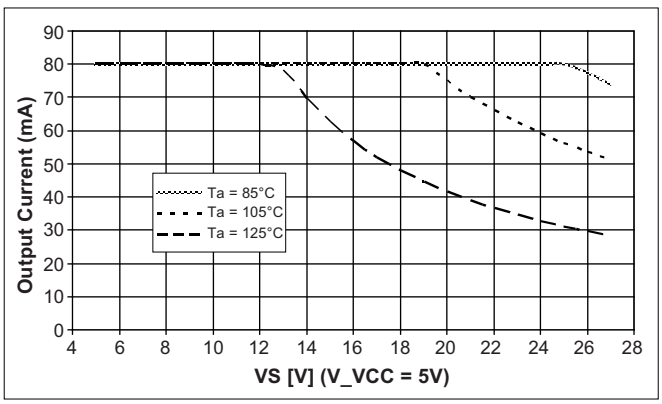
The VCC voltage regulator in Atmel® ATA664151 is a linear low-drop regulator and requires an external capacitor for compensation and for smoothing the disturbances in the microcontroller. It is mandatory to use a capacitor with C > 1.8µF and ESR of below 5Ω. An additional ceramic capacitor with C = 100nF is recommended for EMI suppression. The values of these capacitors can be varied depending on the application.

Figure 9-1. VCC Voltage Regulator: Ramp-up and Undervoltage Detection



The VCC output transistor is contributing to the ICs total power dissipation – defined by the voltage drop over the transistor and the output current I_{VCC}. In the figure below, the safe operating area of Atmel ATA664151 is shown. To avoid a thermal shutdown of the VCC output, the maximum load current decreases with rising ambient temperature and/or battery supply voltage. Please note also that the current sources contribute to power dissipation.

Figure 9-2. Power Dissipation: Safe Operating Area (SOA) of VCC Output Current versus Supply Voltages VS at Different Ambient Temperatures, Rthja = 40K/W and No Current Source (Pins CSx) Active



Because the VCC voltage generation is usually fundamental to system operation, there is a thermal prewarning implemented in the Atmel® ATA664151. The thermal monitor of the VCC output transistor can indicate a critical temperature condition of $T_{VCCprew}$ by means of an interrupt and the status bit OTVCC in the status register of the chip. The microcontroller can thus react to these events by shutting down external loads that use the VCC or reducing its own power consumption in order to avoid a thermal shutdown.

Nevertheless, if the junction temperature of the output transistor exceeds the shutdown threshold T_{jsd}, the transistor as well as the VCC are shut down until the temperature has decreased at least by $T_{jsdhyst}$. After this cooling-down period, the regulator starts again in the same way as when powering up or for a wake-up from sleep mode.

For microcontroller programming, it may be necessary to supply the VCC output via an external power supply. It is then mandatory to disconnect pin VS of the system basis chip, and an operation of Atmel ATA664151 is not possible.

10. Watchdog

The watchdog expects a trigger signal from the microcontroller at the NTRIG (negative edge) input within a time window of t_{wd}. The trigger signal must exceed a minimum time $t_{trigmin}$ > 7µs. If a triggering signal is not received, a reset signal will be generated at output NRES. The timing basis of the watchdog is provided by the internal watchdog oscillator. Its time period, t_{WDosc}, is adjustable via the external resistor R_{wd_osc} (34kΩ to 120kΩ).

During sleep mode the watchdog is switched off to reduce current consumption. In order to enter active low-power mode, the watchdog also needs to be disabled via the configuration register. In order to avoid false watchdog disabling, this configuration bit (WDD) needs to be written twice, i.e., with two consecutive SPI words in order to be altered to '1'.

In order to disable the watchdog right from the start (i.e., after external power-up or after sleep mode), pin VDIV has to be tied to VCC until the startup time t_{reset} of typ. 4ms has elapsed (see Section 3.14 “VDIV Input/Output Pin” on page 7).

The minimum time for the first watchdog pulse is required after the undervoltage reset at NRES disappears. It is defined as lead time t_d. After wake-up from sleep mode, the lead time t_d starts with the positive edge of the NRES output.

10.1 Typical Timing Sequence with R_{WD_OSC} = 51kΩ

The trigger signal T_{wd} is adjustable between 20ms and 64ms using the external resistor R_{WD_OSC}.

For example, with an external resistor of R_{WD_OSC} = 51kΩ ± 1%, the typical parameters of the watchdog are as follows.

$t_{osc} = 0.782 \times R_{WD_OSC} + 1.7 \times 10^{-6} \times (R_{WD_OSC})^2$ [R_{WD_OSC} in kΩ; t_{osc} in µs]

t_{OSC} = 39.9µs due to 51kΩ

$t_d = 3948 \times 39.9\mu s = 157.5ms$

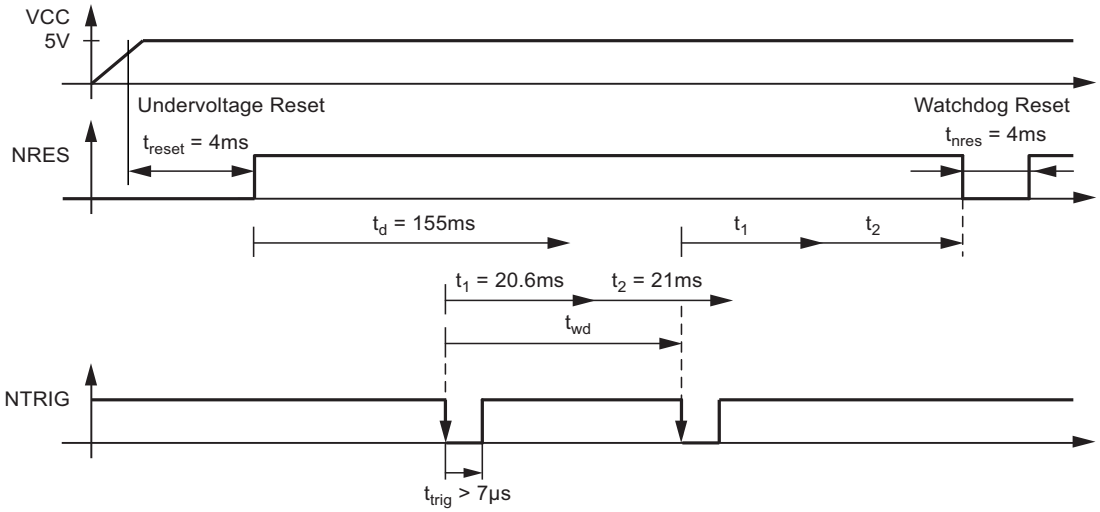
$t_1 = 553 \times 39.9\mu s = 22.1ms$

$t_2 = 527 \times 39.9\mu s = 21ms$

t_{nres} = constant = 4ms

After ramping up the battery voltage, the VCC regulator is switched on. The reset output NRES stays low for the time t_{reset} (typically 4ms), then it switches to high, and the watchdog waits for the trigger sequence from the microcontroller. The lead time, t_d, follows the reset and t_d = 155ms. In this time, the first watchdog pulse from the microcontroller is required. If the trigger pulse NTRIG occurs during this time, the time t_1 starts immediately. If no trigger signal occurs during the time t_d, a watchdog reset with t_{reset} = 4ms resets the microcontroller after t_d = 155ms. The times t_1 and t_2 have a fixed relationship. A triggering signal from the microcontroller is anticipated within the time frame of t_2 = 21.6ms. To avoid false triggering from glitches, the trigger pulse must be longer than $t_{TRIG,min}$ > 7µs. This slope restarts the watchdog sequence. If the triggering signal fails in this open window t_2, the NRES output is drawn to ground. A triggering signal during the closed window t_1 immediately switches NRES to low.

Figure 10-1. Timing Sequence with R_{WD_OSC} = 51kΩ



10.2 Worst Case Calculation with R_{WD_OSC} = 51kΩ

The internal oscillator has a tolerance of 20%. This means that t_1 and t_2 can also vary by 20%. The worst-case calculation for the watchdog period t_{wd} is as follows.

The ideal watchdog time t_{wd} is between the maximum t_1 and the minimum t_1 plus the minimum t_2.

$t_{1,min} = 0.8 \times t_1 = 16.8ms$, $t_{1,max} = 1.2 \times t_1 = 25.2ms$

$t_{2,min} = 0.8 \times t_2 = 17.7ms$, $t_{2,max} = 1.2 \times t_2 = 26.5ms$

$t_{wdmax} = t_{1min} + t_{2min} = 16.8ms + 17.7ms = 34.5ms$

$t_{wdmin} = t_{1max} = 25.2ms$

$t_{wd} = 29.9ms \pm 4.6ms$ (±15%)

A microcontroller with an oscillator tolerance of ±15% is sufficient to supply the trigger inputs correctly.

Table 10-1. Typical Watchdog Timings

R_{WD_OSC} kΩ	Oscillator Period t_{osc}/µs	Lead Time t_d/ms	Closed Window t_1/ms	Open Window t_2/ms	Trigger Period from Microcontroller t_{wd}/ms	Reset Time t_{nres}/ms
34	26.6	105	14.0	14.7	20.13	4
51	39.9	157.5	21	22.1	29.85	4
91	71.2	281	37.5	39.4	53.27	4
120	93.9	370.6	49.5	51.9	70.26	4

Note that in the case of a missing or shorted resistor on pin WDOSC, the watchdog oscillator period will be well below or above the reachable values listed above. In other words, if not disabled after startup by using the VDIV pin or during operation with the SPI configuration, a watchdog reset will be generated all the time for fail-safe reasons.

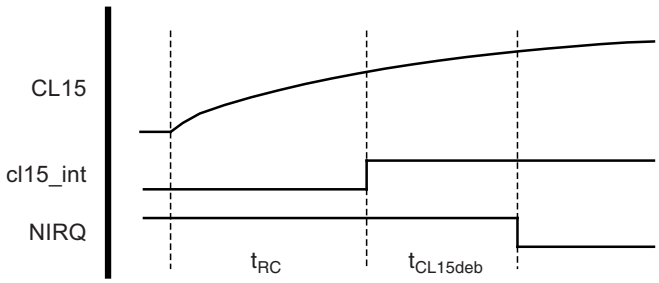
11. CL15 HV Input

The CL15 pin can be used as ignition state detection and wake-up input. It has a weak internal pull-down structure, so if no voltage is connected to this pin, it is at ground level, the passive state of this input. In order to generate an interrupt request or to wake-up from sleep mode, a certain voltage needs to be applied to this pin.

The input voltage threshold can be adjusted by varying the external resistor due to the input current I_{CL_15}. To protect this pin against voltage transients, a serial resistor of 10kΩ and a ceramic capacitor of 47nF are recommended. With this RC combination you can increase the wake-up time $t_{CL15deb}$ as well as enhance sensitivity against transients when ignition of the CL15 pin occurs.

You can also increase the wake-up time using external capacitors with higher values. In Figure 11-1, the reaction of the Atmel® ATA664151 to a signal at the CL15 pin is shown. Note that the pin is connected via an R/C low-pass filter.

Figure 11-1. Timing for CL15 Debouncing



In the diagram above, the voltage at the CL15 pin is shown. Due to the R/C filter, the voltage does not immediately increase but instead slowly over time. As soon as the voltage exceeds approximately 3V, the internal debouncing time $t_{CL15deb}$ starts. After this elapses, a wake-up is indicated by a falling edge on the NIRQ pin.

12. Fail-safe Features

- During a short-circuit at LIN to $V_{Battery}$, the output current is limited to I_{BUS_lim}. Due to power dissipation, the chip temperature might exceed T_{LINoff}, causing a shutdown of the LIN output transistor. That in turn starts the chip cooling phase, and after a hysteresis of T_{hys} the output can be switched on again with TXD = 0. During shutdown, RXD indicates the LIN bus state, which is typically recessive because the output transistor is off. Please note that the VCC voltage regulator works independently from the LIN output transistor temperature monitor because it is equipped with its own monitor.
- During a short-circuit at LIN to GND, the IC can be switched to sleep mode. If the short-circuit disappears, the IC starts with a remote wake-up.
- The reverse current is very low < 2µA at the LIN pin during loss of V_{Batt}. This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.
- During a short circuit at VCC, the output limits the output current to I_{VCClim}. Because of undervoltage, NRES switches to low and can therefore reset the connected microcontroller. If the chip temperature of the VCC output transistor exceeds the value T_{VCCoff}, the VCC output switches off. The chip cools down and after a hysteresis of T_{hys}, the output is reactivated.
- The NCS pin provides a pull-up resistor to force the SPI output into tri-state mode if NCS is disconnected
- The TXD pin provides a pull-up resistor to force the transceiver into recessive mode if TXD is disconnected.
- If the WDOSC pin has a short-circuit to GND or the resistor is disconnected, the watchdog runs with an internal oscillator and ensures a reset takes place.
- If there is no NTRIG signal and short circuit at WDOSC, the NRES switches to low after $t_{WDOfshi}$. For an open circuit (no resistor) at WDOSC it switches to low after $t_{WDOfslo}$.
- The watchdog disable bit WDD in the configuration register needs to be written twice in order to take effect. This avoids unwanted watchdog shutdowns due to data misinterpretation caused by EMI.
- If the IREF pin has a short-circuit to GND or the resistor is disconnected/shorted to VCC, the current sources run with an internal reference current which guarantees basic functionality of the application.

13. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Maximum voltage on supply pin VS[1)]	$V_{sup,Stby}$	–0.4		+40	V
Operating supply voltage (load dump) Pulse time ≤ 500ms T_a = 25°C VCC output current I_{VCC} ≤ 50mA[1)]	$V_{sup,ldump}$			+40	V
Operating supply voltage (jump start) Pulse time ≤ 2min T_a = 25°C Output current I_{VCC} ≤ 50mA[1)]	$V_{sup,jstart}$			27	V
Voltage levels on pins - CS1-8 - CL15 (with 10kΩ/47nF) -> DC voltage[1)] -> Transient voltage due to ISO7637 (coupling via 1nF)		 –2 –150		 +40 +100	 V V
Voltage levels on pins[1)] - LIN - VBATT (with 51Ω/10nF) -> DC voltage		–27		+40	V
Voltage levels on logic/low-voltage pins: RXD, TXD, NRES, NTRIG, WDOSC, PWMy, VDIV, NCS, SCK, MOSI, MISO		–0.4		V_{VCC} + 0.4V	V
Voltage levels on pin VCC	V_{VCC}	–0.4		+5.5	V
ESD according to IBEE LIN EMC Test spec. 1.0 following IEC 61000-4-2 - Pin VS (100nF) to GND - Pin LIN (220pF) to GND - Pin CL15 (10kΩ, 47nF) to GND - Pin VBATT (10nF) to GND - Pins CSx (10nF) to GND		±6			kV
HBM ESD according to ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002) MIL-STD-883 (M3015.7)		±2			kV
CDM ESD according to STM 5.3.1		±750			V
MM ESD according to EIA/JESD22-A115 ESD STM5.2 AEC-Q100 (002)		±200			V

Note: 1. Voltage between any of following pins **must not exceed** 40V: VS, VBATT, CL15, CSx, LIN

13. Absolute Maximum Ratings (Continued)

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
ESD HBM following STM5.1 with 1.5kΩ, 150pF - Pins VS, LIN, CL15 to GND		±8			kV
Junction temperature	T_j	–40		+150	°C
Storage temperature	T_s	–55		+150	°C

Note: 1. Voltage between any of following pins **must not exceed** 40V: VS, VBATT, CL15, CSx, LIN

14. Thermal Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction to heat slug	R_{thjc}		10		K/W
Thermal resistance junction to ambient, where heat slug is soldered to PCB according to Jedec	R_{thja}		35		K/W
Thermal prewarning threshold of VCC regulator temperature monitor	$T_{VCCPreW}$	120		140	°C
Thermal shutdown threshold of all temperature monitors	T_{jsd}	150	165	185	°C
Thermal shutdown hysteresis	$T_{jsdhyst}$	10	17	25	K

15. Electrical Characteristics

5V < V_S < 27V, –40°C < T_j < 150°C, chip configuration as default, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	VS Pin								
1.1	Nominal DC voltage range for full operation		VS	V_S	5		27	V	B
1.2	Supply current in Sleep Mode	V_{LIN} > V_S – 0.5V V_S ≤ 14V (T_j = 25°C)	VS	$I_{VSsleep}$	4	8	12	µA	B
		V_{LIN} > V_S – 0.5V V_S ≤ 14V (T_j = 125°C)	VS	$I_{VSsleep}$	4	11	18	µA	A
		Sleep mode Bus shorted to GND	VS	$I_{VSsleep_short}$		20	35	µA	A
1.3	Supply current in active low-power mode, all peripherals off	V_{LIN} > V_S – 0.5V V_S ≤ 14V (T_j = 25°C) Without load at VCC	VS	I_{VSact_lp}		33	45	µA	B
		V_{LIN} > V_S – 0.5V V_S ≤ 14V (T_j = 125°C) Without load at VCC	VS	I_{VSact_lpt}		40	55	µA	A
		LIN-bus shorted to GND	VS	$I_{VSact_lp_short}$		55	80	µA	B
1.4	Supply current in active mode after startup (WD active), no VCC load	V_{LIN} > V_S – 0.5V V_{VS} ≤ 14V	VS	I_{VSact_wd}		120	200	µA	A
1.5	Supply current in active mode after startup (WD active), high VCC load	Bus recessive V_{VS} = 14V I_{VCC} = –45mA	VS	I_{VSdom}	45.1		46	mA	A
1.10	Supply current in different active modes	Bus recessive V_{VS} = 14V I_{VCC} = 0 R_IREF = 5.6kΩ	VS	I_{VSact_wd} I_{VSact_lin} I_{VSact_cs} I_{VSact_vdiv}		185 300 2600 300		µA	D
1.7	VS undervoltage thresholds	Status bit VSS = 1	VS	V_{VSthU}	4.0		4.4	V	A
		Status bit VSS = 0	VS	V_{VSthO}	4.3		4.95	V	A
1.8	VS undervoltage threshold hysteresis	V_{VSthO} – V_{VsthU}	VS	V_{VSth_hyst}	0.19	0.4	0.65	V	A
1.9	Minimum VS operation voltage	VCC active, SPI operational	VS	$V_{VSopmin}$			3.8	V	A
2	RXD Output Pin								
2.1	Low-level output sink capability	I_{RXD} = 2mA	RXD	$V_{RXDsink}$			0.4	V	A
2.2	High-level output source capability	I_{RXD} = –2mA	RXD	$V_{RXDsource}$	V_{VCC} – 0.4V			V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

15. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C, chip configuration as default, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3	TXD Input Pin								
3.1	Maximum voltage level for logic “low”		TXD	$V_{TXDL,max}$			0.33 x V_{VCC}	V	A
3.2	Minimum voltage-level for logic “high”		TXD	$V_{TXDH,min}$	0.66 x V_{VCC}			V	A
3.3	Pull-up resistor	V_{TXD} = 0V, V_{VCC} = 5V	TXD	R_{TXD}	40	90	140	kΩ	A
3.4	Input leakage current	V_{TXD} = V_{VCC}	TXD	$I_{TXDleakH}$			+1	µA	A
4	NIRQ Output Pin (Open Drain)								
4.1	Low-level output sink capability	I_{IRQ} = 2mA	NIRQ	$V_{IRQsink}$			0.4	V	A
4.2	High-level input leakage current	V_{NIRQ} = V_{VCC}	NIRQ	$I_{NIRQleak,H}$			1	µA	A
4.3	NIRQ pin pull-up resistor value	V_{NIRQ} = 0V	NIRQ	R_{NIRQ}	60	100	200	kΩ	A
5	NTRIG Watchdog Input Pin								
5.1	Maximum voltage level for logic “low”		NTRIG	$V_{NTRIGL,max}$			0.33 × V_{VCC}	V	A
5.2	Minimum voltage-level for logic “high”		NTRIG	$V_{NTRIGH,min}$	0.66 × V_{VCC}			V	A
5.3	Pull-up resistor	V_{NTRIG} = 0V, V_{VCC} = 5V	NTRIG	R_{NTRIG}	40	90	140	kΩ	A
5.4	Input leakage current	V_{NTRIG} = V_{CC}	NTRIG	$I_{NTRIGleakH}$			+1	µA	A
5.5	Minimum NTRIG pulse width for watchdog trigger		NTRIG	t_{trig}	7			µs	B
7	LIN-bus Driver								
7.1	Driver recessive output voltage	External LIN pull-up ≤ 1kΩ	LIN	V_{BUSrec}	0.9 × V_S		V_S	V	B
7.2	Driver dominant voltage	V_{VS} = 7V R_{Bus} = 500Ω	LIN	$V_{BUSLoSUP,max}$			1.2	V	A
7.3	Driver dominant voltage	V_{VS} = 18V R_{Bus} = 500Ω	LIN	$V_{BUSHiSUP,max}$			2	V	A
7.4	Driver dominant voltage	V_{VS} = 7.0V R_{load} = 1000Ω	LIN	$V_{BUSLoSUP,min}$	0.6			V	A
7.5	Driver dominant voltage	V_{VS} = 18V R_{load} = 1000Ω	LIN	$V_{BUSHiSUP,min}$	0.8			V	A
7.6	Internal pull-up resistor to VS	Resistor has a serial rectifier diode	LIN	R_{LIN}	20	30	47	kΩ	A
7.7	Voltage drop at the serial diodes	In pull-up path with R_{slave} $I_{SerDiode}$ = 10mA	LIN	$V_{SerDiode}$	0.4		1.0	V	D
7.8	LIN current limitation V_{BUS} = V_{Batt_max}		LIN	I_{BUS_LIM}	70	120	200	mA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

15. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C, chip configuration as default, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7.9	Leakage current at loss of ground(1)	Module-GND disconnected $V_S = V_{BAT} = 0V$ $V_{LIN} = -18V$	LIN	$I_{BUS_No_Gnd}$	–20		+20	µA	A
7.10	Leakage current at loss of battery(1)	Battery disconnected $V_S = V_{BAT} = 0V$ $0V \le V_{LIN} \le 18V$	LIN	$I_{BUS_No_VS}$			2	µA	A
	Note: 1. Bus communication must not be affected if the module gets disconnected from ground or from battery. Parameters 7.9 and 7.10 cover these LIN specification topics.								
8	LIN bus Receiver								
8.1	Center of receiver threshold	$V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2$ $7V \le V_S \le 27V$	LIN	V_{BUS_CNT}	$0.475 \times V_S$	$0.5 \times V_S$	$0.525 \times V_S$	V	A
8.2	Maximum allowed bus voltage to be detected as dominant state by receiver		LIN	$V_{BUS_dom,max}$			$0.4 \times V_S$	V	A
8.3	Minimum allowed bus voltage to be detected as recessive state by receiver		LIN	$V_{BUSr_ec,min}$	$0.6 \times V_S$			V	A
8.4	Receiver input hysteresis	$V_{hys} = V_{th_rec} - V_{th_dom}$	LIN	V_{BUS_hys}	$0.028 \times V_S$	$0.1 \times V_S$	$0.175 \times V_S$	V	A
8.5	Dominant state receiver input current	Input leakage current Driver off $V_{BUS} = 0V$ $V_S = 12V$	LIN	$I_{BUS_PAS_dom}$	–1	–0.35	–0.2	mA	A
8.6	Recessive state receiver input current	Driver off (recessive state) $V_{Batt} = 18V$ $V_{BUS} = 18V$ $V_{BUS} = 40V$	LIN	$I_{BUS_PAS_rec1}$ $I_{BUS_PAS_rec2}$			11 25	µA	B A
8.7	LIN Pre-wake detection High-level input voltage		LIN	V_{LIN_preH}	$V_S - 2V$		$V_S + 0.3V$	V	A
8.8	LIN Pre-wake detection Low-level input voltage	Activates the LIN receiver	LIN	V_{LIN_preL}	–27		$V_S - 3.3V$	V	A
8.9	LIN Receiver enabling time	Time between rising edge on NCS and receiver ready	RXD	$t_{RXDinvalid}$			15	µs	D
9	Internal Timers								
9.1	Dominant time for wake-up via LIN-bus	$V_{LIN} = 0V$	LIN	t_{bus}	70	90	150	µs	B
9.2	Time delay for LIN TRx enable from active mode via SPI	Delta between NCS high and TXD/RXD transparent	CSN RXD	t_{norm}	2.5		10	µs	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

15. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C, chip configuration as default, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9.3	Time delay for mode change from active mode to sleep mode via SPI	Delta between NCS high and LIN-TRx offline	CSN RXD	t_{sleep}	2.5		10	µs	D
9.4	TXD dominant time-out timer		TXD	t_{dom}	30	40	56	ms	B
9.5	Time delay for mode change from active low-power mode into normal mode via SPI	Delta between CSN high and TXD/RXD transparent	CSN RXD	t_{s_n}	2.5	6	15	µs	D
9.11	TXD time-out timer release time	Time for which TXD must be at least at high level after a dominant state time-out	TXD	t_{TOrel}	10			µs	B
9.12	Monitoring time for wake-up via LIN bus		LIN	t_{mon}	8		14	ms	A
	LIN-bus Driver AC Parameters with Different Bus Loads Load 1 (small): 1nF, 1kΩ Load 2 (large): 10nF, 500Ω; C_{RXD} = 20pF; Load 3 (medium): 6.8nF, 660Ω characterized on samples; 9.6 and 9.7 specifies the timing parameters for proper operation of 20Kbit/s, 9.8 and 9.9 at 10.4Kbit/s								
9.6	Duty cycle 1	$TH_{Rec(max)} = 0.744 \times V_S$ $TH_{Dom(max)} = 0.581 \times V_S$ V_S = 7V to 18V t_{Bit} = 50µs D1 = $t_{bus_rec(min)}/(2 \times t_{Bit})$	LIN	D1	0.396				B
9.7	Duty cycle 2	$TH_{Rec(min)} = 0.422 \times V_S$ $TH_{Dom(min)} = 0.284 \times V_S$ V_S = 7.6V to 18V t_{Bit} = 50µs D2 = $t_{bus_rec(max)}/(2 \times t_{Bit})$	LIN	D2			0.581		B
9.8	Duty cycle 3	$TH_{Rec(max)} = 0.778 \times V_S$ $TH_{Dom(max)} = 0.616 \times V_S$ V_S = 7.0V to 18V t_{Bit} = 96µs D3 = $t_{bus_rec(min)}/(2 \times t_{Bit})$	LIN	D3	0.417				B
9.9	Duty cycle 4	$TH_{Rec(min)} = 0.389 \times V_S$ $TH_{Dom(min)} = 0.251 \times V_S$ V_S = 7.6V to 18V t_{Bit} = 96µs D4 = $t_{bus_rec(max)}/(2 \times t_{Bit})$	LIN	D4			0.590		B
9.10	Slope time falling and rising edge at LIN	V_S = 7V	LIN	t_{SLOPE_fall} t_{SLOPE_rise}	3.5		22.5	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

15. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C, chip configuration as default, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10	Receiver Electrical AC Parameters of the LIN Physical Layer LIN Receiver, RXD Load Conditions (C_{RXD}): 20pF								
10.1	Max propagation delay of receiver	V_S = 7.0V to 18V t_{rx_pd} = max(t_{rx_pdrise}, t_{rx_pdfall})	RXD	t_{rx_pd}			6	µs	A
10.2	Symmetry of receiver propagation delay rising edge minus falling edge	V_S = 7.0V to 18V t_{rx_sym} = t_{rx_pdr} – t_{rx_pdf}	RXD	t_{rx_sym}	–2		+2	µs	A
11	NRES Open Drain Output Pin								
11.1	Low-level output sink capability	I_{NRES} = 2mA	NRES	$V_{NRESsink}$			0.4	V	A
11.2	Low-level at low VCC	V_{VCC} = 2.5V I_{NRES} = 500µA	NRES	V_{NRESLL}			0.4	V	A
11.3	VCC power-up reset time	V_S ≥ 5.5V C_{NRES} = 20pF	NRES	$t_{UVreset}$	2	4	6	ms	B
11.4	Reset debounce time for falling edge at VCC	V_S ≥ 5.5V C_{NRES} = 20pF	NRES	$t_{NRESfall}$	1.5		10	µs	A
11.5	High level input leakage current	V_{NRES} = V_{VCC}	NRES	$I_{NRESLeakH}$			1	µA	A
11.6	NRES pin pull-up resistor value	V_{NRES} = 0	NRES	R_{NRES}	60	100	200	kΩ	A
12	Watchdog Oscillator								
12.1	Voltage at WDOSC in Active Mode, WDO enabled	34kΩ ≤ R_{WDOSC} ≤ 120kΩ V_{VS} ≥ 4V	WDOSC	V_{WDOSC}	1.13	1.23	1.33	V	A
12.2	WDOSC load regulation	dV_{WDOSC} = $V_{WDOSC,34k}$ – $V_{WDOSC,120k}$	WDOSC	dV_{WDOSC}	–20		+20	mV	A
12.3	Oscillator period	R_{OSC} = 34kΩ		$t_{WDOSC,low}$	21.3	26.6	31.9	µs	A
12.4	Oscillator period	R_{OSC} = 120kΩ		$t_{WDOSC,hi}$	75.1	93.9	102	µs	A
12.5	Watchdog oscillator fail-safe periods	WDOSC = 0V WDOSC = open		$t_{WDOfshi}$ $t_{WDOfslo}$	4.5 104		18 200	µs	D
13	Watchdog Window and Reset Timing								
13.1	Watchdog lead time after reset	Cycles are relative to t_{WDOSC}		t_{WDlead}		3948		cycles	B
13.2	Watchdog closed window	Cycles are relative to t_{WDOSC}		$t_{WDclose}$		527		cycles	B
13.3	Watchdog open window	Cycles are relative to t_{WDOSC}		t_{WDopen}		553		cycles	B
13.4	Watchdog reset time NRES		NRES	t_{WDnres}	3	4	6	ms	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

15. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C, chip configuration as default, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
14	CL15 Pin								
14.1	High-level input voltage threshold	SPI status bit ‘CL15S’ readback as ‘1’	CL15	V_{CL15H}	4.5			V	A
14.2	Low-level input voltage threshold	SPI status bit ‘CL15S’ readback as ‘0’	CL15	V_{CL15L}			2	V	A
14.3	CL15 pull-down current	V_S ≤ 27V V_{CL15} = 27V	CL15	I_{CL15}		50	100	µA	A
14.4	Internal debounce time	Without external capacitor	CL15	$t_{CL15deb}$	80	160	250	µs	B
14.5	Hysteresis of input voltage comparator	$V_{CL15H} – V_{CL15L}$	CL15	$V_{CL15hsyt}$	0.5	1	1.5	V	A
17	VCC Voltage Regulator in Active Mode								
17.1	Output voltage VCC	5.5V < V_S < 18V (0mA to 50mA)	VCC	V_{VCCnor}	4.9		5.1	V	A
		6.5V < V_S < 18V (0mA to 80mA)	VCC	V_{VCCnor}	4.9		5.1	V	C
17.2	Output voltage VCC at low VS	3V < V_S < 5.5V	VCC	V_{VCClow}	2.3		5.1	V	A
17.3	Regulator drop voltage for medium load	V_S > 4V I_{VCC} = –20mA $V_{VCCdrop} = V_{VS} – V_{VCC}$	VS, VCC	$V_{VCCdrop1}$			250	mV	A
17.4	Regulator drop voltage for high load	V_S > 4V I_{VCC} = –50mA $V_{VCCdrop} = V_{VS} – V_{VCC}$	VS, VCC	$V_{VCCdrop2}$		400	600	mV	A
17.6	Line regulation	5.5V < V_S < 18V	VCC	VCC_{line}			0,8	%	B
17.7	Load regulation	5mA < I_{VCC} < 50mA 100kHz	VCC	VCC_{load}		0.2	0.8	%	B
17.8	Output current limitation	VS > 5.5V	VCC	I_{VCClim}	–240	–120	-80	mA	A
17.9	External load capacity	ESR < 5Ω at f = 100kHz	VCC	V_{thunN}	1.8	2.2		µF	D
17.10	VCC undervoltage threshold	Referred to VCC V_S > 5.5V	VCC	V_{VCCuv}	2.7		3.1	V	A
17.11	Hysteresis of undervoltage threshold	Referred to VCC V_S > 5.5V	VCC	V_{VCCuv_hys}	190	300	400	mV	A
17.12	Ramp-up time V_S > 5.5V to V_{CC} = 5V	C_{VCC} = 2.2µF I_{load} = –5mA at VCC	VCC	t_{VCC}		400	700	µs	A
18	Battery Voltage Divider								
18.1	Divider ratio		VDIV	r_{div_5V}		1 : 4			D
18.2	Divider precision	V_{VBATT} = 6 to 19V	VDIV	p_{VBATT}	–2		+2	%	A
18.3	Divider resistance	V_{VBATT} = 12V	VBATT	R_{VBATT}	44		120	kΩ	A
18.4	Input leakage current with disabled divider	V_{VBATT} ≤ 27V	VBATT	$I_{VBATTleak}$		0.1	1	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

15. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C, chip configuration as default, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
19	LIN Driver in High-speed Mode (All Tests Using R_{LIN} = 500Ω, C_{LIN} = 600pF)								
19.1	Transmission bit rate	V_{VS} = 7V to 18V	LIN	SP	200			kBit/s	C
19.2	Slope time LIN falling edge	V_{VS} = 7V to 18V	LIN	$t_{HSslope_fall}$	0.3	1	2	µs	A
19.3	Slope time LIN rising edge, depending on RC-load	V_{VS} = 7V to 18V	LIN	$t_{HSslope_rise}$	0.5	2	3	µs	A
20	Switch Interface Unit (CS1-8, IREF)								
20.1	Maximum highside output current	$V_{VS} – V_{CSx} ≥ 2.6V$ $V_{VS} ≥ 7V$ I_{IREF} = –300µA	CSx	$I_{CSx,maxH}$	–35		–20	mA	A
20.2	Maximum lowside output current	$V_{CSx} ≥ 2.6V$ $V_{VS} ≥ 7V$ I_{IREF} = –300µA	CSx	$I_{CSx,maxL}$	20		35	mA	A
20.3	Current source multiplier from reference current I_{IREF}, IMUL=100	$V_{VS} ≥ 7V$ $V_{CSx,HS} = V_{VS} – 2.6V$ I_{IREF} = –200µA	CSx	rI_{CS_H}	95	100	105		A
20.4	Current source multiplier from reference current I_{IREF}, IMUL=50	$V_{VS} ≥ 7V$ $V_{CSx,HS} = V_{VS} – 2.6V$ I_{IREF} = –200µA	CSx	rI_{CS_L}	47.5	50	52.5		A
20.5	Switch input comparator threshold		CSx	V_{CSxth}	3.6		4.4	V	A
20.6	Switch input comparator hysteresis		CSx	$V_{CSxhyst}$	200	300	500	mV	A
20.7	Current source rising voltage slope	V_{VS} = 14V I_{IREF} = 100µA R_{CSx} = 1kΩ 25% to 90%	CSx	$dU_{CSx,rise}$	0.7		8	V/µs	C
20.8	Current source falling voltage slope	V_{VS} = 14V I_{IREF} = 100µA V_{CSx} = 0V 90% to 25%	CSx	$dU_{CSx,fall}$	0.7		8	V/µs	C
20.22	Current source rising voltage slope, slope control disabled	V_{VS} = 14V I_{IREF} = 10µA R_{CSx} = 1kΩ 25% to 90% CSSCD = 1	CSx	$dU_{CSx0,risefast}$	6.5		22	V/µs	C
20.23	Current source falling voltage slope, slope control disabled	V_{VS} = 14V I_{IREF} = 100µA V_{CSx} = 0V 90% to 25% CSSCD = 1	CSx	$dU_{CSx,fallfast}$	6.5		30	V/µs	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

15. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C, chip configuration as default, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
20.9	Output voltage on IREF pin	V_{VS} ≥ 7V 10µA ≤ I_{IREF} ≤ 250µA At least one current source active	IREF	V_{IREF}	1.19	1.23	1.27	V	A
20.10	Internally generated IREF fail-safe current in case of open or shorted IREF pin	V_{IREF} = 0V I_{IREF} = 0µA	IREF	I_{IREFfs}	60 60		140 140	µA	A
20.11	Switch input debouncing time	Time from voltage level change on pin CSx to signal state change visible in SPI register	CSx	t_{CSxdeb}	2		13	µs	B
20.12	Switch input leakage current	Current source and voltage divider off V_{CSx} = 0 V V_{CSx} = V_{VS}	CSx	$I_{CSx,leak}$	–3		+3	µA	A
20.13	Current source enabling time	V_{VS} = 14V V_{CSx} = 0V(H)/V_{CSx} = 14V(L) I_{IREF} = 100µA Test time until abs(I_{CSx}) ≥ 9.5mA	CSx	t_{CSxon}	3		10	µs	A
20.14	Current source shutdown time	V_{VS} = 14V V_{CSx} = 0V(H)/V_{CSx} = 14V(L) I_{IREF} = 100µA Test time until abs(I_{CSx}) ≤ 0.5mA	CSx	$t_{CSx,off}$	3		12	µs	A
20.15	Voltage divider resistance	V_{CSx} = 4V	CSx	R_{CSxdiv}	50	95	150	kΩ	A
20.16	Voltage divider precision	V_{CSx} = 4V	CSx	p_{CSxdiv}	–3		+3	%	A
20.17	Maximum current source switching frequency		CSx	fCSx,max			20	kHz	D
20.18	Maximum voltage level for logic “low”		PWM1..3	$V_{PWML,max}$			0.33	V_{VCC}	A
20.19	Minimum voltage-level for logic “high”		PWM1..3	$V_{PWMH,min}$	0.66			V_{VCC}	A
20.20	PWM input leakage current, low level	V_{PWMy} = 0	PWM1..3	$I_{PWMleakL}$	–1			µA	A
20.21	PWM input pull-down resistor value	V_{PWMy} = V_{VCC}	PWM1..3	R_{PWM}	60	100	220	kΩ	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

15. Electrical Characteristics (Continued)

5V < V_S < 27V, –40°C < T_j < 150°C, chip configuration as default, unless otherwise specified. All values refer to GND pins

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
21	Serial Programming Interface and Control Logic (SPI)								
21.1	Maximum input clock frequency	$f_{SPI} = 1/T_{SCK}$ C_MISO ≤ 140pF (external)	SCK	$f_{SPI,max}$			4	MHz	D
21.2	Maximum input signal low level threshold		MOSI SCK NCS	$V_{SPIL,max}$			0.33 x V_{VCC}	V	A
21.3	Minimum input signal high level threshold		MOSI SCK NCS	$V_{SPIH,min}$	0.66 x V_{VCC}			V	A
21.4	Input pin leakage current	$V_{MOSI} = V_{SCK} = V_{NCS} = V_{VCC}$ $V_{MOSI} = V_{SCK} = 0$	MOSI SCK NCS MOSI SCK	$I_{Leak,H}$ I_{LeakL}	 –1 –1		+1 +1 +1	µA	A
21.5	NCS pin pull-up resistor	$V_{NCS} = 0$; $V_{VCC} = 5V$	NCS	R_{NCS}	60	120	200	kΩ	A
21.6	Output low level sink capability	I_{MISO} = 2mA	MISO	$V_{MISOsink}$			0.4	V	A
21.7	Output high level source capability	I_{MISO} = –2mA	MISO	$V_{MISOsource}$	V_{VCC} – 0.4			V	A
21.8	MISO pin tristate input leakage current	$V_{NCS} = V_{VCC}$ $V_{MISO} = V_{VCC}/2$	MISO	$I_{MISOleak}$	–1		+1	µA	A
21.9	Chip select minimum setup time (-> earliest time to start clocking)		NCS	$t_{SPIsetup,min}$			250	ns	D
21.10	Chip select minimum hold time (-> earliest time after clocking to release chip select)		NCS	$t_{SPIhold,min}$			250	ns	D
21.11	Minimum SPI data evaluation time (-> minimum time between positive and negative edge of chip select)		NCS	$t_{SPIeval,min}$	8		14	µs	D
21.12	Interrupt triggering delay		NIRQ	$t_{NIRQtrig}$	2		7	µs	B
21.13	SPI clock duty cycle limits	t_{SCK_H}/T_{SCK}	SCK	d_{SCK}	0.4		0.6		D
21.14	Propagation delay from SPI clock to MISO data output	C_MISO ≤ 140pF (external)	SCK MISO	$t_{CLK2DATA}$	10		120	ns	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

16. Application Information

Figure 16-1. Definition of Bus Timing Characteristics

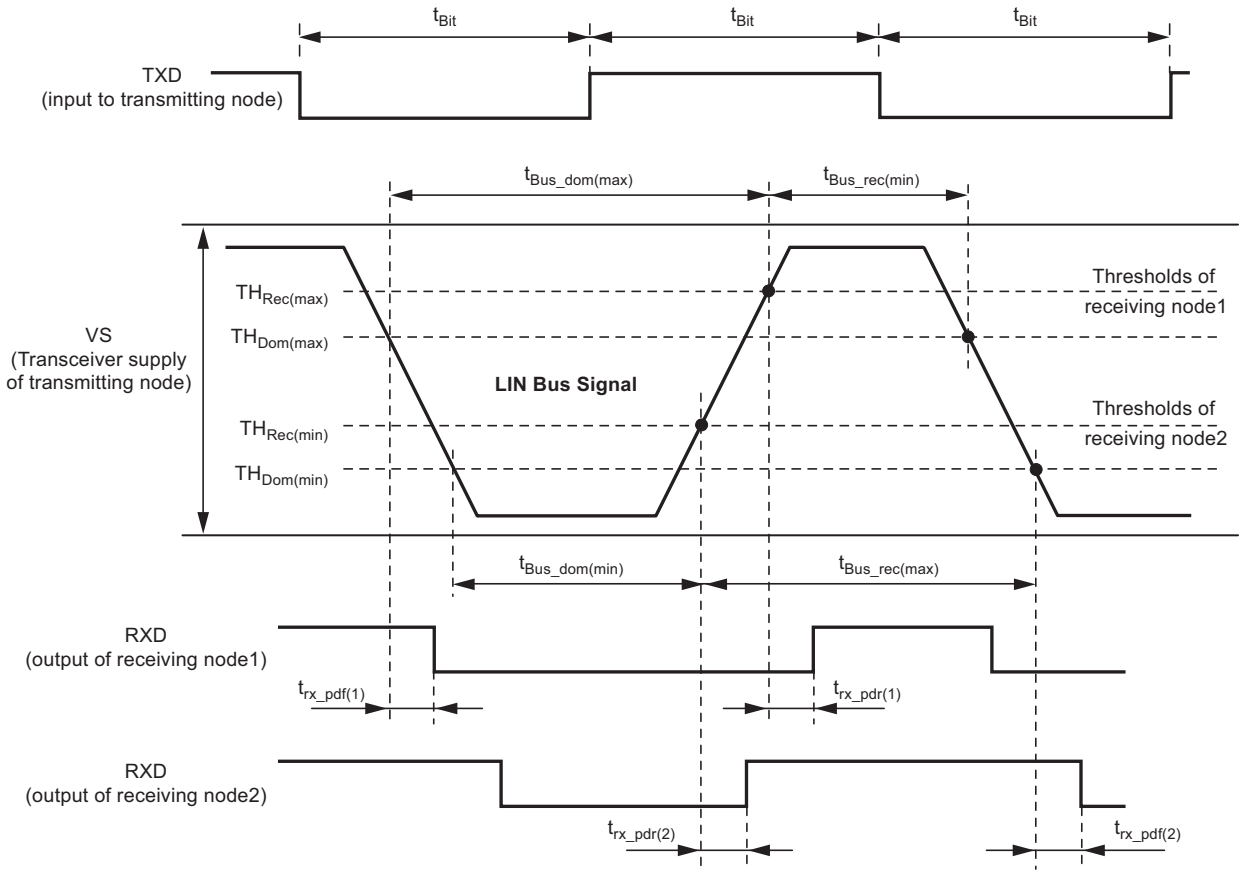
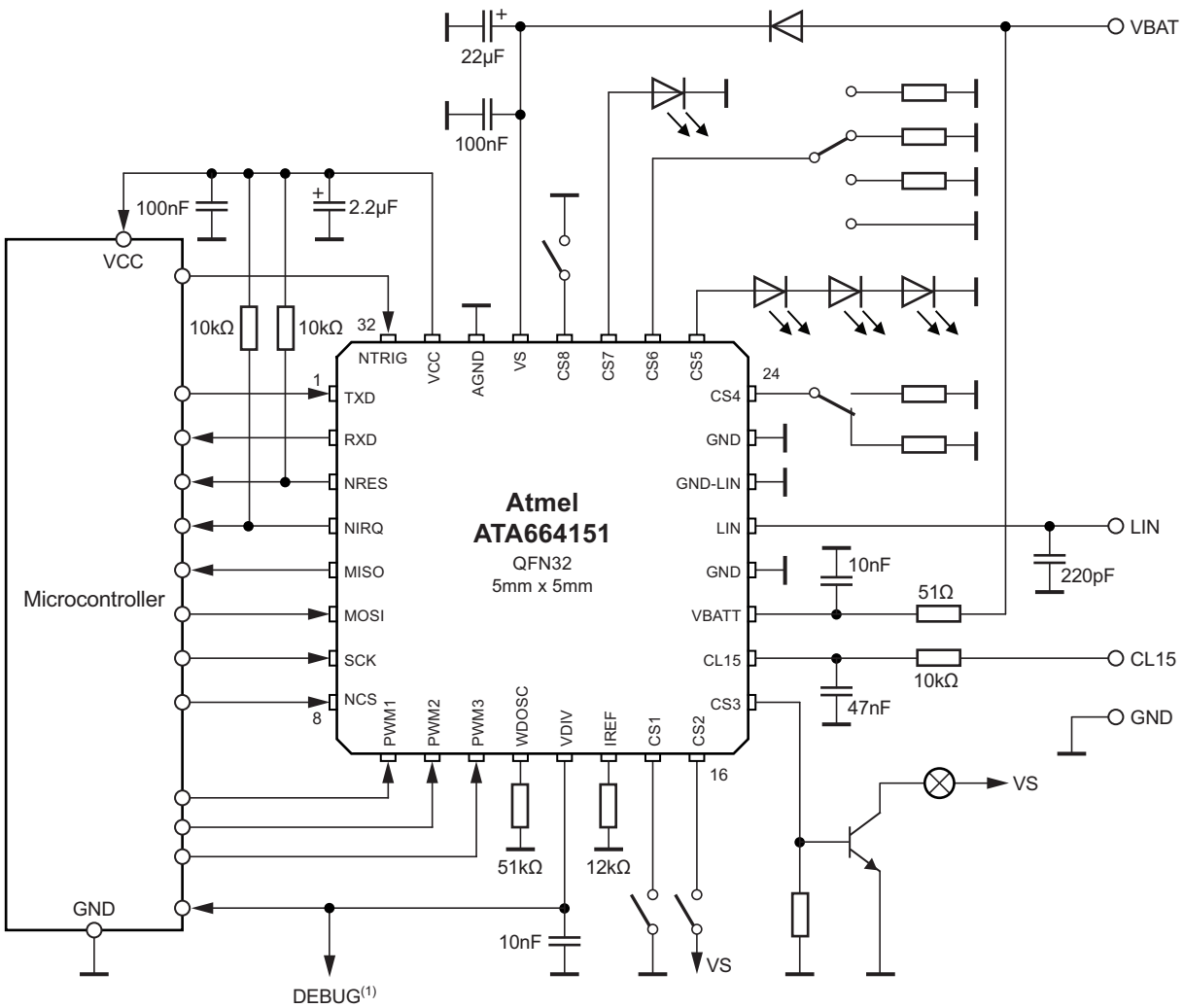
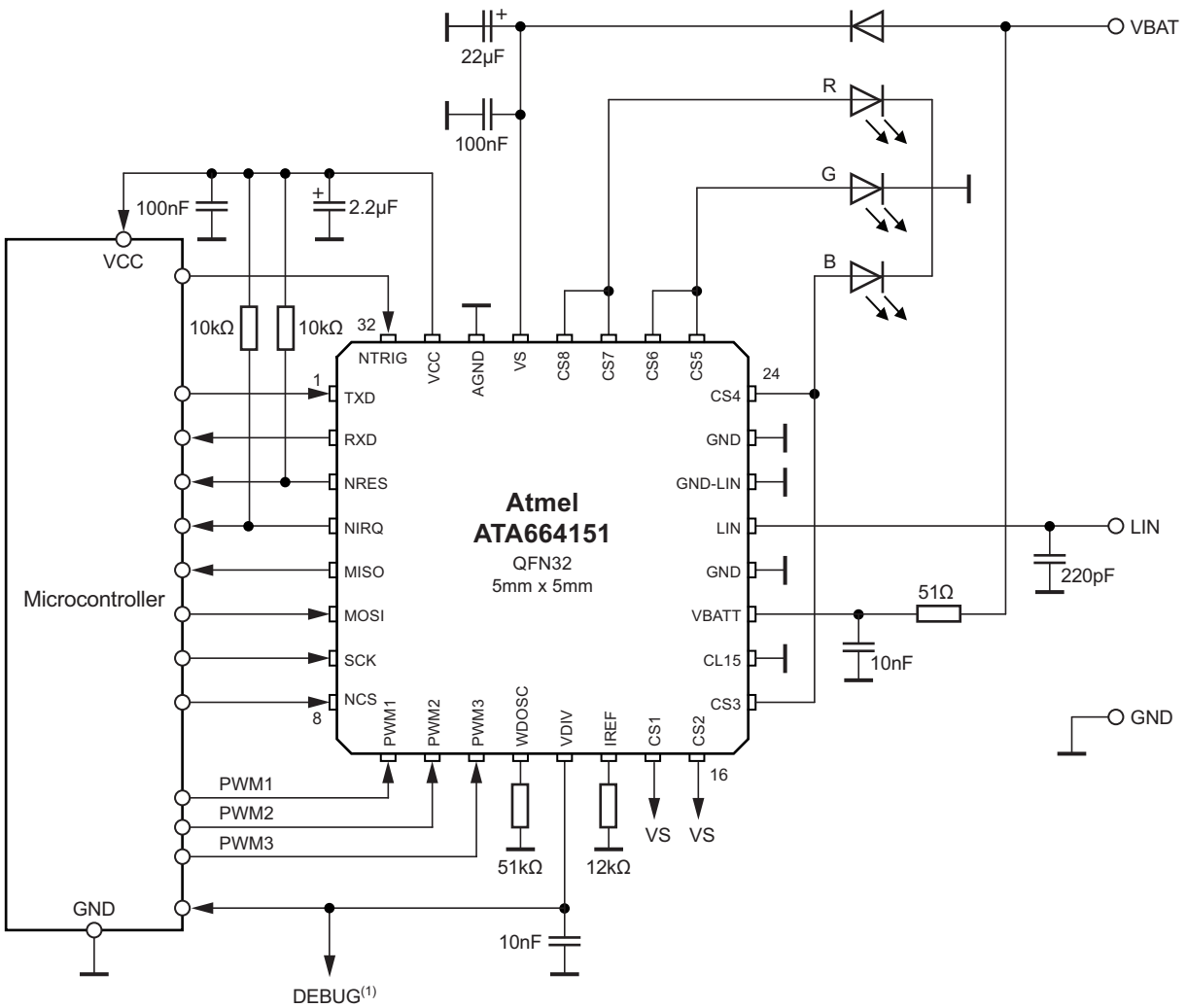


Figure 16-2. Application Example 1: LIN Slave with Different External Circuitry at the CSx-pins



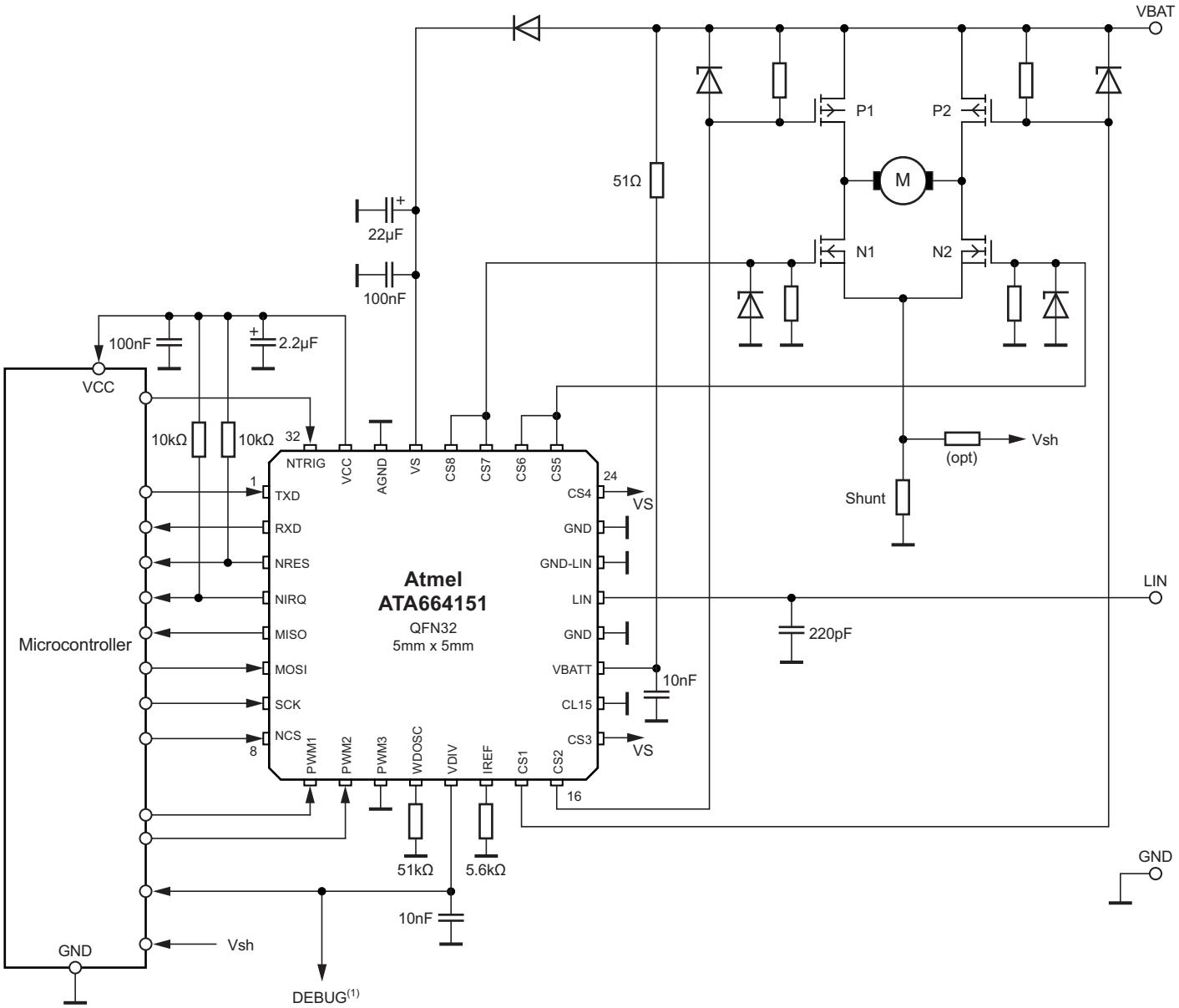
(1)
Note: If the Watchdog shall be disabled directly after power-up (e.g. for microcontroller programming or debugging purposes) the pin VDIV must be tied to High Level until the Reset phase ends (Positive slope at pin NRES).

Figure 16-3. Application Example 2: LIN Slave for RGB-LED-Control



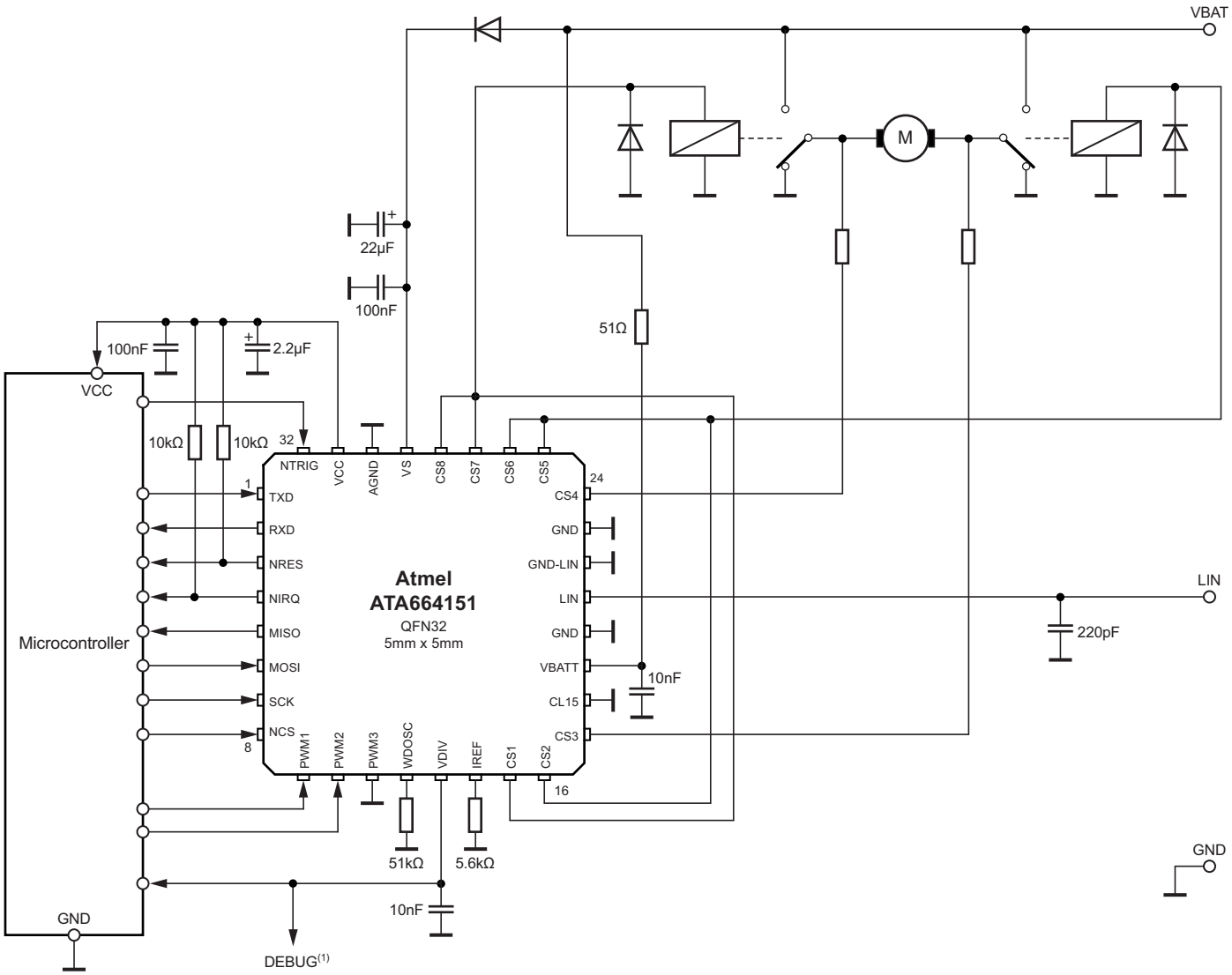
(1)
Note: If the Watchdog shall be disabled directly after power-up (e.g. for microcontroller programming or debugging purposes) the pin VDIV must be tied to High Level until the Reset phase ends (Positive slope at pin NRES).

Figure 16-4. Application Example 3: LIN Slave for H-bridge Control of Small DC-motors



(1)
Note: If the Watchdog shall be disabled directly after power-up (e.g. for microcontroller programming or debugging purposes) the pin VDIV must be tied to High Level until the Reset phase ends (Positive slope at pin NRES).

Figure 16-5. Application Example 4: LIN Slave Relay Driver

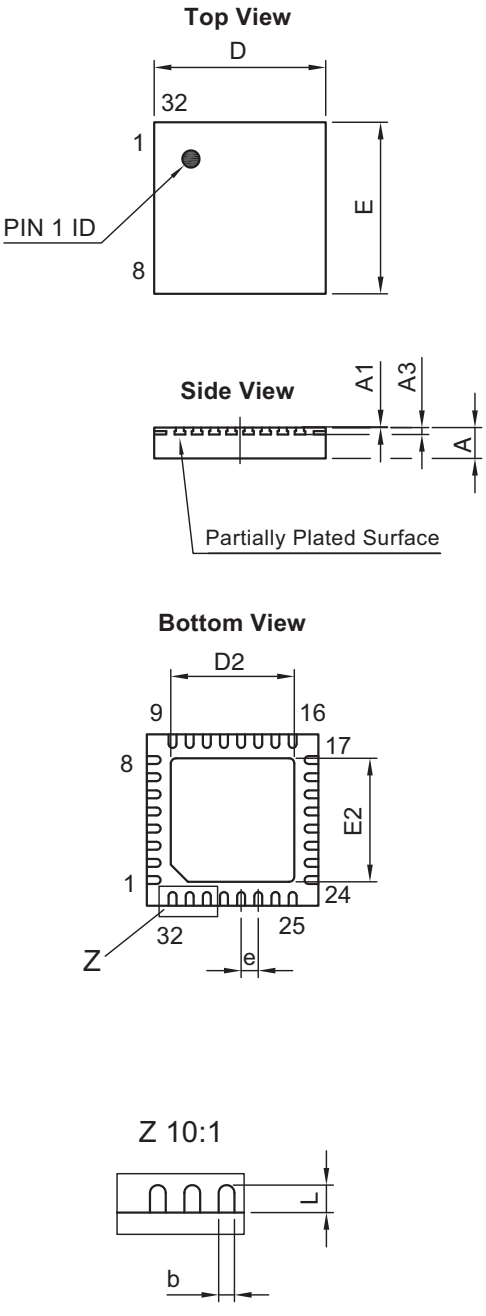


(1)
Note: If the Watchdog shall be disabled directly after power-up (e.g. for microcontroller programming or debugging purposes) the pin VDIV must be tied to High Level until the Reset phase ends (Positive slope at pin NRES).

17. Ordering Information

Extended Type Number	Package	Remarks
ATA664151-WNQW	QFN32 5x5mm	V_{CC} = 5V, Voltage Divider, V_{VCCuv} = 2.9V

18. Package Information



technical drawings according to DIN specifications

Dimensions in mm

Two Step Singulation process

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.8	0.9	1	
A1	0.0	0.02	0.05	
A3	0.15	0.2	0.25	
D	4.9	5	5.1	
D2	3.45	3.6	3.75	
E	4.9	5	5.1	
E2	3.45	3.6	3.75	
L	0.35	0.4	0.45	
b	0.16	0.23	0.3	
e		0.5 BSC		

11/30/11

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** packagedrawings@atmel.com	**Package: VQFN_5x5_32L** Exposed pad 3.6x3.6		6.543-5124.02-4	2

19. Errata

19.1 Atmel ATA664151

1. The current sources, pins CS1 to CS8, may show unexpected behavior when not initialized correctly thus resulting in small amounts of current to be provided.

   Problem Fix/Workaround

   The current sources can be brought into a defined status by disabling the Slope control for the CS-Ports when initializing the device. This can be achieved using the SPI bit CSSCD. The slope control can be turned off 10µs after it was enabled.

20. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9268H-AUTO-08/14	• Put datasheet in the latest template
9268G-AUTO-12/13	• Section 13 “Absolute Maximum Ratings” on pages 31 to 32 updated
9268F-AUTO-07/13	• Section 13 “Absolute Maximum Ratings” on pages 31 to 32 updated • Section 14 “Thermal Characteristics” on page 32 updated • Section 15 “Electrical Characteristics” numbers 3.3, 5.3, 14.3, 20.3, 20.4 and 20.16 on pages 33 to 41 updated
9268E-AUTO-07/13	• Section 10.1 “Typical Timing Sequence with R_{WD_OSC} = 51kΩ” on page 28 updated • Section 10.2 “Worst Case Calculation with R_{WD_OSC} = 51kΩ” on page 29 updated • Section 15 “Electrical Characteristics” numbers 1.7, 1.8, 1.9, 4.3, 11.6, 13.1, 13.2, 13.3, 17.12, 18.3, 20.11, 20.13, 20.14, and 21.5 on pages 33 to 41 updated • Section 19 “Errata” on page 48 added
9268D-AUTO-11/12	• Section 3.12 “NTRIG Input Pin” on page 6 updated • Section 3.13 “VBATT Input Pin” on page 6 updated • Section 3.16 “CS1 to CS8 High-voltage Input/Output Pins” on page 7 updated
9268C-AUTO-09/12	• ATA664131 and ATA664154 removed • Section 17 “Ordering Information” on page 47 updated
9268B-AUTO-05/12	• Section 15 “Electrical Characteristics” numbers 20.7, 20.8, 20.22 and 20.23 on page 40 updated





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