

20 + 1 channel buffer for TFT-LCD panels

Features

- Wide supply voltage: 5.5V to 16.8V
- Low operating current: 8.5mA typ. at 25°C
- Bandwidth at -3dB: 5MHz
- High output current COM amplifier: $\pm 150\text{mA}$
- Industrial temperature range: -40°C to +95°C
- Small package: TQFP48 ePad

Application

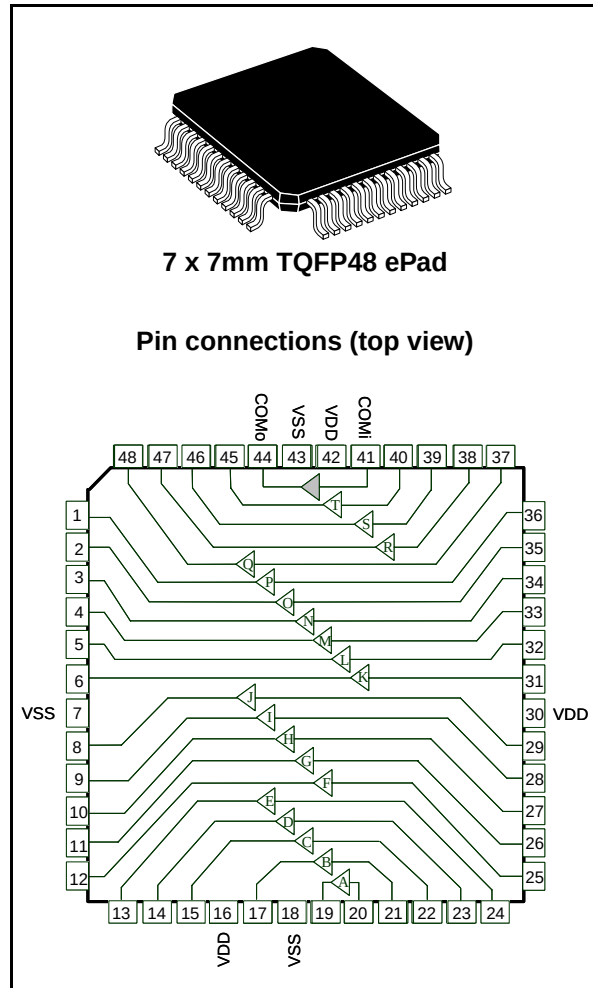
- TFT liquid crystal display (LCD)

Description

The TSL1020 is composed of 20 + 1 channel buffers which are used to buffer the reference voltage for gamma correction in thin film transistor (TFT) liquid crystal displays (LCD).

One COM amplifier is able to deliver high output current, up to $\pm 150\text{mA}$. Amplifiers A and B feature positive single supply inputs for common mode voltage, thus can be used for the highest gamma voltages. The amplifiers C to T inclusive, and the COM amplifier, feature negative single supply inputs and are dedicated to the lowest gamma voltages.

The TSL1020 is fully characterized and guaranteed over a wide industrial temperature range (-40 to +95°C).



1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ($V_{DD} - V_{SS}$)	18	V
V_{in}	Input voltage	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
R_{thja}	Thermal resistance junction to ambient for TQFP48 ePad not thermally connected to PCB ePad thermally connected to PCB	85 36	°C/W
T_{lead}	Lead temperature (soldering 10 seconds)	260	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Junction temperature	150	°C
ESD	Human body model (HBM) ⁽¹⁾	2000	V
	Machine model (MM) ⁽²⁾	200	V

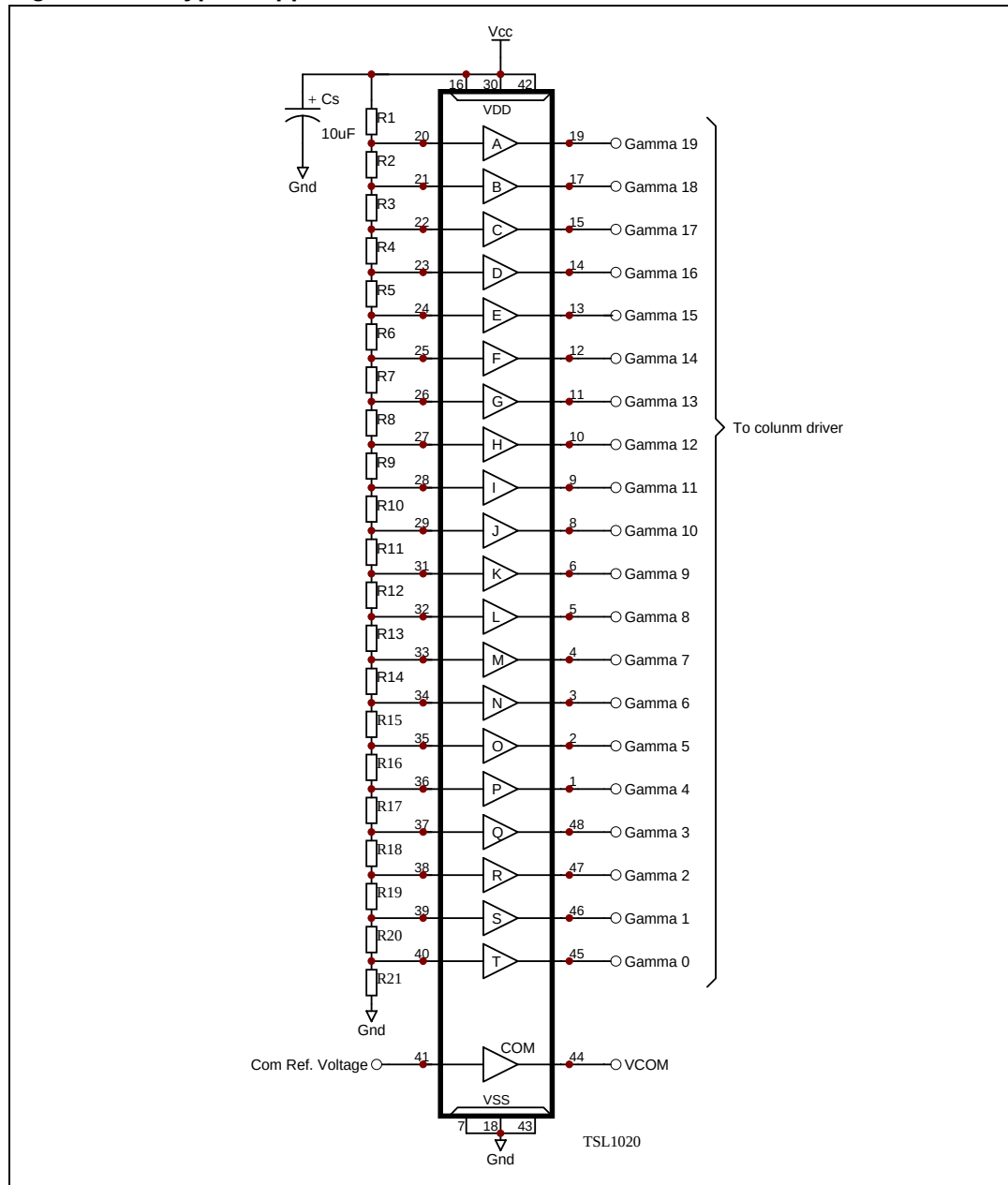
1. Human body model: A 100pF capacitor is charged to the specified voltage, then discharged through a 1.5kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
2. Machine model: A 200pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5Ω). This is done for all couples of connected pin combinations while the other pins are floating.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ($V_{DD} - V_{SS}$)	5.5 to 16.8	V
T_{amb}	Ambient temperature	-40 to +95	°C
V_{in}	Input voltages for buffers A & B	$V_{SS} + 1.5V$ to V_{DD}	V
	Input voltages for buffers C to T & COM	V_{SS} to $V_{DD} - 1.5V$	

2 Typical application schematics

Figure 1. A typical application schematic for the TSL1020



Note that:

- Amplifiers **A** & **B** have their input voltages in the range $V_{SS}+1.5V$ to V_{DD} . This is why they must be used for high level gamma correction voltages.
- Amplifiers **C** to **T** have their input voltages in the range V_{SS} to $V_{DD}-1.5V$. This is why they must be used for medium-to-low level gamma correction voltages.
- Amplifier **COM** has its input voltage range from V_{SS} to $V_{DD}-1.5V$.

3 Electrical characteristics

Table 3. Electrical characteristics for $T_{amb} = 25^{\circ}\text{C}$, $V_{DD} = +5\text{V}$, $V_{SS} = -5\text{V}$, $R_L = 10\text{k}\Omega$, $C_L = 10\text{pF}$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	$V_{icm} = 0\text{V}$			12	mV
ΔV_{io}	Input offset voltage drift	$-40^{\circ}\text{C} < T_{amb} < +95^{\circ}\text{C}$		5		$\mu\text{V}/^{\circ}\text{C}$
I_{ib}	Input bias current	$V_{icm} = 0\text{V}$, buffers A & B $V_{icm} = 0\text{V}$, buffers C to T & COM			140 70	nA
R_{in}	Input impedance			1		$\text{G}\Omega$
C_{in}	Input capacitance			1.35		pF
V_{OL}	Output voltage low	$I_{out} = -5\text{mA}$ Buffers C to R Buffers S, T & COM		-4.88 -4.92	-4.80 -4.85	V
V_{OH}	Output voltage high	$I_{out} = 5\text{mA}$ for buffers A & B	4.82	4.87		V
I_{out}	Short circuit output current	(A to T buffers)		± 40		mA
		COM buffer		± 150		
PSRR	Power supply rejection ratio	$V_{CC} = 6.5$ to 15.5V	80	100		dB
I_{CC}	Supply current	No load		8.5	12	mA
SR	Slew rate (rising & falling edge)	$-3.5\text{V} < V_{out} < +3.5\text{V}$ 10% to 90%		1.1		$\text{V}/\mu\text{s}$
t_s	Settling time	Settling to 0.1%, $V_{out} = 2\text{V}$ step		5		μs
BW	Bandwidth at -3dB	$R_L = 10\text{k}\Omega$, $C_L = 10\text{pF}$		5		MHz
G_m	Phase margin	$R_L = 10\text{k}\Omega$, $C_L = 10\text{pF}$		70		degrees
C_s	Channel separation	$f = 1\text{MHz}$		75		dB

Note: Limits are 100% production tested at 25°C . Behavior at the temperature range limits is guaranteed through correlation and by design.

Figure 2. Supply current vs. supply voltage for various temperatures

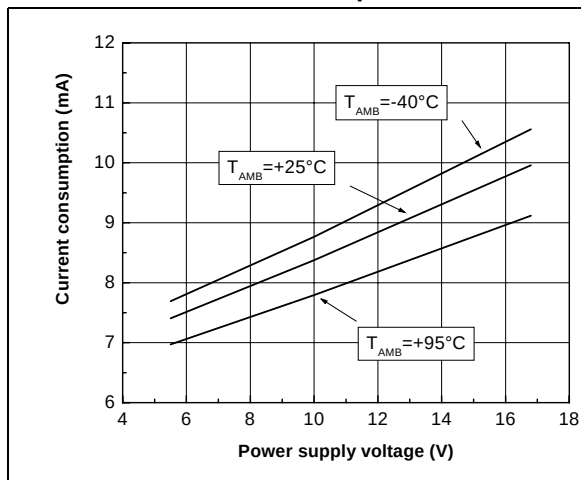


Figure 3. Output offset voltage (eq. V_{io}) vs. temperature

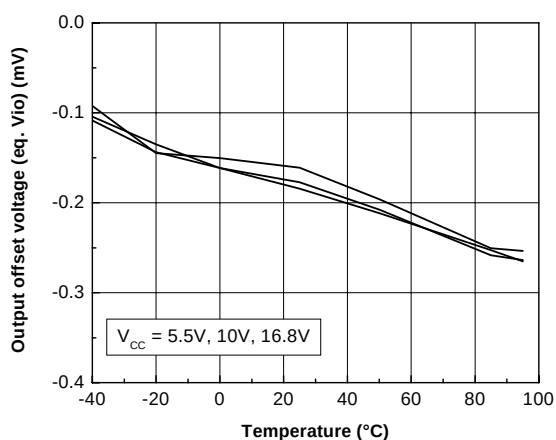


Figure 4. Input current (I_{ib}) vs. temperature

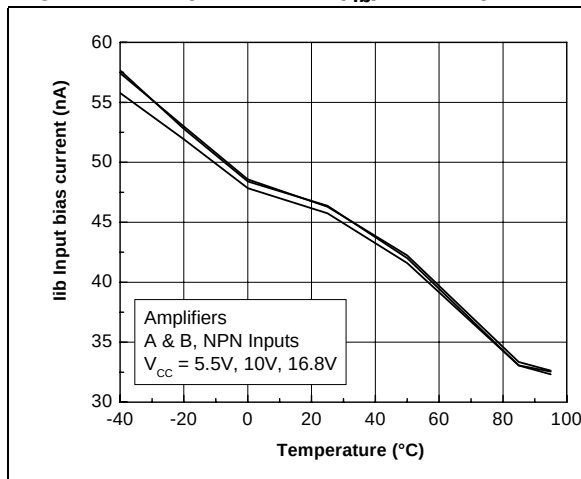


Figure 5. Input current (I_{ib}) vs. temperature

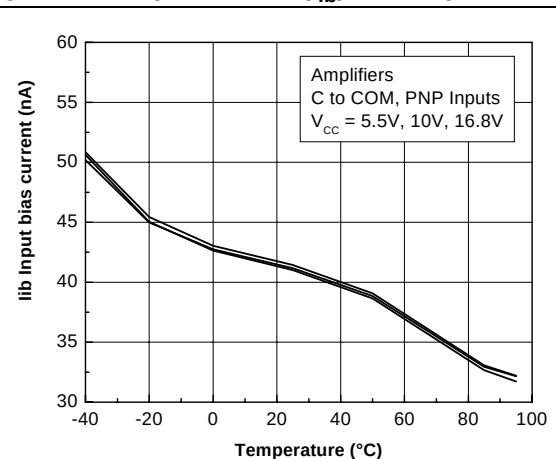


Figure 6. Output current capability vs. temperature

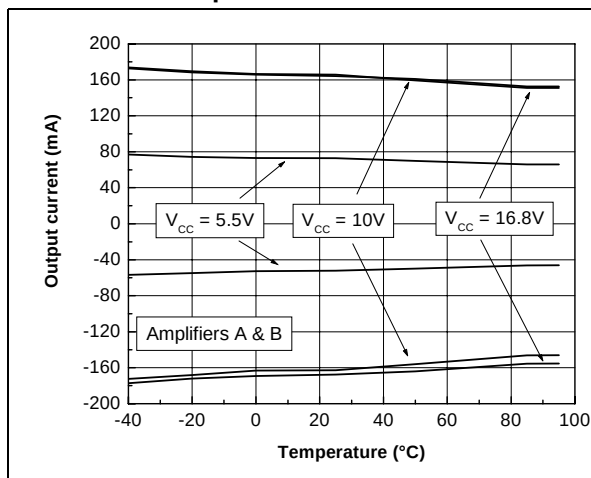


Figure 7. Output current capability vs. temperature

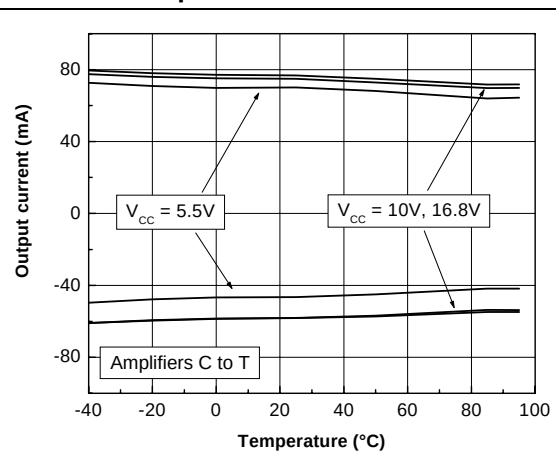


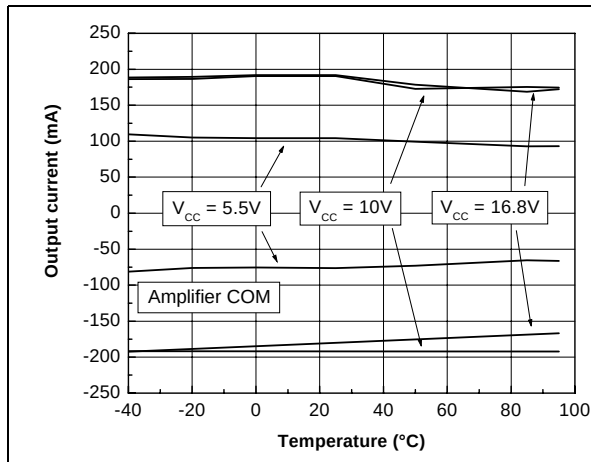
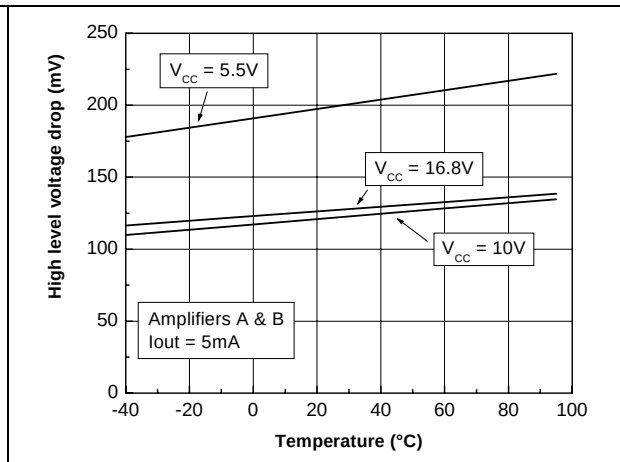
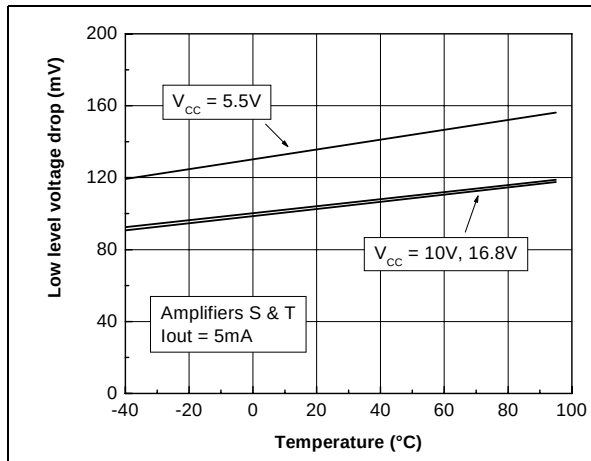
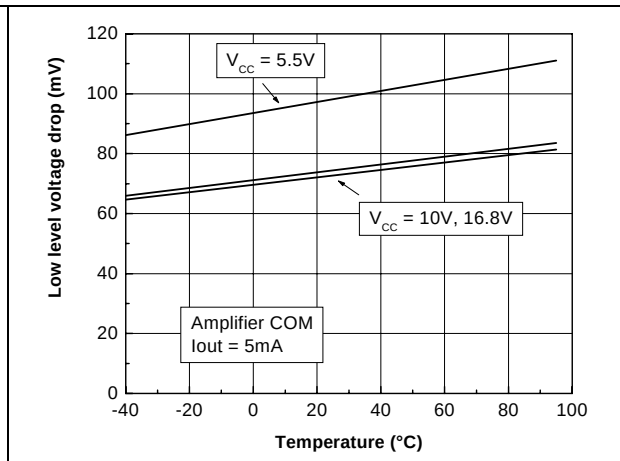
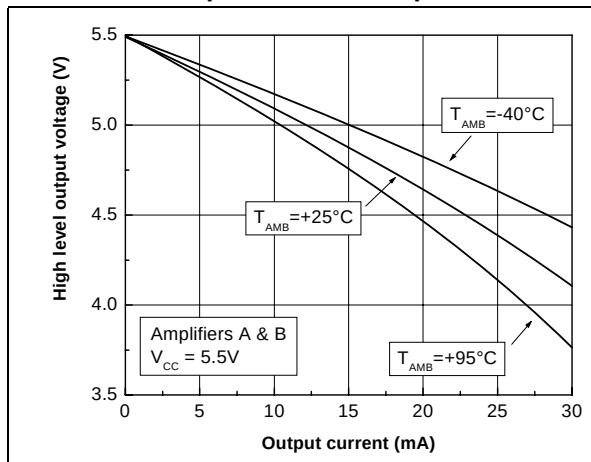
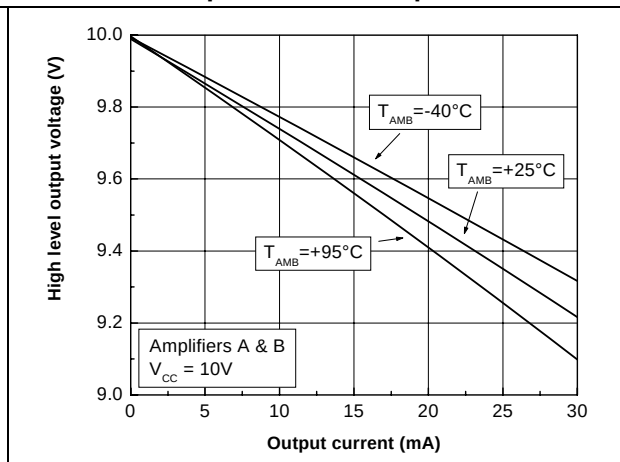
Figure 8. Output current capability vs. temperature**Figure 9. High level voltage drop vs. temperature****Figure 10. Low level voltage drop vs. temperature****Figure 11. Low level voltage drop vs. temperature****Figure 12. Voltage output high (VOH) vs. output current - Amplifiers A & B****Figure 13. Voltage output high (VOH) vs. output current - Amplifiers A & B**

Figure 14. Voltage output high (V_{OH}) vs. output current - Amplifiers A & B

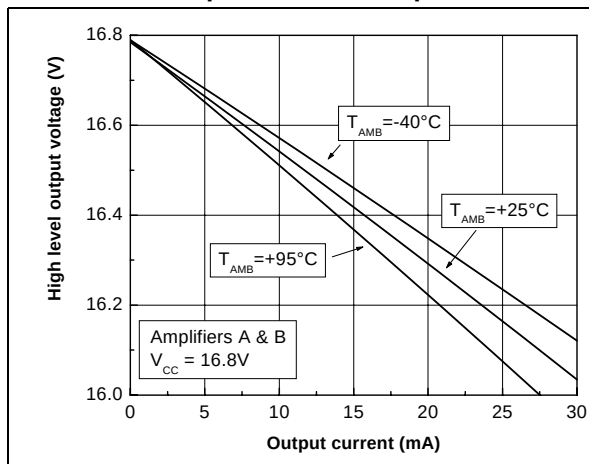


Figure 15. Voltage output low (V_{OL}) vs. output current - Amplifiers C to R

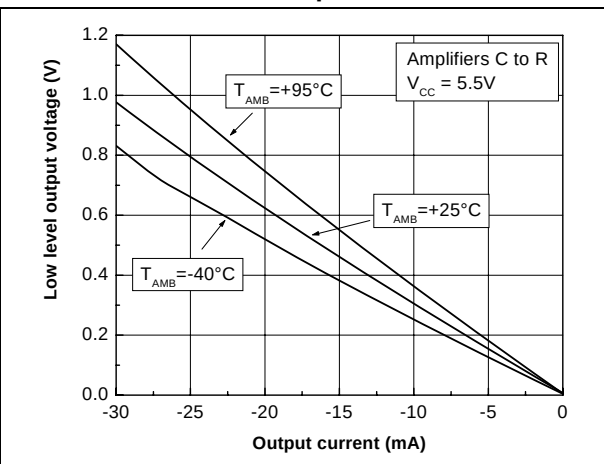


Figure 16. Voltage output low (V_{OL}) vs. output current - Amplifiers C to R

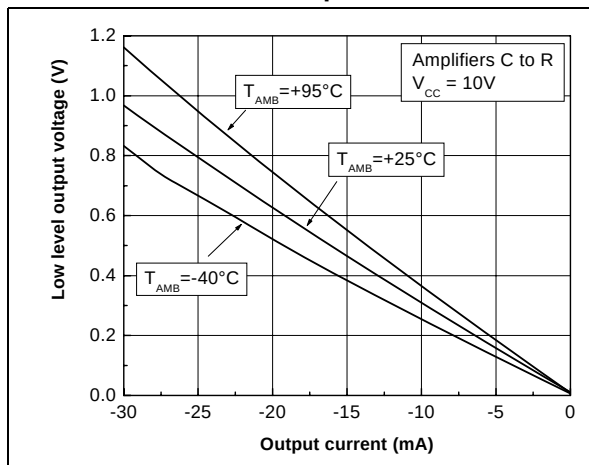


Figure 17. Voltage output low (V_{OL}) vs. output current - Amplifiers C to R

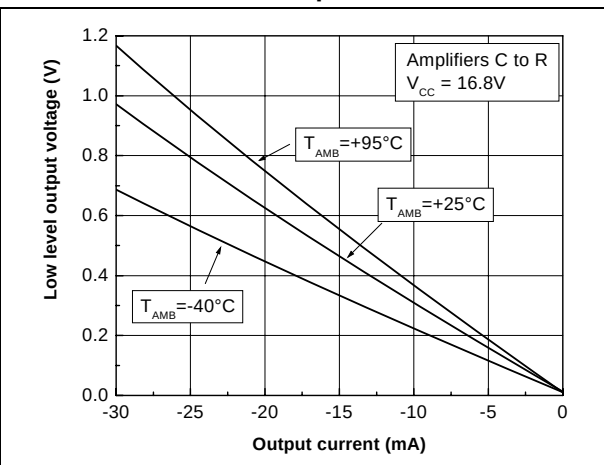


Figure 18. Voltage output low (V_{OL}) vs. output current - Amplifiers S & T

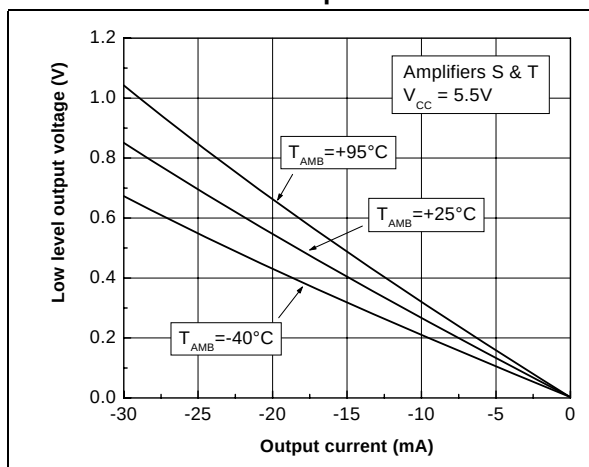


Figure 19. Voltage output low (V_{OL}) vs. output current - Amplifiers S & T

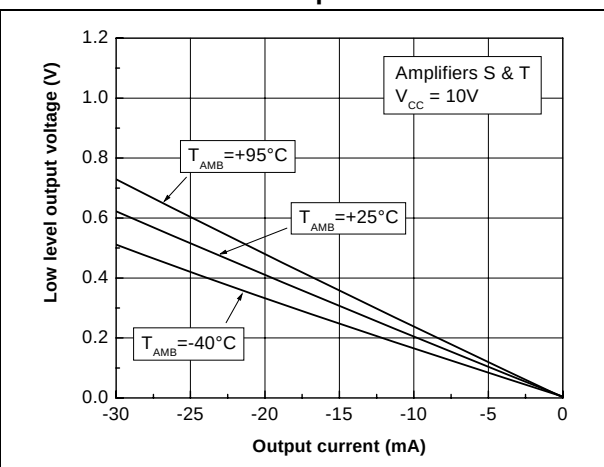


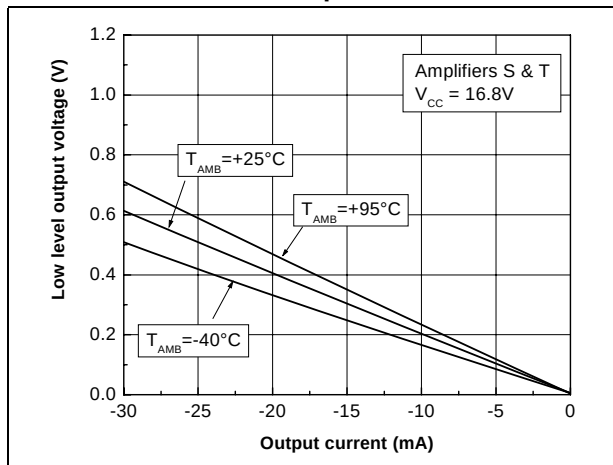
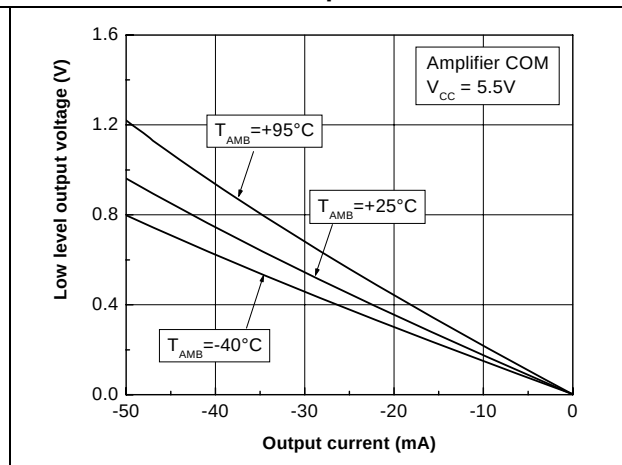
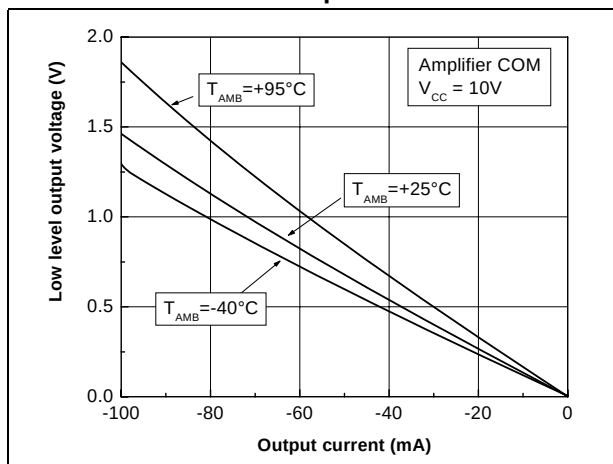
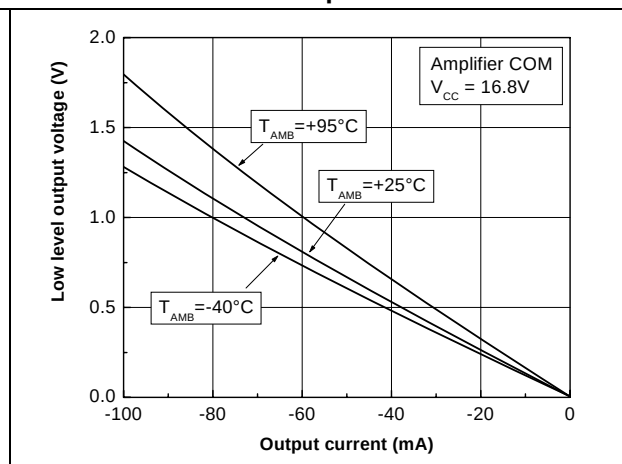
Figure 20. Voltage output low (V_{OL}) vs. output current - Amplifiers S & TFigure 21. Voltage output low (V_{OL}) vs. output current - Amplifier COMFigure 22. Voltage output low (V_{OL}) vs. output current - Amplifier COMFigure 23. Voltage output low (V_{OL}) vs. output current - Amplifier COM

Figure 24. Positive slew rate vs. temperature

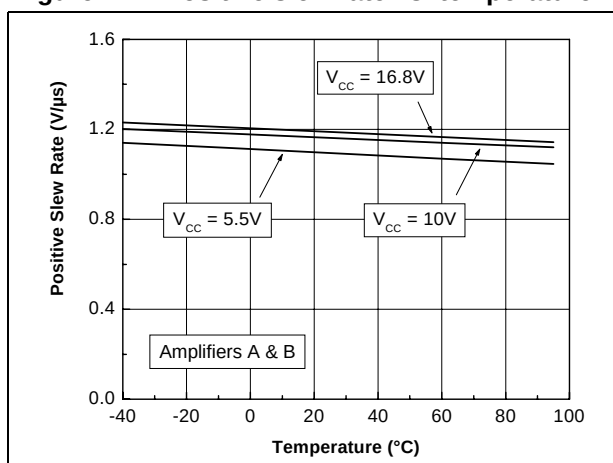


Figure 25. Positive slew rate vs. temperature

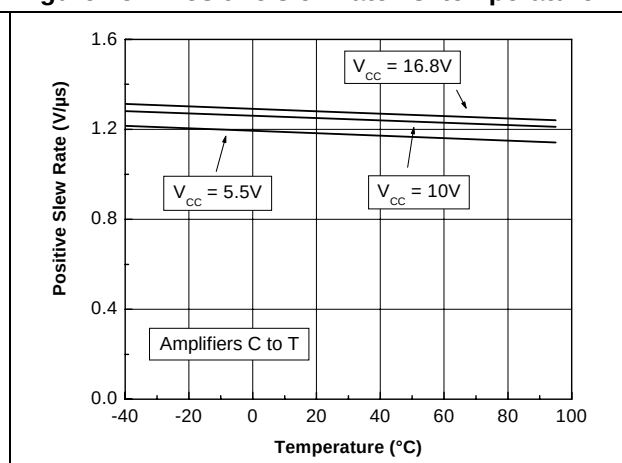


Figure 26. Positive slew rate vs. temperature

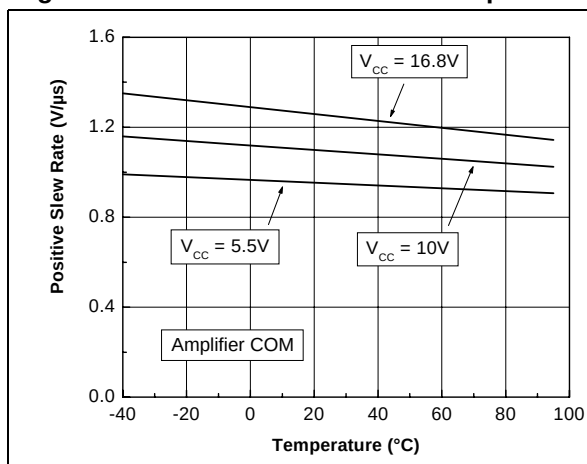


Figure 27. Negative slew rate vs. temperature

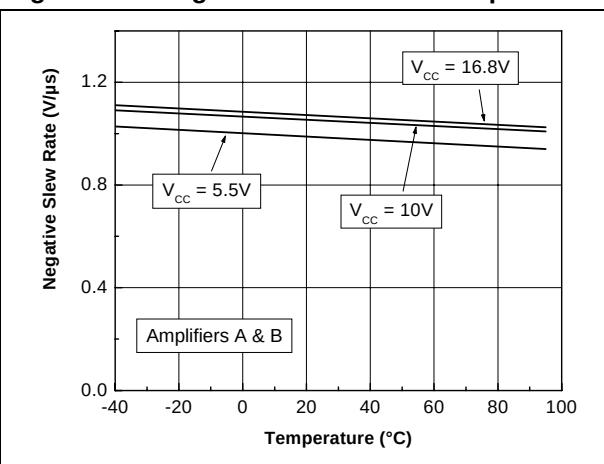


Figure 28. Negative slew rate vs. temperature

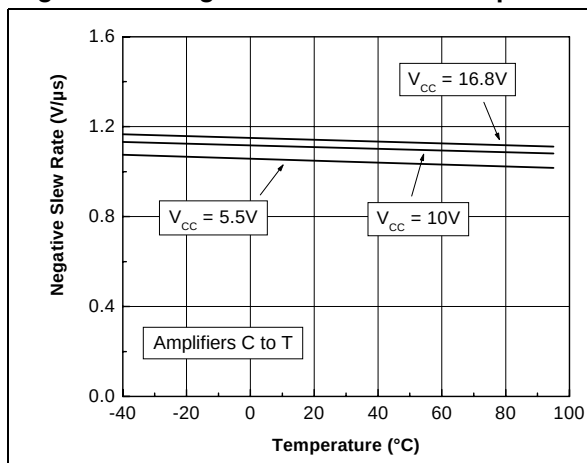


Figure 29. Negative slew rate vs. temperature

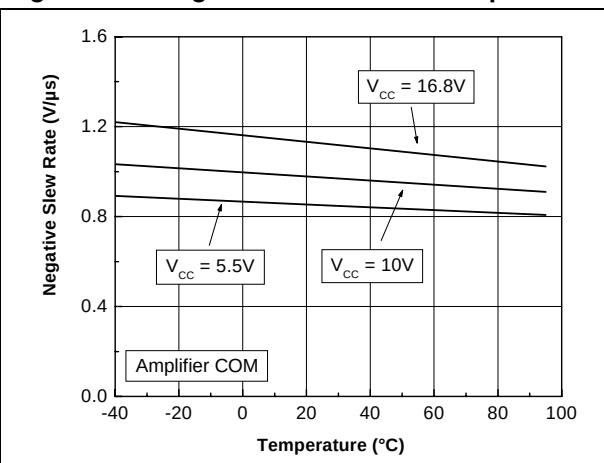


Figure 30. Large signal response - Amplifiers A & B

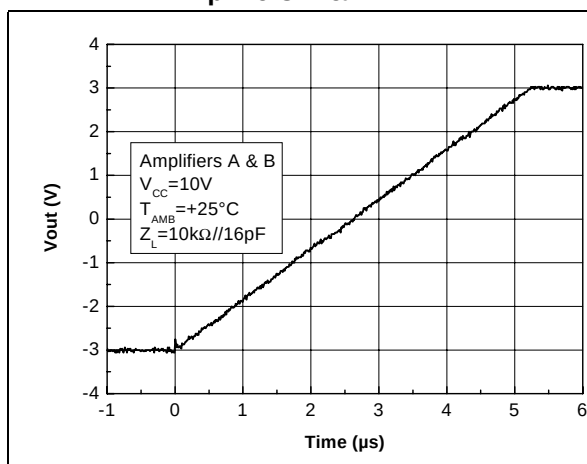


Figure 31. Large signal response - Amplifiers A & B

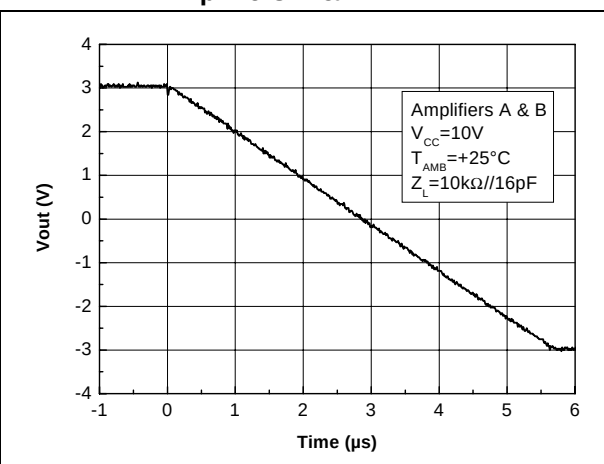


Figure 32. Large signal response - Amplifiers C to T

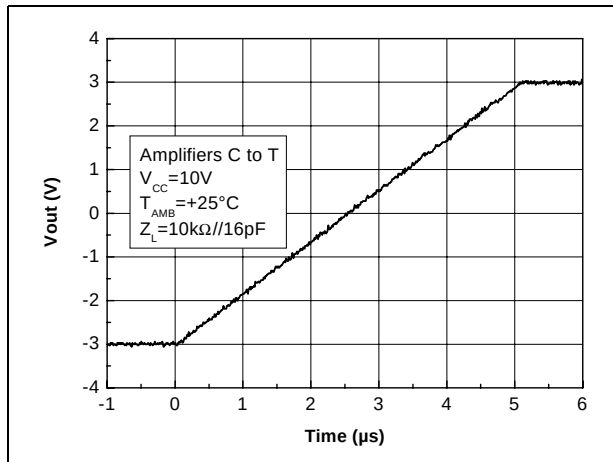


Figure 33. Large signal response - Amplifiers C to T

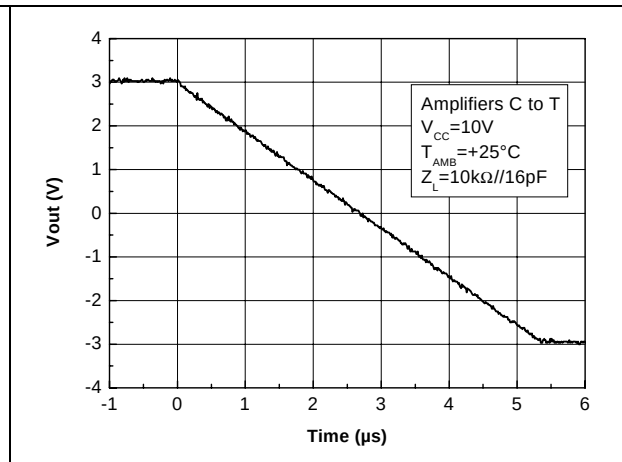


Figure 34. Large signal response - Amplifier COM

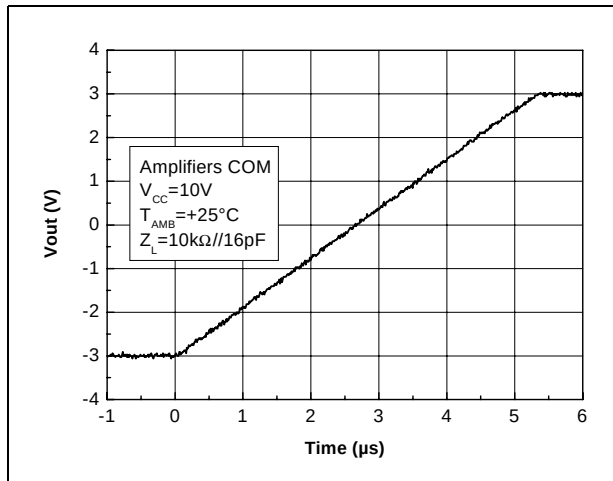


Figure 35. Large signal response - Amplifier COM

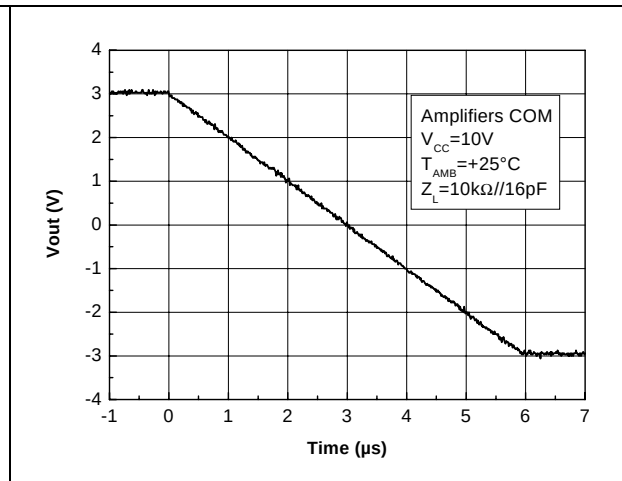


Figure 36. Small signal response - Amplifiers A & B

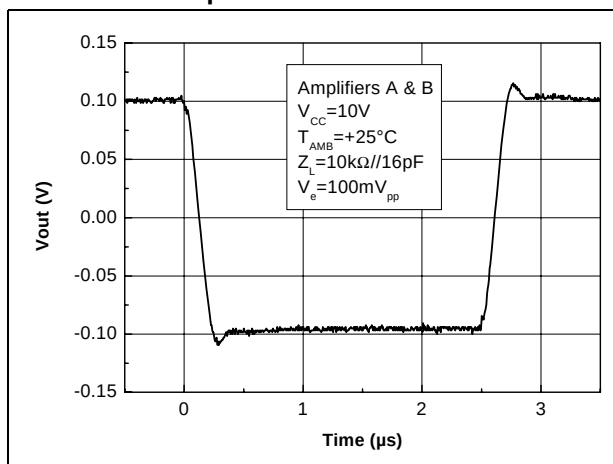


Figure 37. Small signal response - Amplifiers C to T

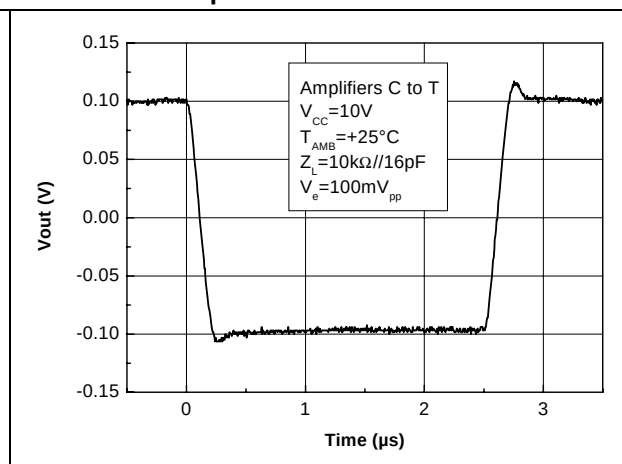


Figure 38. Small signal response - Amplifier COM

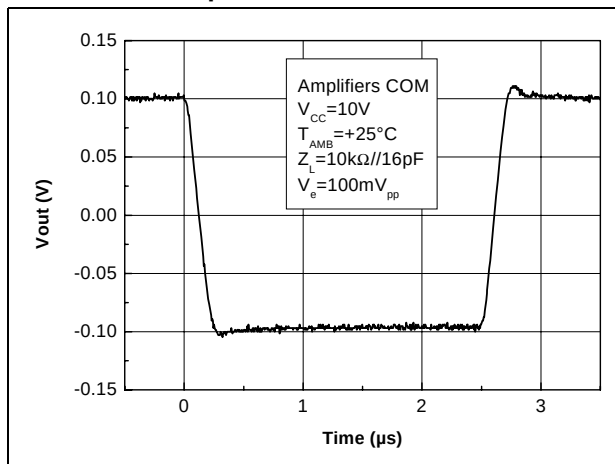


Figure 39. Output voltage response to current transient - Amplifiers A & B

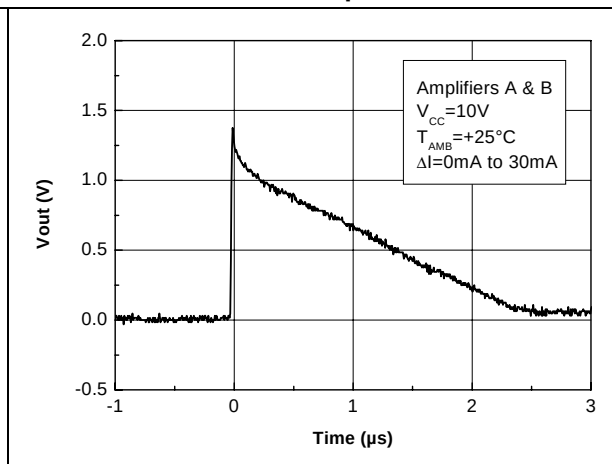


Figure 40. Output voltage response to current transient - Amplifiers A & B

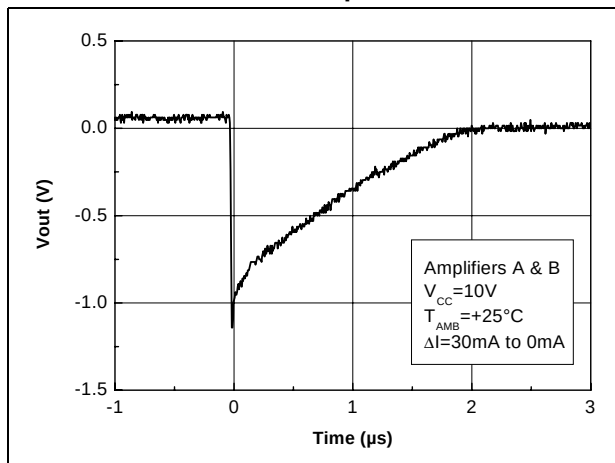


Figure 41. Output voltage response to current transient - Amplifiers C to T

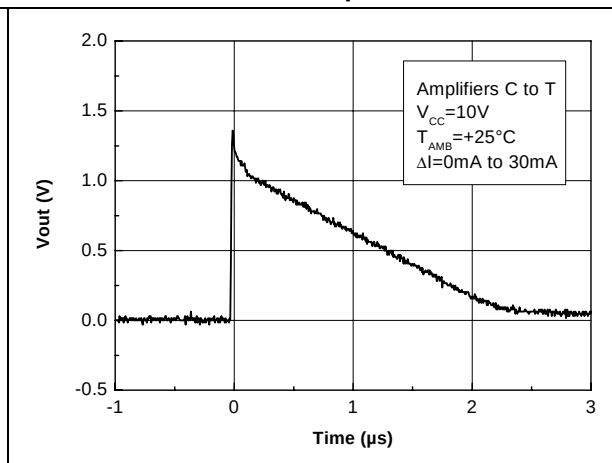


Figure 42. Output voltage response to current transient - Amplifiers C to T

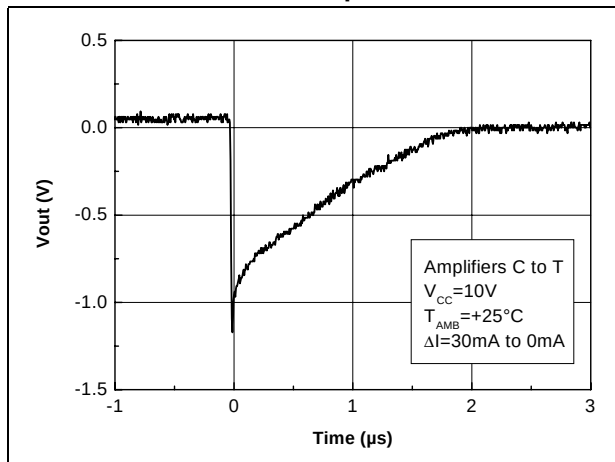


Figure 43. Output voltage response to current transient - Amplifier COM

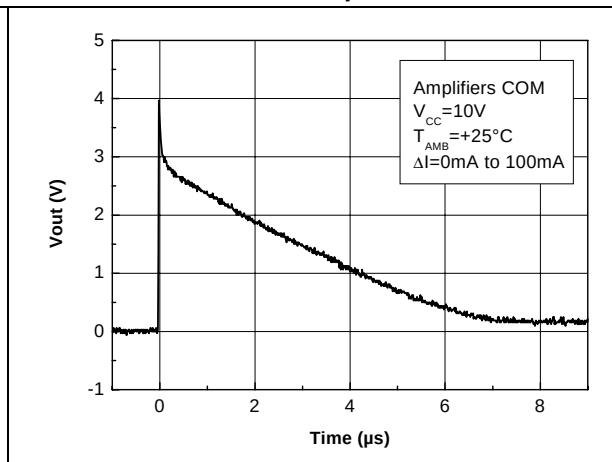
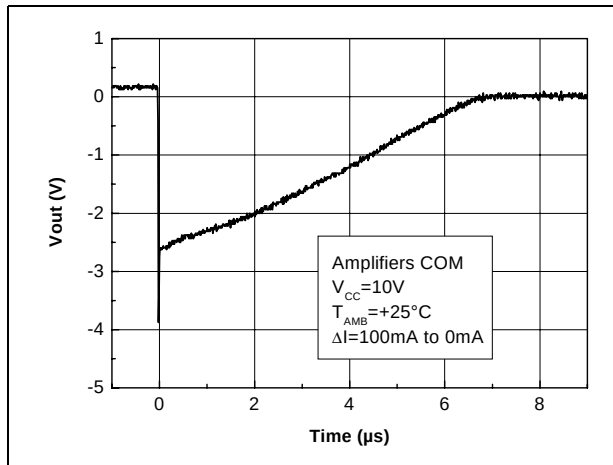
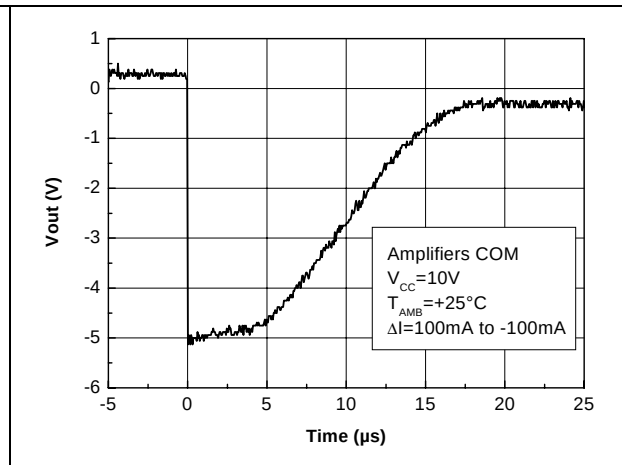
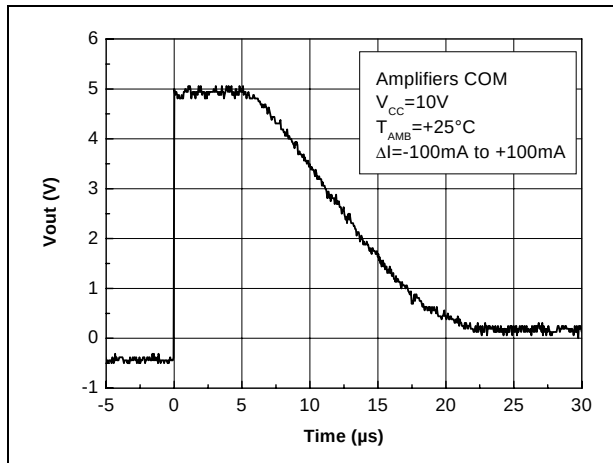


Figure 44. Output voltage response to current transient - Amplifier COM**Figure 45. Output voltage response to current transient - Amplifier COM****Figure 46. Output voltage response to current transient - Amplifier COM**

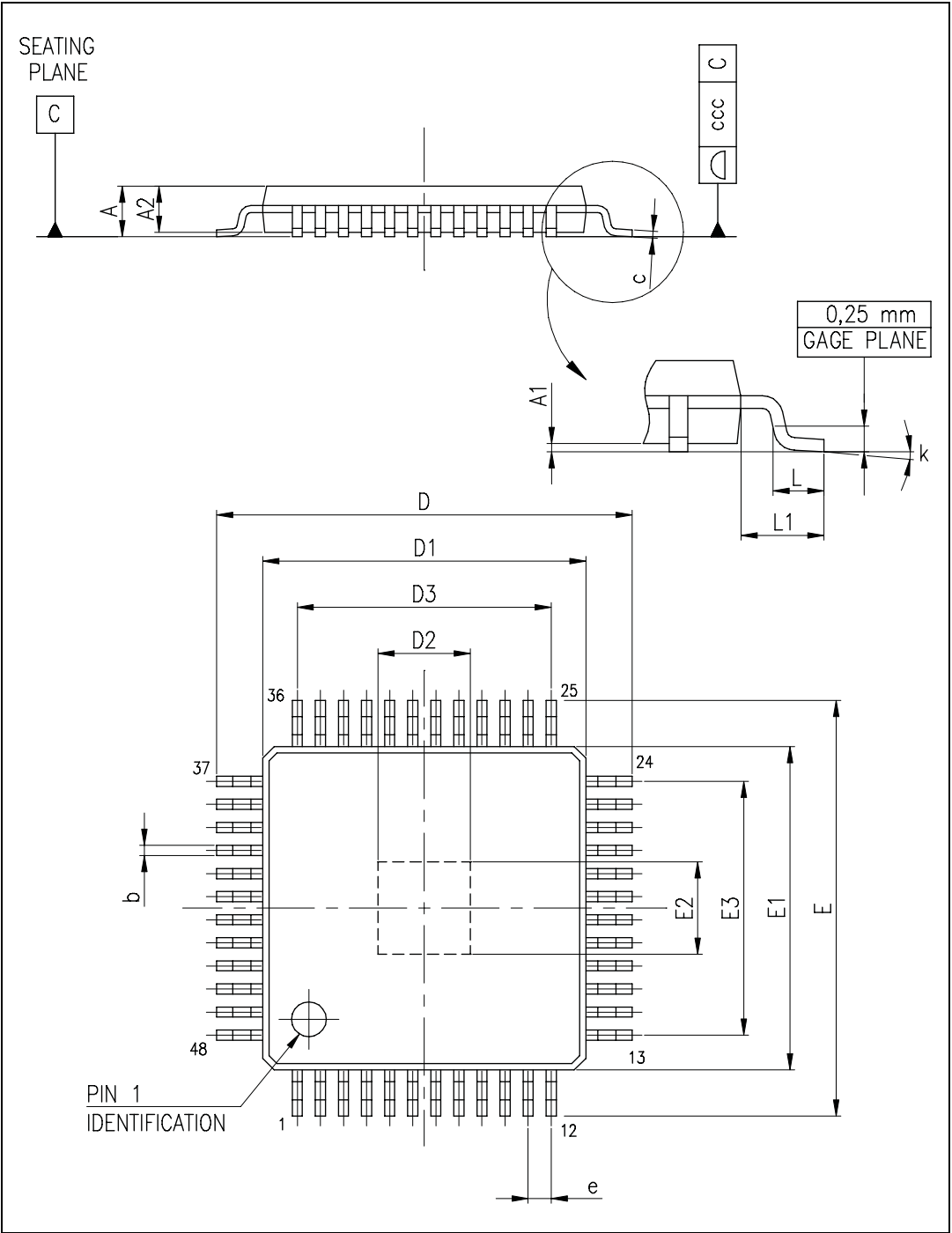
4 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK[®] packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Table 4. TQFP48 ePad package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D	8.80	9.00	9.20	0.346	0.354	0.362
D1	6.80	7.00	7.20	0.268	0.276	0.283
D2	2.00			0.079		
D3		5.50			0.217	
E	8.80	9.00	9.20	0.346	0.354	0.362
E1	6.80	7.00	7.20	0.268	0.276	0.283
E2	2.00			0.079		
E3		5.50			0.217	
e		0.50			0.020	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°	3.5°	7°	0°	3.5°	7°
ccc			0.08			0.003

Figure 47. TQFP48 ePad package drawing



5 Ordering information

Table 5. Order codes

Order code	Temperature range	Package	Packing	Marking
TSL1020IF	-40°C to +95°C	TQFP48 ePad	Tray	SL1020I
TSL1020IFT			Tape & reel	

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
28-Jan-2008	1	Initial release.

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