M66850J/FP, M66851J/FP
M66852J/FP, M66853J/FP

SRAM TYPE FIFO MEMORY

DESCRIPTION

M66850/851/852/853 are very high-speed and clock synchronous FIFO(First-In,First-Out) memories fabricated by high-speed CMOS technology.

These FIFOs are applicable for a data buffer as networks and communications.

The write operation is controlled by a write clock pin(WCLK) and two write enable pins($\overline{WEN1}$,WEN2).

Data present at the data input pins(D0-D8) is written into the Synchronous FIFO on every rising write clock edge when the device is enabled for writing.

The read operation is controlled by a read clock pin(RCLK) and two read enable pins($\overline{REN1}$,$\overline{REN2}$).

Data is read from the Synchronous FIFO on every rising read clock edge when the device is enabled for reading. An output enable pin($\overline{OE}$) controls the states of the data output pins(Q0-Q8).

MITSUBISHI FIFOs have four flags ($\overline{EF}$,$\overline{FF}$,$\overline{PAE}$,$\overline{PAF}$). The empty flag $\overline{EF}$ and the full flag $\overline{FF}$ are fixed flags. The almost empty flag $\overline{PAE}$ and the almost full flag $\overline{PAF}$ are programmable flags. The programmable flag offset is initiated by the load pin($\overline{LD}$).

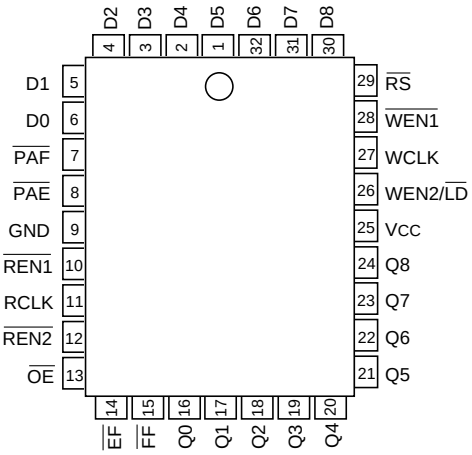
FEATURES

- Memory configuration 64words x 9bits (M66850J/FP)
  256words x 9bits (M66851J/FP)
  512words x 9bits (M66852J/FP)
  1024words x 9bits (M66853J/FP)
- Write and Read Clocks can be independent
- Advanced CMOS technology
- Programmable Almost-Empty and Almost-Full flags
- High-speed : 25ns cycle time
- Package Available :
  32-pin Pastic Leaded Chip Carrier(PLCC)
  32-pin Low profile Quad Flat Package(LQFP)

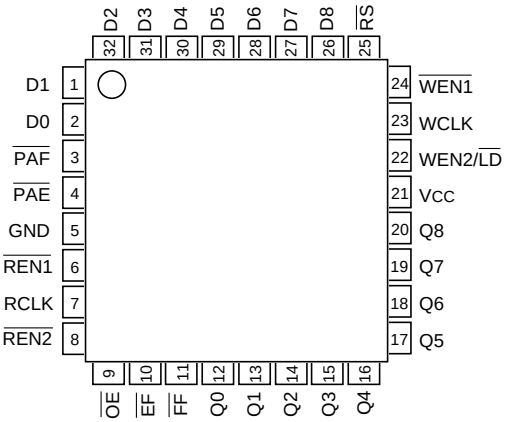
APPLICATION

- Data Buffer for networks communications.

PIN CONFIGURATION (TOP VIEW)

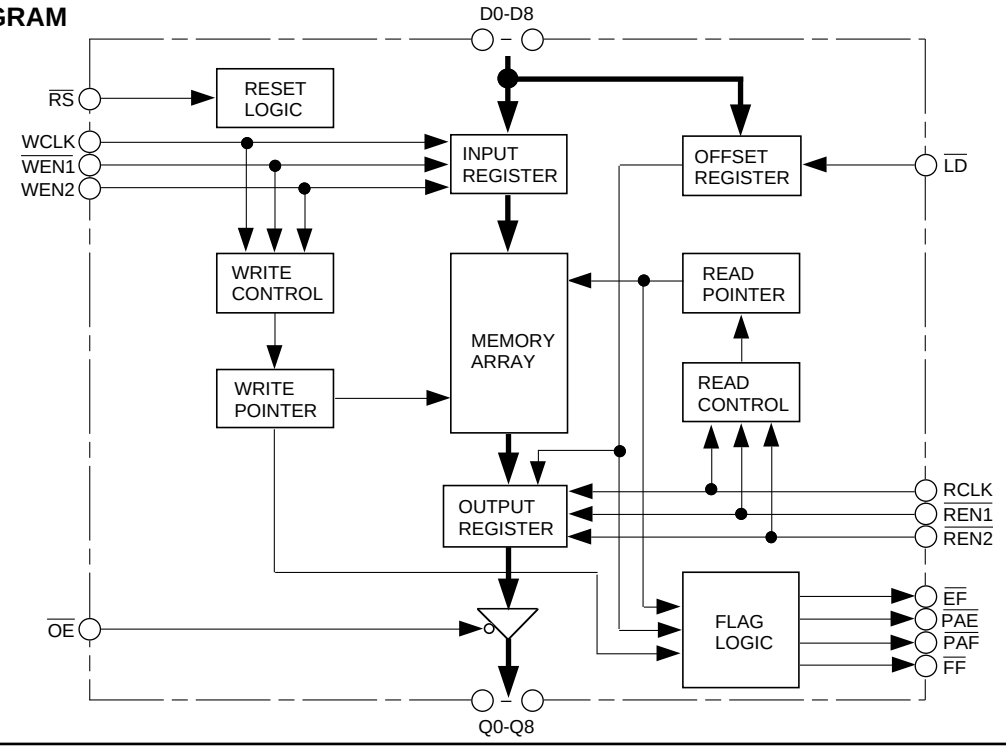


Outline 32P0(M66850 – 853J)



Outline 32P6B(M66850 – 853FP)

BLOCK DIAGRAM



PIN and SIGNAL DESCRIPTIONS

- V_{CC}
  One+5 volt power supply pin.

- GND
  One 0 volt ground pin.

- $\overline{RS}$: Reset(INPUT)
  When $\overline{RS}$ is set LOW, internal read and write pointers are set to the first physical location,the output register is initialized to LOW, $\overline{FF}$ and $\overline{PAF}$ are set HIGH, $\overline{EF}$ and $\overline{PAE}$ are set LOW.
  A reset is required after power-up before a write operation.

- WCLK : Write Clock(INPUT)
  Data present on D0-D8 is written into the FIFO on the rising edge of WCLK when the FIFO is enabled for writing.

- RCLK : Read Clock(INPUT)
  Data is read from the FIFO on the rising edge of RCLK when the FIFO is enabled for reading.

- $\overline{WEN1}$: Write Enable1(INPUT)
  If the FIFO is configured to allow loading of the offset registers, $\overline{WEN1}$ is the only the write enable. When $\overline{WEN1}$ is LOW, data on D0-D8 is written to the FIFO on the rising edge of WCLK.
  If the FIFO is configured to have two writeenables, data on D0-D8 is written to the FIFO on the rising edge of WCLK when $\overline{WEN1}$ is LOW and WEN2 is High. But if the $\overline{FF}$ is LOW, data on D0-D8 will not be written to the FIFO.

- WEN2/$\overline{LD}$: Write Enable2/$\overline{Load}$(INPUT)
  The function of this signal is defined at reset.
  If WEN2/$\overline{LD}$ is HIGH at reset, this signal functions as a second write enable(WEN2). If WEN2/$\overline{LD}$ is LOW at reset, this signal functions as a control to load and read the offset register.
  If the FIFO is configured to have two write enables, data on D0-D8 is written to the FIFO on the rising edge of WCLK when $\overline{WEN1}$ is LOW and WEN2 is High. But if the $\overline{FF}$ is LOW, data on D0-D8 will not be written to the FIFO.
  If the FIFO is configured to have programmable flags, it is possible to write and read from the offset registers. There are four 9-bit offset registers. Two are used to control the programmable Almost-Empty Flag and two are used to control the programmable Almost-Full Flag.
  Data on D0-D8 is written to an offset register on the rising edge of WCLK when $\overline{WEN1}$ is LOW and LD is LOW. Data on D0 – D8 is written to the offset registers in the following order :
  $\overline{PAE}$ LSB, $\overline{PAE}$ MSB, $\overline{PAF}$ LSB, $\overline{PAF}$ MSB.

- $\overline{REN1}$, $\overline{REN2}$: Read Enable(INPUT)
  Data is read from the FIFO and presented Q0-8 on the rising edge of RCLK, when $\overline{REN1}$ and $\overline{REN2}$ are LOW and output port is enabled.
  If either Read Enable is HIGH,the output register holds the previous data.
  When the FIFO is empty, the Read Enable signals are ignored.

- $\overline{OE}$: Output Enable(INPUT)
  When $\overline{OE}$ is LOW, the output port Q0-8 is enabled for output.
  When $\overline{OE}$ is HIGH, the output port Q0-8 is placed in a high impedance state.

- D0-8 : Data Input(INPUT)
  D0-8 is the 9-bit data input port.

- Q0-8 : Data Output(OUTPUT)
  Q0-8 is the 9-bit data Output port.

- $\overline{EF}$: Empty Flag(OUTPUT)
  The Empty flag goes LOW when the read pointer is equal to the write pointer.
  When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the data output are inhibited.
  $\overline{EF}$ is synchronized to the rising edge of RCLK.

- $\overline{PAE}$: Programmable Almost-Empty Flag(OUTPUT)
  When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset. The default offset is Empty+7. $\overline{PAE}$ is synchronized to the rising edge of RCLK.

- $\overline{FF}$: Full Flag(OUTPUT)
  When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the data input are inhibited.
  The Full Flag goes LOW when the FIFO is full of data.
  $\overline{FF}$ is synchronized to the rising edge of WCLK.

- $\overline{PAF}$: Programmable Almost-Full Flag(OUTPUT)
  When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset. The default offset is Full-7. $\overline{PAF}$ is synchronized to the rising edge of WCLK.

OFFSET FLAG

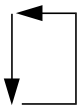
$\overline{LD}$	$\overline{WEN1}$	WCLK	SELECTION
0	0		Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB) 
0	1		No Operation
1	0		Write into FIFO
1	1		No Operation

Figure 1. Write Offset Register

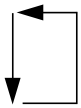
$\overline{LD}$	$\overline{REN1}$	$\overline{REN2}$	RCLK	SELECTION
0	0	0		Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB) 
0	0 1 1	1 0 1		No Operation
1	1	0		Read from FIFO
1	0 1 1	1 0 1		No Operation

Figure 2. Read Offset Register

M66850J(64X9-bit) OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	X	X	E5	E4	E3	E2	E1	E0
	Default Value 007H								
PAE MSB	X	X	X	X	X	X	X	X	X
PAF LSB	X	X	X	F5	F4	F3	F2	F1	F0
	Default Value 007H								
PAF MSB	X	X	X	X	X	X	X	X	X

M66851J(256X9-bit) OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	E7	E6	E5	E4	E3	E2	E1	E0
	Default Value 007H								
PAE MSB	X	X	X	X	X	X	X	X	X
PAF LSB	X	F7	F6	F5	F4	F3	F2	F1	F0
	Default Value 007H								
PAF MSB	X	X	X	X	X	X	X	X	X

E0/F0 are the least significant bits.
X=Don't Care.

M66852J(512X9-bit) OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	E7	E6	E5	E4	E3	E2	E1	E0
	Default Value 007H								
PAE MSB	X	X	X	X	X	X	X	X	E8
	Default Value								0
PAF LSB	X	F7	F6	F5	F4	F3	F2	F1	F0
	Default Value 007H								
PAF MSB	X	X	X	X	X	X	X	X	F8
	Default Value								0

M66853J(1024X9-bit) OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	E7	E6	E5	E4	E3	E2	E1	E0
	Default Value 007H								
PAE MSB	X	X	X	X	X	X	X	E9	E8
	Default Value							0	0
PAF LSB	X	F7	F6	F5	F4	F3	F2	F1	F0
	Default Value 007H								
PAF MSB	X	X	X	X	X	X	X	F9	F8
	Default Value							0	0

Figure 3. Offset Regigter Location

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	A value based on GND pin	-0.5 – +7.0	V
V_I	Input voltage		-0.3 – V_{CC}+0.5	V
V_O	Output voltage		-0.3 – V_{CC}+0.5	V
Pd	Maximum power dissipation	Ta=70˚C	Note	mW
Tstg	Storage temperature		-65 – 150	˚C

Note : 450mW(32P6B), 550mW(32P0)

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vcc	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
Topr	Operating ambient temperature	0		70	˚C

DC ELECTRICAL CHARACTERISTICS (Ta=0 – 70˚C, Vcc=5V±10%, GND=0V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{IH}	"H"input voltage		2.0			V
V_{IL}	"L"input voltage				0.8	V
V_{OH}	"H"output voltage	I_{OH} = -1mA	2.4			V
V_{OL}	"L"output voltage	I_{OL} = 8mA			0.4	V
I_{IH}	"H"input current	V_I = V_{CC}, Any input			1.0	μA
I_{IL}	"L"input current	V_I = GND, Any input			-1.0	μA
I_{OZH}	Off state "H"output current	V_O = V_{CC}			5.0	μA
I_{OZL}	Off state "L"output current	V_O = GND			-5.0	μA
I_{CC1}	Operating power supply current	V_I = V_{CC} or GND, f = 40MHz, Outputs are open			70	mA
I_{CC2}	Power supply current (Static)	V_I = V_{CC} or GND, Outputs are open			500	μA
C_I	Input capacitance	f = 1MHz			10	pF
C_O	Off state output capacitance	f = 1MHz			15	pF

SWITCHING CHARACTERISTICS (Ta=0 – 70˚C, Vcc=5V±10%, GND=0V)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AC}	Data Access Time	3		15	ns
t_{WFF}	Write Clock to Full Flag			15	ns
t_{REF}	Read Clock to Empty Flag			15	ns
t_{PAF}	Write Clock to Almost-Full Flag			15	ns
t_{PAE}	Read Clock to Almost-Empty Flag			15	ns
t_{OE}	Output Enable to Output Valid	3		13	ns
t_{OLZ}	Output Enable to Output in Low-Z	0			ns
t_{OHZ}	Output Enable to Output in High-Z	3		13	ns
t_{RSF}	Reset to Flag and Output Valid time			25	ns

TIMING CONDITIONS (Ta=0 – 70˚C, Vcc=5V±10%, GND=0V)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{CLK}	Clock Cycle Time	25			ns
t_{CLKH}	Clock Pulse Width HIGH	10			ns
t_{CLKL}	Clock Pulse Width LOW	10			ns
t_{DS}	Data Setup Time	6			ns
t_{DH}	Data Hold Time	1			ns
t_{ENS}	Enable Setup Time	6			ns
t_{ENH}	Enable Hold Time	1			ns
t_{RS}	Reset Pulse Width	25			ns
t_{RSS}	Reset Setup Time	25			ns
t_{RSR}	Reset Recovery Time	25			ns
t_{SKEW1}	Skew time between Read Clock and Write Clock for Empty Flag and Full Flag	10			ns
t_{SKEW2}	Skew time between Read Clock and Write Clock for Almost-Empty Flag and Almost-Full Flag	40			ns

AC TEST CONDITIONS

In Pulse Levels	GND – 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 4

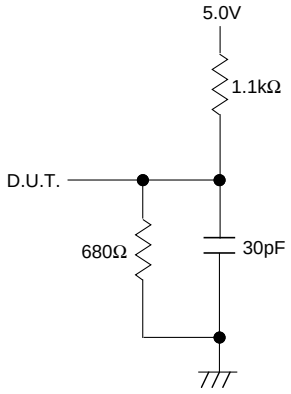
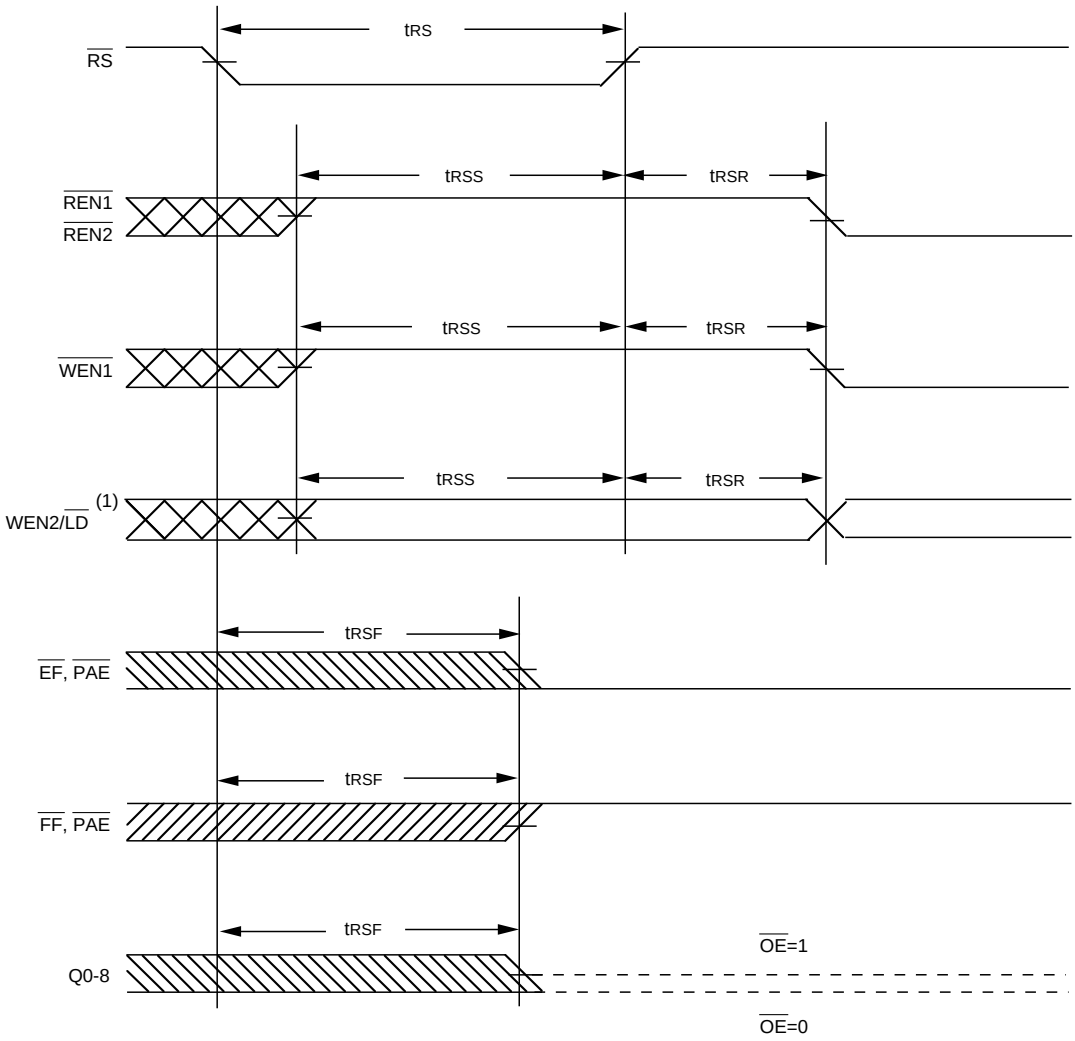


Figure 4. Output Load
Including Test board and scope capacitances.

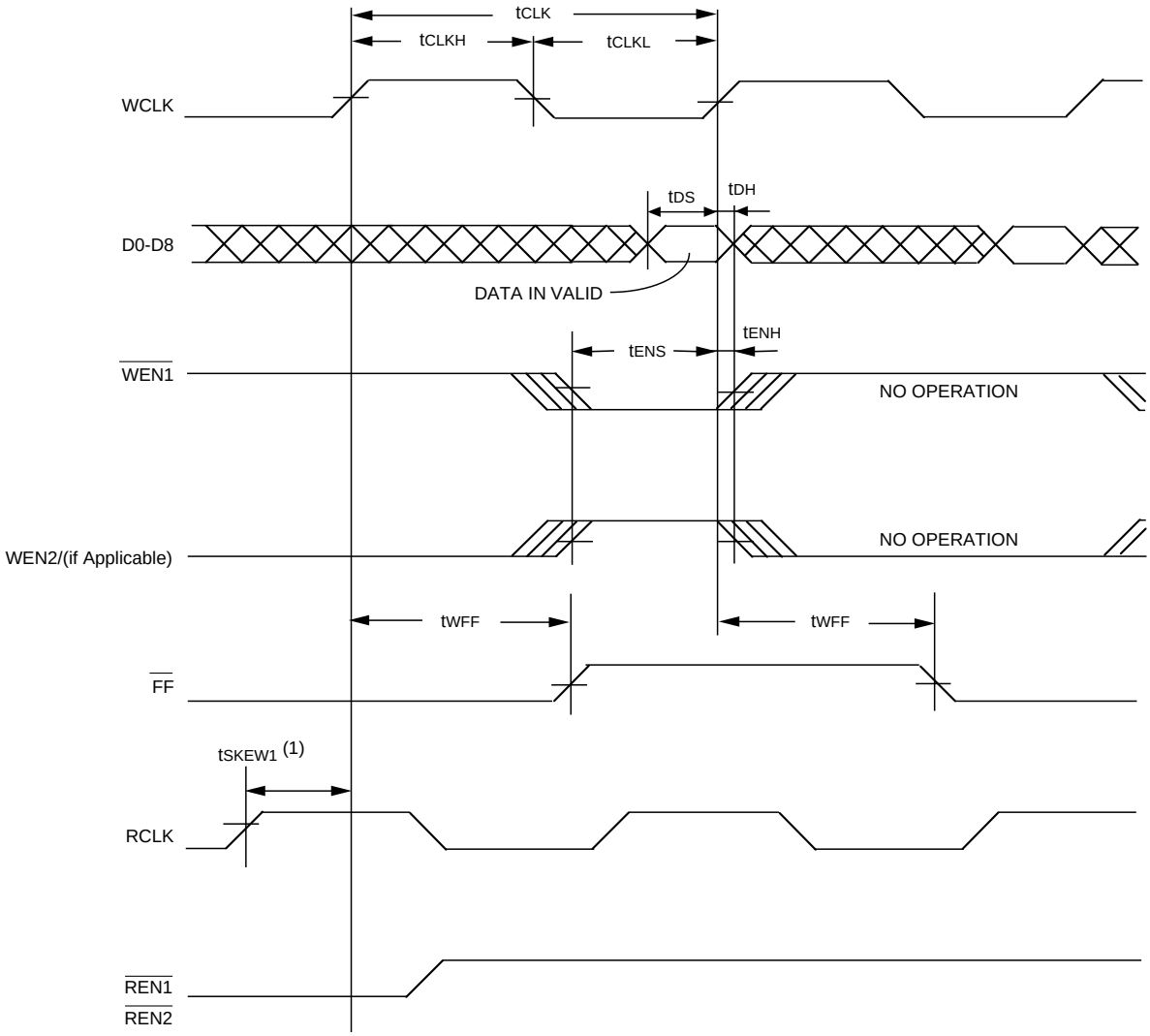
• Reset Timing



NOTE :

1. If during reset WEN2/$\overline{LD}$ is HIGH,this signal functions as a second enable(WEN2).
   If during reset WEN2/$\overline{LD}$ is LOW,this signal functions as an offset register.

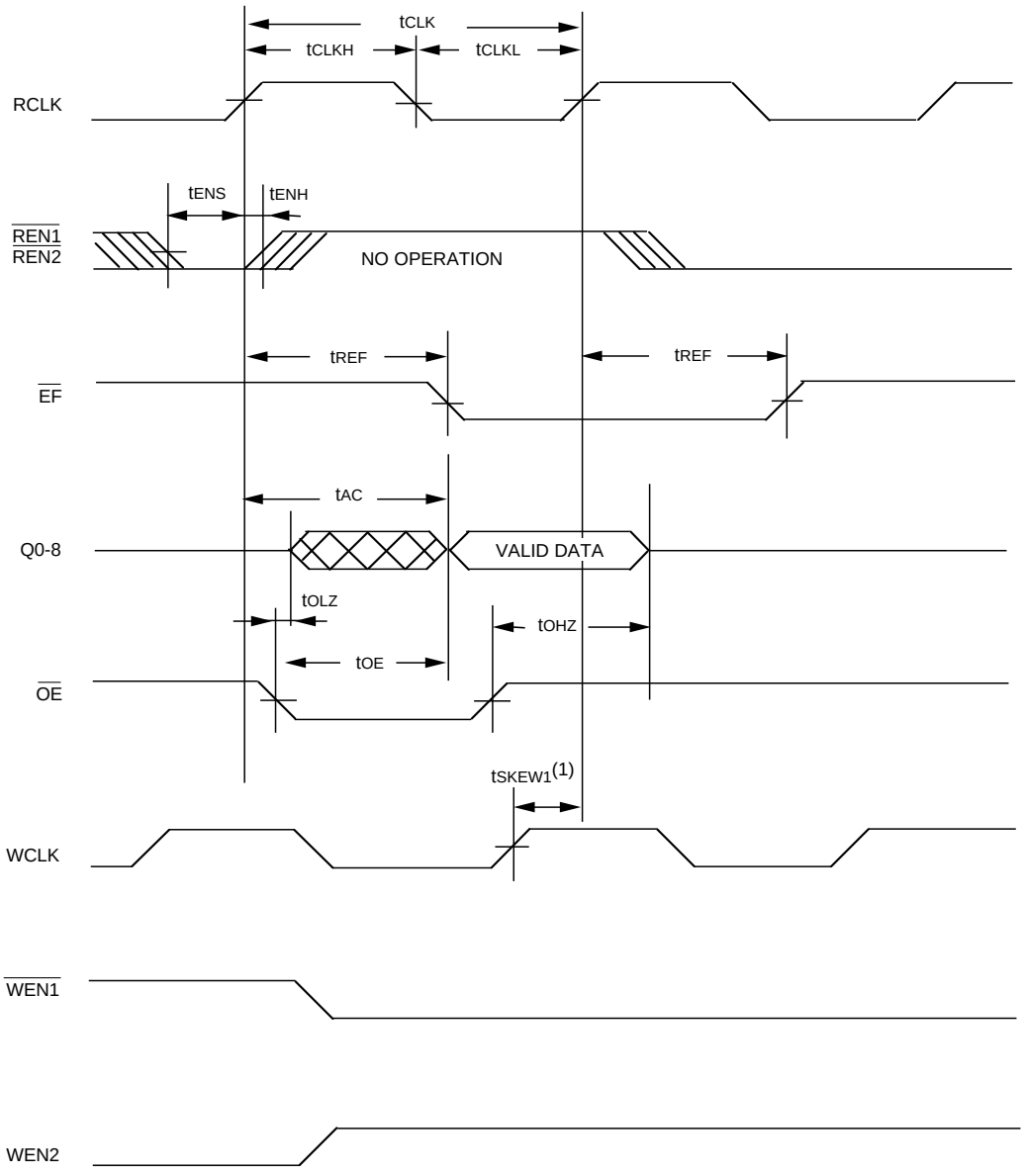
• Write Cycle Timing



NOTE :

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state untill the next WCLK edge.

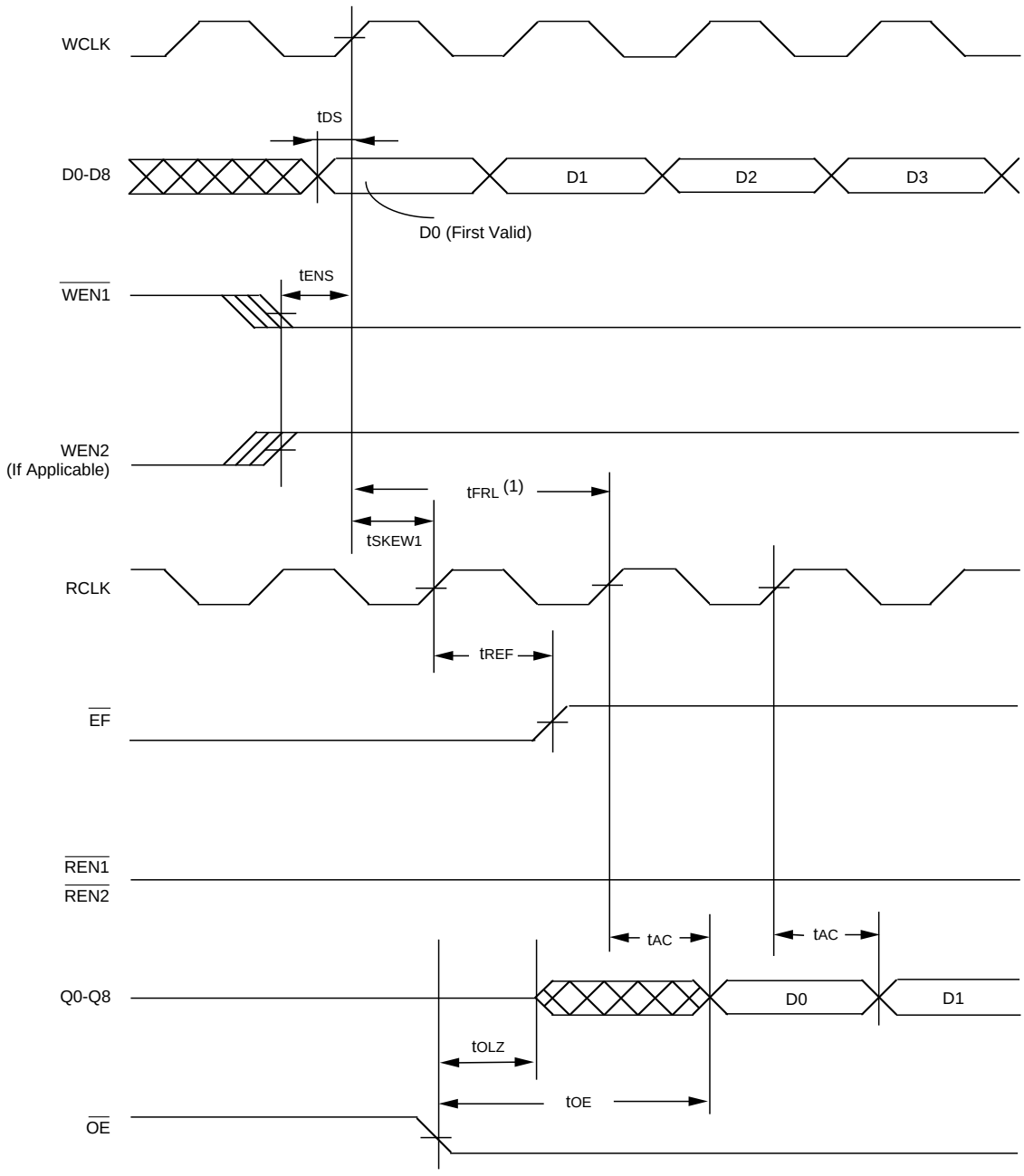
• Read Cycle Timing



NOTE :

1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{EF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1, then $\overline{EF}$ may not change state untill the next RCLK edge.

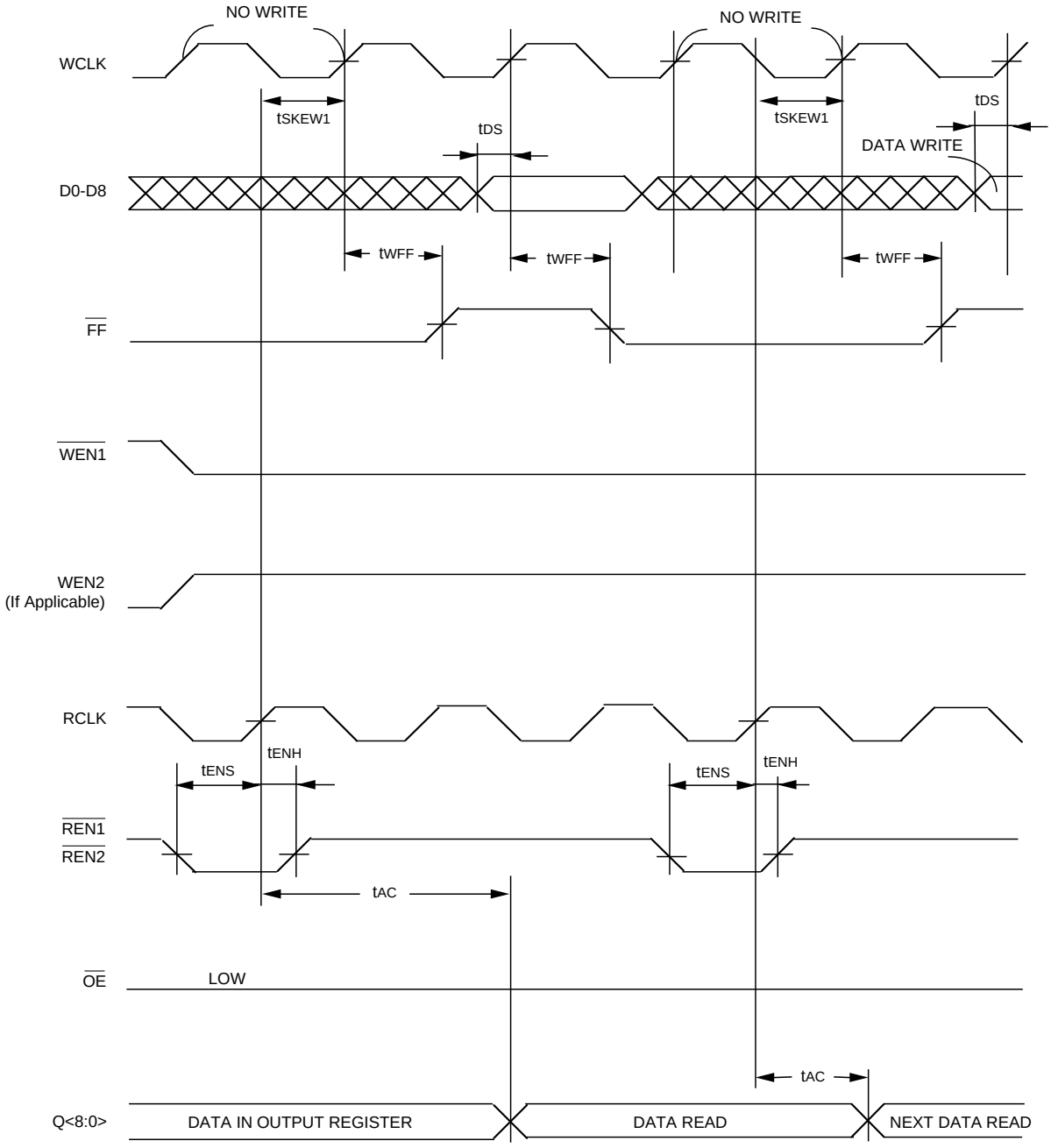
• First Data Word Latency Timing



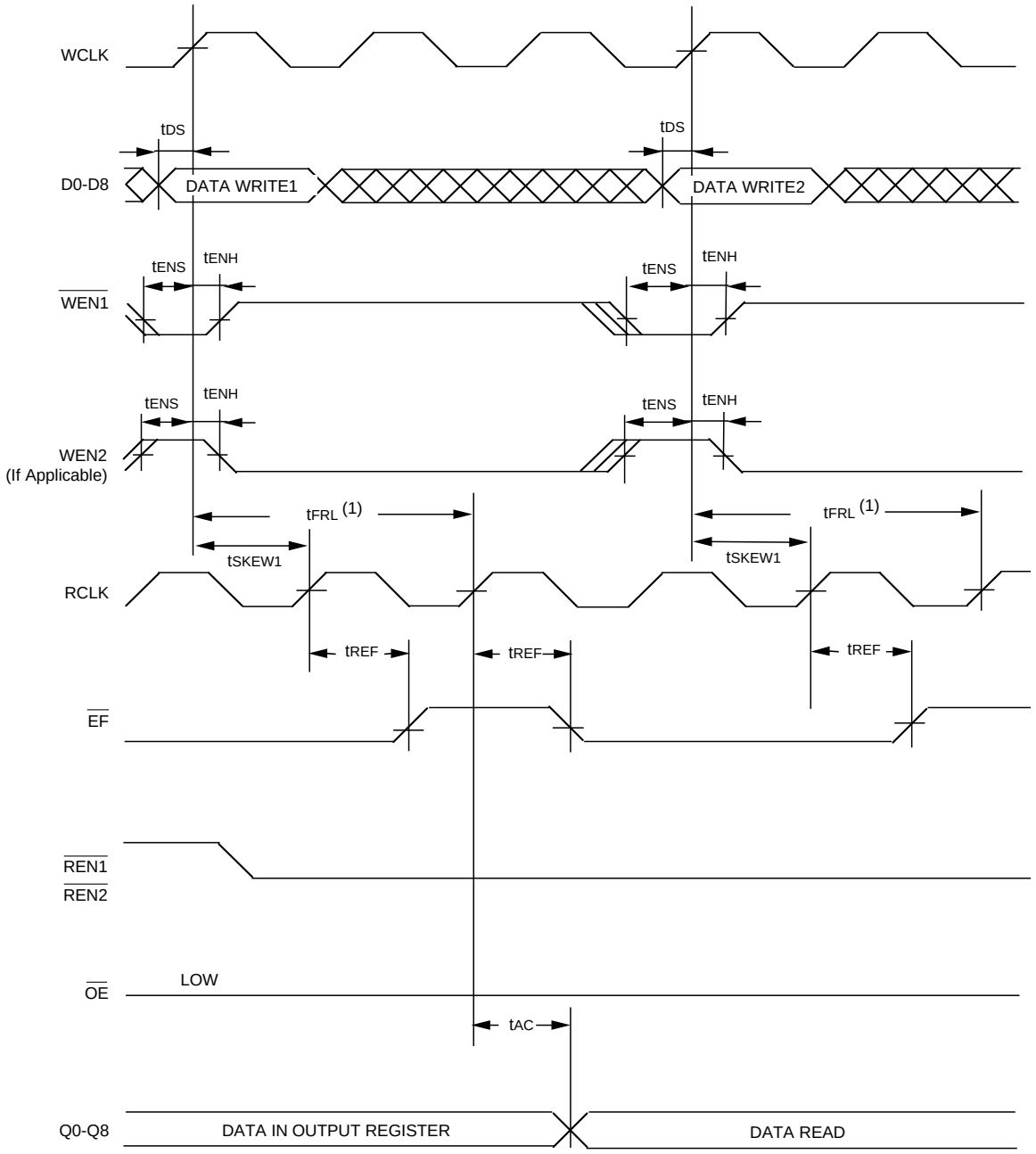
NOTE :

1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum=$t_{CLK}+t_{SKEW1}$.
   When $t_{SKEW1} \leq$ minimum specification, t_{FRL} maximum=$2t_{CLK}+t_{SKEW1}$ or $t_{CLK}+t_{SKEW1}$.

• Full Flag Timing



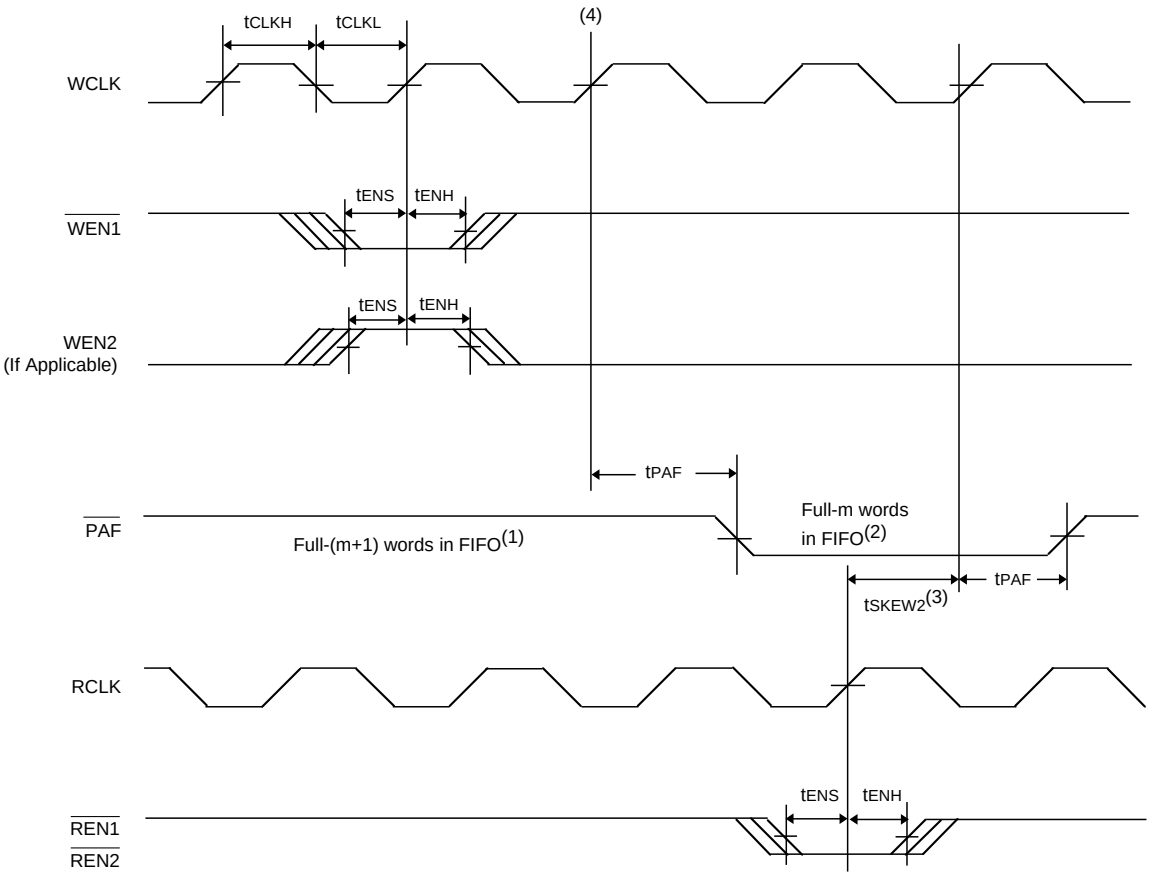
• Empty Flag Timing



NOTE :

1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum=$t_{CLK}+t_{SKEW1}$.
   When $t_{SKEW1} \leq$ minimum specification, t_{FRL} maximum=$2t_{CLK}+t_{SKEW1}$ or $t_{CLK}+t_{SKEW1}$.

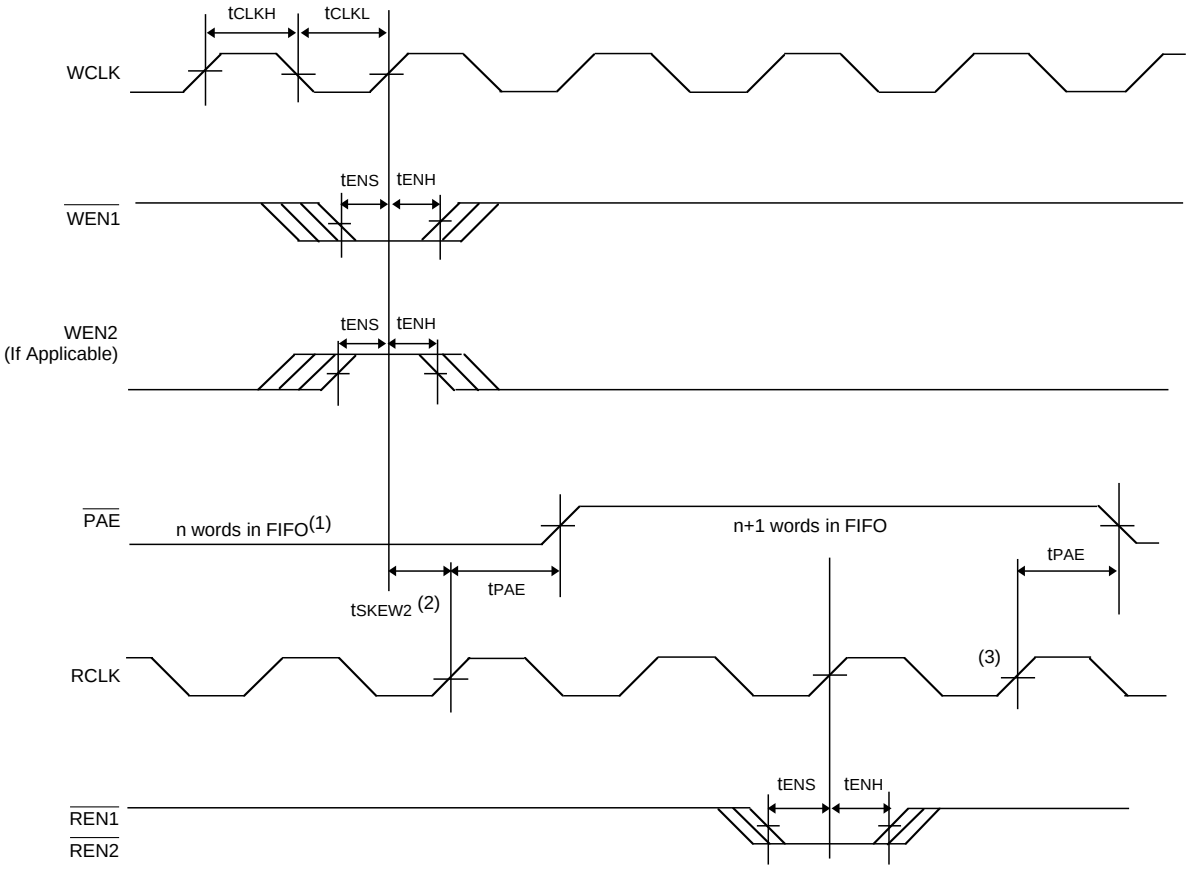
• Programmable Full Flag Timing



NOTES :

1. $\overline{PAF}$ offset=m.
2. 64-m words in for M66850, 256-m words in for M66851,512-m words in for M66852, 1024-m words in for M66853.
3. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state untill the next rising edge of WCLK.
4. If a write is performed on this rising edge of the write clock,there will be Full-(m-1) words in the FIFO when $\overline{PAF}$ goes LOW.

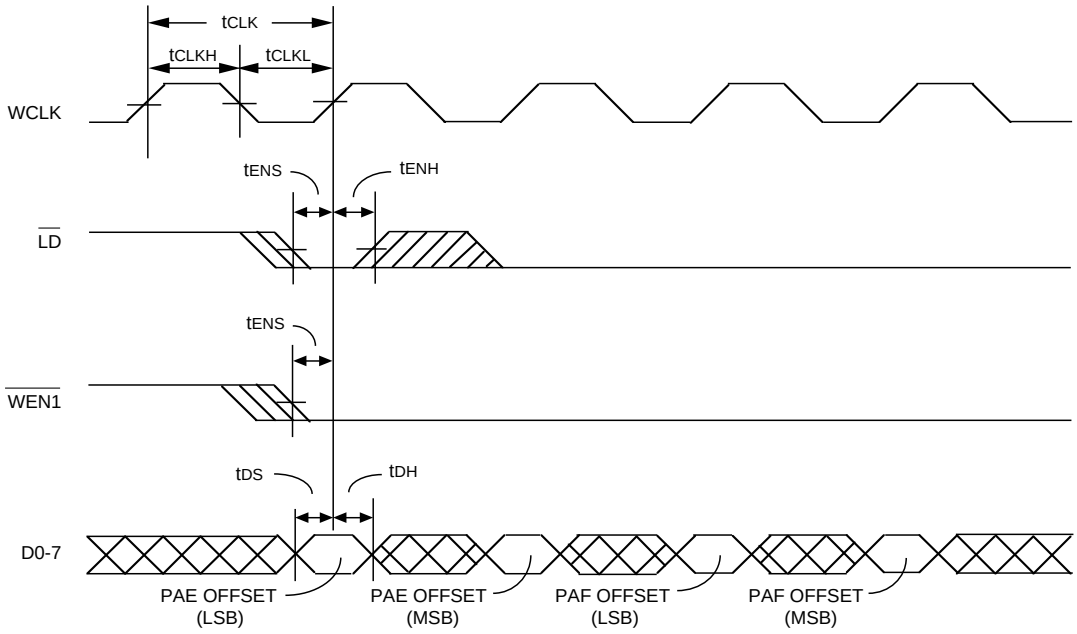
• Programmable Empty Flag Timing



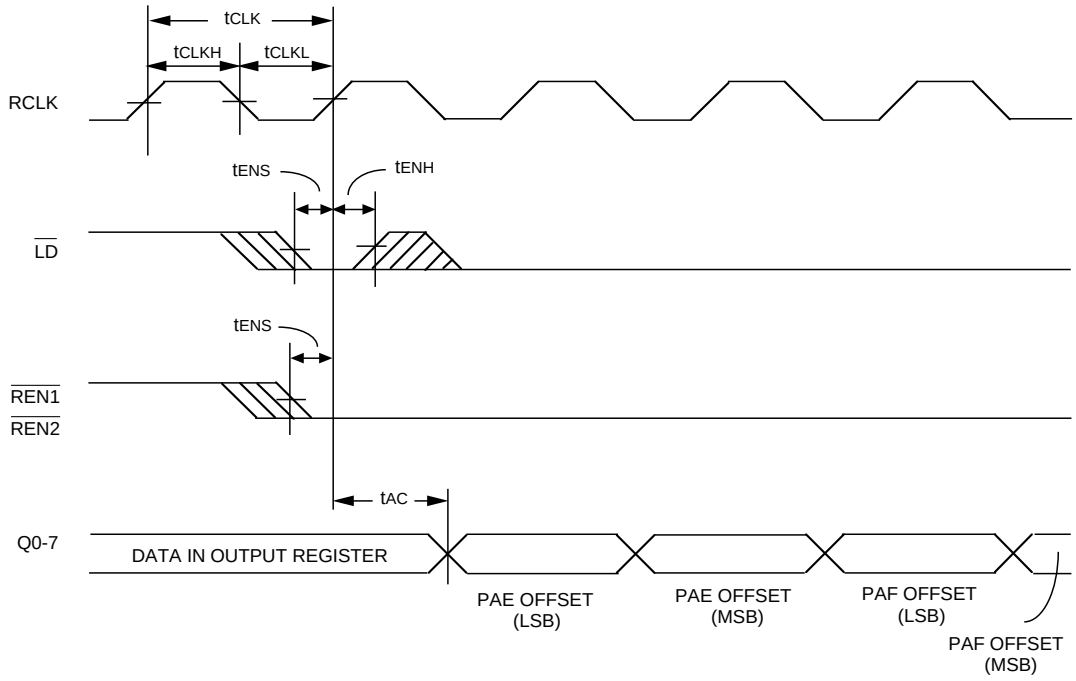
NOTES :

1. $\overline{PAF}$ offset=m.
2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to change during that clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state untill the next rising edge of RCLK.
3. If a read is performed on this rising edge of the read clock, there will be Empty+(n-1) words in the FIFO when $\overline{PAE}$ goes LOW.

• Write Offset Registers Timing



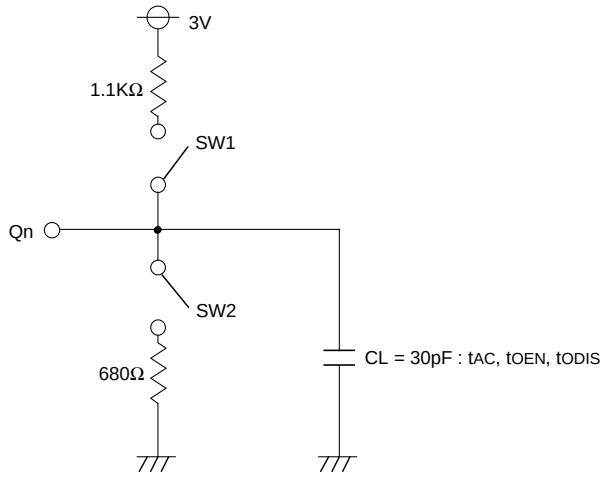
• Read Offset Registers Timing



NOTE :

A read and write should not be performed simultaneously to the offset registers.

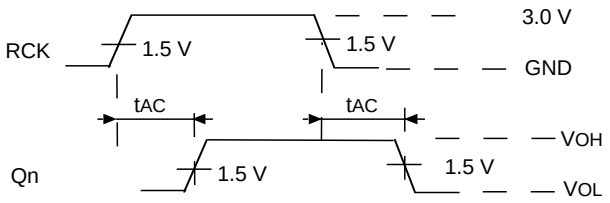
PARAMETER MEASURMENT INFORMATION



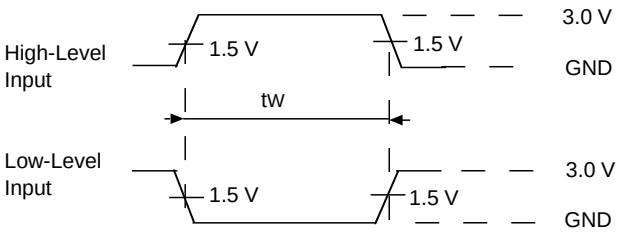
Item	SW1	SW2
tAC	Close	Close
tPLZ	Close	Open
tPHZ	Open	Close
tPZL	Close	Open
tPZH	Open	Close

Input Pulus Level : 0 – 3V
Input Pulus Rising time and Falling time : 3 ns
Threshold voltage of Input / Output : 1.5V
But tPLZ is decided at 10% of output pulse. tPHZ is decided at 90% of output pulse.
Output Load : Including Test board and scope capacitances.

VOLTAGE WAVEFORM PROPAGATION DELAY TIMES



VOLTAGE WAVEFORM PULSE DURATION TIMES



VOLTAGE WAVEFORM ENABLE AND DISABLE TIMES

