Ordering number : ENA1180

SANYO Semiconductors
DATA SHEET

LA74302FN — Monolithic Linear IC
Audio Interface for DSC

Overview

The LA74302FN is a SPEAKER AMP and MIC AMP built-in audio interface for DSC.

Functions

- Three-wire type SERIAL communications, MIC AMP
- MIC power supply provided
- ALC (ALC LEVEL: level changeover in three stages possible)
- REC/PB LPF (fc=4kHz: 3rd order)
- LINE output (with SERIAL MUTE)
- SPEAKER AMP (compatible with BEEP input MIX)
- With serial communications control electronic VOLUME

Specifications

Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		5.0	V
Allowable power dissipation	Pd max	Ta≤85°C *	500	mW
Operating temperature	Topr		-15 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Substrate mounting condition (30mm × 50mm × 0.8mm: glass epoxy) 2S2P

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SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Operating Conditions at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	$V_{CC}L$		3.0	V
	$V_{CC}D$		3.0	V
	$V_{CC}SP$		3.0	V
Allowable operating voltage range	$V_{CC}L$		2.7 to 3.6	V
	$V_{CC}D$		2.7 to 3.6	V
	$V_{CC}SP$	Take care not to exceed Pd max.	2.7 to 3.6	V

Electrical Characteristics at Ta=25°C, V_{CC}L, D, SP=3.0V, f=1kHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current						
Quiescent circuit current 1	$I_{CC}A1$	$V_{CC}A$=3.0V: FULL operation	5.2	7.0	8.8	mA
Quiescent circuit current 2	$I_{CC}A2$	$V_{CC}A$=3.0V: REC BLOCK (MIC/ALC/REC AMP) POWER SAVE	2.4	3.2	4	mA
Quiescent circuit current 3	$I_{CC}A3$	$V_{CC}A$=3.0V: LINE AMP POWER SAVE	4.8	6.4	8.0	mA
Quiescent circuit current 4	$I_{CC}D1$	$V_{CC}D$=3.0V	2.1	2.8	3.5	mA
Quiescent circuit current 5	$I_{CC}SP1$	$V_{CC}SP$=3.0V: SPK POWER ON	1.2	2.5	5	mA
Quiescent circuit current 6	$I_{CC}SP2$	$V_{CC}SP$=3.0V: SPK POWER SAVE	0.3	0.6	0.9	mA
REC output system						
REC reference output LEVEL	VOR	ALC IN, V_{IN}=-44dBV	-15	-14	-13	dBV
REC reference output distortion rate 1	HDR1	ALC IN, VIN=-44dBV, THD: from 2nd to 5th harmonic		0.03	0.1	%
ALC characteristics 1	ALM1	ALC IN, V_{IN}=-28dBV (reference+16dB), ALC LEVEL: reference +10dB	-7	-4	-1	dBV
ALC distortion rate 1	ALMD1	ALC IN, V_{IN}=-28dBV (reference +16dB), ALC LEVEL: reference +10dB		0.3	0.5	%
ALC characteristics 2	ALM2	ALC IN, V_{IN}=-12dBV (reference +32dB), ALC LEVEL: reference +10dB	-7	-4	-1	dBV
ALC distortion rate 2	ALMD2	ALC IN, V_{IN}=-12dBV (reference +32dB), ALC LEVEL: reference +10dB, THD: from 2nd to 5th harmonic		0.4	1	%
REC output noise voltage	VNOR	ALC IN no input, JIS-A Filter		-82	-68	dBV
REC output frequency characteristics 1	FEQR1	ALC IN, V_{IN}=-36dBV, Comparison of f=4kHz/1kHz	-4.5	-3	-1.5	dBV
REC output frequency characteristics 2	FEQR2	ALC IN, V_{IN}=-36dBV, Comparison of f=22kHz/1kHz		-31	-25	dB
REC output frequency characteristics 3	FEQR3	ALC IN, V_{IN}=-36dBV, Comparison of f=100kHz/1kHz		-70	-60	dB
LINE output system						
LINE reference output LEVEL	VOL	PB IN, V_{IN}=-14dBV	-7	-6	-5	dBV
LINE reference output distortion rate	HDL	PB IN, V_{IN}=-14dBV, THD: from 2nd to 5th harmonic		0.1	0.2	%
LINE reference output noise voltage	VNOL	PB IN, no input, JIS-A Filter		-90	-82	dBV
LINE max output LEVEL	VOML	PB IN, LEVEL at which THD (from 2nd to 5th harmonic)=1%	-1	0		dBV
LINE output frequency characteristics 1	FEQP1	PB IN, V_{IN}=-10dBV, Comparison of f=4kHz/1kHz	-4.5	-3	-1.5	dB
LINE output frequency characteristics 2	FEQP2	PB IN, V_{IN}=-10dBV, Comparison of f=22kHz/1kHz		-31	-25	dB
LINE output frequency characteristics 3	FEQP3	PB IN, V_{IN}=-10dBV, Comparison of f=100kHz/1kHz		-70	-60	dB

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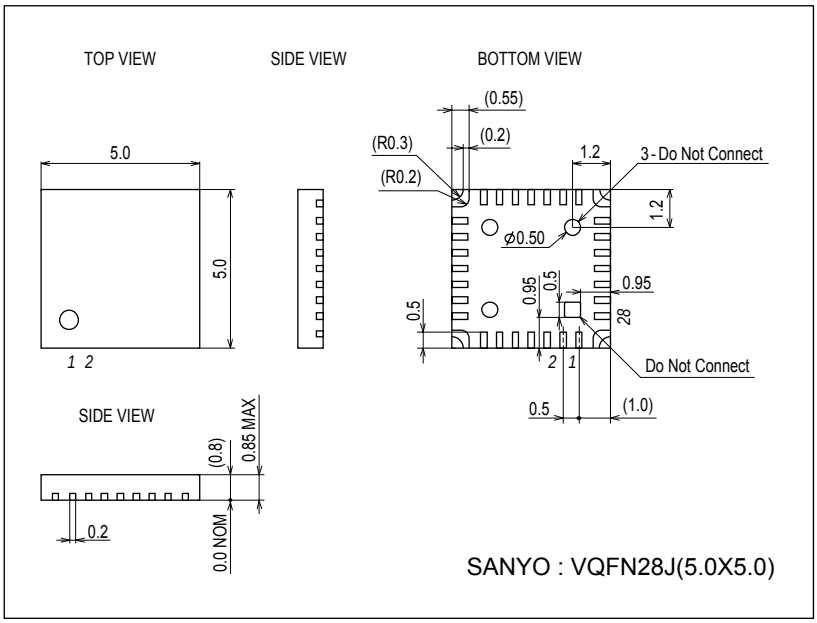
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
SP output system (SP load=as measured at 8Ω end)						
SP reference output LEVEL1 (Vol.MAX)	VOSP1	PB IN, V_{IN}=-14dBV, Vol=MAX (Serial DATA=31)	-8	-4	0	dBV
SP reference output distortion rate	THDSP	PB IN, V_{IN}=-14dBV, Vol=MAX, THD: from 2nd to 5th harmonic		0.7	1.5	%
SP reference output LEVEL2 (Vol.TYP)	VOSP2	PB IN, V_{IN}=-14dBV, Vol=TYP (Serial DATA=12)	-22	-16	-10	dBV
SP reference output LEVEL3 (Vol.MIN)	VOSP3	PB IN, V_{IN}=-14dBV, Vol=MIN (Serial DATA=0), JIS-A Filter		-90	-70	dBV
SP reference output noise voltage	VNOSP	PB IN no input, Vol=MAX, JIS-A Filter		-86	-70	dBV
SP max rated output	VOMSP	PB IN, Vol=MAX, LEVEL at which THD=10%	150	250		mW
MIC output system						
MIC voltage gain	VGMIC	MIC IN, V_{IN}=-40dBV	25	26	27	dB
MIC output distortion rate	HDMIC	MIC IN, V_{IN}=-40dBV, THD: up to quintic		0.1	0.5	%
MIC output noise voltage	VNOMIC	MIC IN, no input, JIS-A Filter		-91	-83	dBV
MIC max output LEVEL	VOMIC	Output LEVEL at which THD=1%	-3	-1		dBV
MIC V_{CC} output voltage	VMIC	At 2.2kΩ load	2.1	2.3	2.5	V
Control system						
Serial CLOCK frequency	FCLK			1.25	1.5	MHz
Serial input LOW level	SERLO		0		0.7	V
Serial input HIGH level	SERHI		2.3		3.5	V

Package Dimensions

unit : mm (typ)

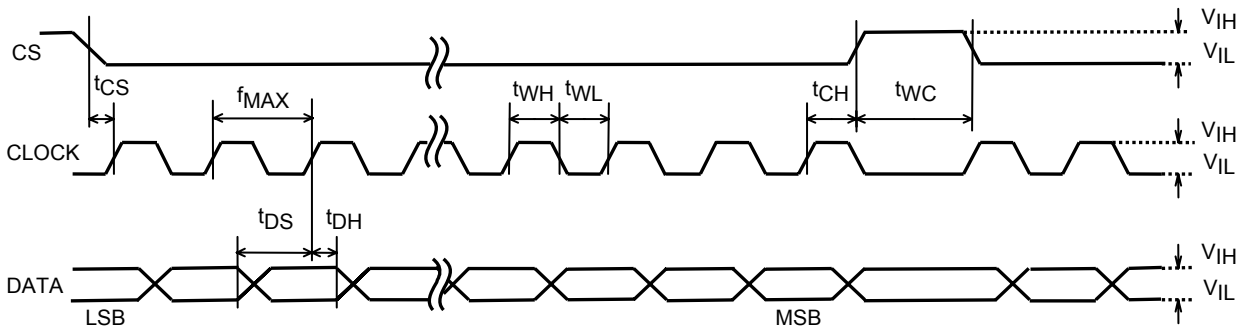
3292A



Description of the Content of Serial Communication

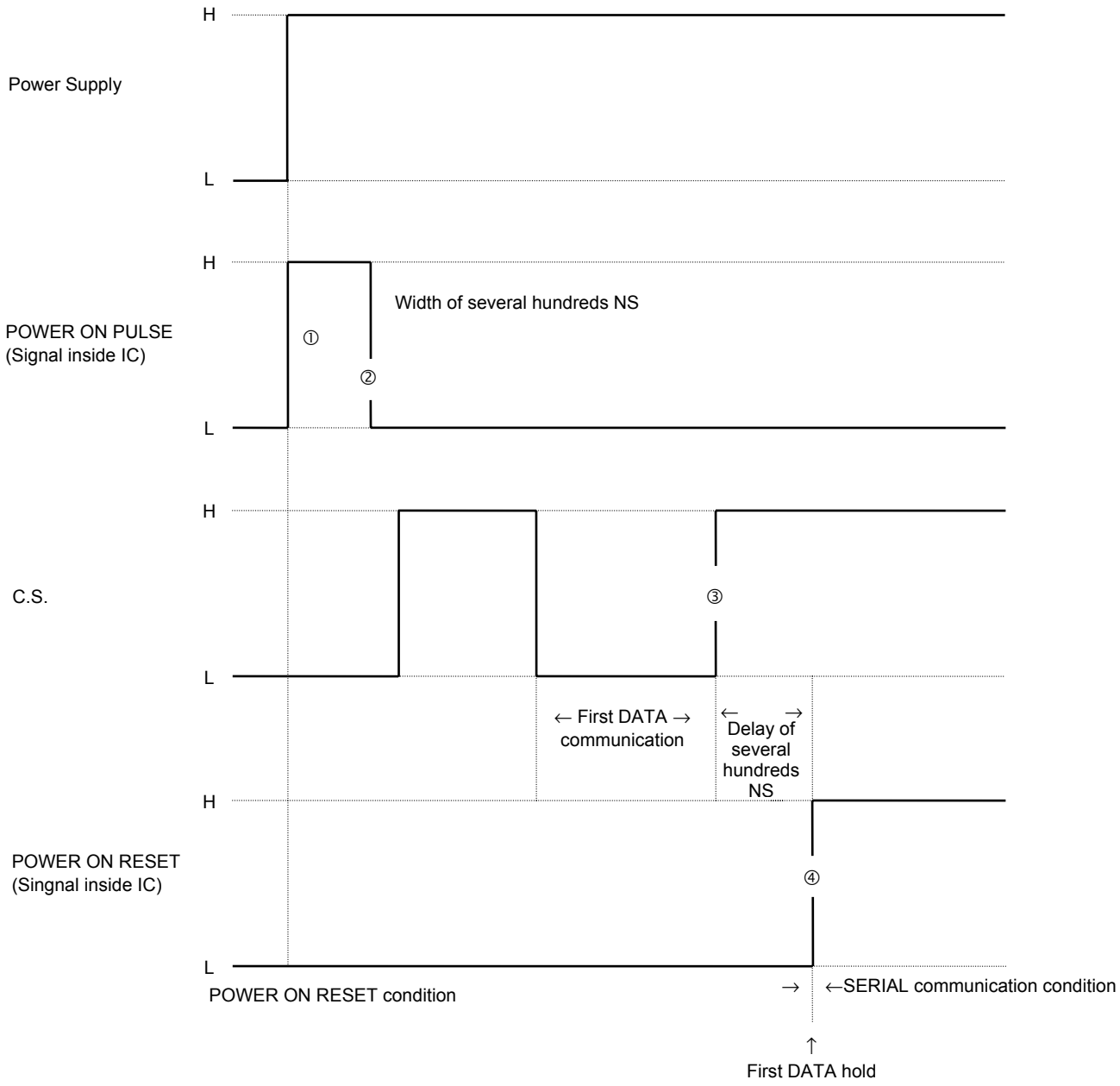
DATA No.	Parameter	Default
0	DUMMY	-
1	DUMMY	-
2	DUMMY	-
3	MIC AMP POWER SW 0: ON, 1: OFF	0
4	ALC AMP POWER SW 0: ON, 1: OFF	0
5	ALC LEVEL CTL +10dB: 0 +12dB: 1 +14dB: 0	0
6	0 0 1	0
7	REC BLOCK POWER SW 0: ON, 1: OFF	0
8	LINE OUT POWER SW 0: ON, 1: OFF	0
9	LINE MUTE SW 0: ON, 1: OFF	0
10	SPK POWER SW 0: ON, 1: OFF	1
11	DATA=1 1 1 1 1 1 : VOL MAX	0
12	DATA=2 ∫	0
13	DATA=4 0 0 0 0 0 : VOL MIN (MUTE)	0
14	DATA=8	0
15	DATA=16 * EVR setting (the numeral shown in the left is decimal. For characteristics, see P9.)	0

Serial Transmission Timing



- f_{MAX} (Max clock frequency) 1.5MHz
- t_{WL} (Clock pulse width: Low) 333ns or more
- t_{WH} (Clock pulse width: High) 333ns or more
- t_{CS} (Chip enable setup time) 333ns or more
- t_{CH} (Chip enable hold time) 333ns or more
- t_{DS} (Data setup time) 333ns or more
- t_{DH} (Data hold time) 333ns or more
- t_{WC} (Chip enable pulse width) 333ns or more
- V_{IH} (High voltage lower limit) 2.3V to 3.5V
- V_{IL} (Low voltage upper limit) 0V to 0.7V

POWER ON Condition (SERIAL communication)



The POWER ON RESET condition continues up to the second C.S rising (③) entered after falling (②) of POWER ON PULSE (①) generated inside IC at a time of power ON.
Actually, because of delay of several hundreds NS in the IC, the first DATA condition begins in (④) and the normal SERIAL communication condition begins after (④).

Electrical Characteristics Measurement Method at Ta=25°C, V_{CC}L, D, SP=3.0V, f=1kHz

Symbol	Input		Output		Serial control setting														
	Pin	Conditions	Pin	Conditions	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Circuit current																				
$I_{CC}A1$	12	$V_{CC}A$=3.0V No input	12	FULL operation	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$I_{CC}A2$	12	$V_{CC}A$=3.0V No input	12	MIC/ALC/REC AMP POWER SAVE	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0
$I_{CC}A3$	12	$V_{CC}A$=3.0V No input	12	LINE AMP POWER SAVE	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
$I_{CC}S1$	26	$V_{CC}SP$=3.0V No input	26	FULL operation	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$I_{CC}S2$	26	$V_{CC}SP$=3.0V No input	26	SPK AMP POWER SAVE	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
$I_{CC}D$	10	$V_{CC}D$=3.0V No input	10	FULL operation	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
REC output system																				
VOR1	16	V_{IN}=-44dBV f=1kHz	13	400 to 30kHz LPF used	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
HDR	16	V_{IN}=-44dBV f=1kHz	13	400 to 30kHz LPF used THD: from 2nd to 5th harmonic	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ALM1	16	V_{IN}=-28dBV f=1kHz	13	400 to 30kHz LPF used	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ALMD1	16	V_{IN}=-28dBV f=1kHz	13	400 to 30kHz LPF used THD: from 2nd to 5th harmonic	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ALM2	16	V_{IN}=-12dBV f=1kHz	13	400 to 30kHz LPF used	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ALMD2	16	V_{IN}=-12dBV f=1kHz	13	400 to 30kHz LPF used THD: from 2nd to 5th harmonic	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VNOR	16	No input	13	JIS-A FILTER used	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FEQR1	16	V_{IN}=-36dBV f=4kHz	13	f=4kHz/1kHz level ratio	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FEQR2	16	V_{IN}=-36dBV f=22kHz	13	f=22kHz/1kHz level ratio	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FEQR3	16	V_{IN}=-36dBV f=100kHz	13	f=100kHz/1kHz level ratio	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LINE output system																				
VOL1	11	V_{IN}=-14dBV f=1kHz	5	400 to 30kHz LPF used	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
HDL	11	V_{IN}=-14dBV f=1kHz	5	400 to 30kHz LPF used THD: from 2nd to 5th harmonic	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
VNOL	11	No input	5	JIS-A FILTER used	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
VOML	11	f=1kHz	5	400 to 30kHz LPF used Level at which THD = 1% (from 2nd to 5th harmonic)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
FEQP1	11	V_{IN}=-10dBV f=4kHz	5	f=4kHz/1kHz level ratio	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
FEQP2	11	V_{IN}=-10dBV f=22kHz	5	f=22kHz/1kHz level ratio	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
FEQP3	11	V_{IN}=-10dBV f=100kHz	5	f=100kHz/1kHz level ratio	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
SPK output system (SPK end: measured with 8Ω)																				
VOSP1	11	V_{IN}=-14dBV f=1kHz	25 27	400 to 30kHz LPF used Vol.=MAX	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
THDSP	11	V_{IN}=-14dBV f=1kHz	25 27	400 to 30kHz LPF used Vol.=MAX, THD: from 2nd to 5th harmonic	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

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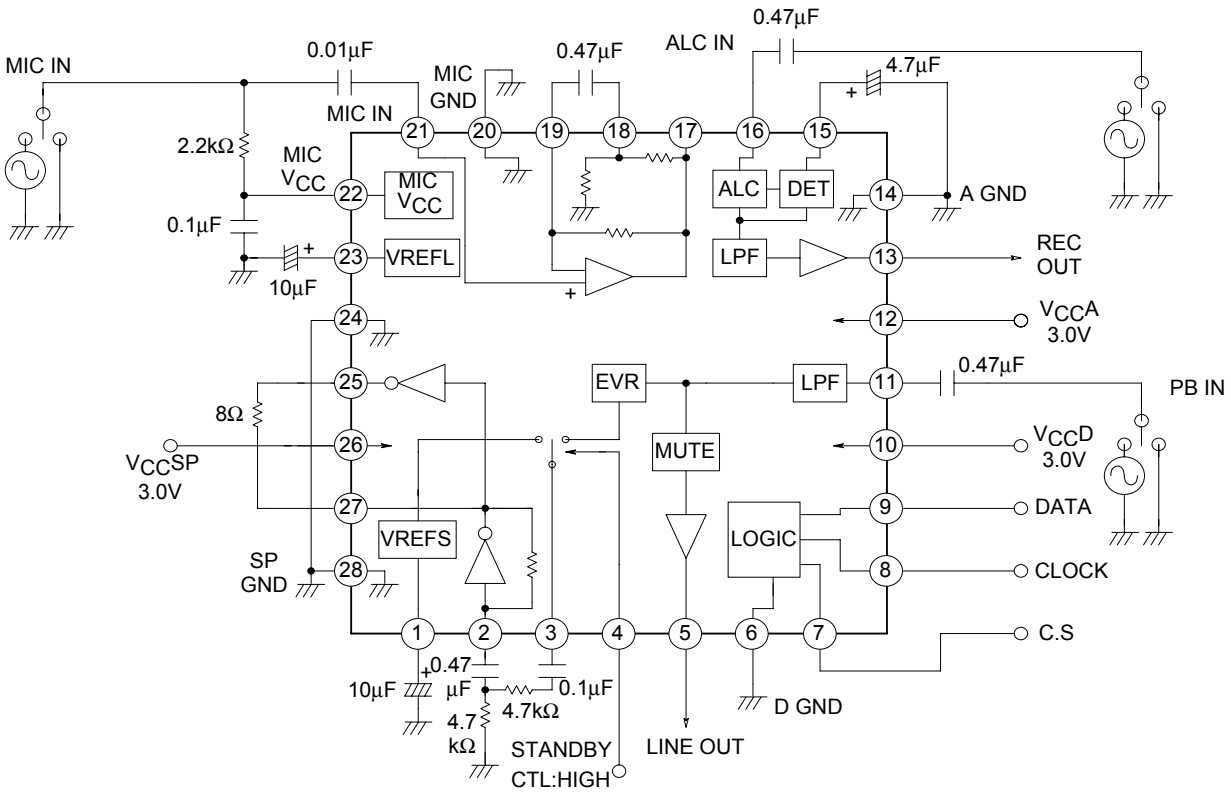
Symbol	Input		Output		Serial control setting															
	Pin	Conditions	Pin	Conditions	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SPK output system (SPK end: measured with 8Ω)																				
VOSP2	11	V_{IN}=-14dBV f=1kHz	25 27	400 to 30kHz LPF used Vol.=TYP	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
VOSP3	11	V_{IN}=-14dBV f=1kHz	25 27	JIS-A FILTER used Vol.=MIN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPK output system (SPK end: measured with 8Ω)																				
VNOSP	11	No input	25 27	JIS-A FILTER used Vol.=MAX	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
VOSSP	11	f=1kHz	25 27	400 to 30kHz LPF used Vol.=MAX, Level at which THD = 10% (from 2nd to 5th harmonic)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
MIC output system																				
VGMIC	21	Vin=-40dBV f=1kHz	17	400 to 30kHz LPF used	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
HDMIC	21	Vin=-40dBV f=1kHz	17	400 to 30kHz LPF used THD: from 2nd to 5th harmonic	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VNOMIC	21	No input	17	JIS-A FILTER used	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VOMIC	21	f=1kHz	17	400 to 30kHz LPF used Level at which THD=1% (from 2nd to 5th harmonic)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VMIC	22	No input	22	Measure the output voltage at 2.2kΩ load	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description of Pin Functions

Pin No.	Pin Description
1	Removal of speaker ripple
2	Speaker input
3	EVR output
4	STANDBY control
5	LINE output
6	D GND
7	C.S. input
8	CLOCK input
9	DATA input
10	V_{CC}D
11	PB input
12	V_{CC}A
13	REC output
14	A GND
15	ALC detection
16	ALC input
17	MIC output
18	MIC Amp attenuator output
19	MIC Amp NFB
20	MIC GND
21	MIC input
22	INT power supply for MIC
23	MIC Removal of ripple for V_{CC} and VREFL
24	SPK GND
25	Speaker positive-phase output
26	V_{CC}SP
27	Speaker negative-phase output
28	SPK GND

LA74302FN BLOCK Diagram and Test Circuit Diagram



LA74302FN EVR characteristics

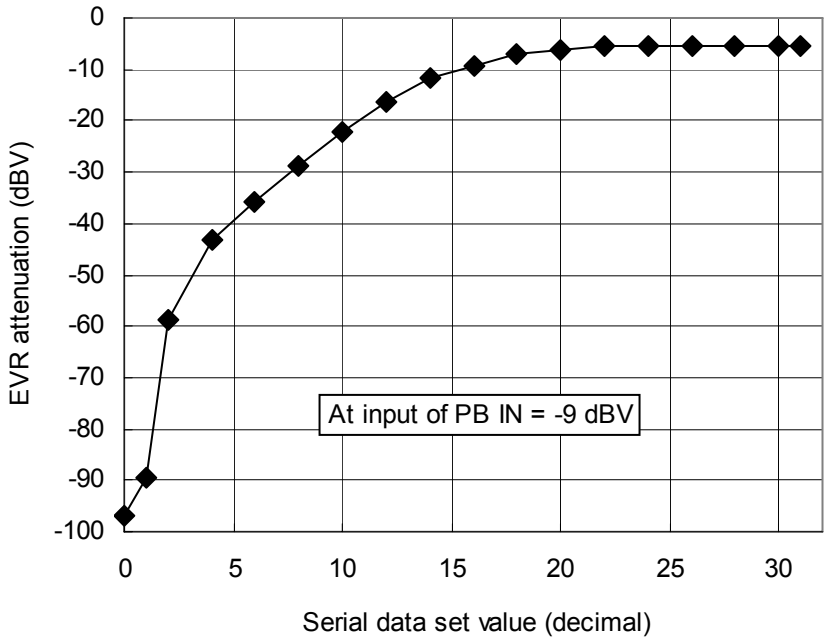
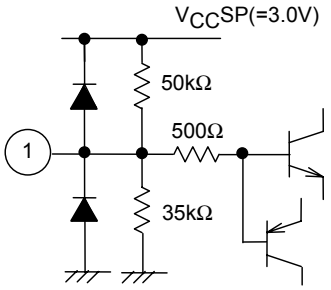
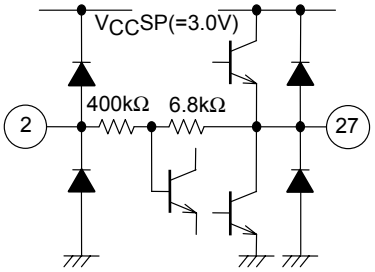
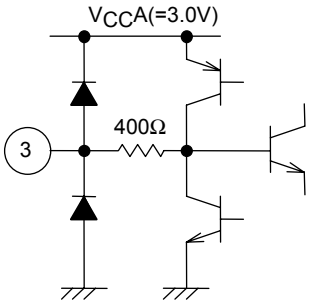
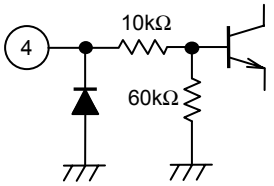
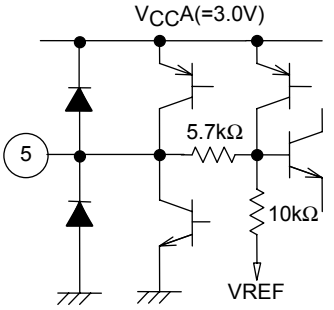
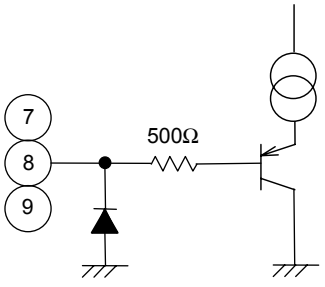


Table of Input/Output Forms of LA74302FN

PIN	Pin Name	DC Voltage	AC Voltage	Description of Functions	Equivalent Circuit Diagram in Pin
1	VREFS	1.25V		Ripple removal pin	
2 27	SP IN SPK OUT-	1.25V 1.25V	-10dBV (EVR MAX at PB reference input) -10dBV (EVR MAX at PB reference input)	Speaker input pin Speaker negative-phase output pin	
3	EVR OUT	1.64V	-10dBV (EVR MAX at PB reference input)	EVR output pin	
4	STANDBY H			STANDBY control pin 2V or more: STANDBY * Puts all amplifiers excluding speakers into the STANDBY state.	
5	LINE OUT	1.50V	-6dBV (At PB reference input)	LINE output pin	
6	D_GND	0V		GND pin for serial communication block	
7 8 9	CS CLOCK DATA			CS input pin CLOCK input pin DATA input pin	

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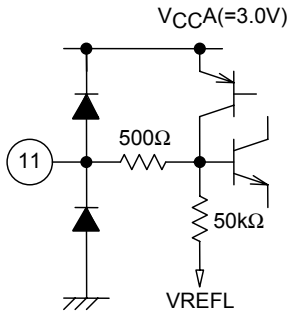
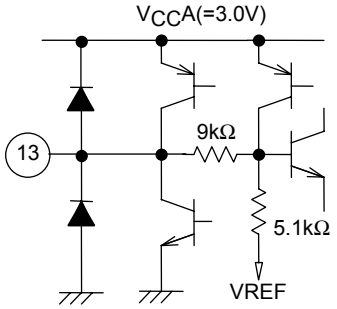
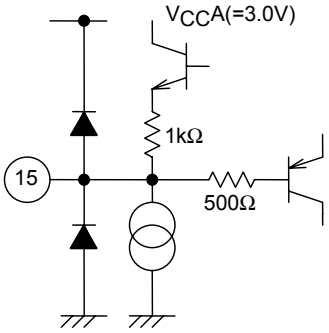
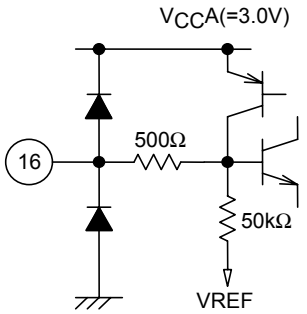
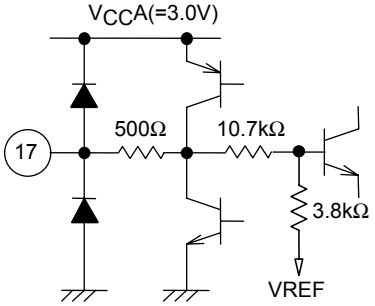
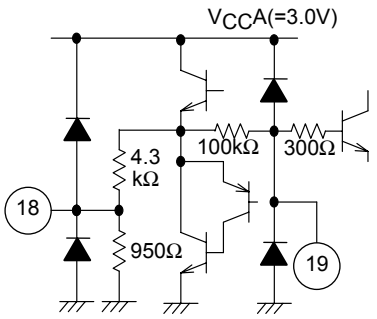
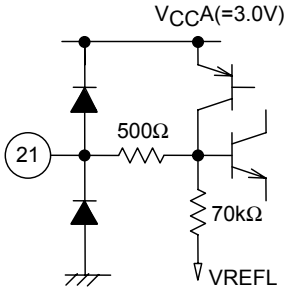
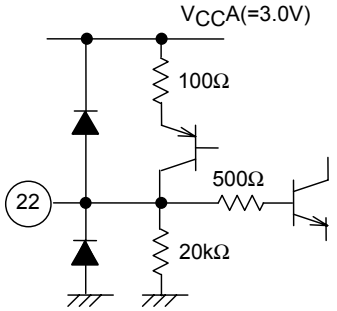
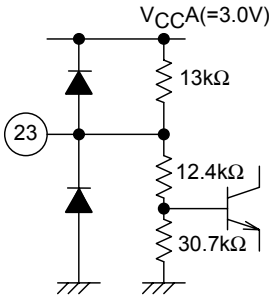
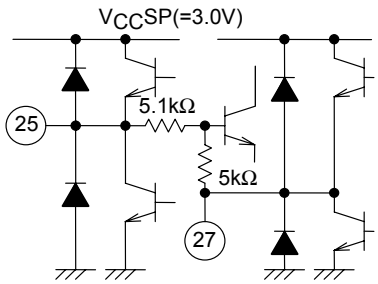
PIN	Pin Name	DC Voltage	AC Voltage	Description of Functions	Equivalent Circuit Diagram in Pin
10	$V_{CC}D$	3.0V		Power pin for driving of the serial communication block and all amplifier starter circuits	
11	PB IN	1.64V	-14dBV (Reference input level)	PB input pin	
12	$V_{CC}A$	3.0V		Analog signal block power pin	
13	REC OUT	1.50V	-14dBV (At MIC reference input)	REC output pin	
14	A GND	0V		Analog signal block GND pin	
15	ALC DET			ALC detection pin	
16	ALC IN	1.64V	-44dBV (At MIC reference input/output)	ALC input pin	
17	MIC OUT	1.64V	-44dBV (At MIC reference input)	MIC output pin	

Continued on next page.

Continued from preceding page.

PIN	Pin Name	DC Voltage	AC Voltage	Description of Functions	Equivalent Circuit Diagram in Pin
18	MIC ATT	0.30V		MIC Amp attenuator output pin	
19	MIC NFB	1.64V		MIC Amp NFB pin	
20	MIC GND	0V		MIC Amp block GND pin	
21	MIC IN	1.64V	-70dBV (Reference input level)	MIC input pin	
22	MIC V_{CC}	2.30V		MIC power pin	
23	VREFL	2.30V		MIC V_{CC} and VREFL ripple removal pin	
24 28	SP GND	0V		Speaker GND pin	
25	SPK OUT+	1.25V	-10dBV (EVR MAX at PB reference input)	Speaker positive-phase output pin	
26	V_{CC}SP	3.0V		Speaker power pin	

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