IS61LV6424

64K x 24 HIGH□SPEED CMOS STATIC RAM WITH 3.3V SUPPLY

FEATURES

- High-speed access time: 9, 10, 12, 15 ns
- CMOS low power operation
  - 594 mW (max.) operating @ 9 ns
  - 36 mW (max.) CMOS standby
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Available in 100-pin LQFP

DESCRIPTION

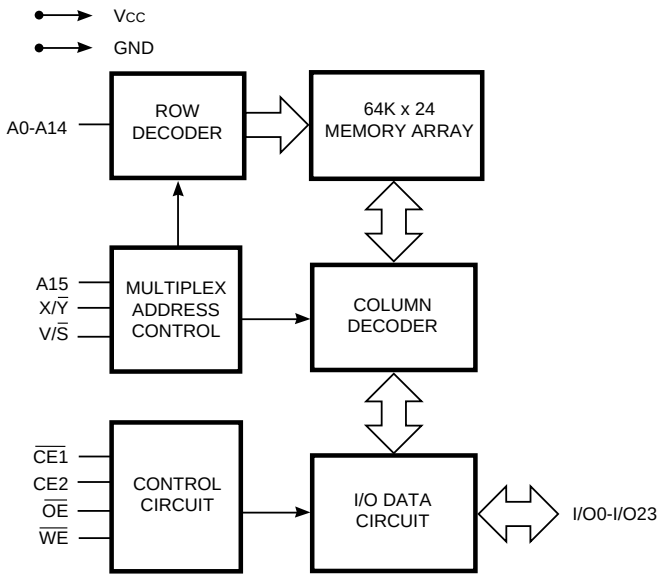
The *ICSI* IS61LV6424 is a high-speed, static RAM organized as 65,536 words by 24 bits. It is fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 9 ns with low power consumption.

When $\overline{CE1}$ is HIGH and CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

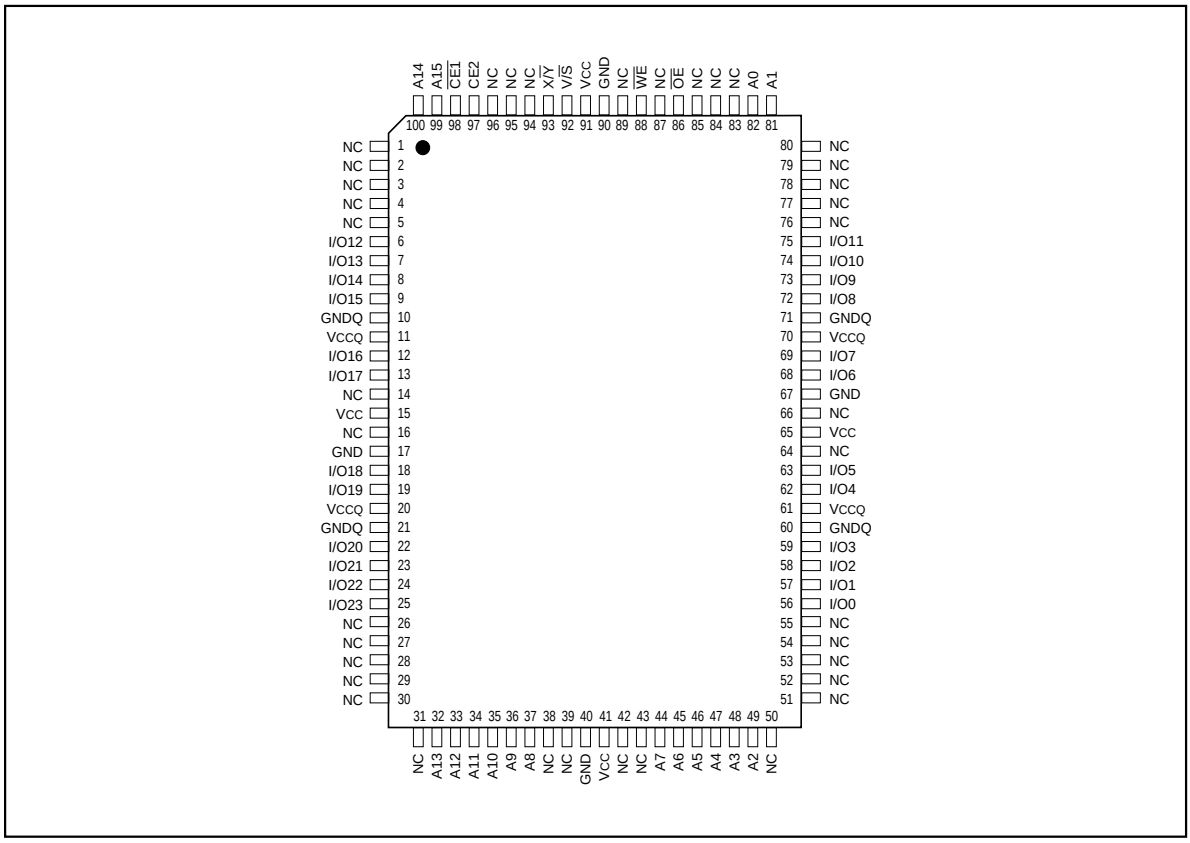
Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE1}$, CE2, and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS61LV6424 is packaged in the JEDEC standard 100-pin 14*20*1.4mm LQFP.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
100 Pin LQFP



PIN DESCRIPTIONS

A0-A14	Address Inputs
A15, X/Y	Multiplexed Address
I/O0-I/O23	Data Inputs/Outputs
$\overline{CE1}$, $\overline{CE2}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
V/S	Address Multiplexer
NC	No Connection
Vcc	Power
VCCQ	Isolated Output Buffer Supply
GND	Ground
GNDQ	solated Output Buffer Ground

TRUTH TABLE

Mode	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	V/$\overline{S}$	I/O0□I/O23	Vcc Current
Not Selected	H	X	X	X	X	High-Z	ISB1, ISB2
	X	H	X	X	X	High-Z	
Read Using X/$\overline{Y}$	L	H	L	H	H	DOUT	ICC
Read Using A15	L	H	L	H	L	DOUT	ICC
Write Using X/$\overline{Y}$	L	H	X	L	H	DIN	ICC
Write Using A15	L	H	X	L	L	DIN	ICC
Output Disable	L	H	H	H	X	High-Z	ICC

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter		Value	Unit
VCC	Power Supply Voltage Relative to GND		–0.5 to 5.0	V
VTERM	Terminal Voltage with Respect to GND		–0.5 to Vcc + 0.5	V
TSTG	Storage Temperature		–65 to + 150	°C
TBIAS	Temperature Under Bias:	Com.	–10 to + 85	°C
		Ind.	–45 to + 90	°C
PT	Power Dissipation		2.0	W
IOUT	DC Output Current		±20	mA

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	VCC (9, 10 ns)	VCC (12, 15 ns)
Commercial	0°C to +70°C	3.3V + 10%, – 5%	3.3V ± 10%
Industrial	–40°C to +85°C	3.3V + 10%, – 5%	3.3V ± 10%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = Min., IOH = –4.0 mA	2.4	—	V
VOL	Output LOW Voltage	VCC = Min., IOL = 8.0 mA	—	0.4	V
VIH	Input HIGH Voltage		2.2	VCC + 0.3	V
VIL	Input LOW Voltage[1]		–0.3	0.8	V
ILI	Input Leakage	GND ≤ VIN ≤ VCC	–1	1	µA
ILO	Output Leakage	GND ≤ VOUT ≤ VCC, Outputs Disabled	–1	1	µA

Note:
1. VIL (min.) = –0.3V DC; VIL (min.) = –2.0V AC (pulse width ≤ 2.0 ns).
VIH (max.) = VCC + 0.3V DC; VIH (max.) = VCC + 2.0V AC (pulse width ≤ 2.0 ns).

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		□9 ns Min.	□9 ns Max.	□10ns Min.	□10ns Max.	□12 ns Min.	□12 ns Max.	□15 ns Min.	□15 ns Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	165	—	150	—	125	—	100	mA
			Ind.	—	170	—	155	—	130	—	105	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, f = max. $\overline{CE1} \geq V_{IH}$, CE2 ≤ V_{IL}	Com.	—	40	—	40	—	35	—	30	mA
			Ind.	—	45	—	45	—	40	—	25	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE1} \geq V_{CC}$ – 0.2V, CE2 ≤ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V, or $V_{IN} \leq$ 0.2V, f = 0	Com.	—	10	—	10	—	10	—	10	mA
			Ind.	—	15	—	15	—	15	—	15	

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	2 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

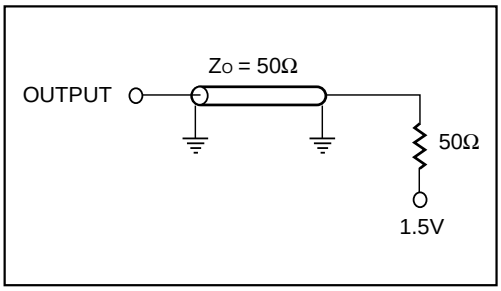


Figure 1

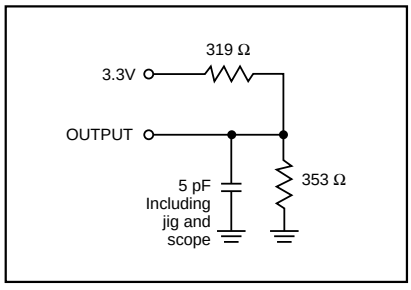


Figure 2

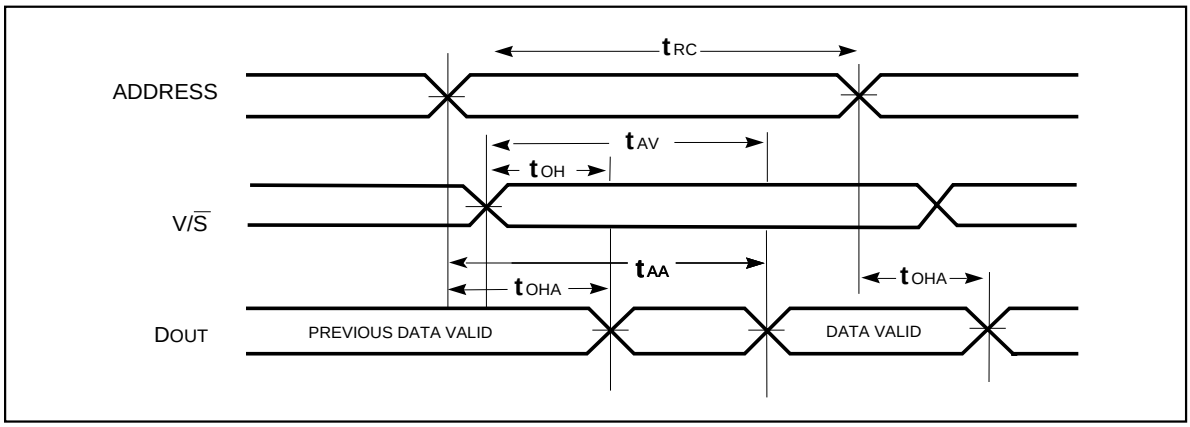
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-9 Min.	-9 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	Unit
t_{RC}	Read Cycle Time	9	—	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	9	—	10	—	12	—	15	ns
t_{AV}	V/$\overline{S}$ Access Time	—	9	—	10	—	12	—	15	ns
t_{OH}	Output Hold Time From MUX Change	3	—	3	—	3	—	3	—	ns
t_{OHA}	Output Hold Time From Address Change	3	—	3	—	3	—	3	—	ns
t_{ACE} t_{ACE2}	$\overline{CE1}$ Access Time CE2 Access Time	—	9	—	10	—	12	—	15	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5	—	5	—	6	—	7	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	3	0	3	0	3	0	3	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t_{HZCE}[2] t_{HZCE2}[2]	$\overline{CE1}$ to High-Z Output CE2 to High-Z Output	0	5	0	5	0	6	0	7	ns
t_{LZCE}[2] t_{LZCE2}[2]	$\overline{CE}$ to Low-Z Output CE2 to Low-Z Output	3	—	3	—	3	—	3	—	ns

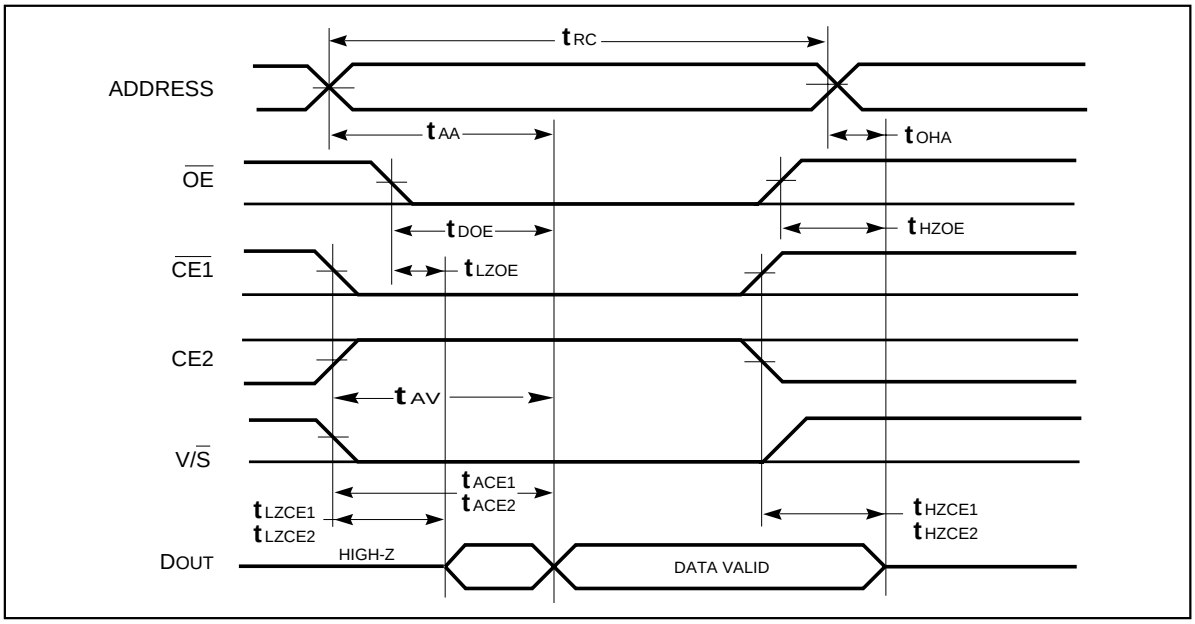
Notes:
1. Test conditions assume signal transition times of 2 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±200 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE1}$= $\overline{OE}$ = V_{IL}; CE2 = V_{IH})



READ CYCLE NO. 2[1,3]



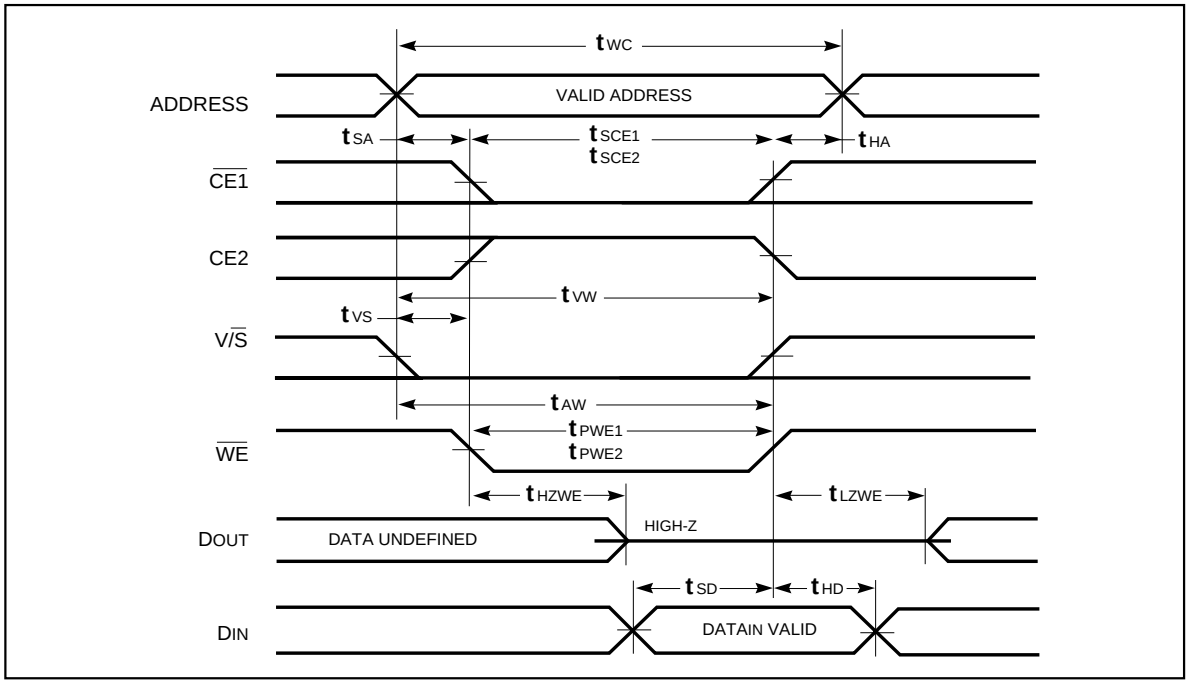
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$= V_{IL}. CE2 = V_{IH}.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and CE2 HIGH transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

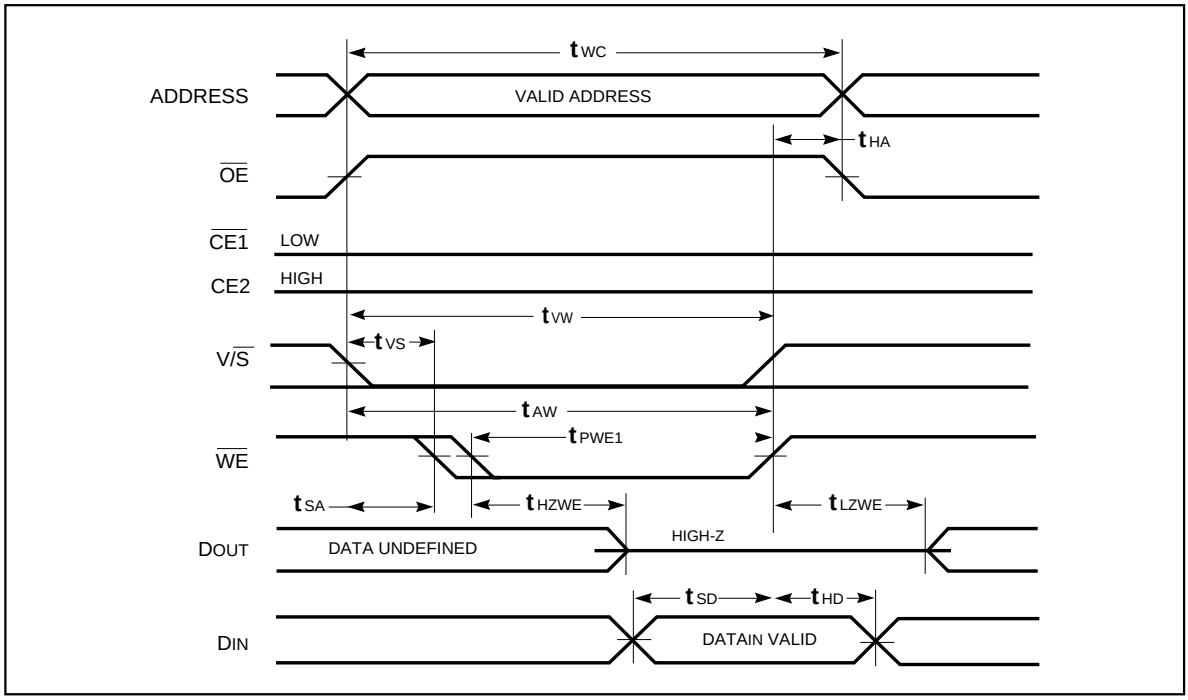
		-9		-10		-12		-15		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{WC}	Write Cycle Time	9	—	10	—	12	—	15	—	ns
t_{SCE}	$\overline{CE1}$ to Write End	7	—	7	—	8	—	10	—	ns
t_{SCE2}	CE2 to Write End	7	—	7	—	8	—	10	—	
t_{AW}	Address Setup Time to Write End	7	—	7	—	8	—	10	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{VS}	V/$\overline{S}$ Setup Time	0	—	0	—	0	—	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	7	—	7	—	8	—	10	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	9	—	10	—	12	—	15	—	ns
t_{SD}	Data Setup to Write End	5	—	5	—	6	—	7	—	ns
t_{VW}	V/$\overline{S}$ to Write End	7	—	7	—	8	—	10	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	4	—	5	—	6	—	7	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	3	—	3	—	ns

Notes:
1. Test conditions assume signal transition times of 2 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±200 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE1}$, LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

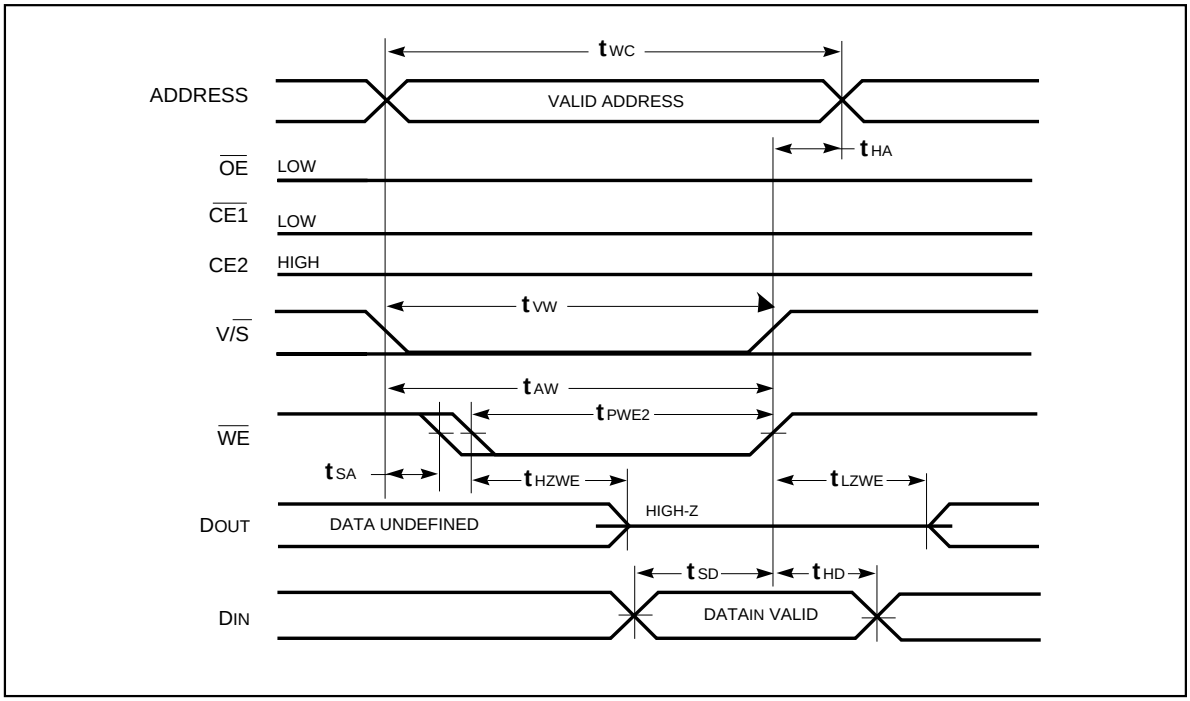
WRITE CYCLE NO. 1 ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)



WRITE CYCLE NO. 2[1] ($\overline{WE}$ Controlled: $\overline{OE}$ = HIGH during Write Cycle)



WRITE CYCLE NO. 3[1] ($\overline{WE}$ Controlled: $\overline{OE}$ IS LOW DURING WRITE CYLE)



Note:
1. The internal Write time is defined by the overlap of $\overline{CE1}$ = LOW, CE2 = HIGH and $\overline{WE}$ = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The Data Input Setup and Hold timing is referenced to the rising or falling edge of the signal that terminates the Write.

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
9	IS61LV6424-9TQ	14*20*1.4mm LQFP
10	IS61LV6424-10TQ	14*20*1.4mm LQFP
12	IS61LV6424-12TQ	14*20*1.4mm LQFP
15	IS61LV6424-15TQ	14*20*1.4mm LQFP

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