



Parameter	Rating	Units
Drain-to-Source Voltage - $V_{DS}$	350	V
Max On-Resistance - $R_{DS(on)}$	14	$\Omega$
Max Power	2.5	W

### Features

- 350V Drain-to-Source Voltage
- Depletion Mode Device Offers Low  $R_{DS(on)}$  at Cold Temperatures
- Low On-resistance:  $8\Omega$  (Typical) @  $25^{\circ}\text{C}$
- Low  $V_{GS(off)}$  Voltage: -2.0V to -3.6V
- High Input Impedance
- Low Input and Output Leakage
- Small Package Size SOT-223
- PC Card (PCMCIA) Compatible
- PCB Space and Cost Savings

### Applications

- Support Component for LITELINK™ Data Access Arrangement (DAA)
- Telecommunications
- Normally On Switches
- Ignition Modules
- Converters
- Security
- Power Supplies

### Description

The CPC5602 is an N-channel depletion mode Field Effect Transistor (FET) that utilizes Clare's proprietary third generation vertical DMOS process. The third generation process realizes world class, high voltage MOSFET performance in an economical silicon gate process. The vertical DMOS process yields a highly reliable device, particularly in difficult application environments such as telecommunications, security, and power supplies.

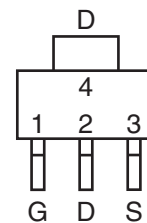
One of the primary applications for the CPC5602 is as a linear regulator/hook switch for the LITELINK family of Data Access Arrangements (DAA) Devices CPC5620A, CPC5621A, and CPC5622A.

The CPC5602 has a typical on-resistance of  $8\Omega$ , a drain-to-source voltage of 350V, and is available in an SOT-223 package. As with all MOS devices, the FET structure prevents thermal runaway and thermal-induced secondary breakdown.

### Ordering Information

Part Number	Description
CPC5602C	N-Channel Depletion Mode FET, SOT-223 Pkg. Cut-Tape, Available in Quantities of 200, 300, 400, 500, and 600
CPC5602CTR	N-Channel Depletion Mode FET, SOT-223 Pkg. Tape and Reel (1000/reel)

### Package Pinout



Pin Number	Name
1	GATE
2	DRAIN
3	SOURCE
4	DRAIN



### Absolute Maximum Ratings @ 25°C

Parameter	Ratings	Units
Drain-to-Source Voltage ( $V_{DS}$ )	350	V
Gate-to-Source Voltage ( $V_{GS}$ )	±20	V
Total Package Dissipation	2.5	W
Operational Temperature	-40 to +85	°C
Storage Temperature	-40 to +125	°C

*Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.*

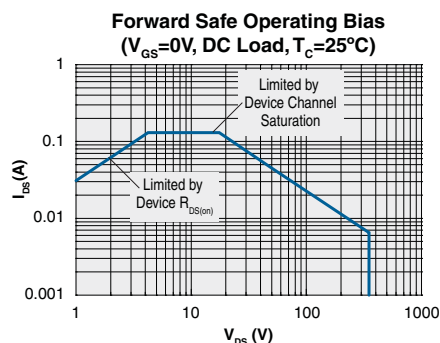
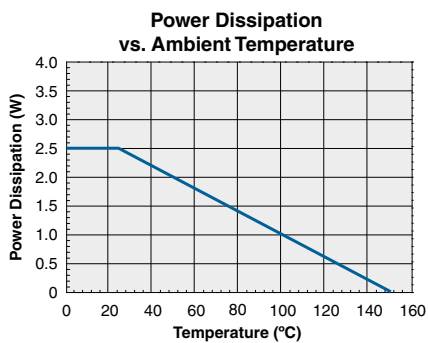
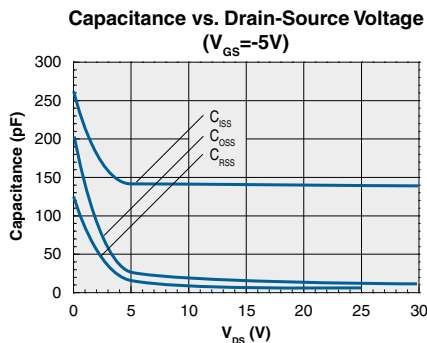
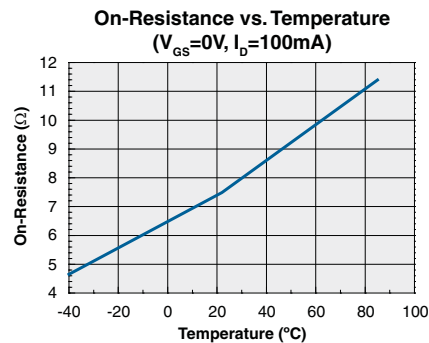
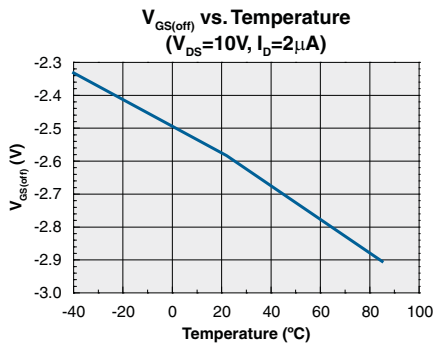
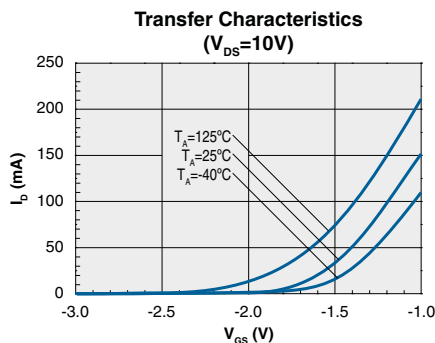
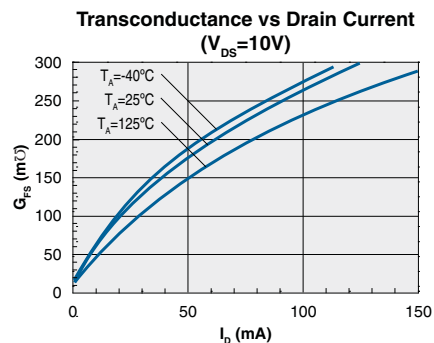
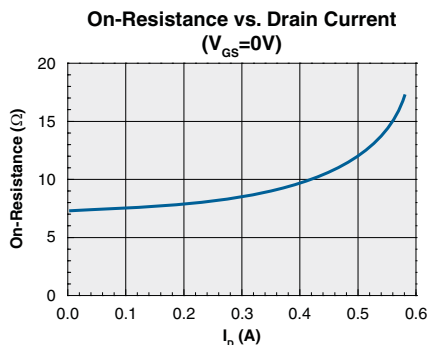
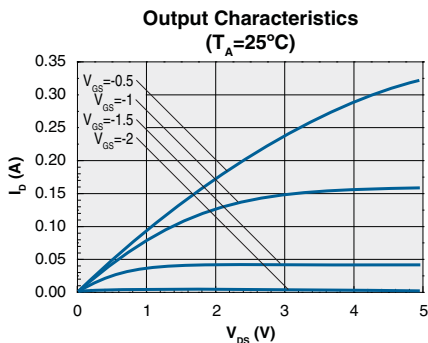
### Electrical Characteristics @25°C (Unless Otherwise Specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Gate-to-Source Off Voltage	$V_{GS(off)}$	$I_D = 2\mu A, V_{DS} = 10V, V_{DS} = 100V$	-3.6	-2.62	-2	V
Drain-to-Source Leakage Current	$I_{DS(off)}$	$V_{GS} = -5V, V_{DS} = 190V$	-	-	20	nA
		$V_{GS} = -5V, V_{DS} = 350V$	-	-	1	μA
Drain Current	$I_D$	$V_{GS} = -2.7V, V_{DS} = 5V, V_{DS} = 50V$	-	-	5	mA
		$V_{GS} = -0.57V, V_{DS} = 5V$	130	-	-	mA
On-Resistance	$R_{DS(on)}$	$V_{GS} = -0.35V, I_{DS} = 50mA$	-	8	14	Ω
Gate Leakage Current	$I_{GSS}$	$V_{GS} = 10V, V_{GS} = -10V$	-	-	0.1	μA
Gate Capacitance	$C_{ISS}$	$V_{DS} = V_{GS} = 0V$	-	-	300	pF

### Thermal Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Thermal Resistance	$R_{\theta JC}$	-	-	-	14	°C/W

**PERFORMANCE DATA\***



\*The Performance data shown in the graphs above is typical of device performance. For guaranteed parameters not indicated in the written specifications, please contact our application department.

## Manufacturing Information

### Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. Clare classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
CPC5602C	MSL 1

### ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

### Reflow Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

Device	Maximum Temperature x Time
CPC5602C	260°C for 30 seconds

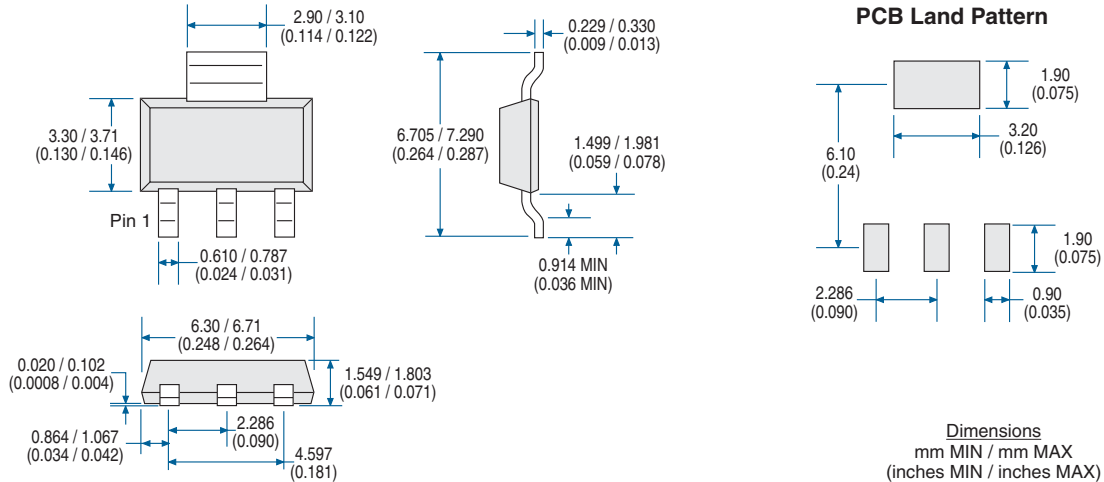
### Board Wash

Clare recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable. Since Clare employs the use of silicone coating as an optical waveguide in many of its optically isolated products, the use of a short drying bake could be necessary if a wash is used after solder reflow processes. Chlorine- or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

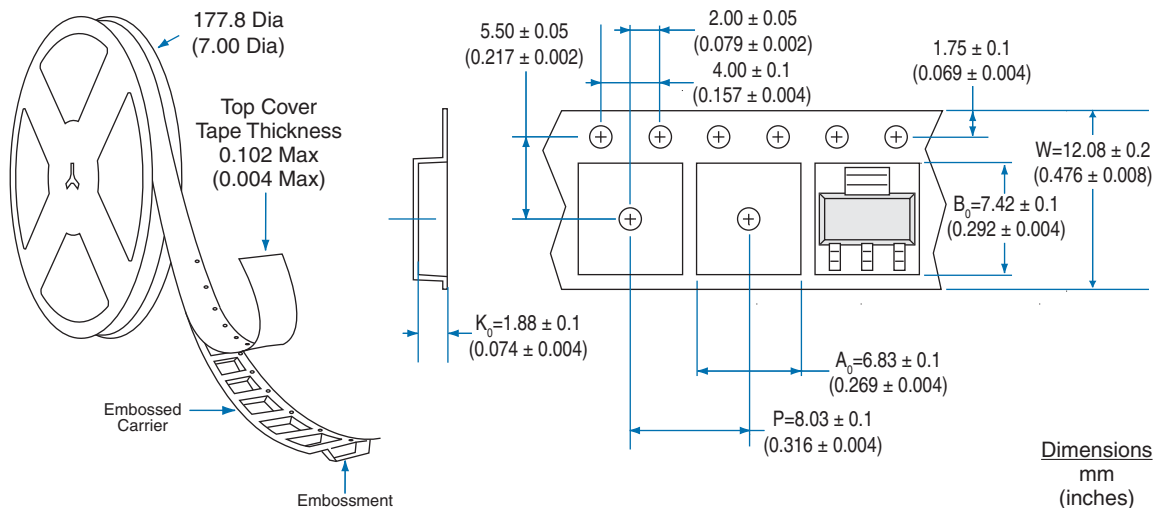


**MECHANICAL DIMENSIONS**

**CPC5602C**



**CPC5602C Tape & Reel**



**For additional information please visit our website at: [www.clare.com](http://www.clare.com)**

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