MP2303A

3A, 28V, 360kHz Synchronous Rectified Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2303A is a monolithic synchronous buck regulator. The device integrates a 150mΩ high-side MOSFET and a 80mΩ low-side MOSFET that provide 3A continuous load current over a wide operating input voltage of 4.7V to 28V. Current mode control provides fast transient response and cycle-by-cycle current limit.

An adjustable soft-start prevents inrush current at turn-on. In shutdown mode, the supply current drops to lower than 1μA.

This device, available in an 8-pin SOIC and PDIP-8 packages, provides a very compact system solution with minimal reliance on external components.

FEATURES

- 3A Output Current
- Wide 4.7V to 28V Operating Input Range
- Integrated MOSFET Switches
- Output Adjustable from 0.80V to 25V
- Up to 95% Efficiency
- Programmable Soft-Start
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 360kHz Frequency
- Cycle-by-Cycle Over Current Protection
- Input Under Voltage Lockout
- Available in thermally enhanced 8-Pin SOIC and PDIP-8 packages

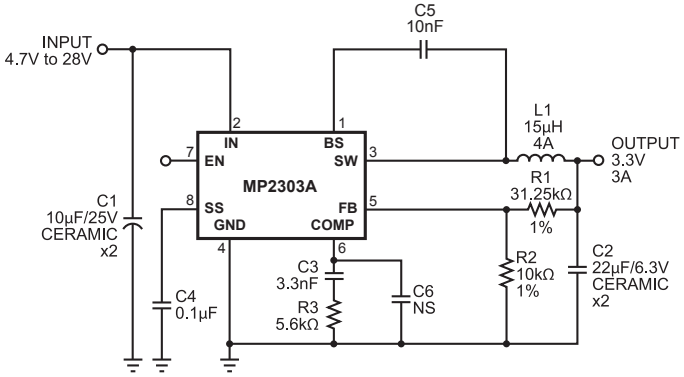
APPLICATIONS

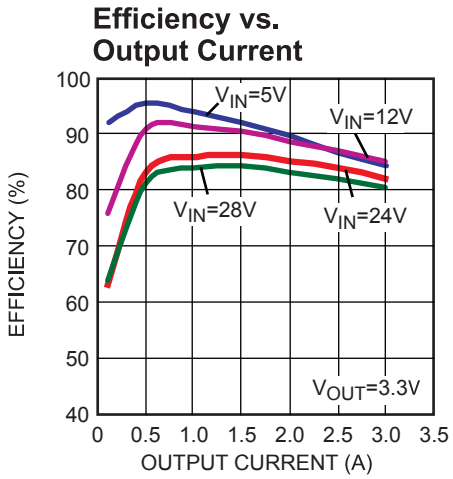
- Distributed Power Systems
- Pre-Regulator for Linear Regulators
- Notebook Computers

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TYPICAL APPLICATION





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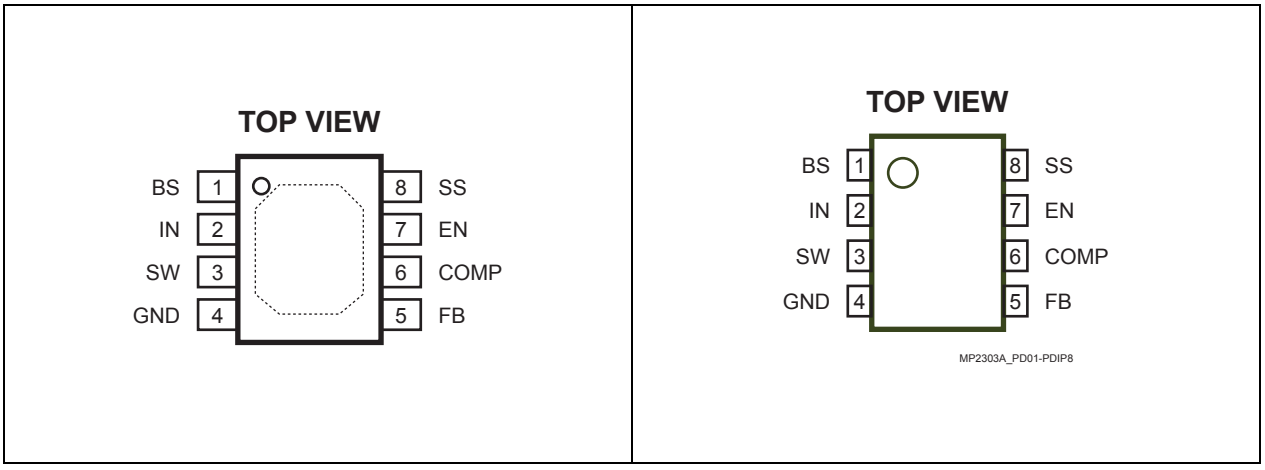
ORDERING INFORMATION

Part Number	Package	Top Marking	Free Air Temperature (T_A)
MP2303ADN*	SOIC8E	M2303ADN	-40°C to +85°C
MP2303ADP**	PDIP8	MP2303A	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP2303ADN–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP2303ADN–LF–Z)

** For Tape & Reel, add suffix –Z (e.g. MP2303ADP–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP2303ADP–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} ..... -0.3V to +30V
Switch Voltage V_{SW} ..... -1V to V_{IN} + 0.3V
Boost Voltage V_{BS} ..... V_{SW} - 0.3V to V_{SW} + 6V
All Other Pins ..... -0.3V to +6V
Junction Temperature ..... 150°C
Continuous Power Dissipation (T_A = +25°C)(2)
SOIC8E 2.5W
PDIP8 ..... 1.2W
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Input Voltage V_{IN} ..... 4.7V to 28V
Output Voltage V_{OUT} ..... 0.80V to 25V
Maximum Junction Temp. (T_J) ..... +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC8E	50	10	°C/W
PDIP8	105	45	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB..

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ELECTRICAL CHARACTERISTICS (5)

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ (5)	Max	Units
Shutdown Supply Current		V_{EN} = 0V		0.3	3.0	µA
Supply Current		V_{EN} = 2.7V, V_{FB} = 1.0V		1.45	1.6	mA
Feedback Voltage	V_{FB}	4.7V ≤ V_{IN} ≤ 28V, T_A = +25°C	0.780	0.800	0.820	V
		-40°C ≤ T_A ≤ +85°C	0.765		0.835	V
OVP Threshold Voltage			0.90	0.95	1.00	V
Error Amplifier Voltage Gain	A_{EA}			400		V/V
Error Amplifier Transconductance	G_{EA}	ΔI_C = ±10µA	550	820	1100	µA/V
High-Side Switch-On Resistance	$R_{DS(ON)1}$			150		mΩ
Low-Side Switch-On Resistance	$R_{DS(ON)2}$			80		mΩ
High-Side Switch Leakage Current		V_{EN} = 0V, V_{SW} = 0V		0	10	µA
Upper Switch Current Limit			4.3	6.0		A
Lower Switch Current Limit		From Drain to Source		1.25		A
COMP to Current Sense Transconductance	G_{CS}			7		A/V
Oscillation Frequency	F_{osc1}	T_A = +25°C	310	360	410	kHz
		-40°C ≤ T_A ≤ +85°C	290		430	kHz
Short Circuit Oscillation Frequency	F_{osc2}	V_{FB} = 0V		55		kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V	85	90		%
Minimum On Time				180		ns
EN Shutdown Threshold Voltage		V_{EN} Rising	1.0	1.3	1.6	V
EN Threshold Voltage Hysteresis				205		mV
EN Input Current		V_{EN} = 5V			2	µA
Input Under Voltage Lockout Threshold	UVLO	V_{IN} rising, T_A = +25°C	3.6	3.95	4.3	V
		0°C ≤ T_A ≤ +70°C	3.2		4.5	V
Input Under Voltage Lockout Threshold Hysterisis				125		mV
Soft-Start Current		V_{SS} = 0V		6		µA
Thermal Shutdown				160		°C

Notes:

5) 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

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PIN FUNCTIONS

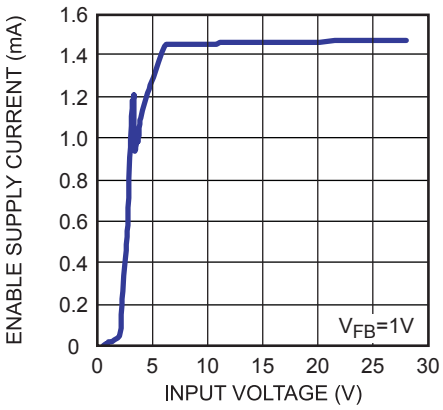
Pin #	Name	Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 0.01µF or greater capacitor from SW to BS to power the high side switch.
2	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.7V to 28V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See *Input Capacitor*.
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground (Connect Exposed Pad to Pin 4)
5	FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 0.80V. See *Setting the Output Voltage*.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required. See *Compensation Components.*
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. Connect EN with IN through a resistive voltage divider for automatic startup. Do not float this pin.
8	SS	Soft-start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1µF capacitor sets the soft-start period to 15ms. To disable the soft-start feature, leave SS unconnected.

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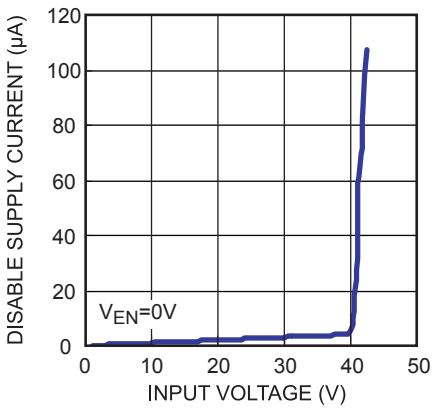
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = +27ºC, unless otherwise noted.

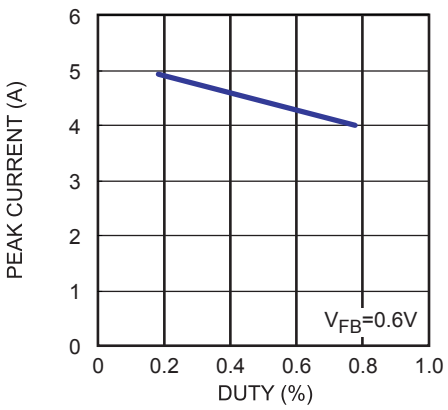
Enable Supply Current vs. Input Voltage



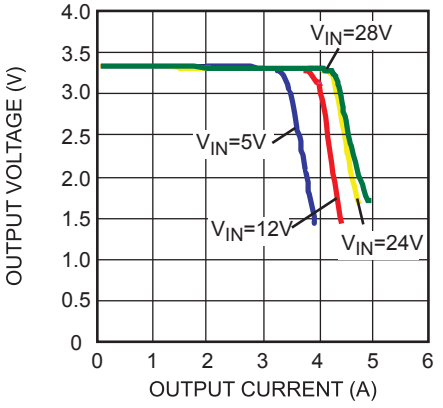
Disable Supply Current vs. Input Voltage



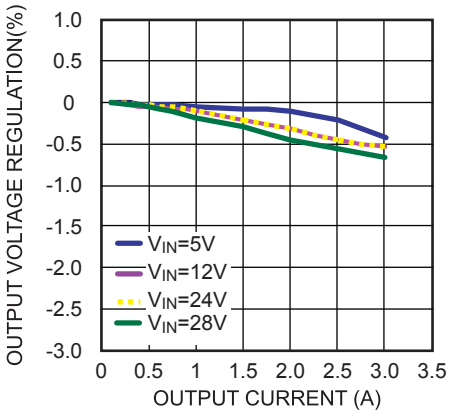
Current Limit vs. Duty Cycle



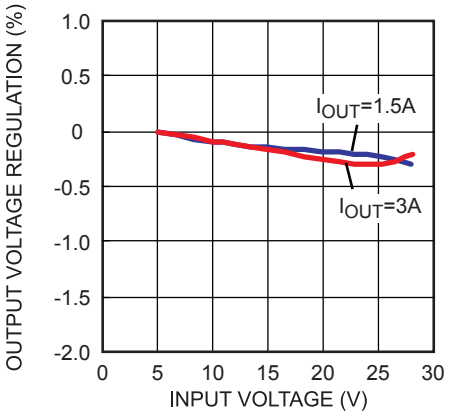
Output Current Capablity



Load Regulation



Line Regulation

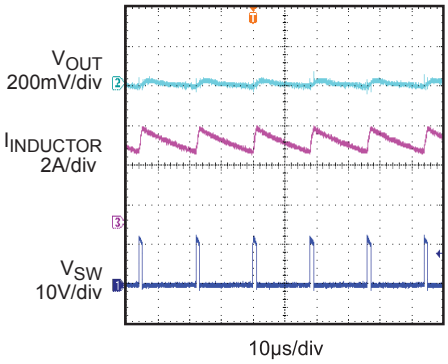


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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

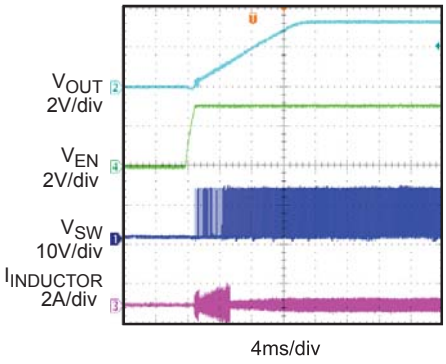
V_{IN} = 12V, V_{OUT} = 3.3V, T_A = +27ºC, unless otherwise noted.

Output Short State



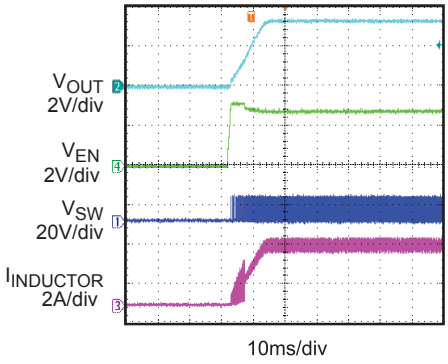
Enable Startup

I_{OUT}=0A



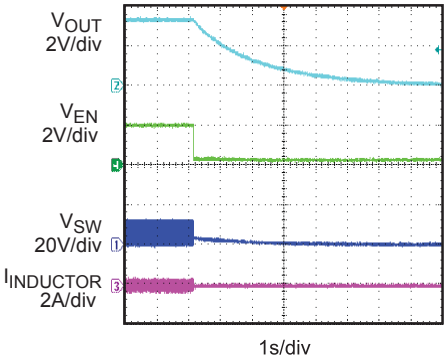
Enable Startup

I_{OUT}=3A



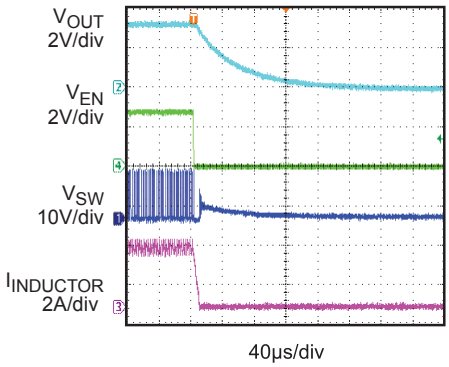
Enable Shutdown

I_{OUT}=0A



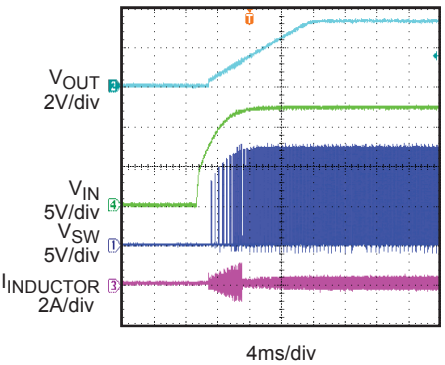
Enable Shutdown

I_{OUT}=3A



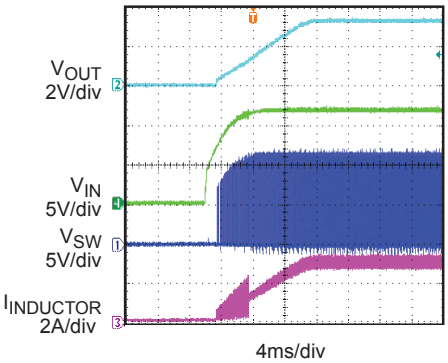
Power On

I_{OUT}=0A



Power On

I_{OUT}=3A



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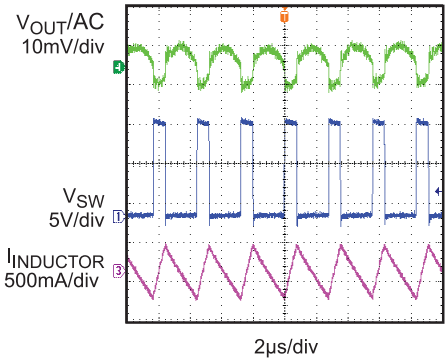
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = +27ºC, unless otherwise noted.

Output Ripple Voltage

Static V_{OUT_RIPPLE}=13.2mV

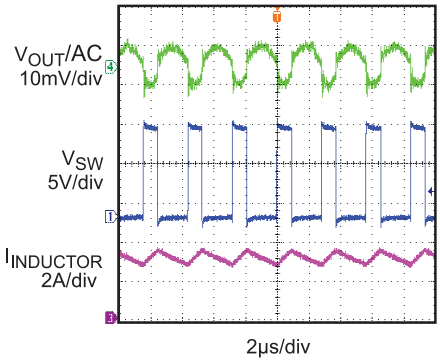
I_{OUT}=0A



Output Ripple Voltage

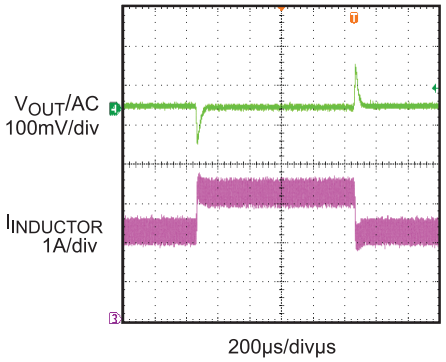
Static V_{OUT_RIPPLE}=15mV

I_{OUT}=3A



Load Transient Response

I_{OUT}=2-3A Step@1A/µs



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BLOCK DIAGRAM

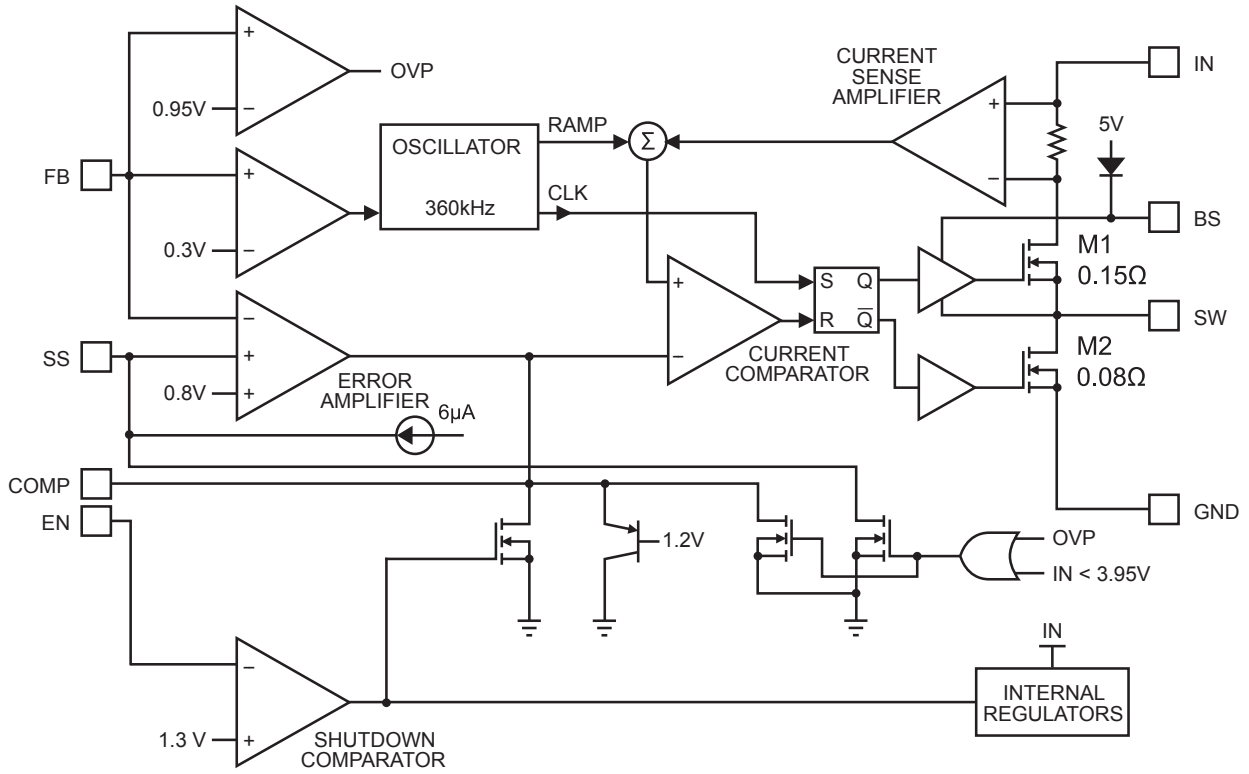


Figure 1—Functional Block Diagram

OPERATION

FUNCTIONAL DESCRIPTION

The MP2303A is a synchronous rectified, current-mode, step-down regulator. It regulates input voltages from 4.7V to 28V down to an output voltage as low as 0.80V, and supplies up to 3A of load current.

The MP2303A uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal transconductance error amplifier. The voltage at COMP pin is compared to the switch current measured internally to control the output voltage.

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS is needed to drive the high side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

When the MP2303A FB pin exceeds 20% of the nominal regulation voltage of 0.80V, the over voltage comparator is tripped and latched; the COMP pin and the SS pin are discharged to GND, forcing the high-side switch off.

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APPLICATIONS INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1+R2}$$

Thus the output voltage is:

$$V_{OUT} = 0.80 \times \frac{R1+R2}{R2}$$

Where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

A typical value for R2 can be as high as 100kΩ, but a typical value is 10kΩ. Using that value, R1 is determined by:

$$R1 = 12.5 \times (V_{OUT} - 0.80)(k\Omega)$$

For example, for a 3.3V output voltage, R2 is 10kΩ, and R1 is 31.25kΩ.

Configuring the EN control

EN high to turn on the regulator and EN low to turn it off. Do not float the pin.

For automatic start-up the EN pin can be pulled up to input voltage through a resistive voltage divider. Choose the values of the pull-up resistor (R_{UP} from V_{IN} to EN pin) and pull-down resistor (R_{DOWN} from EN pin to GND) to determine the automatic start-up voltage:

$$V_{IN-START} = 1.3 \times \frac{(R_{UP} + R_{DOWN})}{R_{DOWN}} (V)$$

For example, for R_{UP}=100kΩ and R_{DOWN}=20kΩ, the $V_{IN-START}$ is set at 7.8V.

Note the EN voltage should be no greater than 6V. If the resistive voltage divider will make it run over, please use a zener (below 6V) to clamp it.

To avoid noise, a 10nF ceramic capacitor from EN to GND is recommended.

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \times \Delta I} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current.

Optional Schottky Diode

During the transition between high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency. Table 2 lists example Schottky diodes and their Manufacturers.

Table 2—Diode Selection Guide

Part Number	Voltage/Current Rating	Vendor
B340	40V, 3A	Diodes, Inc.
SK34	40V, 3A	Diodes, Inc.
MBRS340	40V, 3A	International Rectifier

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Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where C2 is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2303A can be optimized for a wide range of capacitance and ESR values.

Compensation Components

MP2303A employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system.

The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{V_{OUT}}$$

Where A_{VEA} is the error amplifier voltage gain, G_{CS} is the current sense transconductance, R_{LOAD} is the load resistor value.The system has 2 poles of importance. One is due to the compensation capacitor (C3) and the output resistor of error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

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$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}}$$

Where G_{EA} is the error amplifier transconductance, and R_{LOAD} is the load resistor value.

The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

In this case, a third pole set by the compensation capacitor (C6) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C6 \times R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important.

Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system unstable. A good rule of thumb is to set the crossover frequency to approximately one-tenth of the switching frequency. Switching frequency for the MP2303A is 360kHz, so the desired crossover frequency is 36kHz.

Table 3 lists the typical values of compensation components for some standard output voltages with various output capacitors and inductors. The values of the compensation components have been optimized for fast transient responses and good stability at given conditions.

Table 3—Compensation Values for Typical Output Voltage/Capacitor Combinations

V_{OUT}	L1	C2	R3	C3	C6
1.8V	4.7µH	100µF Ceramic	8.2kΩ	3.3nF	None
2.5V	4.7-6.8µH	47µF Ceramic	5.6kΩ	4.7nF	None
3.3V	6.8-10µH	22µFx2 Ceramic	7.5kΩ	4.7nF	None
5V	10-15µH	22µFx2 Ceramic	10kΩ	3.3nF	None
12V	15-22µH	22µFx2 Ceramic	25kΩ	3.3nF	None
2.5V	4.7-6.8µH	560µF Al. 30mΩ ESR	70kΩ	3.3nF	150pF
3.3V	6.8-10µH	560µF Al 30mΩ ESR	90kΩ	3.3nF	100pF
5V	10-15µH	470µF Al. 30mΩ ESR	100kΩ	3.3nF	50pF
12V	15-22µH	220µF Al. 30mΩ ESR	120kΩ	3.3nF	50pF

To optimize the compensation components for conditions not listed in Table 3, the following procedure can be used.

1. Choose the compensation resistor (R3) to set the desired crossover frequency. Determine the R3 value by the following equation:

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where f_C is the desired crossover frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero, fZ1, below one forth of the crossover frequency provides sufficient phase margin. Determine the C3 value by the following equation:

$$C3 > \frac{4}{2\pi \times R3 \times f_C}$$

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3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_S}{2}$$

If this is the case, then add the second compensation capacitor (C6) to set the pole f_{P3} at the location of the ESR zero. Determine the C6 value by the equation:

$$C6 = \frac{C2 \times R_{ESR}}{R3}$$

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, and it will be a must if the applicable condition is:

- V_{OUT} is 5V or 3.3V, and duty cycle is high:

$$D = \frac{V_{OUT}}{V_{IN}} > 65\%$$

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST pin, as shown in Figure.2

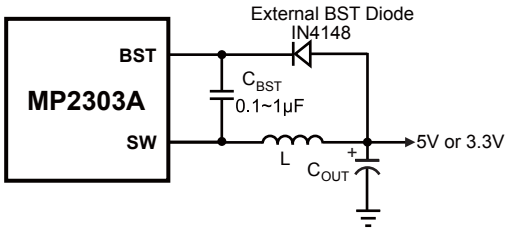


Figure 2—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1~1µF.

TYPICAL APPLICATION CIRCUITS

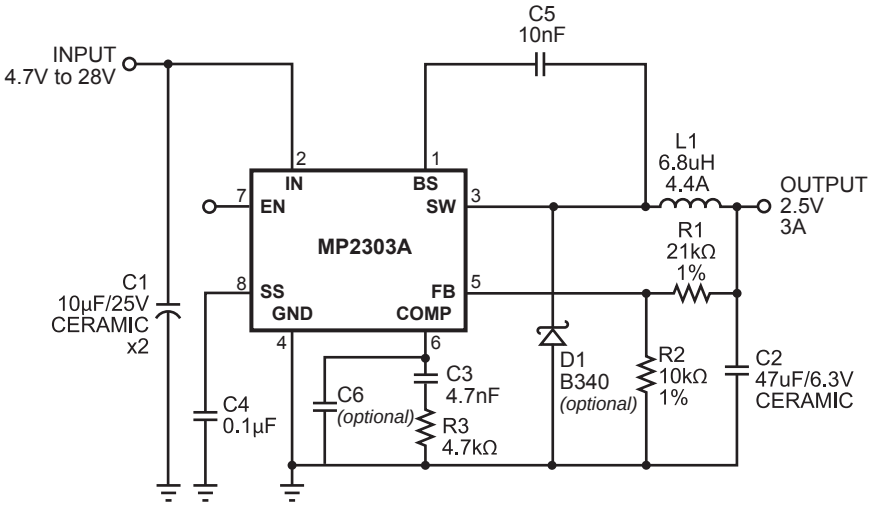


Figure 3—MP2303A with AVX 47µF, 6.3V Ceramic Output Capacitor

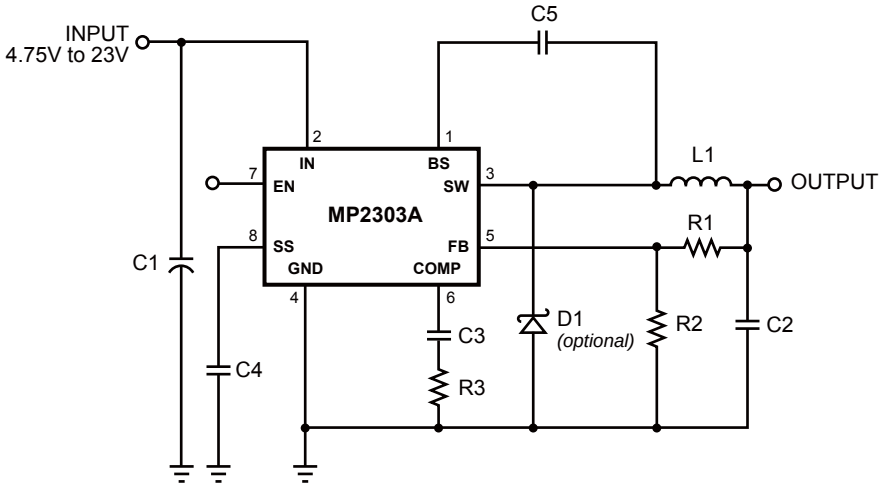
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PCB LAYOUT GUIDE

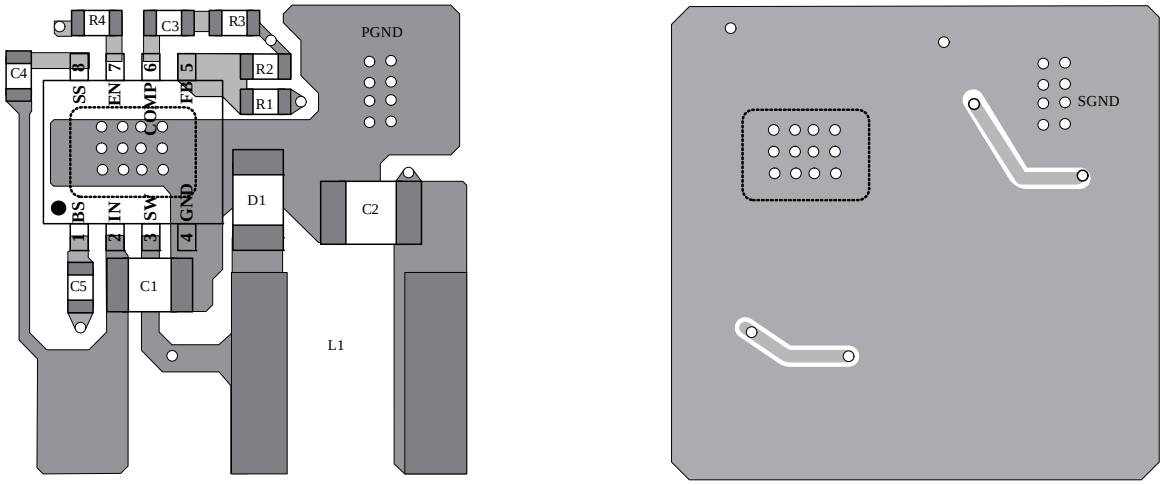
PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary, please follow these guidelines and take Figure 4 for reference.

1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side MOSFET and low-side MOSFET.
2) Bypass ceramic capacitors are suggested to be put close to the V_{IN} Pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Rout SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



MP2303A Typical Application Circuit



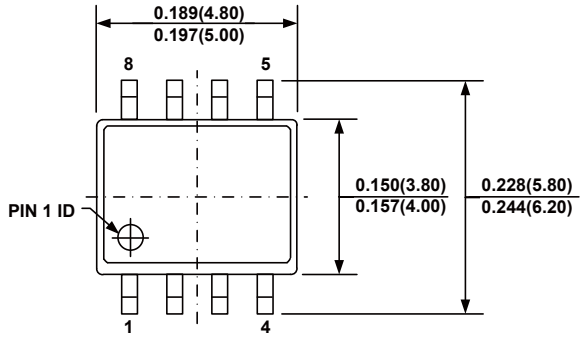
TOP Layer **Bottom Layer**

Figure 4—MP2303A Typical Application Circuit and PCB Layout Guide

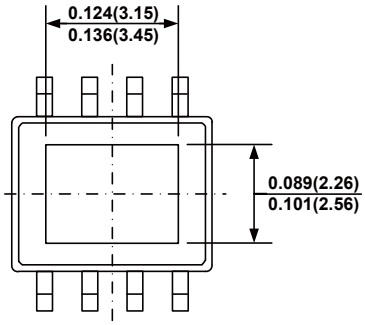
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PACKAGE INFORMATION

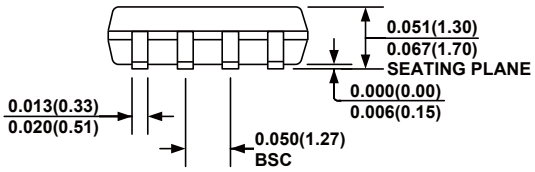
SOIC8E



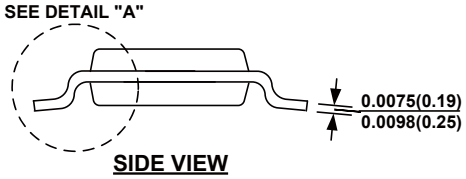
TOP VIEW



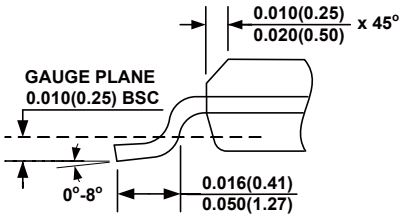
BOTTOM VIEW



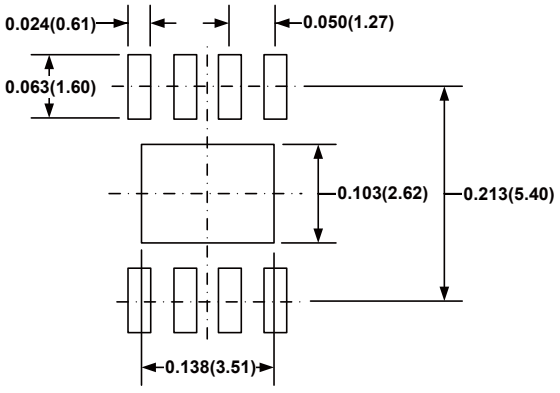
FRONT VIEW



SIDE VIEW



DETAIL "A"



RECOMMENDED LAND PATTERN

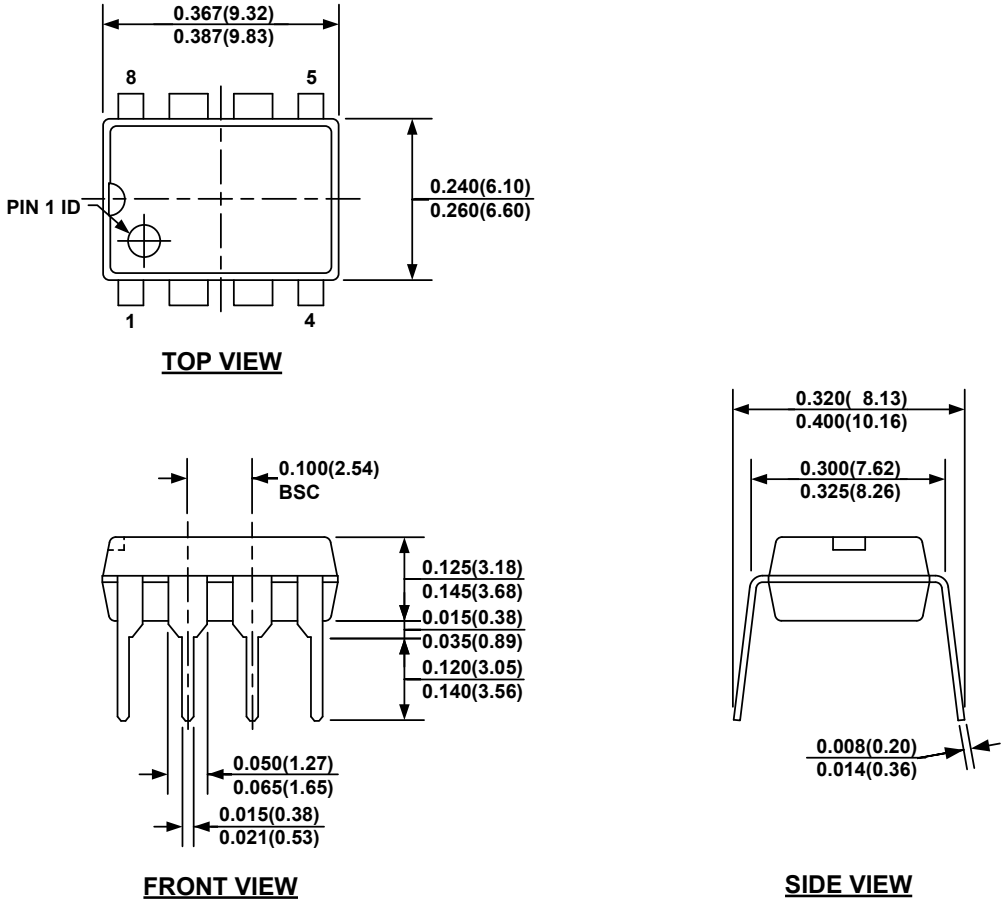
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3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
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