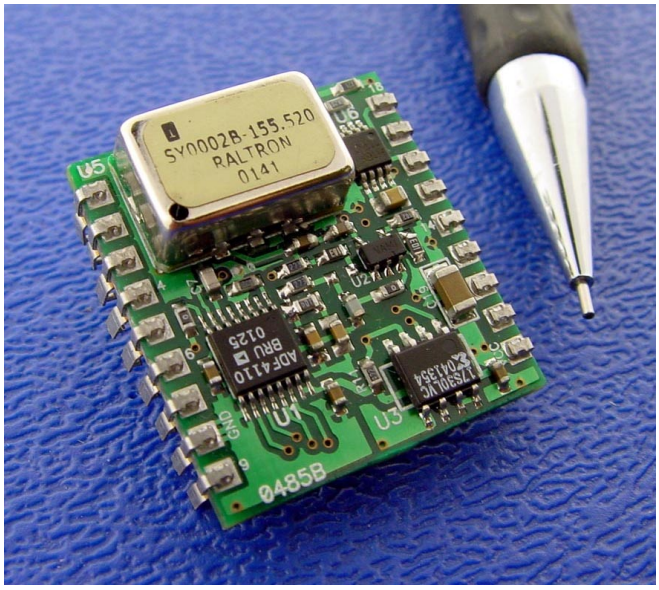
SY02-HPLL

Date: May 18, 2004



• INTRODUCTION

The SY02-HPLL is a high frequency crystal-based PLL synchronizer designed as a module level subsystem for easy incorporation into telecommunication equipment.

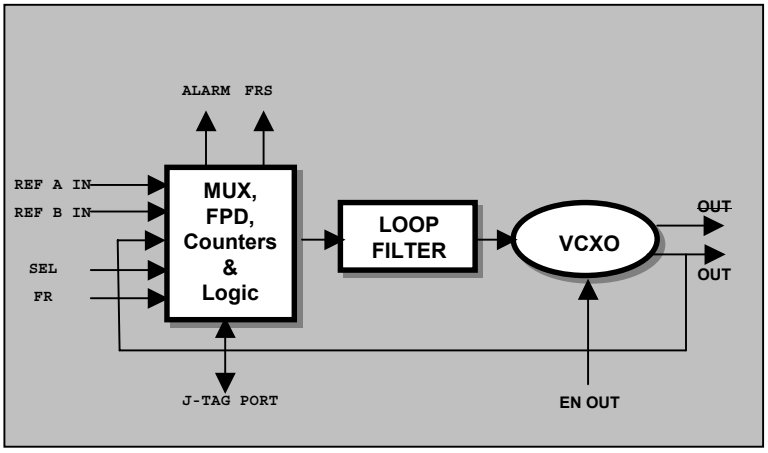
• FEATURES

- Low jitter output from intrinsically low jitter VCXO or VCSO;
- Two references inputs from 8kHz to 77.76MHz; (see table on pg. 3)
- One high frequency LVPECL output with enable/disable function from 51.84MHz to 800MHz (see table on pg. 3)
- Alarms and status;
- Provides free running clock output;
- The unit changes timing modes in response to external events;
- J-TAG service port for re-programming and servicing;
- 3.3V DC power supply
- Small dimensions: 0.96” x 1.050”

• APPLICATIONS

- ATM
- SDH
- PDH
- SONET
- Other telecommunication equipment.

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• DESCRIPTION

The SY02-HPLL is a High Frequency Phase Lock Loop has been designed as a module level subsystem for easy incorporation into telecommunication equipment. The module generates the high frequency (up to 622.08MHz) output from a low jitter VCXO or VCSO (SAW based oscillators). The output can be disabled externally by setting OUTEN pin high. The SY02-HPLL can be locked to one of two reference inputs frequencies of 8 kHz. The module has fast locking time and tolerates reference inputs with different duty cycles. The loop bandwidth is optimized according to used VCXO and wanted output performance. The ALARM output signals monitor the status of the phase loop LOL (Loss of Lock) and LOR (Loss of Reference). If the both references REFA and REFB are absent SY02-HPLL will automatically switch to free run mode and FRS output will indicate it. The SMD package dimensions are 0.96x1.050 inch and power supply is 3.3V.

- INPUT REFERENCE SELECTION

SEL	Reference
0	REF A
1	REF B

- OUTPUT PROGRAMMING

OUTEN	FR	OUTPUT
0	0	Locked to Reference
1	X	Output Disabled
0	1	Free-Run

- ALARM STATES

LOL	LOR	ALARM
0	0	No alarm
1	0	1
0	1	1

- **PIN DESCRIPTION**

Pin #	Name	Description
1	ENABLE	Output Enable - > the input pin to enable the output, active low
2	TCK	J-TAG port for factory usage – TCK
3	TDO	J-TAG port for factory usage – TDO
4	REFA IN	Reference A Input -> Reference A input signal
5	SEL	Select Input Reference -> input to select A (SEL=0) or B (SEL=1)
6	RESET	Reset input -> Reset active high
7	REFB IN	Reference B Input -> Reference B input signal
8	GND	Ground
9	FRS	Free-Run Status -> Output indicates that the module is in free run, active high
10	Vcc	Positive supply voltage
11	NC	Not Connected
12	ALARM	Alarm -> Alarm output indicates loss of reference or loss of lock
13	FR	Free-Run -> Control input to select free run of the module, active high
14	TDI	J-TAG port for factory usage – TDI
15	TMS	J-TAG port for factory usage – TMS
16	OUT	Oscillator Output -> Output of the module
17	GND	Ground
18	~~OUT~~	Oscillator Complementary Output -> Output of the module

- **ORDERING INFORMATION**

  - Output Frequencies available;

Frequency	Suffix	Frequency	Suffix
51.8400MHz	D2	167.3316MHz	C1
61.4400MHz	U1	168.0407MHz	C2
62.5000MHz	G5	175.0000MHz	C3
65.5360MHz	B2	178.9440MHz	C4
77.7600MHz	O3	184.3200MHz	C5
78.125MHz	B3	311.0400MHz	O6
78.6432MHz	B4	622.0800MHz	O7
82.9440MHz	B5	625.000MHz	C8
92.6000MHz	U3	644.5312MHz	C9
100.000MHz	B6	666.5143MHz	C10
112.000MHz	B7	669.1281MHz	F1
114.000MHz	B8	669.3266MHz	F2
125.000MHz	G2	690.5692MHz	F3
133.000MHz	G4	710.9486MHz	F4
139.264MHz	E6	719.7344MHz	F5
155.520MHz	O4	777.6000MHz	F6
156.250MHz	G6		
161.1328MHz	B9		
166.6286MHz	B10		

- Input Frequencies;

Frequency	Suffix	Frequency	Suffix
8KHz	F8	20.4800MHz	A4
1.024MHz	E0	22.2171MHz	A5
1.544MHz	T1	26.0000MHz	G2
2.048MHz	E1	27.0000MHz	A6
4.096MHz	E2	29.4912MHz	A7
6.1760MHz	T2	32.768MHz	E4
6.480MHz	D1	34.560MHz	A8
8.192MHz	E3	37.0560MHz	A9
10.000MHz	A1	38.880MHz	O2
12.800MHz	S1	44.4343MHz	B1
13.000MHz	G1	44.7360MHz	T3
15.000MHz	A2	51.8400MHz	D1
16.384MHz	E4	61.4400MHz	U1
19.440MHz	O1	62.5000MHz	G1
20.000MHz	M1	65.5360MHz	B2
20.1416MHz	A3	77.7600MHz	O3

- **P/N System**

SY02-HPLL– IP < Input Frequency> - OU<Output Frequency>-S-T<Temp. Range>-P <Package Option>

- See above Chart
If not listed Place **NL** and state the Freq.)

- See above Chart
(If Output Freq. Not applied place **NA** and state the Freq.)

- Supply Voltage;
  4 – 3.3V
- Operating Temperature Range;
  C - 0°C to 70°C
  I - 40°C to +85°C
- Package Option;
  J – J Lead
  S1 - SMT Option 1 **
  S2 – SMT Option 2

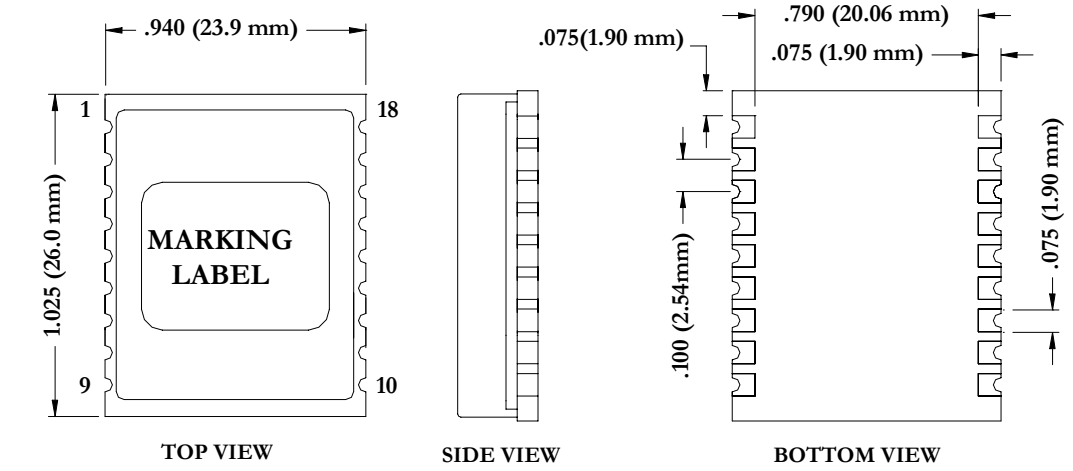
For other Options please contact the factory!
*** S1 May not be available at all frequency options, please consult factory*

- **SPECIFICATION**

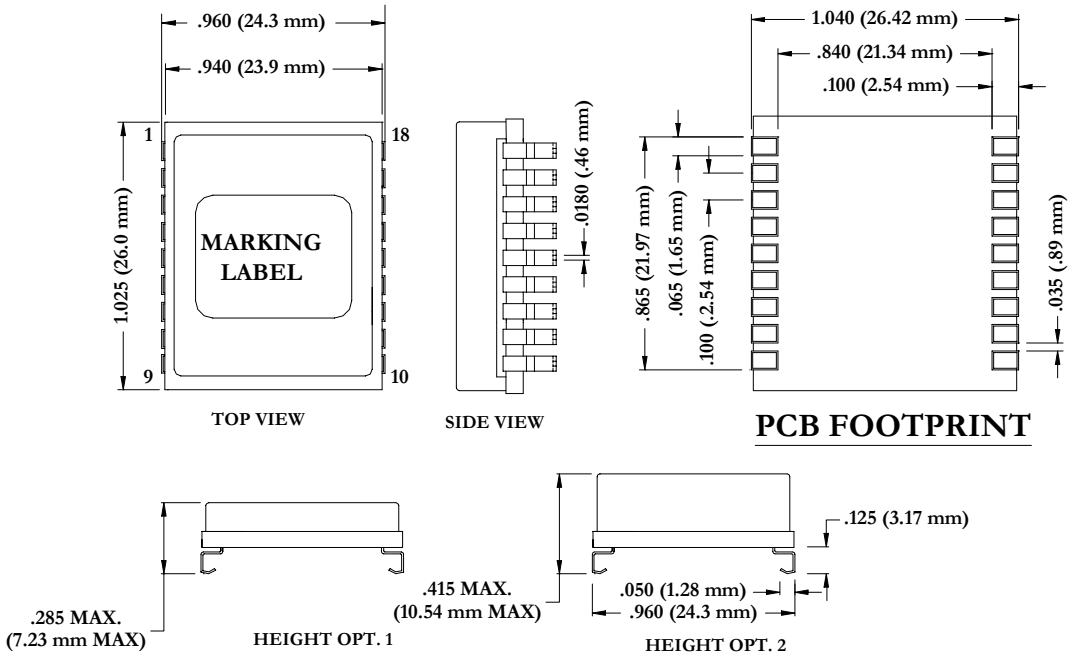
General Specifications	Mechanical	0.96" x 1.050"	SMT Module FR4 18 pins dual-in-line
	Power Environment Internal Oscillators	3.3VDC, <200mA Operating Temperature Humidity VCXO or VCSO	Regulated 0°C to 70°C 5% to 95% non-condensing Depend of the frequency
Input Signals	Number of Reference Inputs	2	
	Input reference frequency Signal Level	8kHz HCMOS/TTL Compatible	
Output Signals	Number of Outputs	1	
	Output 1	51.84MHz to 800MHz	other frequency contact Raltron
	Output 1 Signal Level	LVPECL	
	Tracking/Capture Range	±25ppm min	
Signal Quality Performance	Jitter generation	<0.03Uip-p	
	Jitter tolerance	2 μs, 10 Hz (0.05 UI @ 8KHz)	
Frequency Output Performance	Free run accuracy	±32ppm max. @ 25°C	No reference signal

- **OUTLINE DRAWING**

SMT Version



J-Lead Version



NOTES:
1. UNLESS OTHERWISE SPECIFIED,
DIMENSIONAL TOLERANCES ARE ±.010