FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27802-1E

ASSP For Power Management Applications (Mobile Phones)

Power Management IC for Mobile Phone

MB3892

■ DESCRIPTION

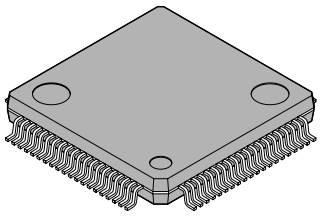
MB3892 is a low-saturation voltage type series regulator contains 3 channels for the baseband regulator, 1 channel for the backup regulator, 6 channels for the RF regulator, and 1 channel for the variable regulator. MB3892 is built in reset circuit, serial control circuit, operation Amp. for charge control of Lithium ion battery, LED drive circuit, receiver Amp., loudspeaker drive Amp., sounder circuit, vibrator drive circuit, and 4-ch D/A converter and the devices is miniaturized by systematization of built-in power supply for mobile phone.

■ FEATURES

- Power supply voltage range : VB = 2.85 V to 5.5 V
  : EXTVCC = 3.0 V to 6.5 V
- Low power consumption current during standby : 100 μA (Max.)
- Built-in low-saturation voltage type series regulator
- Built-in power-on reset function
- Built-in serial control function
- Built-in operation Amp. for charge control of Lithium ion battery
- Special power off function
  (To prevent battery discharge, this function controls the power consumption current of main IC under 11 μA (typ.) on the shipment.)

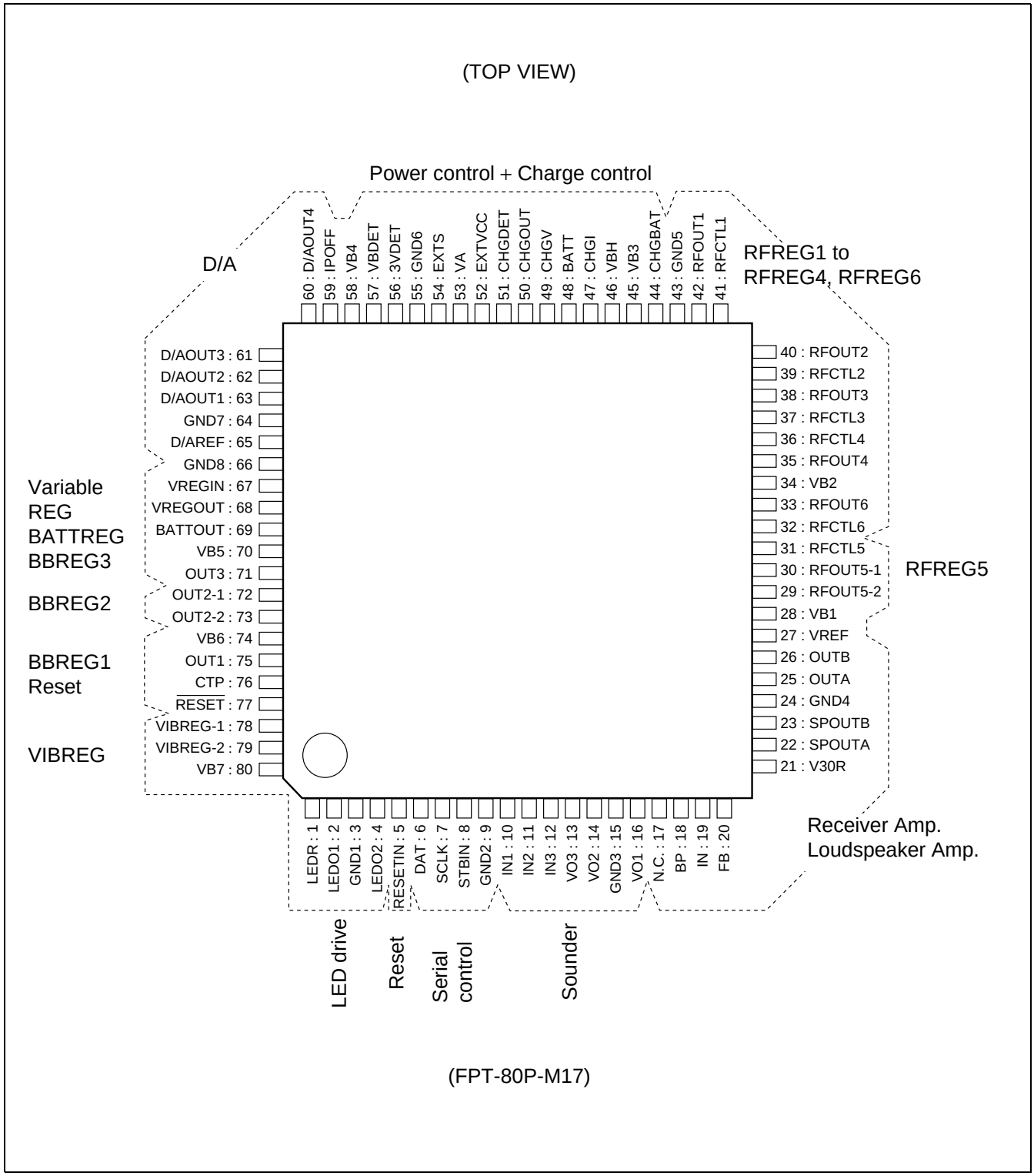
■ PACKAGE

80-pin plastic LQFP



(FPT-80P-M17)

■ PIN ASSIGNMENT



(FPT-80P-M17)

■ PIN DESCRIPTION

Pin No.	Symbol	I/O	Descriptions
1	LEDR	O	LEDR output pin. (an open collector output)
2	LEDO1	O	LED1 output pin. (an open drain output)
3	GND1	—	Ground pin.
4	LEDO2	O	LED2 output pin. (an open drain output)
5	RESETIN	I	Reset detect comparator input pin.
6	DAT	I	Serial data input pin.
7	SCLK	I	Serial clock input pin.
8	STBIN	I	Strobe input pin.
9	GND2	—	Ground pin.
10	IN1	I	Sounder1 control input pin.
11	IN2	I	Sounder2 control input pin.
12	IN3	I	Sounder3 control input pin.
13	VO3	O	Sounder3 control output pin. (an open drain output)
14	VO2	O	Sounder2 control output pin. (an open drain output)
15	GND3	—	Ground pin.
16	VO1	O	Sounder1 control output pin. (an open drain output)
17	N.C.	—	No connection pin.
18	BP	—	Bypass pin.
19	IN	I	Non-inverted input pin.
20	FB	I	Inverted input pin.
21	V30R	—	Power supply pin for speaker Amp.
22	SPOUTA	O	Output A pin for loudspeaker Amp.
23	SPOUTB	O	Output B pin for loudspeaker Amp.
24	GND4	—	Ground pin.
25	OUTA	O	Output A pin for receiver Amp.
26	OUTB	O	Output B pin for receiver Amp.
27	VREF	O	Reference output voltage pin.
28	VB1	—	Power supply pin.
29	RFOUT5-2	O	RF REG5 output pin2. (Short circuiting to pin 30)
30	RFOUT5-1	O	RF REG5 output pin1. (Short circuiting to pin 29)
31	RFCTL5	I	RF REG5 control pin.
32	RFCTL6	I	RF REG6 control pin.
33	RFOUT6	O	RF REG6 output pin.
34	VB2	—	Power supply pin.

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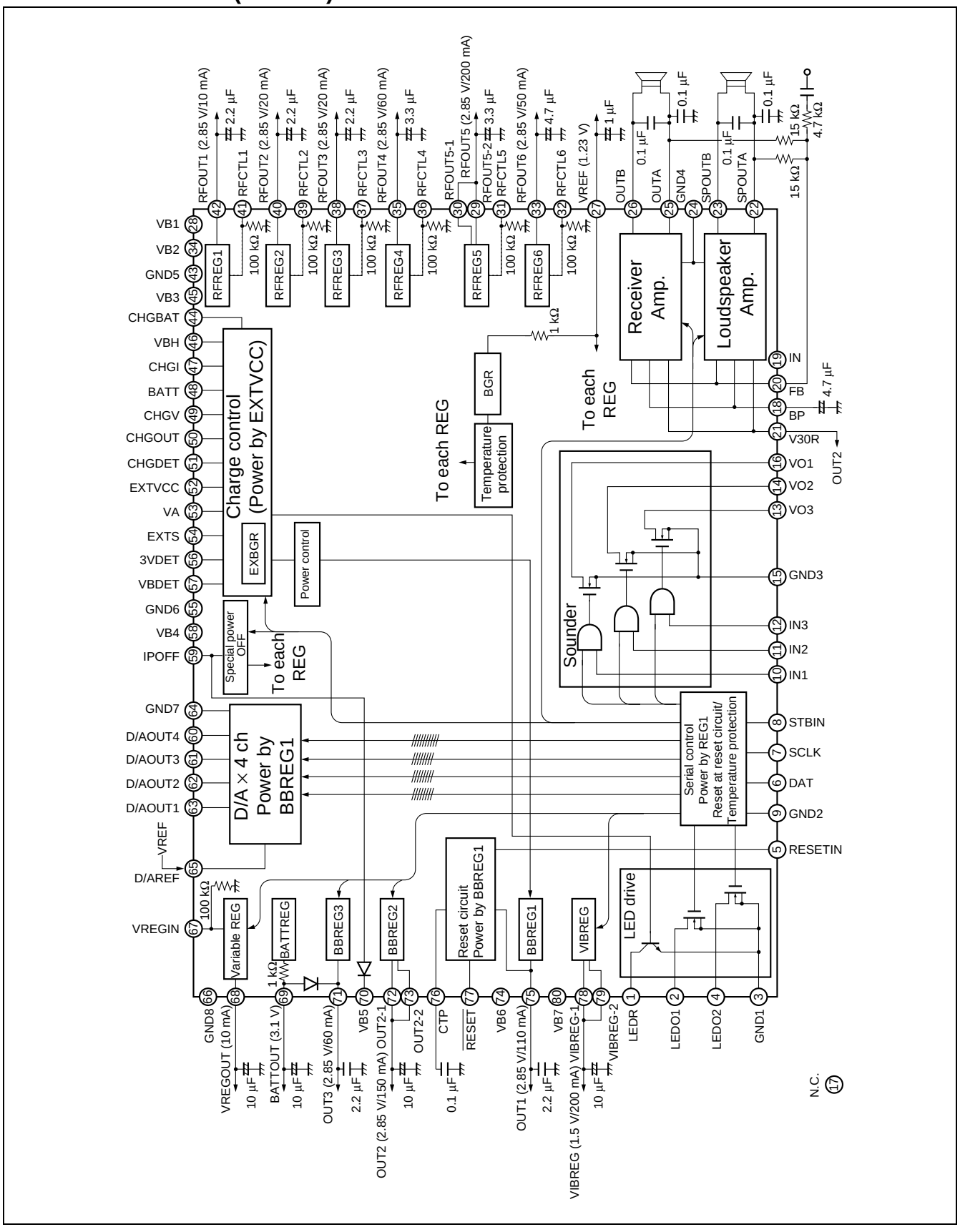
Pin No.	Symbol	I/O	Descriptions
35	RFOUT4	O	RF REG4 output pin.
36	RFCTL4	I	RF REG4 output pin.
37	RFCTL3	I	RF REG3 control pin.
38	RFOUT3	O	RF REG3 output pin.
39	RFCTL2	I	RF REG2 control pin.
40	RFOUT2	O	RF REG2 output pin.
41	RFCTL1	I	RF REG1 control pin.
42	RFOUT1	O	RF REG1 output pin.
43	GND5	—	Ground pin.
44	CHGBAT	—	Main charge pin.
45	VB3	—	Power supply pin.
46	VBH	I	Main charge pin.
47	CHGI	O	Main charge pin.
48	BATT	O	A/D input pin.
49	CHGV	I	Main charge pin.
50	CHGOUT	O	Main charge pin.
51	CHGDET	O	Main charge pin.
52	EXTVCC	—	Power supply pin for charge control.
53	VA	I	Preliminary charge pin.
54	EXTS	O	Preliminary charge pin.
55	GND6	—	Ground pin.
56	3VDET	O	Power supply detector pin.
57	VBDET	I	Power supply detector pin.
58	VB4	—	Power supply pin.
59	IPOFF	I	Special power off input pin.
60	D/AOUT4	O	10 bit D/A output pin.
61	D/AOUT3	O	8 bit D/A3 output pin.
62	D/AOUT2	O	8 bit D/A2 output pin.
63	D/AOUT1	O	8 bit D/A1 output pin.
64	GND7	—	Ground pin.
65	D/AREF	I	D/A reference voltage input pin.
66	GND8	—	Ground pin.
67	VREGIN	I	Variable REG reference voltage input pin.
68	VREGOUT	O	Variable REG output pin.

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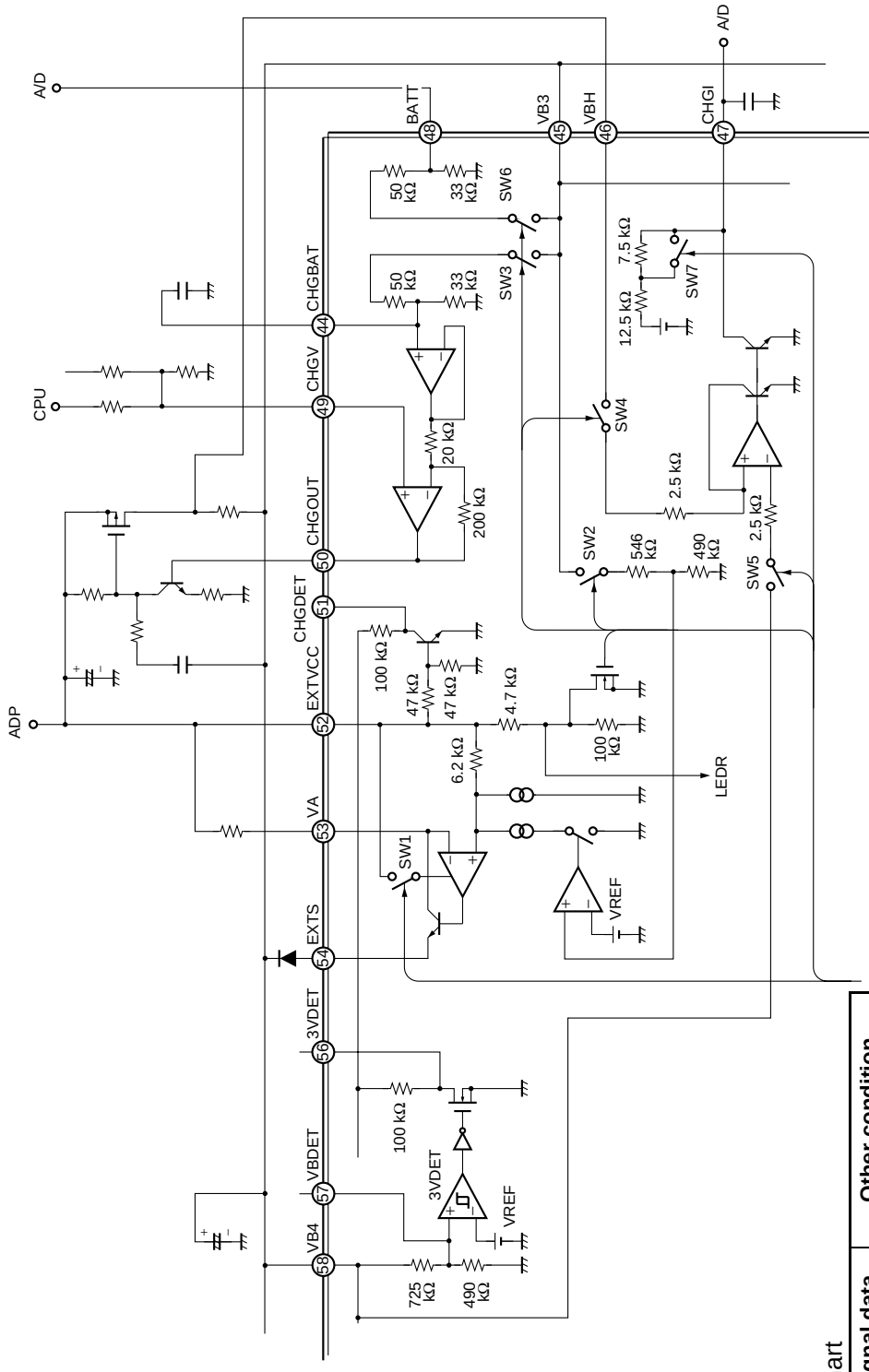
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Pin No.	Symbol	I/O	Descriptions
69	BATTOUT	O	Backup REG output pin.
70	VB5	—	Power supply pin.
71	OUT3	O	Baseband REG3 output pin.
72	OUT2-1	O	Baseband REG2 output pin. (Short circuiting to pin 73)
73	OUT2-2	O	Baseband REG2 output pin. (Short circuiting to pin 72)
74	VB6	—	Power supply pin.
75	OUT1	O	Baseband REG1output pin.
76	CTP	I	Setting pin for power-on reset hold time.
77	$\overline{\text{RESET}}$	O	Reset output pin.
78	VIBREG-1	O	Vibrator REG output pin. (Short circuiting to pin 79)
79	VIBREG-2	O	Vibrator REG output pin. (Short circuiting to pin 78)
80	VB7	—	Power supply pin.

■ BLOCK DIAGRAM (General)



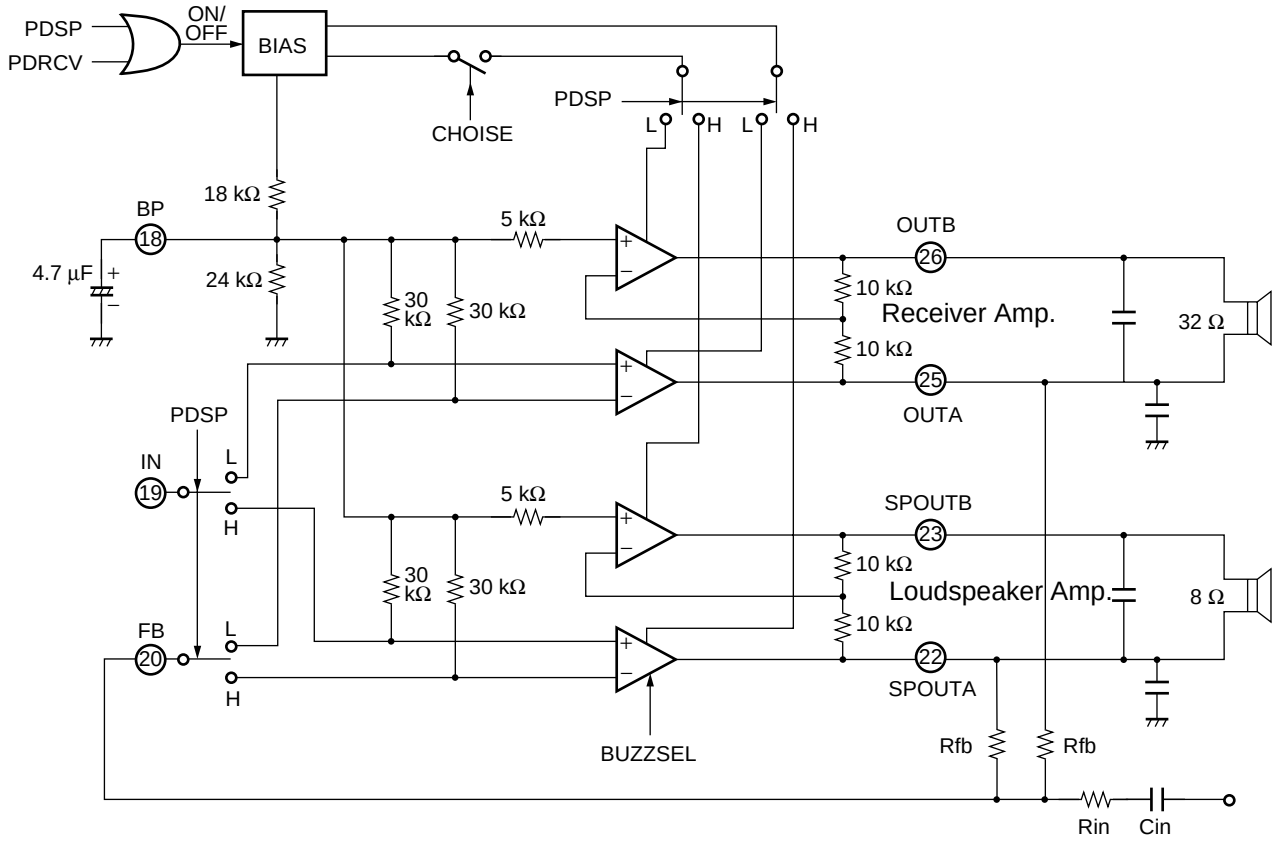
• Charge control



SW Condition chart

SW	Serial signal data		Other condition
SW1 SW2	PRCHGOFF	H : OFF L : ON	Special power off : OFF VB 4 V detector : OFF
SW3 SW4 SW5	BIASSW	H : OFF L : ON	Special power off : OFF No EXTVCC : OFF
SW6	BIASSW	H : OFF L : ON	Special power off : OFF
SW7	CHGISEL	H : ON L : OFF	

• Speaker Amp.



PDRCV	PDSP	CHOISE	BUZZSEL	Operating Amp.	Operation mode
L	L	×	×	—	Standby
H	L	H	L	Receiver Amp.	Receiver (BTL drive)
H	L	L	L	Receiver Amp.	Earphone mode (single drive)
L	H	H	L	Loudspeaker Amp.	Loudspeaker Amp. (BTL drive)
L	H	L	H	Loudspeaker Amp.	Short wave form output (open collector)
H	H	×	L	Loudspeaker Amp.	When both of PDRCV/PDSP is “H” level, the operation of loudspeaker Amp. has priority.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Power supply voltage	VB	—	—	7	V
	EXTVCC	—	—	7	V
Baseband regulator output current	I_O	BBREG1	—	−110	mA
	I_O	BBREG2	—	−150	mA
	I_O	BBREG3	—	−60	mA
Receiver Amp. output current	I_O	—	—	150	mA
Loudspeaker Amp. output current	I_O	—	—	400	mA
Vibrator regulator output current	I_O	—	—	−200	mA
RF regulator output current	I_O	RFREG1	—	−10	mA
	I_O	RFREG2	—	−20	mA
	I_O	RFREG3	—	−20	mA
	I_O	RFREG4	—	−60	mA
	I_O	RFREG5	—	−200	mA
	I_O	RFREG6	—	−50	mA
Variable regulator output current	I_O	—	—	−15	mA
Power dissipation	P_D	Ta ≤ +25 °C	—	1420 *	mW
Storage temperature	Tstg	—	−55	+125	°C

*: The packages are mounted on the dual-sided epoxy board(10 cm × 10 cm)

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage	VB	—	2.85	—	5.5	V
	EXTVCC	Under 4.5 V preliminary charge circuit is not operated normally	3.0	—	6.5	V
REG capacitor ESR guarantee value	R_{ESR}	—	0.4	—	7	Ω
Operating ambient temperature	Ta	—	–30	+25	+80	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

• Power control

(Ta = +25 °C, VB = 3.6 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Reference voltage	Reference voltage	V_{REF}	27	VREF = 0 mA	1.19	1.23	1.27	V
Baseband regulator [BBREG1]	Output voltage	V_{O1}	75	OUT1 = 0 mA	2.79	2.85	2.91	V
		V_{OLD1}	75	OUT1 = –110 mA	2.79	2.85	2.91	V
	Line regulation	Line	75	VB = 3.1 to 4.8 V, OUT1 = –10 mA	—	—	20	mV
	Load regulation	Load	75	OUT1 = 0 to –110 mA	–30	—	0	mV
	Ripple rejection	R.R	75	Vin = 0.2 Vrms, f = 1 kHz, OUT1 = –10 mA	—	–50*	—	dB
	Reverse current	I_{REV}	75	VB = 0 to 5 V or VB = Open	—	30	43	µA
	Rise time	T_R	75	OUT1 = 2.2 µF, OUT1 = 27 Ω	—	—	60	µs
Baseband regulator [BBREG2]	Output voltage	V_{O2}	72, 73	OUT2 = 0 mA	2.79	2.85	2.91	V
		V_{OLD2}	72, 73	OUT2 = –150 mA	2.79	2.85	2.91	V
	Line regulation	Line	72, 73	VB = 3.1 to 4.8 V, OUT2 = –10 mA	—	—	20	mV
	Load regulation	Load	72, 73	OUT2 = 0 to –150 mA	–30	—	0	mV
	Ripple rejection	R.R	72, 73	Vin = 0.2 Vrms, f = 1 kHz, OUT2 = –10 mA	—	–50*	—	dB
	Rise time	T_R	72, 73	OUT2 = 10 µF, OUT2 = 20 Ω	—	—	190	µs
Baseband regulator [BBREG3]	Output voltage	V_{O3}	71	OUT3 = 0 mA	2.79	2.85	2.91	V
		V_{OLD3}	71	OUT3 = –60 mA	2.79	2.85	2.91	V
	Line regulation	Line	71	VB = 3.1 to 4.8 V, OUT3 = –10 mA	—	—	20	mV
	Load regulation	Load	71	OUT3 = 0 to –60 mA	–30	—	0	mV
	Ripple rejection	R.R	71	Vin = 0.2 Vrms, f = 1 kHz, OUT3 = –10 mA	—	–50*	—	dB
	Reverse current	I_{REV}	71	VB = 0 to 5 V or VB = Open	—	0	1	µA
	Rise time	T_R	71	OUT3 = 2.2 µF, OUT3 = 47 Ω	—	—	105	µs

* : Standard design value

(Continued)

(Ta = +25 °C, VB = 3.6 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Backup regulator [BATTREG]	Output voltage	V_{BATT}	69	BATTOUT = 0 mA	3.00	3.10	3.20	V
	Output current	I_{BATT}	69	BATTOUT = 0 V	—	–3.1	—	mA
	Reverse current	I_{REV}	69	VB = 0 to 5 V or VB = Open	—	0	1	µA
Vibrator drive circuit [VIBREG]	Output voltage	V_O	78, 79	VIBREG = 0 mA	1.44	1.50	1.56	V
		V_{OLD}	78, 79	VIBREG = –200 mA	1.38	1.50	1.56	V
RF regulator [RFREG1]	Output voltage	V_{O1}	42	RFOUT1 = 0 mA	2.79	2.85	2.91	V
		V_{OLD1}	42	RFOUT1 = –10 mA	2.79	2.85	2.91	V
	Line regulation	Line	42	VB = 3.1 to 4.8 V, RFOUT1 = –10 mA	—	—	20	mV
	Load regulation	Load	42	RFOUT1 = 0 to –10 mA	–30	—	0	mV
	Ripple rejection	R.R	42	Vin = 0.2 Vrms, f = 1 kHz, RFOUT1 = –10 mA	—	–55*	—	dB
	Rise time	T_R	42	RFOUT1 = 2.2 µF, RFOUT1 = 300 Ω	—	—	630	µs
RF regulator [RFREG2]	Output voltage	V_{O2}	40	RFOUT2 = 0 mA	2.79	2.85	2.91	V
		V_{OLD2}	40	RFOUT2 = –20 mA	2.79	2.85	2.91	V
	Line regulation	Line	40	VB = 3.1 to 4.8 V, RFOUT2 = –10 mA	—	—	20	mV
	Load regulation	Load	40	RFOUT2 = 0 to –20 mA	–30	—	0	mV
	Ripple rejection	R.R	40	Vin = 0.2 Vrms, f = 1 kHz, RFOUT2 = –10 mA	—	–55*	—	dB
	Rise time	T_R	40	RFOUT2 = 2.2 µF, RFOUT2 = 150 Ω	—	—	315	µs
RF regulator [RFREG3]	Output voltage	V_{O3}	38	RFOUT3 = 0 mA	2.79	2.85	2.91	V
		V_{OLD3}	38	RFOUT3 = –20 mA	2.79	2.85	2.91	V
	Line regulation	Line	38	VB = 3.1 to 4.8 V, RFOUT3 = –10 mA	—	—	20	mV
	Load regulation	Load	38	RFOUT3 = 0 to –20 mA	–30	—	0	mV
	Ripple rejection	R.R	38	Vin = 0.2 Vrms, f = 1 kHz, RFOUT3 = –10 mA	—	–55*	—	dB
	Rise time	T_R	38	RFOUT3 = 2.2 µF, RFOUT3 = 150 Ω	—	—	315	µs

* : Standard design value

(Continued)

(Ta = +25 °C, VB = 3.6 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
RF regulator [RFREG4]	Output voltage	V_{O4}	35	RFOUT4 = 0 mA	2.79	2.85	2.91	V
		V_{OLD4}	35	RFOUT4 = –60 mA	2.79	2.85	2.91	V
	Line regulation	Line	35	VB = 3.1 to 4.8 V, RFOUT4 = –10 mA	—	—	20	mV
	Load regulation	Load	35	RFOUT4 = 0 to –60 mA	–30	—	0	mV
	Ripple rejection	R.R	35	Vin = 0.2 Vrms, f = 1 kHz, RFOUT4 = –10 mA	—	–55*	—	dB
	Rise time	T_R	35	RFOUT4 = 3.1 µF, RFOUT4 = 51 Ω	—	—	160	µs
RF regulator [RFREG5]	Output voltage	V_{O5}	29, 30	RFOUT5 = 0 mA	2.79	2.85	2.91	V
		V_{OLD5}	29, 30	RFOUT5 = –200 mA	2.79	2.85	2.91	V
	Line regulation	Line	29, 30	VB = 3.1 to 4.8 V, RFOUT5 = –10 mA	—	—	20	mV
	Load regulation	Load	29, 30	RFOUT5 = 0 to –200 mA	–30	—	0	mV
	Ripple rejection	R.R	29, 30	Vin = 0.2 Vrms, f = 1 kHz, RFOUT5 = –10 mA	—	–55*	—	dB
	Rise time	T_R	29, 30	RFOUT5 = 3.3 µF, RFOUT5 = 15 Ω	—	—	50	µs
RF regulator [RFREG6]	Output voltage	V_{O6}	33	RFOUT6 = 0 mA	2.79	2.85	2.91	V
		V_{OLD6}	33	RFOUT6 = –50 mA	2.79	2.85	2.91	V
	Line regulation	Line	33	VB = 3.1 to 4.8 V, RFOUT6 = –10 mA	—	—	20	mV
	Load regulation	Load	33	RFOUT6 = 0 to –50 mA	–30	—	0	mV
	Ripple rejection	R.R	33	Vin = 0.2 Vrms, f = 1 kHz, RFOUT6 = –10 mA	—	–55*	—	dB
	Rise time	T_R	33	RFOUT6 = 4.7 µF, RFOUT6 = 62 Ω	—	—	270	µs

* : Standard design value

(Continued)

(Continued)

(Ta = +25 °C, VB = 3.6 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
RF regulator control	Input voltage	V_{IL}	41, 39, 37, 36, 31, 32	—	0	—	OUT1× 0.3	V
		V_{IH}	41, 39, 37, 36, 31, 32	—	OUT1× 0.7	—	OUT1	V
	Input current	I_{IL}	41, 39, 37, 36, 31, 32	RFCTL1 to RFCTL6 = 0 V	–1	—	1	µA
		I_{IH}	41, 39, 37, 36, 31, 32	RFCTL1 to RFCTL6 = 2.85 V	22	28.5	41	µA
Variable bias regulator [VARREG]	Input voltage range	V_{IN}	67	—	1.67	—	2.38	V
	Output voltage range	V_O	68	—	2.00	—	2.85	V
	Output voltage precision	V_{OP}	68	—	–2.5	—	2.5	%
	Output current	I_O	68	—	–10	—	—	mA
	Input current	I_{IL}	67	VREGIN = 0 V	–1	—	1	µA
		I_{IH}	67	VREGIN = 2.85 V	22	28.5	41	µA
D/A converter	System resolution	—	63, 62, 61	D/A1 to D/A3	—	—	8	bit
		—	60	D/A4	—	—	10	bit
	Differential non-linear type linearity error	L_E	60	D/A4 (Input code is 200)	–12	—	+12	LSB
			60	D/A4 (Input code is 100, and 300)	–9	—	+9	LSB
			60	D/A4 (Input code is 080, 180, 280, and 380)	–7	—	+7	LSB
			63, 62, 61	D/A1 to D/A3 (Input code is 040, 080, and 0C0)	–4	—	+4	LSB
			63, 62, 61, 60	Other input code	–1.0	—	+1.0	LSB
	Output voltage range	V_{OC}	63, 62, 61, 60	D/AOUT1 to D/AOUT4 = –330 µA to 1 mA	0.5	—	2.5	V
	Rise time	T_R	63, 62, 61, 60	D/AOUT1 to D/AOUT4 = 100 pF	—	—	20	µs
	Output Noise	V_{NOVL}	63, 62, 61, 60	—	—	—	–77.8	dBm

(Continued)

(Ta = +25 °C, VB = 3.6 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Power-on reset	Detected voltage	V_{SL1}	75	—	2.63	2.685	2.74	V
		V_{SH1}	75	—	2.695	2.75	2.805	V
	Output voltage	V_{OH}	77	$\overline{RESET}$ = –200 µA	OUT1 – 0.3	OUT1	—	V
		V_{OH}	77	$\overline{RESET}$ = 200 µA	—	0.01	0.4	V
	POR hold time	T_{PR}	77	CTP ≤ 0.1 µF	25	70	115	ms
	Rise time	T_R	77	$\overline{RESET}$ = 50 pF	—	—	500	ns
	Fall time	T_F	77	$\overline{RESET}$ = 50 pF	—	—	500	ns
Supply voltage detector	Detected voltage	V_{3VDH}	56	—	2.99	3.05	3.11	V
		V_{3VDL}	56	—	2.79	2.85	2.907	V
Power control (General)	Power consumption current	I_{B1}	28, 34, 45, 58, 70, 74, 80	Special power off	—	11	20	µA
		I_{B2}	28, 34, 45, 58, 70, 74, 80	Standby	50	70	100	µA
		I_{B3}	28, 34, 45, 58, 70, 74, 80	Power on (waiting) intermittent	50	70	100	µA
		I_{B4}	28, 34, 45, 58, 70, 74, 80	Power on (waiting) receiving	190	250	360	µA
		I_{B5}	28, 34, 45, 58, 70, 74, 80	Power on (conversation) transmission	170	220	315	µA
		I_{B6}	28, 34, 45, 58, 70, 74, 80	Power on (conversation) receiving	190	250	360	µA

* : Standard design value

Note: I_{B1} to I_{B6} of general power control means the total current at VB1 to VB7 terminals the load current is not included. As for the condition of each regulators at the measurement of power consumption current , please refer to “■ CONDITIONS of EACH REGURATORS at MEASUREMENT of CONSUMPTION CURRENT”.

- Speaker Amp.

(Ta = +25 °C, VB = V30R = 3.6 V, f = 1 kHz)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Receiver Amp.	Voltage gain	A_{V1}	25	Single drive, INV input FB = 4.7 kΩ, FB to OUTA = 15 kΩ	8.1	10.1	12.1	dB
		A_{V2}	25, 26	BTL drive, INV input FB = 4.7 kΩ, FB to OUTA = 15 kΩ	14.1	16.1	18.1	dB
	Open-ended voltage gain	A_{VO}	25, 26	f ≤ 100 Hz	—	80*	—	dB
	Output power	P_{O1}	25, 26	V30R = 3.6 V, OUTA to OUTB = 32 Ω, THD = 10%	60	90	—	mW
		P_{O2}	25, 26	V30R = 2.85 V, OUTA to OUTB = 32 Ω, THD = 10%	30	45	—	mW
	Output voltage	V_O	25, 26	OUTA to OUTB = no load	3.8	5.5	—	V
	Offset voltage between output	V_{OO}	25, 26	—	–50	—	50	mV
	Total harmonic distorition rate	THD	25, 26	P_O = 25 mW	—	0.5	1.0	%
	Ripple rejection	R.R	25, 26	—	—	–45*	—	dB
	Rise time	T_R	25, 26	BP = 1 V, BP = 4.7 μF	—	—	0.1	s
Loud speaker Amp.	Voltage gain	A_V	22, 23	BTL drive, INV input FB = 4.7 kΩ, FB to SPOUTA = 15 kΩ	14.1	16.1	18.1	dB
	Open-ended voltage gain	A_{VO}	22, 23	f ≤ 100 Hz	—	80*	—	dB
	Output power	P_{O1}	22, 23	V30R = 3.6 V, SPOUTA to SPOUTB = 8 Ω, THD = 10%	160	260	—	mW
		P_{O2}	22, 23	V30R = 2.85 V, SPOUTA to SPOUTB = 8 Ω, THD = 10%	50	110	—	mW
	Output voltage	V_O	22, 23	SPOUTA to SPOUTB = no load	3.8	5.5	—	V
	Offset voltage between output	V_{OO}	22, 23	—	–50	—	50	mV
	Overall harmonic distorition rate	THD	22, 23	P_O = 60 mW	—	0.5	1.0	%
	Ripple rejection	R.R	22, 23	—	—	–45*	—	dB
	Rise time	T_R	22, 23	BP = 1 V, BP = 4.7 μF	—	—	0.1	s
Speaker Amp.	Input impedance	R_{IN}	19, 20	—	20	30	50	kΩ
	Standby supply current	I_{CC1}	21	—	—	0	10	μA

* : Standard design value

• Sounder

(Ta = +25 °C, VB = 3.6 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Sounder	Output voltage	V_{O1}	16	VO1 = 200 mA	—	0.3	0.5	V
		V_{O2}	14	VO2 = 100 mA	—	0.3	0.5	V
		V_{O3}	13	VO3 = 50 mA	—	0.3	0.5	V
	Output leakage current	I_{LEAK}	16, 14, 13	VB = VO1 to VO3 = 6 V	—	—	10	µA
	Conditions for input ON	V_{ON}	10, 11, 12	—	VB × 0.7	—	VB	V
		V_{OFF}	10, 11, 12	—	0.0	—	VB × 0.3	V
	Input current	I_{IH}	10, 11, 12	IN1 to IN3 = 3 V	–1	—	1	µA
		I_{IL}	10, 11, 12	IN1 to IN3 = 0.4V	–1	—	1	µA

• LED drive

(Ta = +25 °C, VB = 3.6 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
LED drive	Output voltage	V_{LE1}	2	LEDO1 = 25 mA	—	0.2	0.4	V
		V_{LE2}	4	LEDO2 = 25 mA	—	0.2	0.4	V
		V_{LER}	1	LEDR = 25 mA	—	0.2	0.4	V
	Output leakage current	I_{LEAK}	2, 4, 1	VB = VO1 to VO3 = 6 V	—	—	10	µA

• Charge control

(Ta = +25 °C, EXTVCC = 5.2 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Charge control	Control input range	ΔV_{CHG}	49	—	0.8	—	2.5	V
	Control output minimum voltage	V_{COL}	50	EXTVCC = 6 V	—	—	0.1	V
	Control output maximum voltage	V_{COH}	50	EXTVCC = 6 V	EXTVCC – 0.5	—	—	V
	Control input current	I_{CHGV}	49	CHGV = 4 V	—	—	5	µA
	Control output voltage	V_{GG1}	50	VB = 4 V, CHGV = 1.59 V	0.85	1.44	2.15	V
		V_{GG2}	50	VB = 4 V, CHGV = 1.69 V	1.85	2.44	3.15	V
	Control gain	V_{GG}	50	20 log{ (V_{GG2} – V_{GG1}) / 0.1}	18.8	20.8	22.8	dB
	BATT detected voltage	V_{BATT}	48	VB = 3.6 V	1.35	1.43	1.52	V
		V_{CHGBAT}	44	VB = 3.6 V	1.35	1.43	1.52	V
Charge current detector	VBH input voltage range	V_{BH}	46	EXTVCC = 6 V	1.0	—	5.0	V
	VBH input leakage current	I_{LBH}	46	VB = VBH = 4 V, EXTVCC = 0 V	—	—	10	µA
	Chage control output voltage	V_{CUR1}	47	Low precision VB = VBH = 3.6 V	1.8	2.0	2.2	V
		V_{CUR2}	47	Low precision VB = 3.6 V, VBH = 3.75 V	1.05	1.25	1.45	V
		V_{CUR3}	47	High precision VB = VBH = 3.6 V	1.8	2.0	2.2	V
		V_{CUR4}	47	High precision VB = 3.6 V, VBH = 3.75 V	0.48	0.8	1.12	V
	Current detected sensitivity	V_{CURG1}	47	20 log{ (V_{CUR1} – V_{CUR2}) / 0.15}	12	14	16	dB
		V_{CURG2}	47	20 log{ (V_{CUR3} – V_{CUR4}) / 0.15}	16	18	20	dB

(Continued)

(Continued)

(Ta = +25 °C, EXTVCC = 5.2 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Preliminary charge circuit	Switching voltage of charge current	V_{B1}	28, 34, 45, 58, 70, 74, 80	—	2.5	2.6	2.7	V
		V_{B2}	28, 34, 45, 58, 70, 74, 80	—	3.8	4.0	4.2	V
	Charge current	I_{B1}	54	—	40	50	60	mA
		I_{B2}	54	—	80	100	120	mA
Exterenal power supply detector	CHGDET output voltage	V_{CDL}	51	EXTVCC = 2 V, CHGDET = 0 A	—	—	0.3	V
		V_{CDH}	51	EXTVCC = 0.6 V, CHGDET = 0 A	OUT1 – 0.2	OUT1	—	V

• Serial control

(Ta = +25 °C, VB = 3.6 V)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Serial control	Input voltage	V_{IL}	6, 7, 8	—	0	—	OUT1 × 0.3	V
		V_{IH}	6, 7, 8	—	OUT1 × 0.7	—	OUT1	V
	Input current	I_{IL}	6, 7, 8	DAT = SCLK = STBIN = 0 V	–1	—	1	µA
		I_{IH}	6, 7, 8	DAT = SCLK = STBIN = 2.85 V	–1	—	1	µA

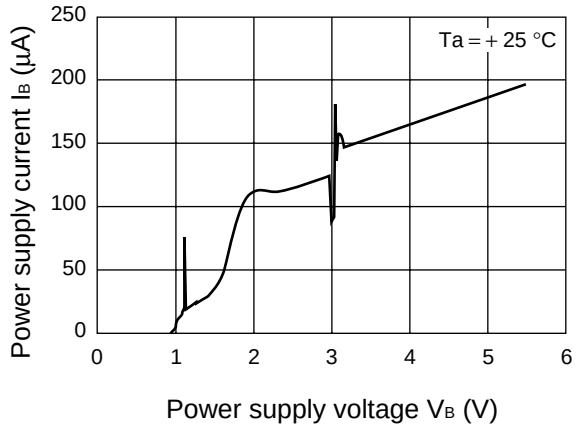
• Special power off

(Ta = +25 °C, VB = 3.6 V)

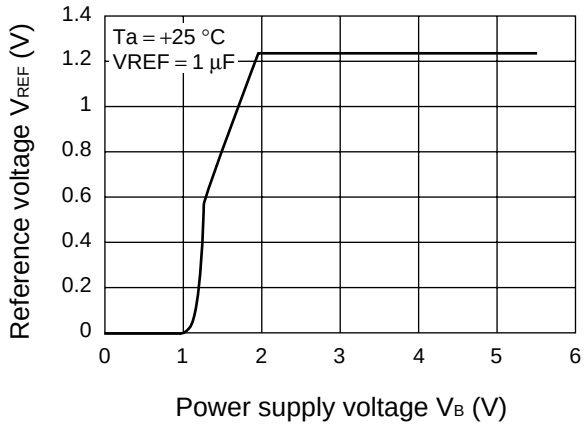
Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min.	Typ.	Max.	
Special power off	Output voltage	V_{IPOFF}	59	IPOFF = 0 A	VB – 0.1	VB	—	V
	IPOFFmode release voltage	$V_{RELEASE}$	59	—	—	—	VB × 0.3	V

■ TYPICAL CHARACTERISTICS

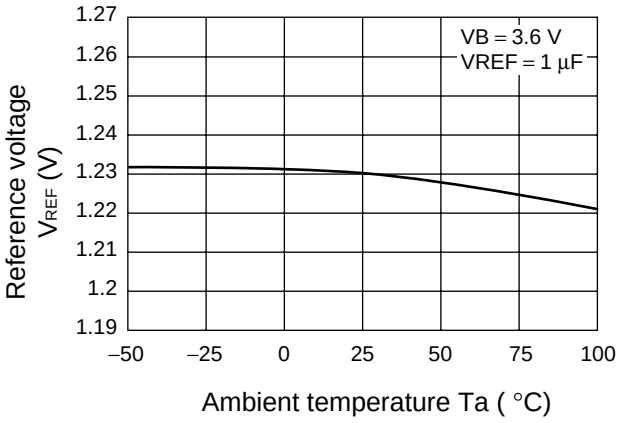
Power supply current vs. power supply voltage



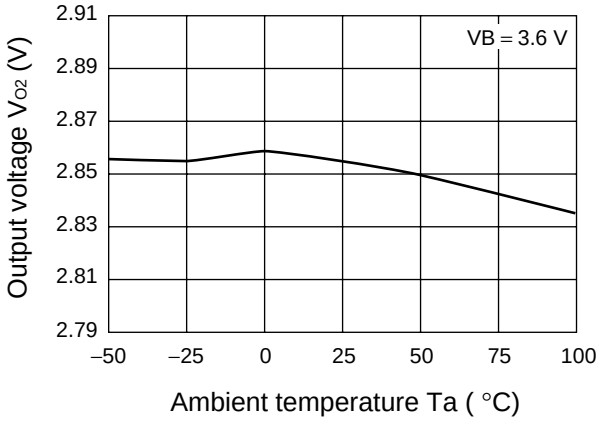
Reference voltage vs. power supply voltage



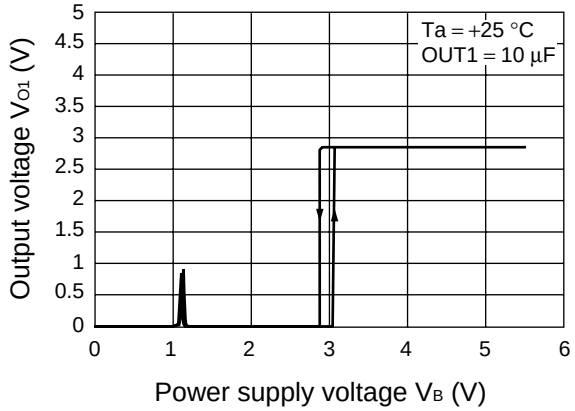
Reference voltage vs. ambient temperature



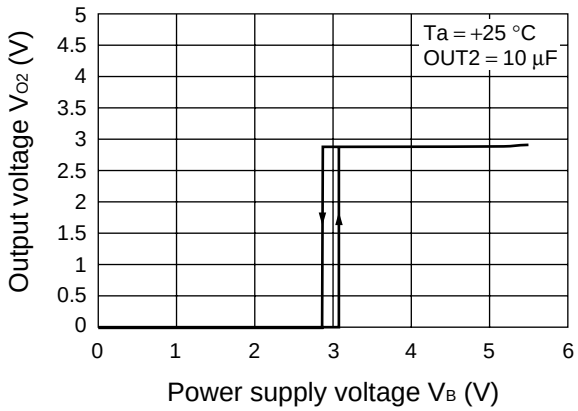
Output voltage vs. ambient temperature (BBREG2)



Output voltage vs. power supply voltage (BBREG1)

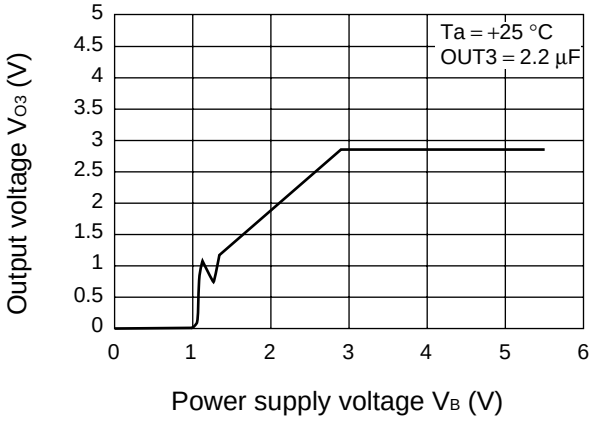


Output voltage vs. power supply voltage (BBREG2)

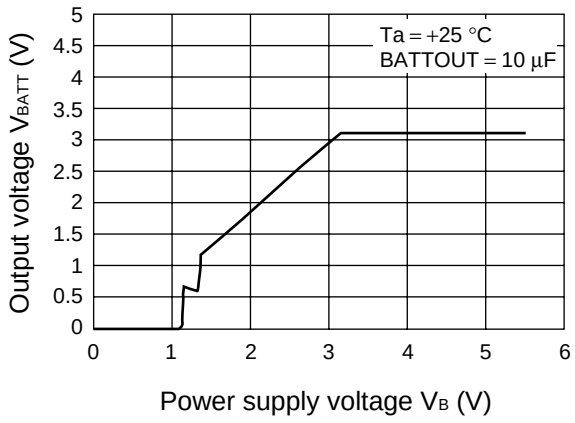


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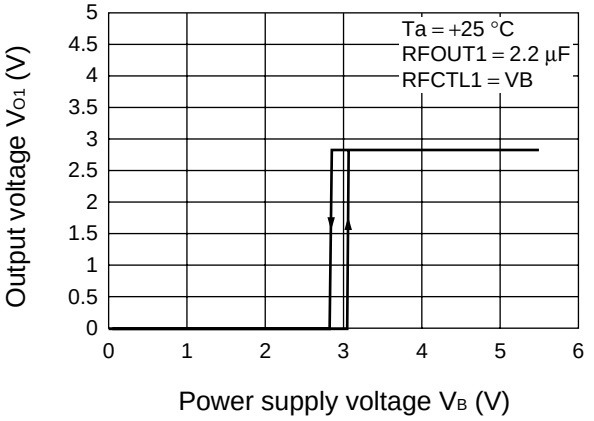
Output voltage vs. power supply voltage (BBREG3)



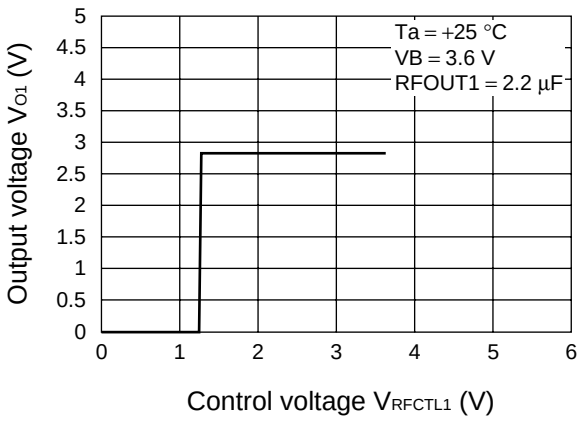
Output voltage vs. power supply voltage (BATTREG)



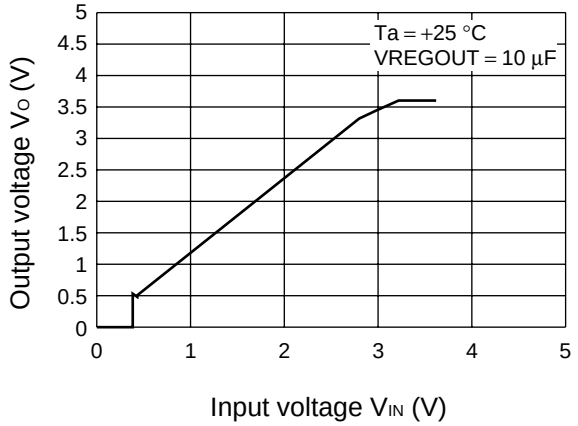
Output voltage vs. power supply voltage (RFREG1)



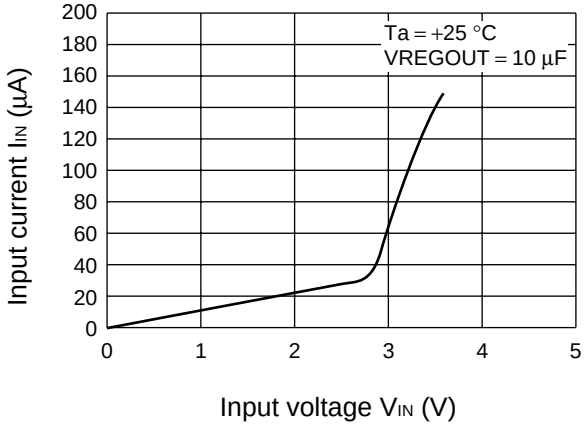
Output voltage vs. control voltage (RFREG1)



Output voltage vs. input voltage (Variable REG)

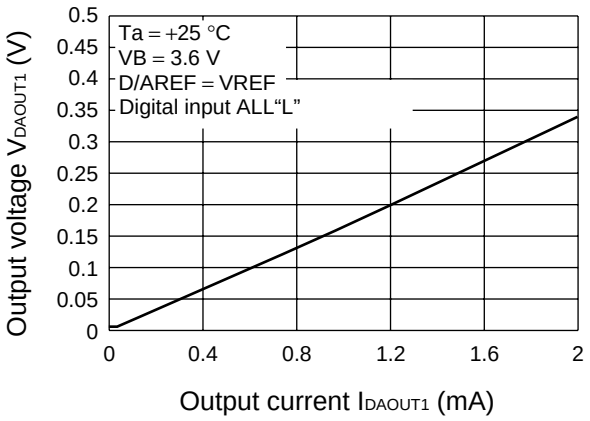


Input current vs. input voltage (Variable REG)

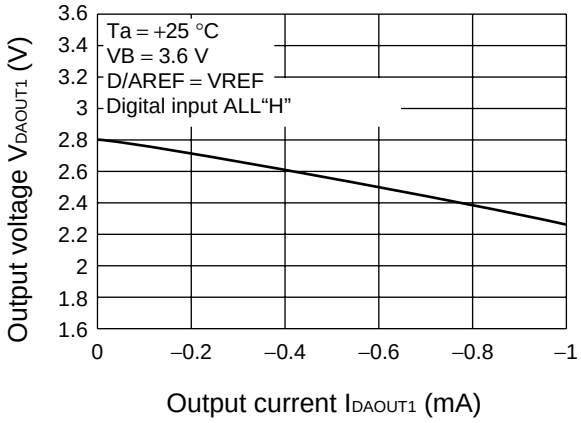


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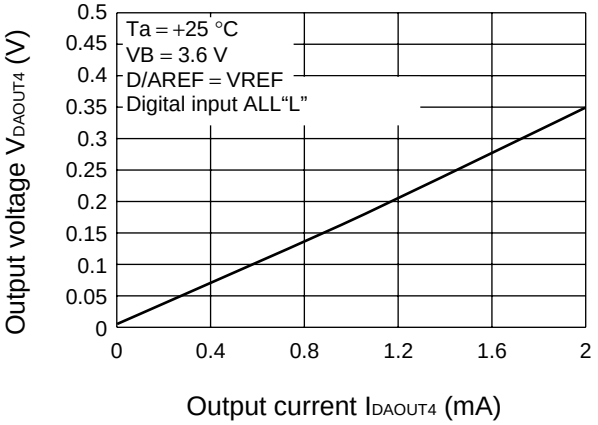
DA1 output voltage vs. output current



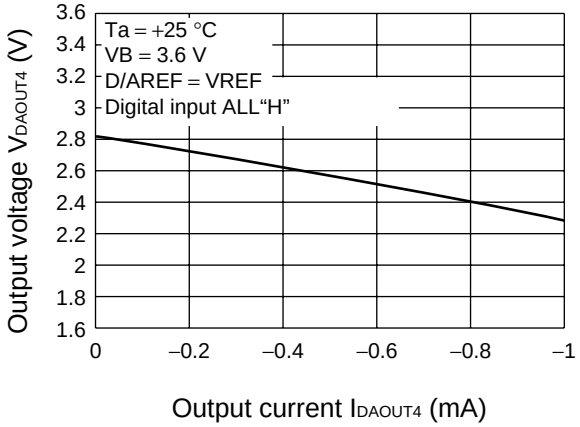
DA1 output voltage vs. output current



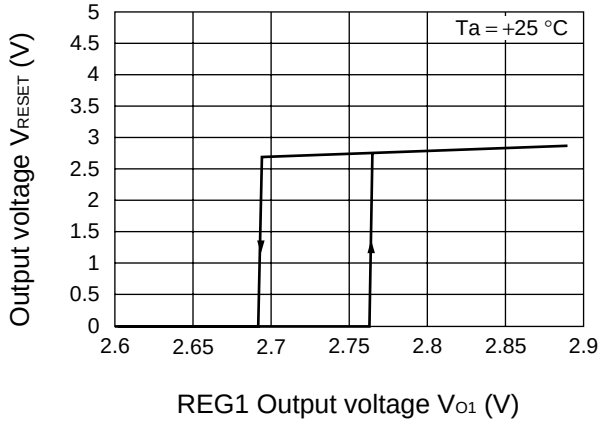
DA4 output voltage vs. output current



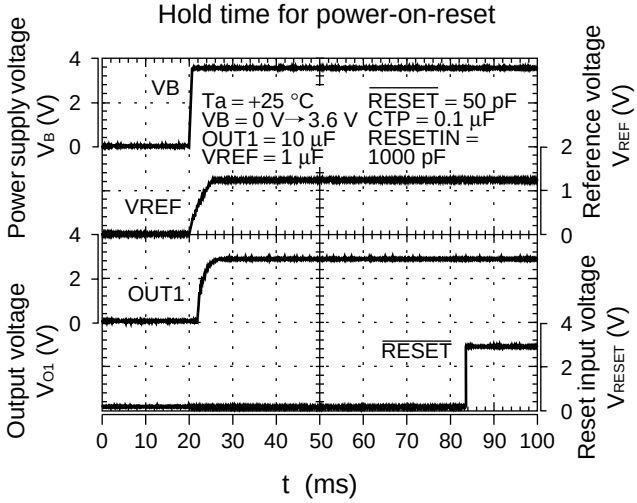
DA4 output voltage vs. output current



Reset output voltage vs. REG1 output voltage

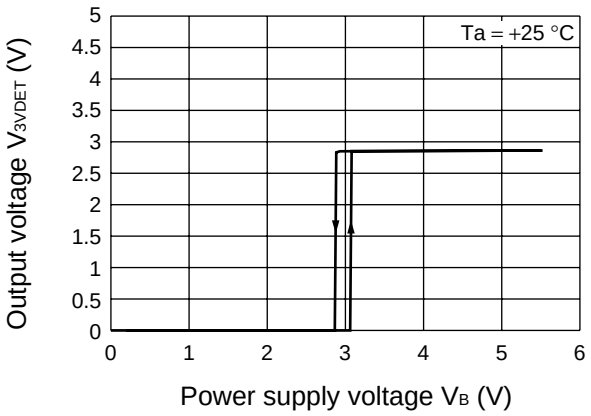


Hold time for power-on-reset

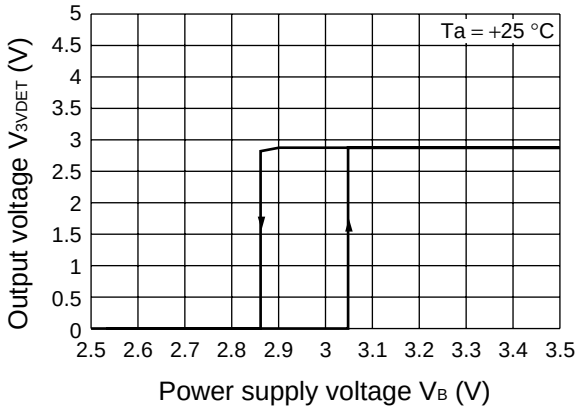


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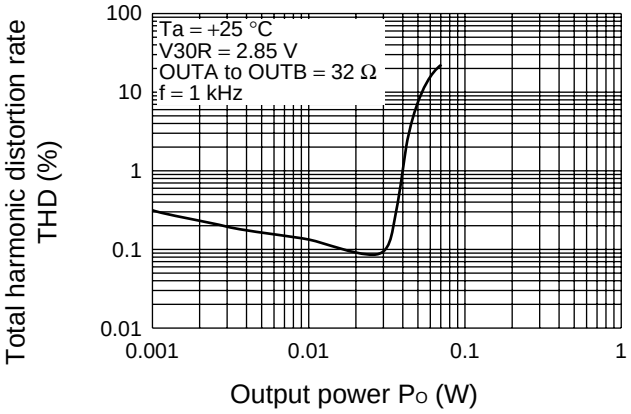
Power supply voltage detected output voltage vs. power supply voltage



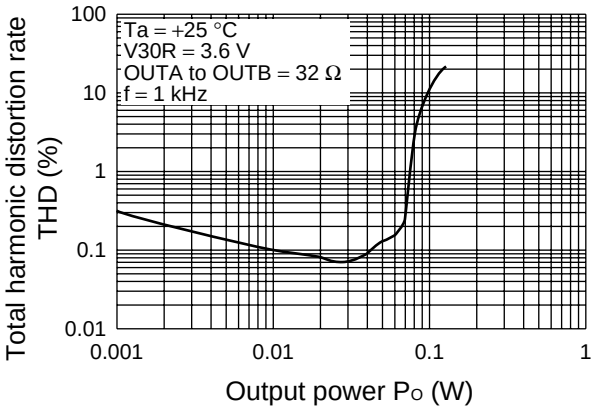
Power supply voltage detected output voltage vs. power supply voltage



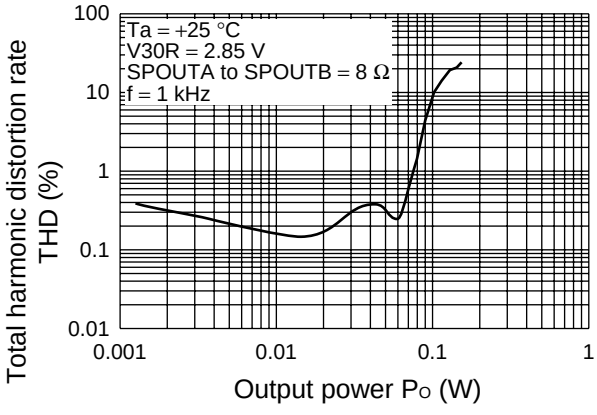
Total harmonic distortion rate vs. output power (receiver Amp.)



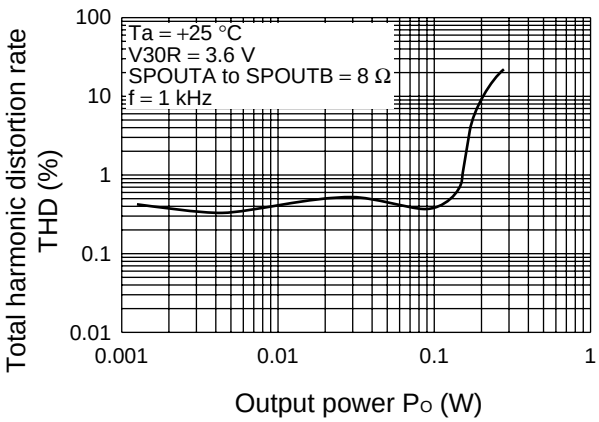
Total harmonic distortion rate vs. output power (receiver Amp.)



Total harmonic distortion rate vs. output power (Loudspeaker Amp.)

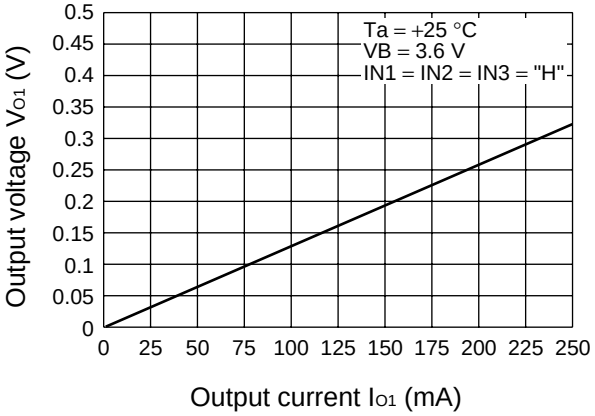


Total harmonic distortion rate vs. output power (Loudspeaker Amp.)

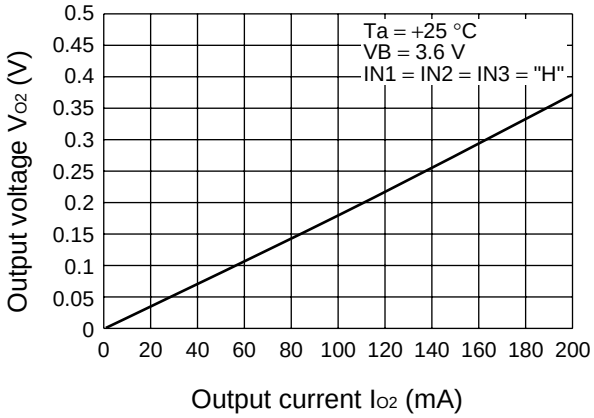


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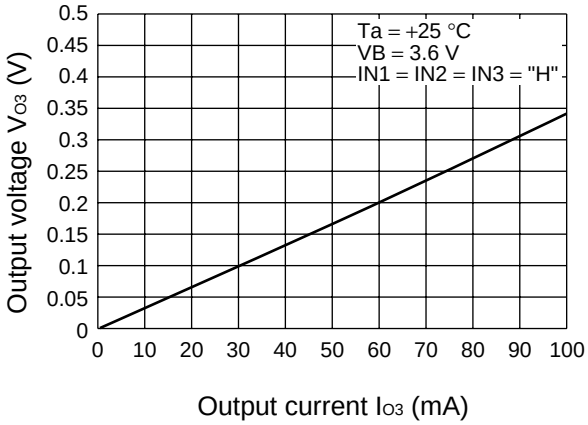
Sounder1 output voltage vs. output current



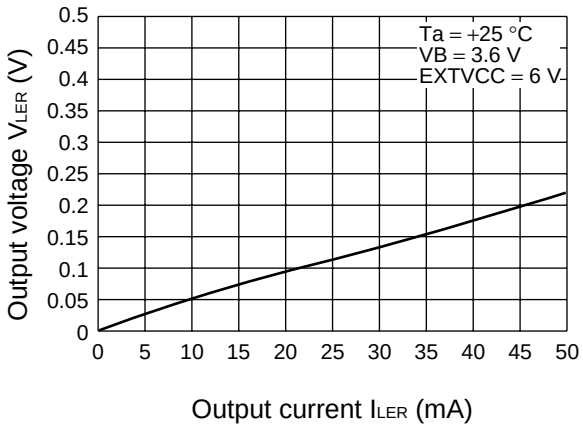
Sounder2 output voltage vs. output current



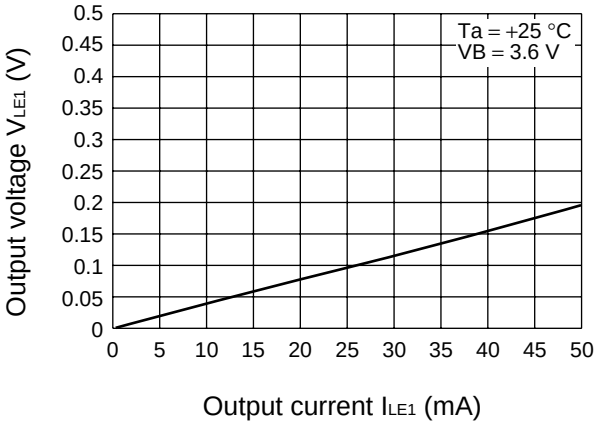
Sounder3 output voltage vs. output current



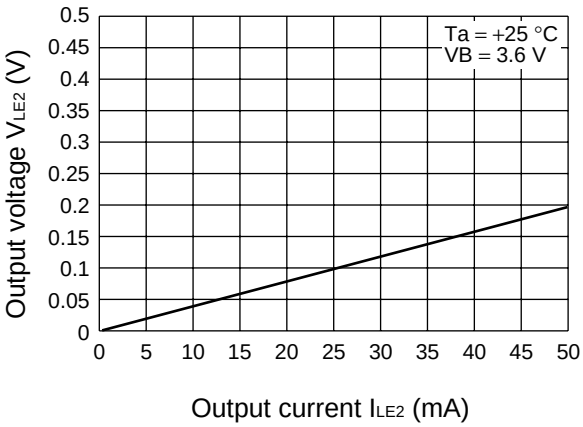
LEDR output voltage vs. output current



LED1 output voltage vs. output current

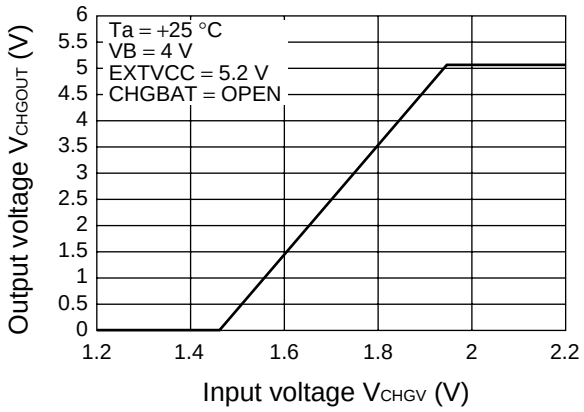


LED2 output voltage vs. output current

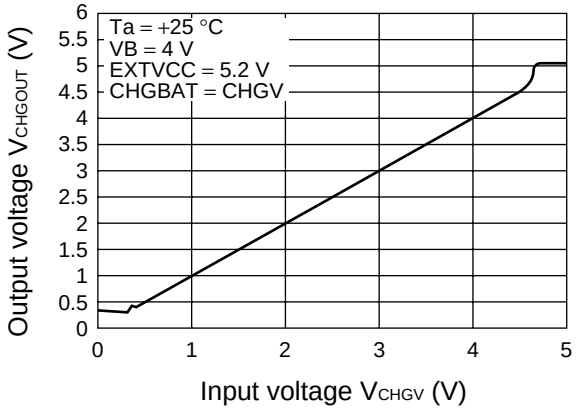


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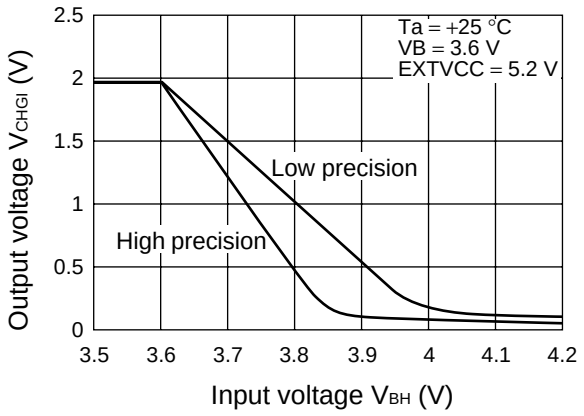
CHGOUT output voltage vs. CHGV input voltage



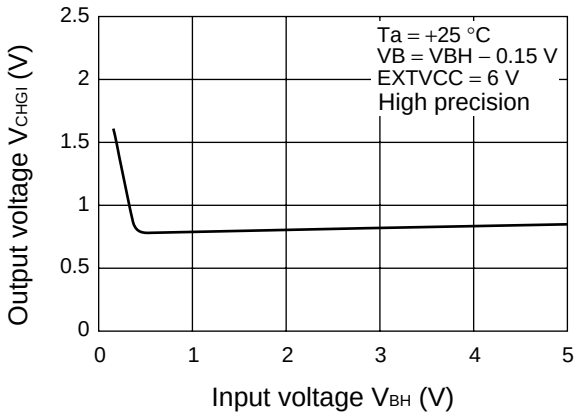
CHGOUT output voltage vs. CHGV input voltage



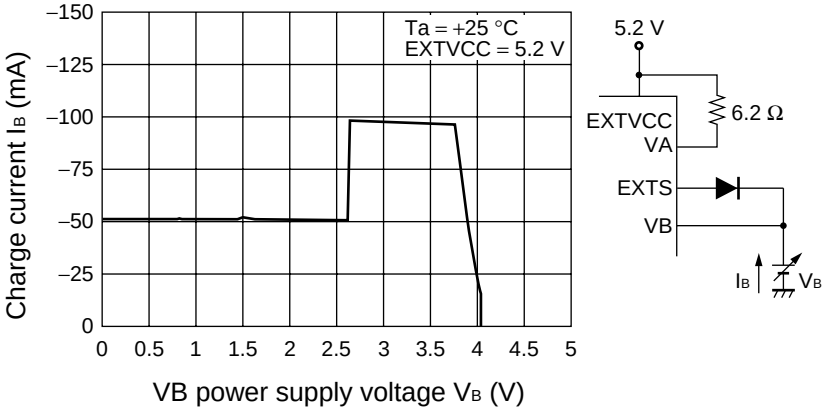
CHGI output voltage vs. VBH input voltage



CHGI output voltage vs. VBH input voltage



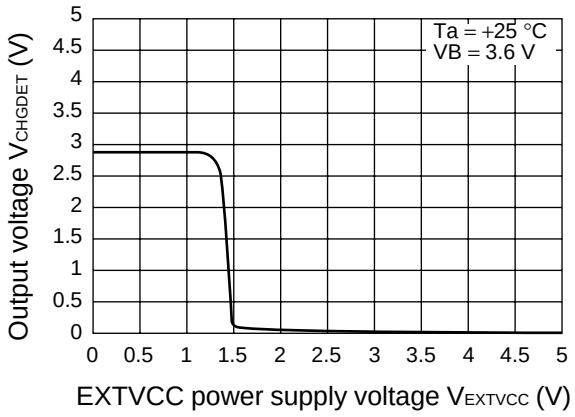
Preliminary charge current vs. VB power supply voltage



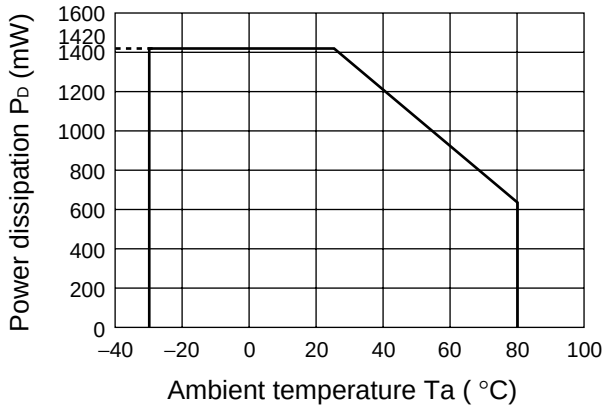
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CHGDET output voltage vs. EXTVCC power supply voltage



Power dissipation vs. ambient temperature



■ FUNCTIONAL DESCRIPTION

1. Power Control

(1) Reference voltage

This circuit uses the voltage generated by VB1 terminal (pin 28) to produce a temperature compensated reference voltage (1.23 V typ.) for power control and uses this reference voltage on power control.

(2) Baseband regulator (BBREG1)

This regulator uses the reference voltage to produce an output voltage (2.85V typ.) at OUT1 terminal (pin 75).
Power can be drawn from OUT1 terminal for external use, up to a maximum load current of 110 mA.

(3) Baseband regulator (BBREG2)

This regulator uses the reference voltage to produce an output voltage (2.85 V typ.) at OUT2 terminal (OUT2-1 terminal (pin 72), OUT2-2 terminal (pin73)).
Power can be drawn from OUT2 terminal for external use, up to a maximum load current of 150 mA.

(4) Baseband regulator (BBREG3)

This regulator uses the reference voltage to produce an output voltage (2.85V typ.) at OUT3 terminal (pin 71).
Power can be drawn from OUT3 terminal for external use, up to a maximum load current of 60mA.

(5) Battery backup regulator (BATTREG)

This regulator uses the reference voltage to produce an output voltage (3.1V typ.) at BATTOUT terminal (pin 69).

(6) Vibrator drive circuit (VIBREG)

This circuit uses the reference voltage to produce an output voltage (1.5V typ.) at VIBREG terminal (VIBREG-1 terminal (pin 78), VIBREG-2 terminal (pin 79)).
Power can be drawn from VIBREG terminal for external use, up to a maximum load current of 200mA.

(7) RF regulator (RFREG1)

This regulator uses the reference voltage to produce an output voltage (2.85V typ.) at RFOUT1 terminal (pin 42) when an "H" level signal is input at the RFCTL1 terminal (pin 41).
Power can be drawn from RFOUT1 terminal for external use, up to a maximum load current of 10mA.

(8) RF regulator (RFREG2)

This regulator uses the reference voltage to produce an output voltage (2.85V typ.) at RFOUT2 terminal (pin 40) when an "H" level signal is input at the RFCTL2 terminal (pin 39).
Power can be drawn from RFOUT2 terminal for external use, up to a maximum load current of 20mA.

(9) RF regulator (RFREG3)

This regulator uses the reference voltage to produce an output voltage (2.85V typ.) at RFOUT3 terminal (pin 38) when an "H" level signal is input at the RFCTL3 terminal (pin 37).
Power can be drawn from RFOUT3 terminal for external use, up to a maximum load current of 20mA.

(10) RF regulator (RFREG4)

This regulator uses the reference voltage to produce an output voltage (2.85V typ.) at RFOUT4 terminal (pin 35) when an "H" level signal is input at the RFCTL4 terminal (pin 36).
Power can be drawn from RFOUT4 terminal for external use, up to a maximum load current of 60mA.

(11) RF regulator (RFREG5)

This regulator uses the reference voltage to produce an output voltage (2.85V typ.) at RFOUT5 terminal (RFOUT5-1 terminal (pin 30), RFOUT5-2 terminal (pin 29)) when an "H" level signal is input at the RFCTL5 terminal (pin 31).
Power can be drawn from RFOUT5 terminal for external use, up to a maximum load current of 200mA.

(12) RF regulator (RFREG6)

This regulator uses the reference voltage to produce an output voltage (2.85V typ.) at RFOUT6 terminal (pin 33) when an "H" level signal is input at the RFCTL6 terminal (pin 32).
Power can be drawn from RFOUT6 terminal for external use, up to a maximum load current of 50mA.

(13) Variable bias regulator

This regulator uses the voltage generated by VREGIN terminal (pin 67) to produce an amplified output voltage at VREGOUT terminal (pin 68).
Power can be drawn from VREGOUT terminal for external use, up to a maximum load current of 10mA.

(14) D/A converter

D/A1 to D/A3 converter process 8 bit input signal and D/A4 converter processes 10 bit input signal.
This converter generates an output voltage (0.5 to 2.5V) at D/AOUT1 terminal (pin 63) to D/AOUT4 terminal (pin 60) according to the signal from serial control.

(15) Power-on reset

When the OUT1 terminal (pin 75) voltage exceeds 2.75V(typ.) , after a delay interval set by a capacitor (0.1 µF typ.) connected to the CTP terminal (pin 76) , the $\overline{\text{RESET}}$ terminal (pin 77) voltage becomes "H" level from "L" level and the reset signal is canceled.
When the OUT1 terminal voltage falls below 2.685V (typ.), the $\overline{\text{RESET}}$ terminal voltage becomes "L" level from "H" level and the reset signal is dispatched. (refer to "■POWER-ON RESET TIMING DIAGRAM", "■SETTING OF HOLD TIME FOR POWER-ON RESET".)

(16) Battery voltage detect

This function is to observe the battery voltage. When the VB4 terminal (pin 58) voltage exceeds 3.05V (typ.), the 3VDET terminal (pin 56) voltage goes to "H" level and when the VB4 terminal voltage falls below 2.85V (typ.), the 3VDET terminal goes to "L" level. (refer to ■BATTERY VOLTAGE DETECTOR)

2. Speaker Amp.

(1) Receiver Amp.

This is the BTL output type Amp. driving speaker directly. When the output power is 90mW typ. (at 32Ω), the serial control processes the on/off and the earphone switching control.
The optional gain can be set by the connection of feedback resistor from FB terminal (pin 20) to OUTA terminal (pin 25) and the connection of input resistor to FB terminal.

(2) Loudspeaker Amp.

This is the BTL output type Amp. driving speaker directly. When the output power is 260mW typ. (at 8Ω), the serial control processes the on/off control.
The optional gain can be set by the connection of feedback resistor from FB terminal (pin 20) to SPOUTA terminal (pin 22) and the connection of input resistor to FB terminal.

3. Sounder

Three low-saturation output transistors are built in for buzzer drive. When the signal from serial control is "H" level and IN1 terminal (pin 10) voltage is "H" level, the V01 terminal (pin 16) voltage is 0.3V (typ.). When IN2 terminal (pin 11) voltage and IN3 terminal (pin 12) voltage are "H" level, the V02 terminal (pin 14) voltage and V03 terminal (pin 13) voltage are also 0.3V (typ.).

4. LED drive

The LEDO1 terminal (pin 2) voltage and LEDO2 terminal (pin 4) voltage is 0.2V (typ.), when the signal from serial control is "H" level. When the signal from charge control is "H" level, the LEDR terminal (pin 1) voltage is 0.2V (typ.).

5. Charge control

(1) Charge control

The main charge is started by the signal from serial control indicates preliminary charge is finished.
According to the voltage level at CHGV terminal (pin 49) generated by microprocessor on the microprocessor operation, the charge current is controlled by adjusting gate voltage from outside FET.

(2) Charge current detector

The charge current detector sensitivity (gain) can be switched by the signal from serial control.
The VBH terminal (pin 46) voltage and VB4 terminal voltage (pin 58) are detected and CHGI terminal (pin 47) voltage is generated.

(3) Preliminary charge circuit

When the battery voltage is low, the charge is controlled until the microprocessor starts the operation.
Before the battery voltage reaches 2.6V (typ.), 50mA (typ.) is used for the charge and before 4V (typ.), 100mA (typ.) is used.

(4) External power supply detector

This function is to detect if the case is attached to the battery charger.

When the case is attached to the battery charger, EXTVCC terminal (pin 52) voltage is "H" level and generate "L" level voltage at CHGDET terminal (pin 51). When the case is not attached to the battery charger, EXTVCC terminal voltage is "L" level and generate "H" level voltage at CHGDET terminal.

6. Serial control

After the input signal from microprocessor at DAT terminal (pin 6) is captured at the rising edge of SCLK terminal (pin 7), the signal is input in the internal register at the rising edge of STBIN terminal (pin8) and mode is set.

7. Special power off

This function can control the power consumption current of main IC under 11μA (typ.) and the battery can be kept for the long period under the conditions that battery package is attached to the mobile phone on the shipment.

■ CONDITIONS of EACH REGULATORS at MEASUREMENT of CONSUMPTION CURRENT

Each regulators conditions at the measurment of consumption current are as the following table.
[BIASSW] siganl of serial control is “H” level (BIASSW OFF) .

		BBREG1	BBREG2	BBREG3	BATTREG	VIBREG	VARREG	RFREG1
Special power off	IB1	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Standby	IB2	ON	OFF	ON	ON	OFF	OFF	OFF
Power on (waiting/intermittent)	IB3	ON	OFF	ON	ON	OFF	OFF	OFF
Power on (waiting/receiving)	IB4	ON	ON	ON	ON	OFF	OFF	ON
Power on (conversation/ transmission)	IB5	ON	ON	ON	ON	OFF	OFF	ON
Power on (conversation/receiving)	IB6	ON	ON	ON	ON	OFF	OFF	ON

		RFREG2	RFREG3	RFREG4	RFREG5	RFREG6	Receiver Amp.	Loudspeaker Amp.
Special power off	IB1	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Standby	IB2	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Power on (waiting/intermittent)	IB3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Power on (waiting/receiving)	IB4	ON	ON	ON	OFF	ON	OFF	OFF
Power on (conversation/ transmission)	IB5	ON	OFF	OFF	ON	ON	ON	OFF
Power on (conversation/ receiving)	IB6	ON	ON	ON	OFF	ON	ON	OFF

■ LOGICS

(1) Serial Control Setting Table

A7	A6	A5	A4	A3	A2	A1	A0
1	1	1	1	1	1	1	0

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data	PDSP	PDRCV	CHOISE	LEDC1 (green)	LEDC2 (red)	BIASSW	REG2CTL	VIBCTL	LEDRCTL	VREGCTL
Operation at data “1”	Loud AMPON	Receiver AMPON	BTL drive	ON	ON	OFF	OFF	VIB REGON	Charge red LEDOFF	Variable REGON
Operation at data “0”	Loud AMPOFF	Receiver AMPOFF	Single drive	OFF	OFF	ON	ON	VIB REGOFF	Charge red LEDON	Variable REGOFF
Initial value after reset	0	0	0	0	0	0	0	0	0	0

A7	A6	A5	A4	A3	A2	A1	A0
1	1	1	1	1	1	0	1

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data	REG3CTL		PWOFFCTL		CHGISEL	PRCHGOFF	BUZZSEL	SOUND1	SOUND2	SOUND3
Operation at data “1”	REG3ON	REG3OFF	Special power off setting	*	Low precision	PRCHGOFF	Loud-speaker Amp. short waveform output	Sounder1 ON	Sounder2 ON	Sounder3 ON
Operation at data “0”	REG3OFF	REG3ON	*	Special power off setting	High precision (× 8)	PRCHGON	Loud-speaker Amp. usual output	Sounder1 OFF	Sounder2 OFF	Sounder3 OFF
Initial value after reset	1	0	0	1	0	0	0	0	0	0

*: Unused

A7	A6	A5	A4	A3	A2	A1	A0
1	1	1	1	1	1	0	0

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data	DAR4_9	DAR4_8	DAR4_7	DAR4_6	DAR4_5	DAR4_4	DAR4_3	DAR4_2	DAR4_1	DAR4_0
Operation at data “1”	DA4 setting data									
Operation at data “0”										
Initial value after reset	0	0	0	0	0	0	0	0	0	0

A7	A6	A5	A4	A3	A2	A1	A0
1	1	1	1	1	0	1	1

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data	PDNDA4	PDNDA3	DAR3_7	DAR3_6	DAR3_5	DAR3_4	DAR3_3	DAR3_2	DAR3_1	DAR3_0
Operation at data “1”	DA4ON	DA3ON	DA3 setting data							
Operation at data “0”	DA4OFF	DA3OFF								
Initial value after reset	0	0	0	0	0	0	0	0	0	0

A7	A6	A5	A4	A3	A2	A1	A0
1	1	1	1	1	0	1	0

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data	*	PDNDA2	DAR2_7	DAR2_6	DAR2_5	DAR2_4	DAR2_3	DAR2_2	DAR2_1	DAR2_0
Operation at data “1”	*	DA2ON	DA2 setting data							
Operation at data “0”	*	DA2OFF								
Initial value after reset	*	0	0	0	0	0	0	0	0	0

*:Unused

A7	A6	A5	A4	A3	A2	A1	A0
1	1	1	1	1	0	0	1

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data	*	PDNDA1	DAR1_7	DAR1_6	DAR1_5	DAR1_4	DAR1_3	DAR1_2	DAR1_1	DAR1_0
Operation at data “1”	*	DA1ON	DA1setting data							
Operation at data “0”	*	DA1OFF								
Initial value after reset	*	0	0	0	0	0	0	0	0	0

A7	A6	A5	A4	A3	A2	A1	A0
1	1	1	1	1	0	0	0

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data	*	*	*	*	*	*	*	REG3CTL	PWOFFCTL	
Operation at data “1”	*	*	*	*	*	*	*	REG3ON	Special power off setting	*
Operation at data “0”	*	*	*	*	*	*	*	REG3OFF	*	Special power off setting
Initial value after reset	*	*	*	*	*	*	*	1	0	1

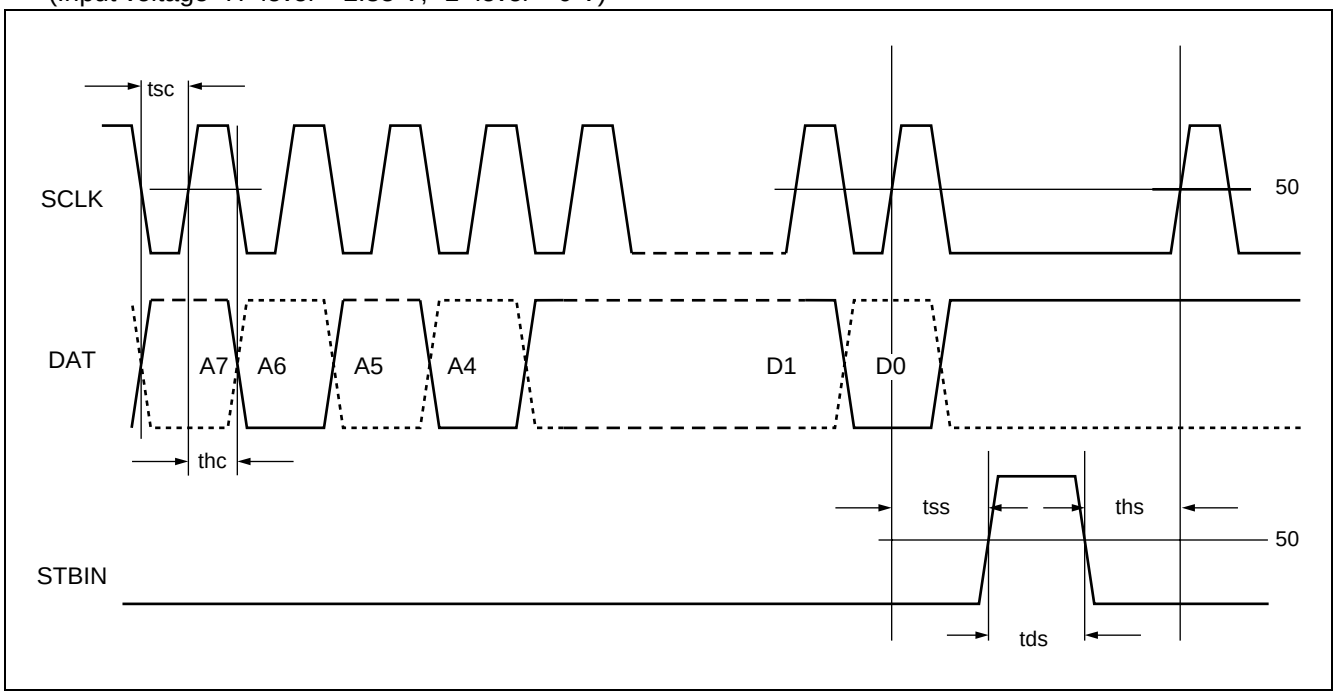
*:Unused

(2) Input Signal Timimg

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Data setup time	tsc	100	—	—	ns	
Data hold time	thc	100	—	—	ns	
STB setup time	tss	100	—	—	ns	
STB pulse duration	tds	100	—	—	ns	
Removal time	ths	100	—	—	ns	

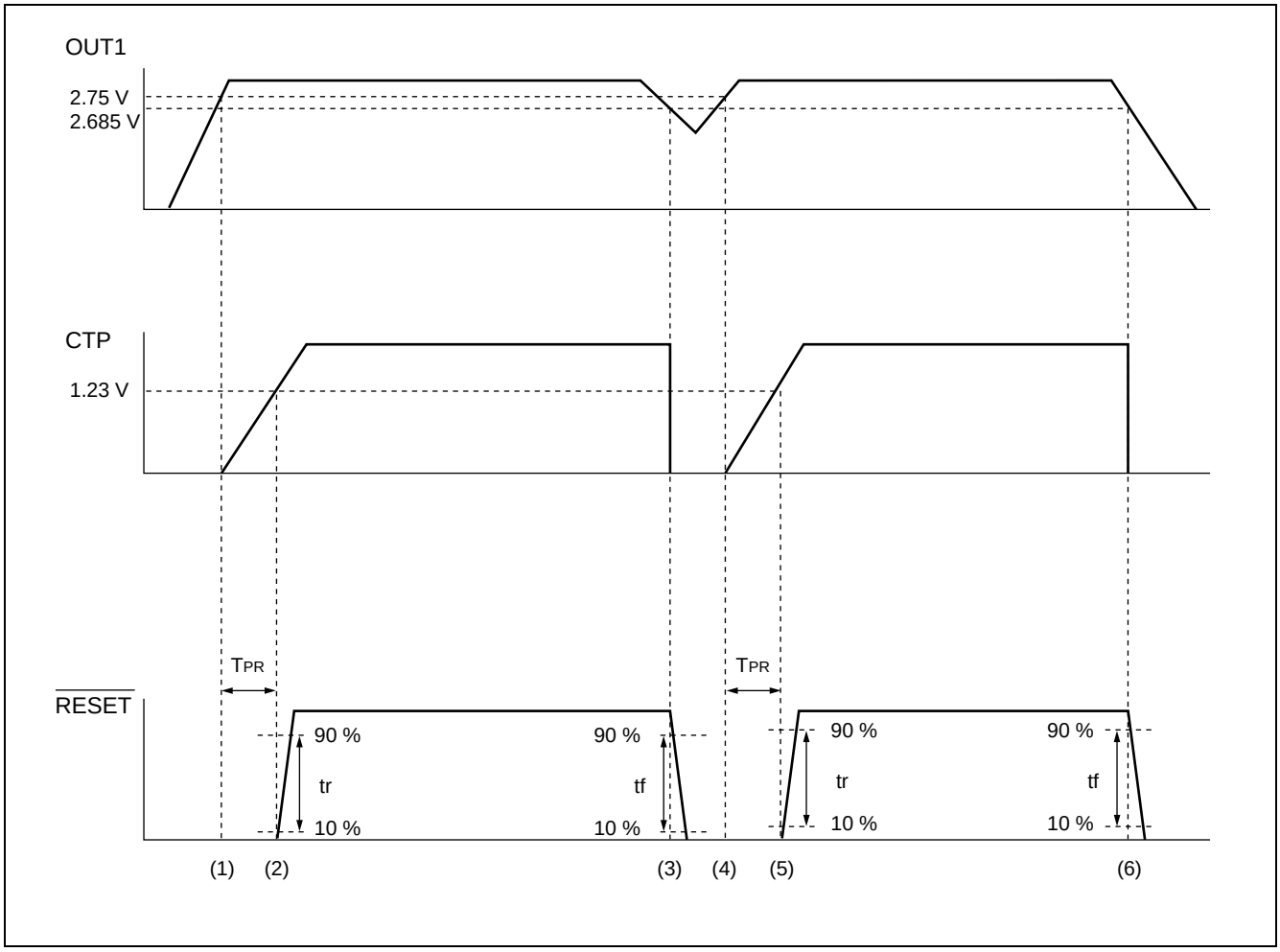
(3) Input Signal Timing Diagram

(Input voltage “H” level = 2.85 V, “L” level = 0 V)



Note : Data is defined at the rising edge of SCLK and IC mode is set through latching of DAT at rising edge STBIN.

■ POWER-ON RESET TIMING DIAGRAM



(1) When the OUT1 terminal (pin 75) voltage exceeds detected rising voltage (2.75V typ.), the charge for timing capacitor (C_{TP}) for hold time for power-on reset starts .

(2) When the CTP terminal (pin 76) voltage exceeds 1.23V (typ.), the reset is canceled. (The $\overline{\text{RESET}}$ terminal voltage becomes "H" level from "L" level.: rising time from 10% to 90% = tr)

(3) When OUT1 terminal voltage falls below detected rising voltage (2.685V typ.), the CTP terminal voltage is down and the reset signal is output. ($\overline{\text{RESET}}$ terminal voltage becomes "L" level from "H" level.)

(4) When OUT1 terminal voltage exceeds rising voltage detect, charging of C_{TP} is started.

(5) When CTP terminal voltage rises above threshold voltage, the reset is canceled.

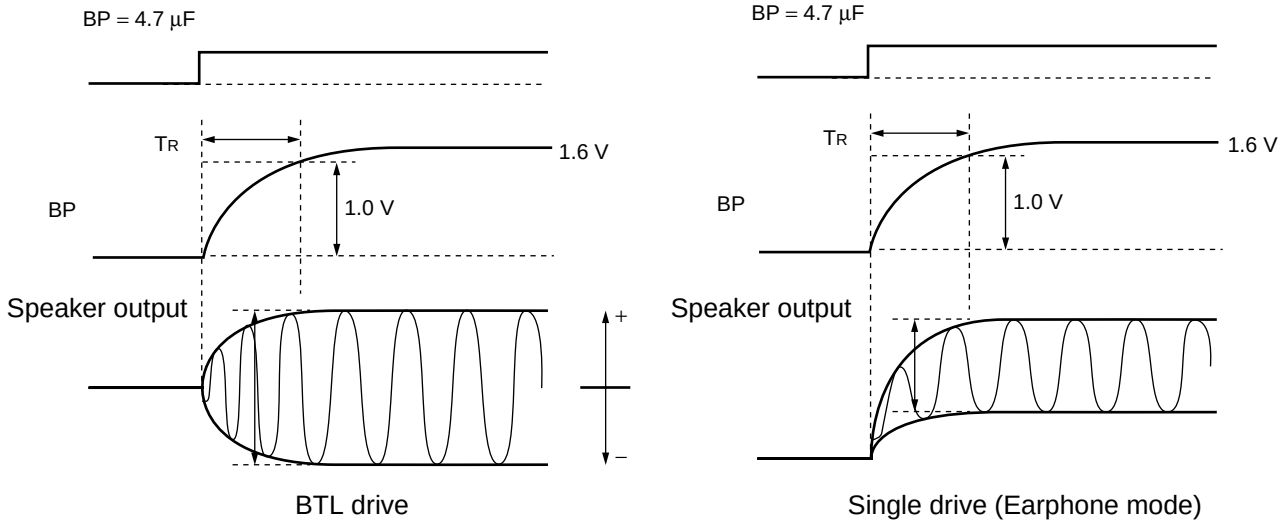
(6) When OUT1 terminal voltage falls below the voltage detect, the reset signal is output.

■ SETTING OF HOLD TIME FOR POWER-ON RESET

According to the time constant set by capacitor (C_{TP}) connected to CTP terminal (pin 76), rise time (hold time) of $\overline{\text{RESET}}$ terminal (pin 77) voltage can be set after OUT1 terminal (pin 75) voltage exceeds 2.75V (typ.).

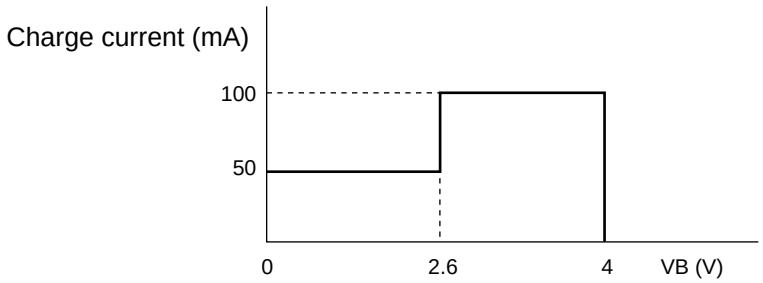
$$\text{POR hold time : } T_{PR}\ (s) \fallingdotseq \frac{1.23\ (V) \times C_{TP}\ (\mu F)}{1.75\ (\mu A)}$$ (tr of $\overline{\text{RESET}}$ is not included)

■ RISE TIME FOR SPEAKER Amp.

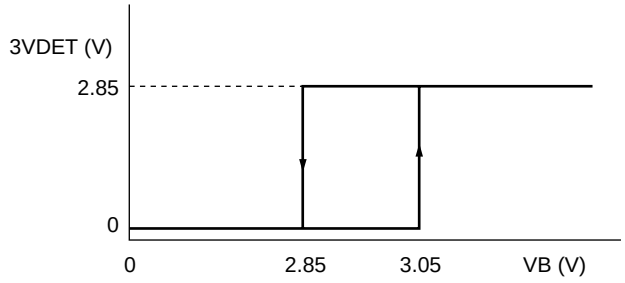


Rise time T_R (ms) ≒ 10.3 (kΩ) × C_{BP} (µF)

■ PRELIMINARY CHARGE CURRENT



■ BATTERY VOLTAGE DETECTOR



■ USAGE PRECAUTIONS

• Printed circuit board ground lines should be set up with consideration for common impedance.

• Take appropriate static electricity measures.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or Containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personal should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

• Do not apply negative voltages

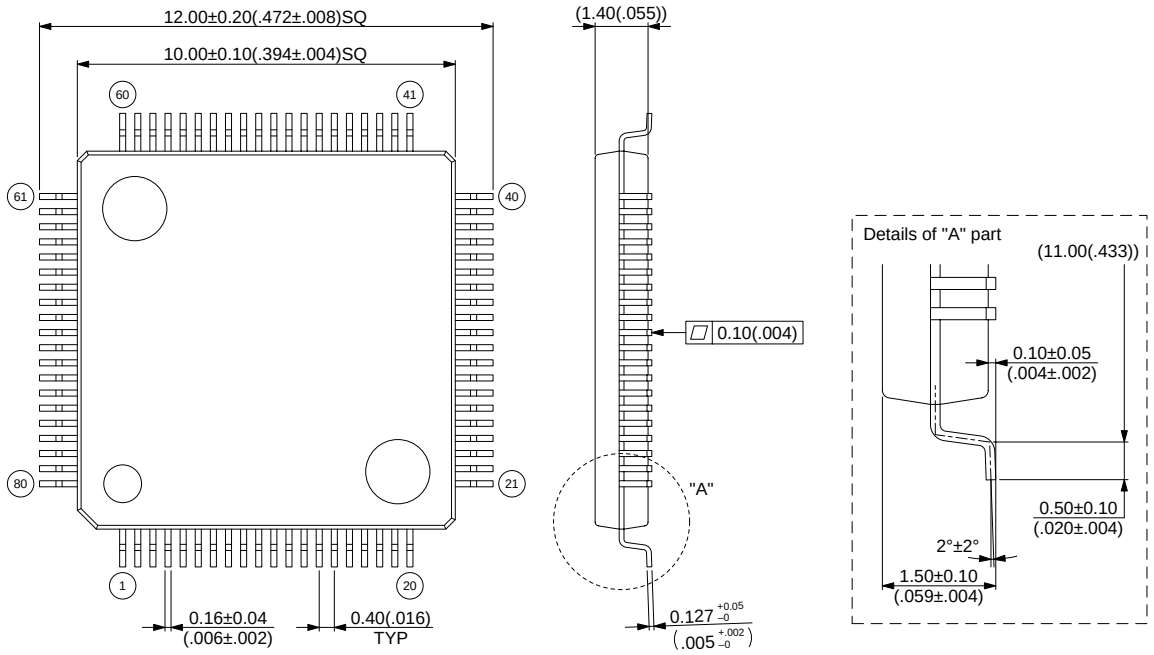
The use of negative voltages below -0.3V may create parasitic transistors on LSI lines, Which can cause abnormal operation.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB3892PFF	80-pin plastic LQFP (FPT-80P-M17)	

■ PACKAGE DIMENTION

80-pin plastic LQFP
(FPT-80P-M17)



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Dimansions in mm (inches) .

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