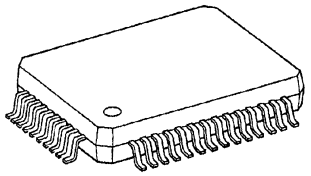
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA1270BFG

PAL / NTSC VIDEO CHROMA AND
SYNC PROCESSING SYSTEM FOR PIP / POP / PAP

TA1270BFG is a PAL / NTSC color TV signal processor IC suitable for PIP / POP / PAP. The IC integrates video, chroma and sync processor circuits. It comes in a 48pin flat package.
The video block uses a chroma trap, the chroma block a PAL / NTSC automatic identifier circuit, and the sync processor block a 50 / 60 Hz automatic identifier circuit. The PAL demodulator circuit contains a baseband signal processor, making the circuit adjustment free.
The TA1270BFG incorporates an I^2C bus, enabling control to be set via the bus line.



QFP48-P-1014-0.80

Weight: 0.83 g (Typ.)

FEATURES

Video block

- Chroma trap
- Y delay line
- Sub contrast adjustment (±3 dB)

CHROMA block

- UV / CbCr demodulation for NTSC ; UV demodulation for PAL
- Tint control
- PAL demodulation baseband signal processing
- PAL / NTSC automatic identification
- Sub color adjustment (±3 dB)

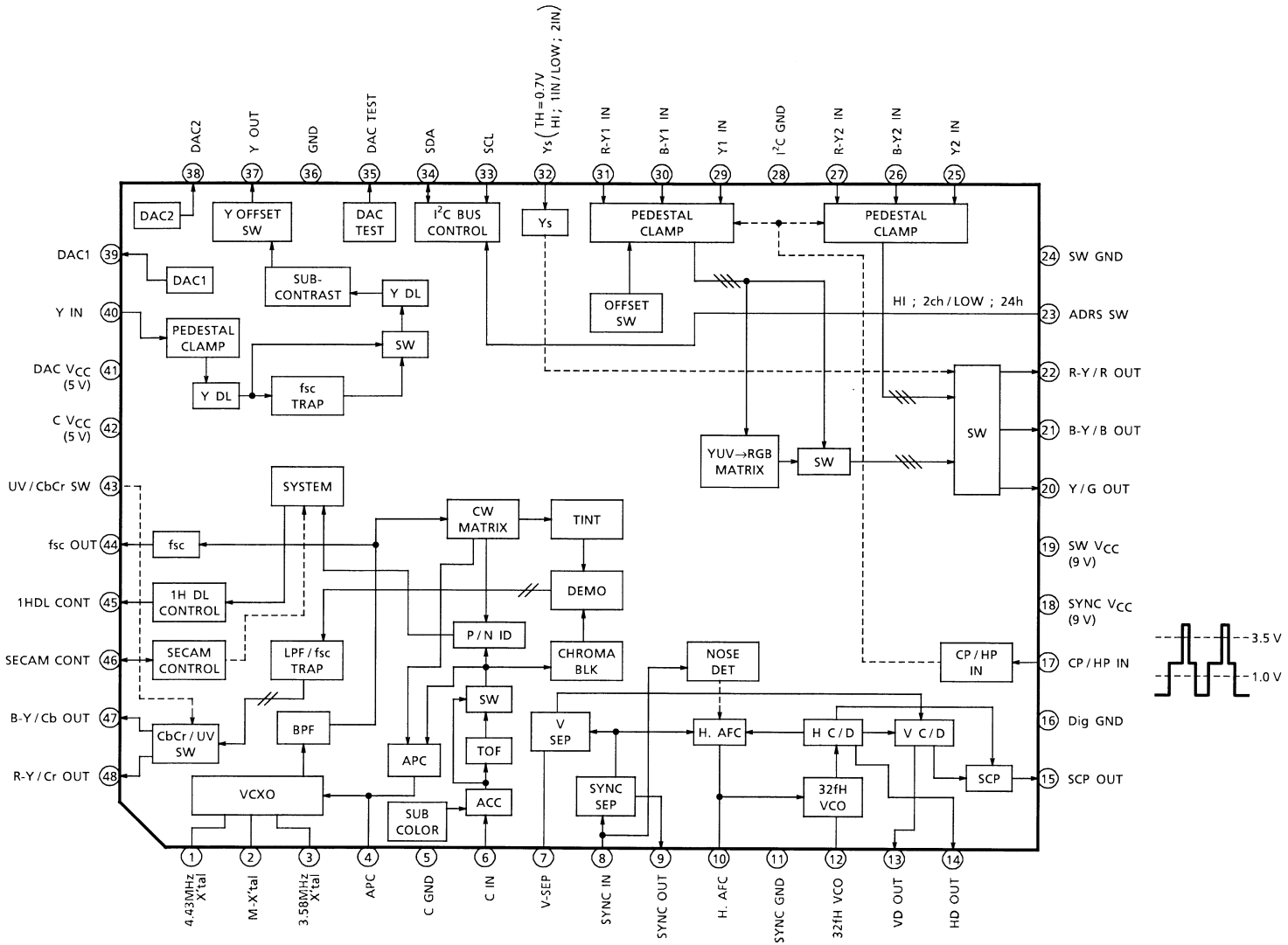
Sync processor block

- High-performance sync separator circuit
- Adjustment-free horizontal and vertical oscillator circuit using count down method
- 50 / 60 Hz automatic identifier circuit

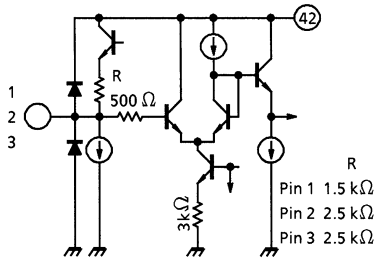
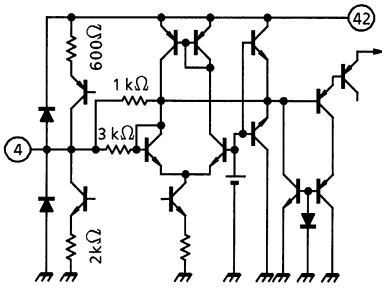
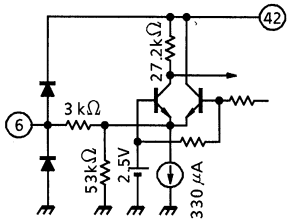
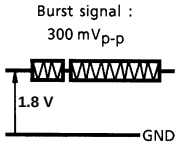
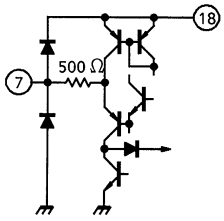
Switch block

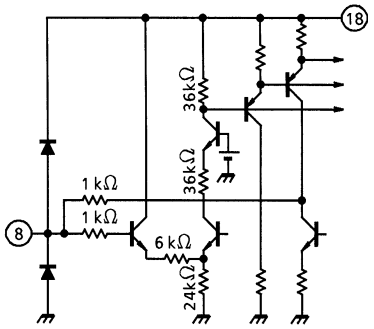
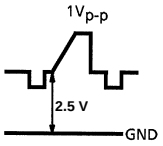
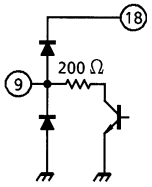
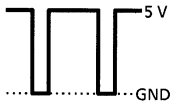
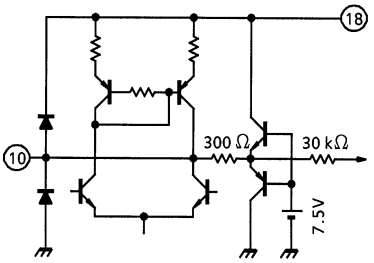
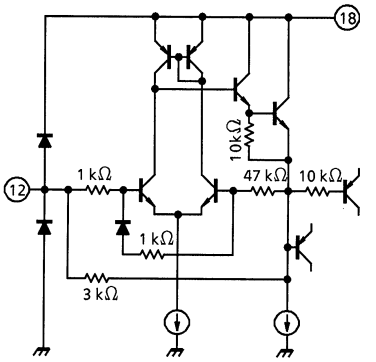
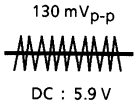
- High-speed switcher circuit
- YUV or RGB input
- Built-in RGB matrix circuit
- YUV or RGB output

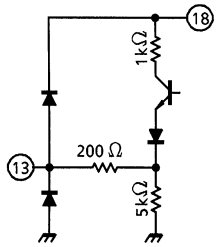
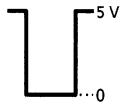
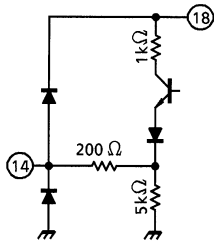
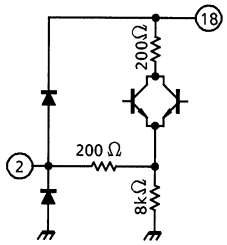
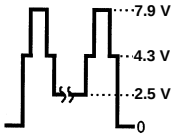
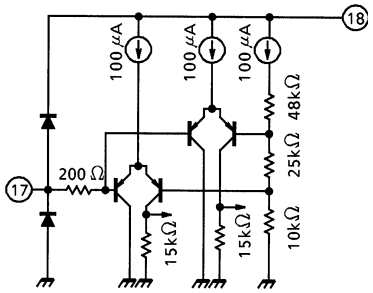
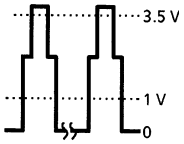
BLOCK DIAGRAM

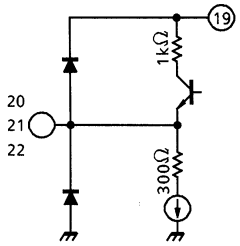
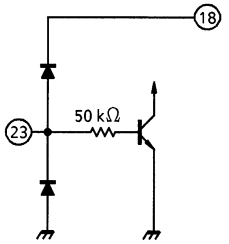
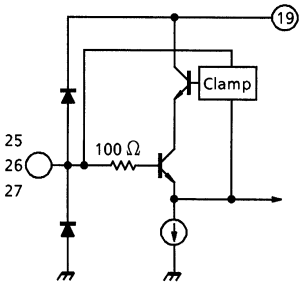
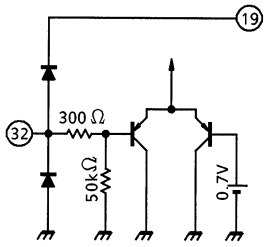


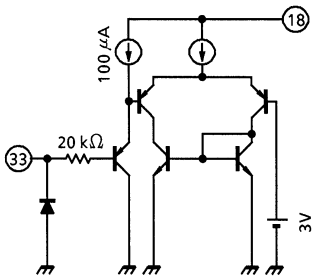
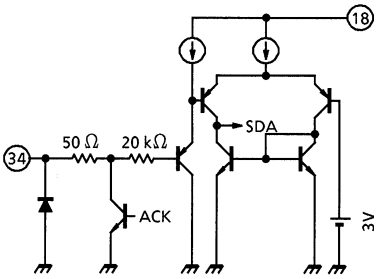
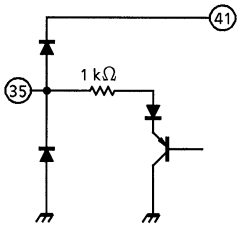
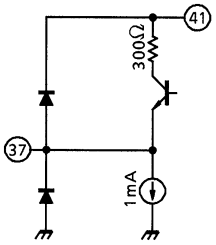
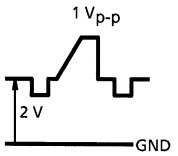
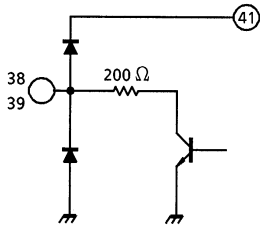
PIN FUNCTION

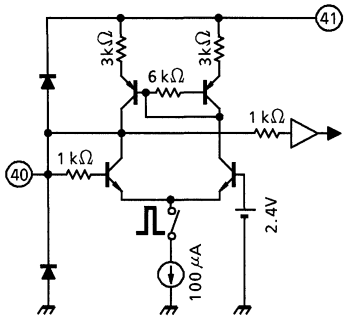
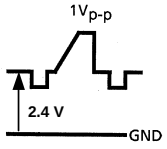
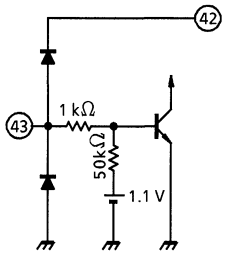
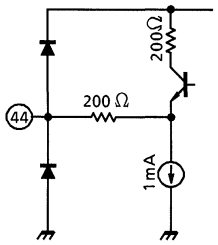
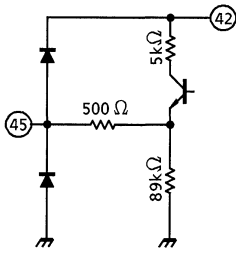
PIN No.	PIN NAME	FUNCTION	INTERFACE	INPUT / OUTPUT SIGNAL
1 2 3	X'tal-1 X'tal-2 X'tal-3	Connect crystal. Serial capacitance can vary oscillator frequency f_0 ; parallel capacitance can vary oscillator adjustment range.		DC 4.0 V 90 mV_{p-p}
4	APC filter	Connect APC filter for CHROMA demodulation. The voltage of this pin determines the VCXO oscillator frequency.		DC
5	C GND	CHROMA processor GND pin	—	—
6	CHROMA input	CHROMA input pin. Input CHROMA signal after Y / C separation.		
7	V-SEP	Connect vertical sync separation filter.		DC 6.4 V

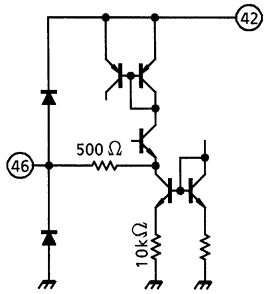
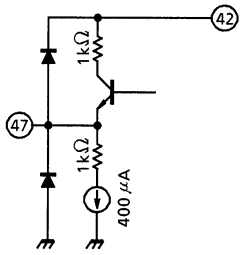
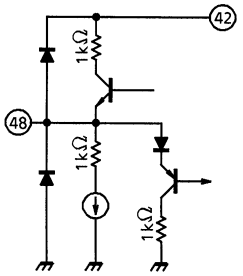
PIN No.	PIN NAME	FUNCTION	INTERFACE	INPUT / OUTPUT SIGNAL
8	Sync input	Sync separator circuit input pin. Input via the clamp capacitor.		
9	Sync output	Outputs sync signal separated using the sync separator circuit. Open collector output. Connect a pull-up resistor.		
10	AFC filter	Connect a horizontal AFC filter. The voltage of this pin determines the horizontal output frequency.		DC
11	SYNC GND	Sync processor GND pin	—	—
12	32 fH VCO	Connect a ceramic oscillator for horizontal oscillation. Use a CSBLA503KECZF30 oscillator manufactured by Murata Mfg Co., Ltd.		

PIN No.	PIN NAME	FUNCTION	INTERFACE	INPUT / OUTPUT SIGNAL
13	VP output	Vertical pulse output pin		
14	HD output	Outputs HD pulse processed by the AFC. HD output phase or pulse width can be changed by bus setting.		
15	SCP output	Outputs sand castle pulse (SCP). The output signals are clamp pulse, horizontal blanking pulse, and vertical blanking pulse. The minimum load resistance is 3 kΩ.		
16	Dig GND	Logic block GND pin	—	—
17	CP / HP input	Input pin for CP / HP pulse used to operate the SW circuit. CP is used as clamp pulse ; HP as blanking pulse.		
18 19	SYNC V_{CC} SW V_{CC}	V_{CC} pins for sync processor block and SW block. Connect 9 V (Typ.).	—	—

PIN No.	PIN NAME	FUNCTION	INTERFACE	INPUT / OUTPUT SIGNAL
20 21 22	Y / G output B-Y / B output R-Y / R output	Output Y / B-Y / R-Y or R / G / B. YUV / RGB output is switched by bus setting.		
23	ADRS SW	Pin used to switch slave addresses. GND — 24H, V_{CC} — 2CH		2CH —— 0.7 V 24H —— GND
24	SW GND	Switch block GND pin	—	—
25 26 27	Y2 input B-Y2 input R-Y2 input (YUV2)	Y2 / B-Y2 / R-Y2 (YUV2 input) or R2 / G2 / B2 input pin. Input via capacitor used for clamp operation.		
28	I^2C GND	I^2C block GND pin	—	—
29 30 31	Y1 input B-Y1 input R-Y1 input (YUV1)	Y1 / B-Y1 / R-Y1 (YUV1 input) or R1 / G1 / B1 input pin. Input via capacitor used for clamp operation.	Same as those for pins 25, 26 and 27	
32	Ys	High-speed switch for switching input pins 25, 26, and 27 (YUV2) and input pins 29, 30, and 31 (YUV1). The threshold is 0.7 V.		YUV1 —— 0.7 V YUV2 —— GND

PIN No.	PIN NAME	FUNCTION	INTERFACE	INPUT / OUTPUT SIGNAL
33	SCL	I^2C Bus SCL pin		—
34	SDA	I^2C Bus SDA pin		—
35	DAC TEST	DAC monitor pin for IC shipping inspection.		—
36	GND	GND pin	—	—
37	Y output	Outputs Y signal which passed fsc trap (trap is set on or off by Bus) and Y delay line circuit.		
38 39	DAC2 DAC1	1 bit DAC output pins		—

PIN No.	PIN NAME	FUNCTION	INTERFACE	INPUT / OUTPUT SIGNAL
40	Y input	Composite video signal or Y signal input pin. Input via the clamp capacitor.		
41 42	DAC V_{CC} C V_{CC}	V_{CC} pins for DAC block and CHROMA processing block. Connect 5 V (Typ.).	—	—
43	UV / CbCr SW	UV / CbCr demodulation switch. OPEN —— UV GND —— CbCr CbCr demodulation is effective for NTSC only.		UV —— 0.7 V CbCr —— 0
44	fsc output	Outputs crystal oscillator fsc. The pin voltage goes high only when 3.58NTSC is received.		AC ; 0.6 V_{p-p} DC ; 3.58NTSC ———3.2 V OTHERS ———1.6 V
45	1HDL CONT	Outputs PAL / SECAM / NTSC identification result. Adjust to DC and connect output to 1H DL IC.		4.3 V ; PAL 2.5 V ; SECAM 0 V ; NTSC

PIN No.	PIN NAME	FUNCTION	INTERFACE	INPUT / OUTPUT SIGNAL
46	SECAM CONT	I / O pin used to control SECAM demodulator IC. If 250 μA or more flows from this pin, SECAM is determined.		At PAL / NTSC : 3.7 V At SECAM (Black and white) : 0.7 V
47	B-Y / Cb output	Outputs B-Y (U) signal or Cb signal. Incorporates LPF to reject carrier.		Pedestal level: 2.4 V
48	R-Y / Cr output	Outputs R-Y (V) signal or Cr signal. Incorporates LPF to reject carrier. Pulling up the pin with 10 kΩ monitors CHROMA signal after ACC and TOF circuits (before demo input).		R-Y output Pedestal level: 2.7 V Cr output Pedestal level: 2.5 V

BUS CONTROL MAP

Write data
Slave address : 24H (00100100) pin 23-GND or 2CH (00101100) pin 23-V_{CC}

SUB ADDRESS	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	POWER-ON INITIAL VALUE MSB	LSB
00	TINT							DAC1	1000	0000
01	TOF-f0			TOF-Q			Y-DL	P / N-ID	1000	0000
02	SUB CONTRAST					C-TRAP	HD-PHS	DAC2	1000	0000
03	SUB COLOR					COLOR SYSTEM			1000	0000
04	Y BLACK LEVEL ADJ.				SW-OFT	V-FREQ / AFC-G			1000	0000
05	R-Y BLACK LEVEL ADJ.						GP-PHS	Y-OFST	1000	0000
06	B-Y BLACK LEVEL ADJ.						OUTPUT MODE		1000	0000

Read data
Slave address : 25H (00100101) pin 23-GND or 2DH (00101101) pin 23-V_{CC}

	D7	D6	D5	D4	D3	D2	D1	D0
0	PORET	COLOR SYSTEM		X'tal		V-FREQ	V-STD	H-LOCK
1	1	COLOR SYSTEM		X'tal		N-DET	U2 / V2-IN	Y2-IN

BUS CONTROL FUNCTION

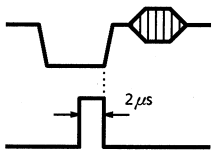
Write function

PARAMETER	DESCRIPTION	POWER-ON INITIAL VALUE
TINT	Adjusts hue. −32°~+32°	0°
DAC1 / 2	Controls 1 bit DAC. 0 : LOW, 1 : HIGH	LOW
TOF-f0	Switches TOF peak frequency. (000) : TOF OFF, (001) : 0.8 fsc, (111) : 1.5 fsc	(100) CENTER
TOF-Q	Switches TOF Q ; (000) : 0.6~(111) : 1.2	MIN
Y-DL	Switches Y-DL delay time ; (0) : OFF, (1) : ON (+80 ns)	OFF
P / N ID	Switches PAL / NTSC identification sensitivity. (0) : LOW (Digital comb filter in use), (1) : Normal	LOW
SUB CONTRAST	Adjusts sub contrast ; −3.0 dB~+3.0 dB	0dB
C-TRAP	Switches CHROMA trap ; (0) : OFF, (1) : ON	OFF
HD-PHS	Switches HD output pulse phase ; (0) : PHASE-1, (1) : PHASE-2 (SCP)	PHASE-1
SUB COLOR	Sub color ; −5.3 dB~0 dB~+3.0 dB	0dB
COLOR SYSTEM	Switches color system. (000) : AUTO / (001) : 3NTSC / (010) : 4NTSC (011) : PAL / (100) : M-PAL / (101) : N-PAL (101) : N-PAL / (110) : SECAM / (111) : TRINORMA	(000) AUTO
Y BLACK LEVEL ADJ.	Adjusts Y black level ; −75 mV~+65 mV	(1000)
SW-OFT	Switches SW output offset ; Y : −10 IRE & UV : +60 mV ON / OFF (0) : OFF, (1) : ON	OFF

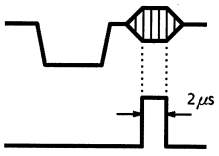
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<tr><th>PARAMETER</th><th>DESCRIPTION</th><th>POWER-ON INITIAL VALUE</th></tr>
<tr><td>V-FREQ / AFC-G</td><td>Controls vertical frequency and horizontal free run.
<table>
<tr><th></th><th>V FREQUENCY</th><th>AFC-Gain</th><th>V pull-in range</th></tr>
<tr><td>(000)</td><td>AUTO1
(50 / 60 Hz MODE)</td><td>Normal</td><td>224.5H~353H</td></tr>
<tr><td>(001)</td><td>60 Hz MODE</td><td>Normal</td><td>224.5H~297H</td></tr>
<tr><td>(010)</td><td>262.5H forced</td><td>Free run</td><td>—</td></tr>
<tr><td>(011)</td><td>312.5H forced</td><td>Free run</td><td>—</td></tr>
<tr><td>(100)</td><td>AUTO2
(50 / 60 Hz MODE)</td><td>Normal</td><td>32.5H~353H</td></tr>
<tr><td>(101)</td><td>60 Hz mode</td><td>Normal</td><td>32.5H~297H</td></tr>
<tr><td>(110)</td><td>262H forced</td><td>Free run</td><td>—</td></tr>
<tr><td>(111)</td><td>312H forced</td><td>Free run</td><td>—</td></tr>
</table></td><td>(000)
AUTO1</td></tr>
<tr><td>B-Y / R-Y
BLACK LEVEL ADJ.</td><td>Adjusts B-Y / R-Y black level ; −68 mV~+68 mV</td><td>(100000)
CENTER</td></tr>
<tr><td>GP-PHS</td><td>Switches gate pulse phase ; (0) : Normal , (1) : −200 ns (Ahead)</td><td>Normal</td></tr>
<tr><td>Y-OFST</td><td>Switches Y output offset ; +10 IRE : ON / OFF
(0) : OFF, (1) : ON</td><td>OFF</td></tr>
<tr><td>OUTPUT MODE</td><td>Switches SW output mode.
Switches YUV / RGB (matrix coefficient) output.
(00) : Y / U / V, (01) : RGB / PAL, (10) : RGB / NTSC1,
(11) : RGB / NTSC2</td><td>(00)
Y / U / V</td></tr>
</table>

HD-PHS

(0) : PHASE-1



(1) : PHASE-2 (SCP)



Read function

PARAMETER	DESCRIPTION
PORSET	Power-on reset. (0) : RESISTER PRESET, (1) NORMAL
COLOR SYSTEM	Color system. Received system (ID, no ID) (00) : B / W, (01) : SECAM, (10) : PAL, (11) : NTSC
X'tal	X'tal mode (00) : −, (01) : 4.43 (N), (10) : M, (11) : 3.58
V-FREQ	Vertical frequency ; (0) : 50 Hz, (1) : 60 Hz
V-STD	Decides vertical standard ; (0) : STANDARD, (1) : NON-STANDARD
H-LOCK	Decides horizontal lock ; (0) : LOCK, (1) : UN-LOCK
N-DET	Decides noise level ; (0) : Low, (1) : High
Y2-IN, U2 / V2-IN	Outputs self diagnosis result. ; (0) : NG, (1) : OK

I²C BUS COMMUNICATION AND RECEPTION METHODS

Slave address : Slave addresses can be changed using the pin 23 voltage.

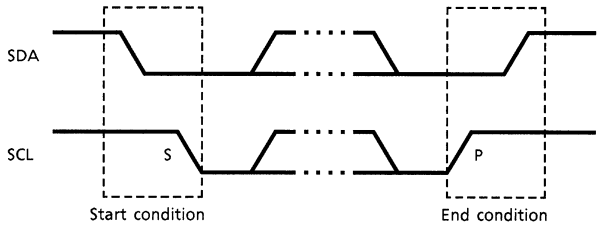
24H (Pin 23-GND)

A_6	A_5	A_4	A_3	A_2	A_1	A_0	W / R
0	0	1	0	0	1	0	0 / 1

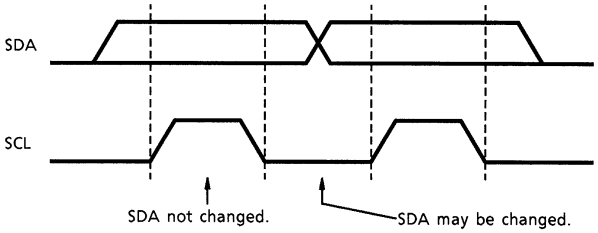
2CH (Pin 23-V_{CC})

A_6	A_5	A_4	A_3	A_2	A_1	A_0	W / R
0	0	1	0	1	1	0	0 / 1

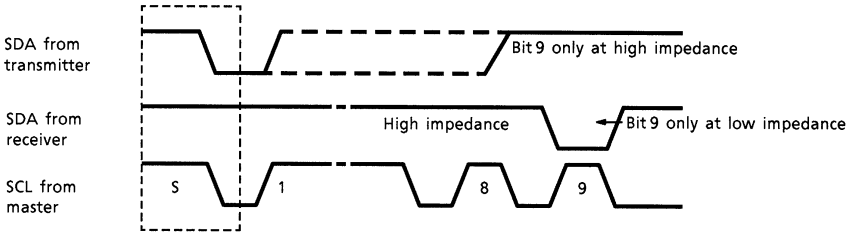
Start and end conditions



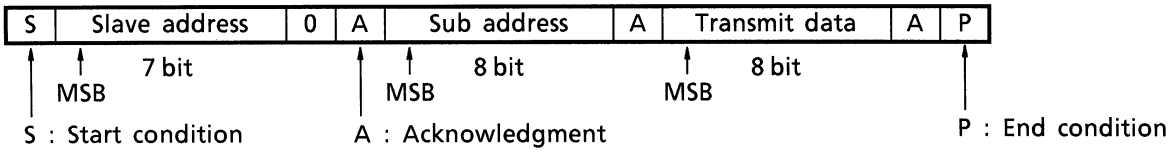
Bit transmission



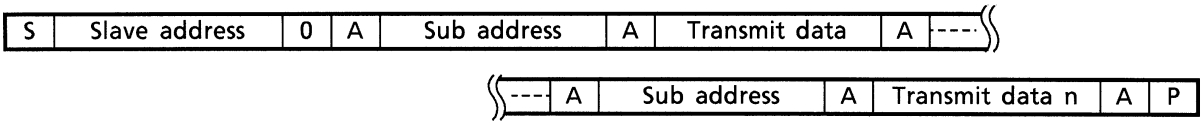
Acknowledgment



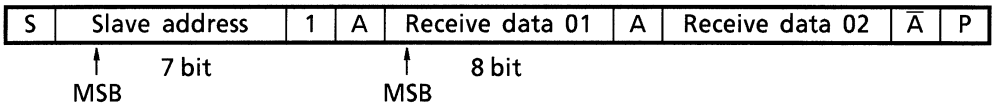
Data transmit format 1



Data transmit format 2



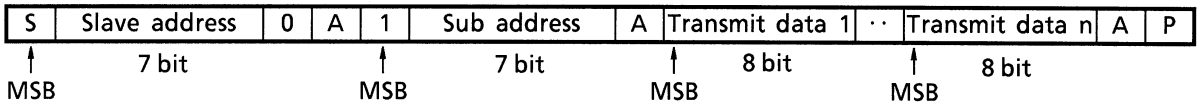
Data receive format



At data reception, the master transmitter changes to the receiver immediately after the first acknowledgment and the slave receiver changes to the transmitter.
The end condition is always generated by the master.

(* important) The data read from THIS IC should always be completed in whole two words, not one word, otherwise the IICBUS may cause error.

Option data transmit format



This transmission method automatically increments sub addresses starting from the specified sub address and sets data.

I^2C BUS Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Low level input voltage	V_{IL}	0	—	1.5	V
High level input voltage	V_{IH}	3.0	—	Vcc	V
Low level output voltage at 3 mA sink current	V_{OL1}	0	—	0.4	V
Input current each I/O pin with an input voltage between 0.1 VDD and 0.9 VDD	I_i	−10	—	10	μA
Capacitance for each I/O pin	C_i	—	—	10	pF
SCL clock frequency	f_{SCL}	0	—	100	kHz
Hold time START condition	$t_{HD;STA}$	4.0	—	—	μs
Low period of SCL clock	t_{LOW}	4.7	—	—	μs
High period of SCL clock	t_{HIGH}	4.0	—	—	μs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	—	—	μs
Data hold time	$t_{HD;DAT}$	350	—	—	ns
Data set-up time	$t_{SU;DAT}$	250	—	—	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	—	—	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	—	—	μs

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CCmax}	12	V
Input Pin Voltage	V_{in}	GND − 0.3 to V_{CC} + 0.3	V
Power Dissipation	PD (Note 1)	844	mW
Power Dissipation Reduction Rate	1 / θja	6.75	mW / °C
Operating Temperature	T_{opr}	−20~65	°C
Storage Temperature	T_{stg}	−55~150	°C

Note 1: See figure below.
Note 2: Since the device is susceptible to surge, handle with care.
Note 3: This IC is not proof enough against a strong E-M field by CRT which may cause function errors and / or poor characteristics.
Keeping the distance from CRT to the IC longer than 20 cm, or if cannot, placing shield metal over the IC, is recommended in an application.

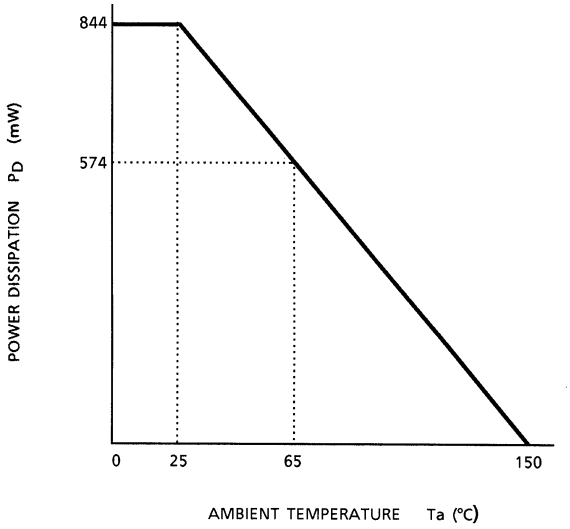


Fig. Power dissipation temperature reduction curve

OPERATING CONDITION

CHARACTERISTIC	CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage	Pins 18, 19	8.5	9.0	9.5	V
	Pins 41, 42	4.7	5.0	5.3	
Pin 40 Y Input Signal Level	White 100%. Including sync signal	0.9	1.0	1.1	V_{p-p}
Pin 6 Chroma Input Signal Level	TOF : OFF, burst level	200	300	400	mV_{p-p}
	TOF : ON, burst level	100	200	300	
Pin 8 Sync Signal Input level	White 100%. Including sync signal	0.9	1.0	1.1	V_{p-p}
Pin 9 Sink Current	—	—	0.5	1.0	mA

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, SYNC / SW V_{CC} = 9 V, DAC / C V_{CC} = 5 V, Ta = 25°C ± 3°C)

Current dissipation

PIN No.	PIN NAME	SYMBOL	TEST CIR-CUIT	MIN	TYP.	MAX	UNIT
18	SYNC V_{CC}	I_{CC1}	—	13	19	25	mA
19	SW V_{CC}	I_{CC2}	—				
41	DAC V_{CC}	I_{CC3}	—	24	35	46	
42	C V_{CC}	I_{CC4}	—				

PIN VOLTAGE

PIN No.	PIN NAME	SYMBOL	TEST CIR-CUIT	MIN	TYP.	MAX	UNIT
1	4.43 MHz X'tal	V1	—	3.60	4.00	4.40	V
2	N-X'tal	V2	—	3.60	4.00	4.40	
3	3.58 MHz X'tal	V3	—	3.60	4.00	4.40	
6	C input	V6	—	1.30	1.75	2.20	
7	V-SEP	V7	—	5.10	5.50	5.90	
12	32 fH VCO	V12	—	5.30	5.70	6.10	
20	Y / G output	V20	—	3.90	4.30	4.70	
21	B-Y / B output	V21	—	3.90	4.30	4.70	
22	R-Y / R output	V22	—	3.90	4.30	4.70	
25	Y2 input	V25	—	5.30	5.70	6.10	
26	B-Y2 input	V26	—	5.30	5.70	6.10	
27	R-Y2 input	V27	—	5.30	5.70	6.10	
29	Y1 input	V29	—	5.30	5.70	6.10	
30	B-Y1 input	V30	—	5.30	5.70	6.10	
31	R-Y1 input	V31	—	5.30	5.70	6.10	
37	Y output	V37	—	1.60	2.00	2.40	
40	Y input	V40	—	2.10	2.50	2.90	

AC CHARACTERISTICS

Video block

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Y Input Clamp Voltage	VYI	—	Y input-AC GND	2.1	2.4	2.8	V
Y Input to Y Output AC Gain	GYs	—	(Note V1)	−0.13	0	0.13	dB
	GYt	—		−0.13	0	0.13	
Y Input to Y Output Frequency Bandwidth	GfY	—	−3 dB	8	10	—	
TRAP Filter Characteristic	GTC3	—	fO = 3.579545 MHz	—	−25	−13	
	GTC4	—	fO = 4.433619 MHz	—	−25	−13	
Y Input Dynamic Range	VD	—	Sub contrast : min.	1.3	1.6	—	V_{p-p}
Y Input to Y Output Transmission Characteristic 1	TYa	—	Black and white, Y-DL : OFF	255	295	335	ns
	TYb	—	Black and white, Y-DL : ON	335	375	415	
Y Input to Y Output Transmission Characteristic 2	TY3	—	3.58 NTSC, Y-DL : OFF	255	295	335	
	TY4	—	4.43 PAL, Y-DL : OFF	255	295	335	
	TYS	—	SECAM, Y-DL : OFF	445	495	535	
Sub Contrast Range	ΔVSU+	—	20 ℓog (Data max. / data center)	2.5	3.0	3.5	dB
	ΔVSU−	—	20 ℓog (Data max. / data center)	−3.5	−3.0	−2.5	
Y Output Offset Amount	VYO	—	(Note V2)	60	95	130	mV

Chroma block

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
ACC Characteristics	F600	—	(Note C1)	300	360	420	mV_{p-p}
	F300	—		300	360	420	
	F30	—		300	360	420	
	F10	—		170	245	290	
	A	—		0.95	1.00	1.05	—
Sub Color Control Characteristic	es+	—	20 ℓog (Data max. / data center)	2.0	3.0	4.0	dB
	es−	—	20 ℓog (Data max. / data center)	−7.4	−5.3	−2.4	
APC Frequency Control Sensitivity	β3	—	(Note C2)	0.5	1.65	2.2	Hz / mV
	β4	—		0.5	1.65	2.2	
	βM	—		0.5	1.65	2.2	
APC Pull-In Range	f3ph	—	At 3.58 NTSC, upper side	250	600	2000	Hz
	f3pl	—	At 3.58 NTSC, lower side	−2000	−1400	−250	
	f4ph	—	At 4.43 PAL, upper side	250	600	2000	
	f4pl	—	At 4.43 PAL, lower side	−2000	−950	−250	
	fMph	—	At M-PAL, upper side	250	600	2000	
	fMpl	—	At M-PAL, lower side	−2000	−1100	−250	
APC Hold Range	f3hh	—	At 3.58 NTSC, upper side	250	600	2000	
	f3hl	—	At 3.58 NTSC, lower side	−2000	−1400	−250	
	f4hh	—	At 4.43 PAL, upper side	250	600	2000	
	f4hl	—	At 4.43 PAL, lower side	−2000	−950	−250	
	fMhh	—	At M-PAL, upper side	250	600	2000	
	fMhl	—	At M-PAL, lower side	−2000	−1100	−250	
fsc Free-Run Frequency	fO3	—	fO = 3.579545 MHz	−200	0	200	
	fO4	—	fO = 4.433619 MHz	−200	0	200	
	fOM	—	fO = 3.575611 MHz	−200	0	200	
fsc Output Amplitude	f3c	—	At 3.58 NTSC input	0.45	0.75	0.95	V_{p-p}
	f4c	—	At 4.43 PAL input	0.50	0.65	0.80	
	fMc	—	At M-PAL input	0.45	0.75	0.95	
fsc Output DC Level	V44a	—	At 3.58 NTSC input	2.9	3.2	3.5	V
	V44b	—	At other than 3.58 NTSC input	1.15	1.55	1.75	
Color Difference Output Level	vRNUV	—	3.58 NTSC − UV mode, B : C = 1 : 1	300	360	420	mV_{p-p}
	vBNUV	—		280	340	400	
	vRNCbCr	—	3.58 N−CbCr mode, B : C = 1 : 1	215	272	320	
	vBNCbCr	—		280	340	400	
	vRP	—	4.43 PAL, B : C = 1 : 1	315	380	440	
	vBP	—		315	380	440	
Relative Amplitude	vR / BUV	—	3.58 NTSC − UV mode	0.94	1.00	1.15	—
	vR / BCbCr	—	3.58 N − CbCr mode	0.94	1.00	1.15	
	vR / BPAL	—	4.43 PAL	0.94	1.00	1.15	

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Demodulation Angle	θB_{NUV}	—	3.58 NTSC − UV mode, TINT ; center	0	3	8	°
	θR_{NUV}	—		90	93	96	
	θB_{NCbCr}	—	3.58 N−CbCr mode, TINT ; center	0	3	8	
	θR_{NCbCr}	—		90	93	96	
	θB_P	—	4.43 PAL	−3.0	0	5.5	
	θR_P	—		87	90	95	
Color Difference Output Tint Adjustment Characteristic	θUV_{MAX}	—	UV Mode, TINT ; max.	29	32	35	°
	θUV_{MIN}	—	UV Mode, TINT ; min.	−35	−32	−29	
	$\theta CbCr_{MAX}$	—	CbCr Mode, TINT ; max.	29	32	35	
	$\theta CbCr_{MIN}$	—	CbCr Mode, TINT ; min.	−35	−32	−29	
Residual Carrier Level	ve	—	fsc level	—	1.9	4.0	mV_{p-p}
Residual Harmonic Level	vHe	—	(fsc × 2) level	—	1.9	4.0	
1HDL CONT Output DC Level Change	VDLP	—	PAL signal input	4.0	4.3	4.6	V
	VDLS	—	SECAM signal input	2.2	2.5	2.8	
	VDLN	—	NTSC signal input	0	0.1	0.2	
Sand Castle Pulse Wave High Value	SCH	—	CP level	7.6	7.9	8.2	
	SCM	—	HP level	4.05	4.3	4.55	
	SCL	—	VP level	2.25	2.5	2.75	
SECAM ID Output DC Level	SEN	—	(Note C3)	3.4	3.7	4.0	
	SEP	—		3.4	3.7	4.0	
	SES	—		0.4	0.7	1.0	
NTSC Ident Sensitivity	vNCL	—	(Note C4)	2.0	2.9	4.0	mV_{p-p}
	vNCH	—		0.5	1.8	4.0	
	vNBL	—		1.7	2.7	5.8	
	vNBH	—		0.3	1.6	3.6	
PAL Ident Sensitivity	vPCL	—	(Note C5)	1.5	4.5	6.5	
	vPCH	—		1.0	2.8	3.1	
	vPBL	—		1.5	4.1	6.1	
	vPBH	—		1.0	2.5	4.5	
TOF Characteristic	GFH3	—	(Note C6)	14.0	16.5	19.0	dB
	GFC3	—		12.5	15.0	17.5	
	GFL3	—		10.5	13.0	15.5	
	GFH4	—		15.5	18.0	20.5	
	GFC4	—		14.0	16.5	19.0	
	GFL4	—		12.0	14.5	17.0	

Switch block

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Y Gain (Through Mode)	GY1	—	(Note S1)	−1.0	0	1.0	dB
	GY2	—		−1.0	0	1.0	
Color Difference Gain (Through Mode)	GBY1	—	(Note S2)	−1.0	0	1.0	
	GRY1	—		−1.0	0	1.0	
	GBY2	—		−1.0	0	1.0	
	GRY2	—		−1.0	0	1.0	
Y Gain (Matrix Mode)	GY1GP	—	(Note S3)	−1.0	0	1.0	
	GY1GN1	—		−1.0	0	1.0	
	GY1GN2	—		−1.0	0	1.0	
	GY1BP	—		−1.0	0	1.0	
	GY1BN1	—		−1.0	0	1.0	
	GY1BN2	—		−1.0	0	1.0	
	GY1RP	—		−1.0	0	1.0	
	GY1RN1	—		−1.0	0	1.0	
	GY1RN2	—		−1.0	0	1.0	
Color Difference Gain (Matrix Mode)	GGYP	—	(Note S4)	−0.6	0.6	1.6	
	GGYN1	—		−0.6	0.6	1.6	
	GGYN2	—		−1.0	0	1.0	
	GBYP	—		8.9	9.9	10.9	
	GBYN1	—		7.5	8.5	9.5	
	GBYN2	—		7.5	8.5	9.5	
	GRYP	—		3.9	4.9	5.9	
	GRYN1	—		5.6	6.6	7.6	
	GRNY2	—		4.2	5.2	6.2	
R-Y Relative Phase	θRP	—	RGB / PAL Mode	87	90	93	°
	θRN1	—	RGB / NTSC1 Mode	89	92	95	
	θRN2	—	RGB / NTSC2 Mode	93	96	99	
R-Y Relative Amplitude	vPR / B	—	RGB / PAL Mode	0.53	0.56	0.59	—
	vN1R / B	—	RGB / NTSC1 Mode	0.77	0.80	0.83	
	vN2R / B	—	RGB / NTSC2 Mode	0.65	0.68	0.71	
G-Y Relative Phase	θGP	—	RGB / PAL Mode	234	237	240	°
	θGN1	—	RGB / NTSC1 Mode	237	240	243	
	θGN2	—	RGB / NTSC2 Mode	237	240	243	
G-Y Relative Amplitude	vPG / B	—	RGB / PAL Mode	0.31	0.34	0.37	—
	vN1G / B	—	RGB / NTSC1 Mode	0.37	0.40	0.43	
	vN2G / B	—	RGB / NTSC2 Mode	0.34	0.37	0.40	

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Switch Output Switch Offset	ΔVY	—	—	—	0	50	mV
	ΔVB	—	—	—	0	50	
	ΔVR	—	—	—	0	50	
Switch Output Offset Amount	ΔVYO	—	(Note S5)	−85	−75	−65	
	ΔVBO	—		61	68	75	
	ΔVRO	—		61	68	75	
Y / G Output Black Level Range	ΔVYB+	—	(Note S6)	59	65	71	
	ΔVYB−	—		−82	−75	−68	
	ΔVYO+	—		59	65	71	
	ΔVYO−	—		−82	−75	−68	
B-Y / G Output Black Level Range	ΔVBB+	—	(Note S7)	61	68	75	
	ΔVBB−	—		−75	−68	−61	
	ΔVBO+	—		61	68	75	
	ΔVBO−	—		−75	−68	−61	
R-Y / G Output Black Range	ΔVRB+	—	(Note S8)	61	68	75	
	ΔVRB−	—		−75	−68	−61	
	ΔVRO+	—		61	68	75	
	ΔVRO−	—		−75	−68	−61	
Smoothing Level	VYSM	—	Blanking period voltage	4.0	4.3	4.6	V
	VBSM	—		4.0	4.3	4.6	
	SRSM	—		4.0	4.3	4.6	
Switch Output Dynamic Range	DTH	—	Through mode	1.5	2.3	—	V_{p-p}
	DMT	—	Matrix mode	0.9	1.2	—	
Inter-Input Crosstalk	GCR	—	Crosstalk between inputs	—	−50	−40	dB

Sync processor block

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
32 fH VCO Oscillation Start Voltage	V_{VCO}	—	Pin 18 voltage	3.7	4.0	4.3	V
Horizontal Free-Run Frequency	f50HO	—	AUTO mode	15.455	15.625	15.795	kHz
	f60HO	—	60 Hz mode	15.564	15.734	15.904	
Horizontal Oscillation Frequency Range	fHmin	—	Pin 10 ; 10 kΩ−V_{CC}	14.700	15.000	15.300	
	fHmax	—	Pin 10 ; 10 kΩ−GND	16.500	16.700	16.900	
Horizontal Oscillation Frequency Control Sensitivity	βH	—	—	2.3	2.8	3.3	kHz / V
Horizontal Sync Phase	Sph1	—	(Note D1)	0.30	0.40	0.50	μs
	Sph2	—		0.11	0.21	0.31	
External Pulse Input Threshold (Pin 17)	CPV17	—	Clamp pulse	3.2	3.5	3.8	V
	HPV17	—	Horizontal blanking	0.7	1.0	1.3	
Horizontal Blanking Start Phase	HPs	—	(Note D2)	4.1	4.4	4.7	μs
Horizontal Blanking Width	HPw	—		11.0	11.5	12.0	
Gate Pulse Start Phase	GPs	—	(Note D3)	2.8	3.0	3.2	
Gate Pulse Width	GPw	—		1.8	2.0	2.2	
Horizontal Blanking Pulse Start Phase	HPs	—	(Note D4)	3.8	4.0	4.2	μs
Horizontal Blanking Pulse Width	HPw	—		9.5	10.0	10.5	
HD Output Start Phase	HDs	—	(Note D5)	−0.2	0	0.2	
HD Output Pulse Width	HDw	—		1.6	1.8	2.0	
HD Amplitude	VHD	—		4.7	5.0	5.3	V
Vertical Blanking Pulse Start Phase	VP50s1	—	(Note D6)	46	48	50	μs
	VP60s1	—		46	48	50	
Vertical Blanking Pulse Width	VP50s2	—		—	23	—	H
	VP60s2	—		—	21	—	
Vertical Free-Run Frequency	f50vo	—	AUTO mode (353H)	40	45	50	Hz
	f60vo	—	60 Hz mode (297H)	48	53	58	
Vertical Output Voltage	Vvh	—	Pin 13 high voltage	4.7	5.0	5.3	V
	Vvl	—	Pin 13 low voltage	—	0	0.3	

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Vertical Output Pulse Width	Td	—	(Note D7)	42	44	46	μs
	Tw	—		—	8	—	
Vertical Pull-In Range (1)	fPL1	—		—	224.5	—	
	fPH1	—		—	353	—	
Vertical Pull-In Range (2)	fPL2	—		—	32.5	—	
	fPH2	—	(Note D8)	—	353	—	H
Vertical Pull-In Range (3)	fPL3	—		—	224.5	—	
	fPH3	—		—	297	—	
Vertical Pull-In Range (4)	fPL4	—		—	32.5	—	
	fPH4	—		—	297	—	
Address Switch Threshold Value	Vadd	—	Pin 23 voltage	0.5	0.65	0.8	V

TEST METHODS (Unless otherwise specified, SYNC / SW V_{CC} = 9 V, DAC / C V_{CC} = 5 V, preset bus data, Ta = 25°C ± 3°C)

Video block

NOTE	CHARACTERISTIC	TEST CONDITION								TEST METHOD
		SUB ADDRESS & DATA					SW MODE			
		00	01	02	03	05	SW1	SW2	SW12	
V1	Y Input to Y Output AC Gain	80	80	80 or 84	80	80	B	A	A	(1) Input signal 2 to Y input (Pin 40) and Yin2 input. (f_0 = 100 kHz, picture period amplitude = 0.2 V_{p-p}) (2) Change the sub address (02) data to TRAP-OFF (80h) and TRAP-ON (84h) and perform the following : (3) Measure the picture period amplitude (v37) of the Y output (Pin 37) and determine the gain from Y input. GYs, GYt = 20 log (v37 / 0.2) (GYs ; TRAP-OFF, GYt ; TRAP-ON)
V2	Y Output Offset Amount	80	0	80	80	80 or 81	B	A	A	(1) Input signal 2 to Y input (Pin 40) and Yin2 input. (f_0 = 100 kHz, picture period amplitude = 0.2 V_{p-p}) (2) Set the sub address (01) data to 00 and measure the minimum potential (VYO1) of the Y output (Pin 37) picture period amplitude. (3) Set the sub address (05) data to Y-OFST-ON (81), measure the minimum potential (VYO2) of the Y output picture period amplitude, and determine the difference from VYO1. VYO = VYO2 − VYO1

Chroma block

NOTE	CHARACTERISTIC	TEST CONDITION								TEST METHOD
		SUB ADDRESS & DATA					SW MODE			
		00	01	02	03	05	SW1	—	—	
C1	ACC Characteristics	80	80	80	80	80	B	—	—	(1) Input 3.58-NTSC signal 1 rainbow signal (Burst : chroma = 1 : 1) to the chroma input (Pin 6). (2) Measure the amplitude, F10, F30, F300, and F600, of the B-Y output (Pin 47) when the amplitude of the chroma input signal is set to 10, 30, 300, and 600 mV_{p-p}. (3) Calculate A = F30 / F300.
C2	APC Frequency Control Sensitivity	80	80	80	81 or 83 or 84	80 or 81	B	—	—	(1) Connect the chroma input pin (Pin 6) to GND via a capacitor. (2) Change the sub address (03) data to (81h), (83h), and (84h) and perform the following for each. (3) Connect external power source (V4) to the APC filter (Pin 4). (4) Vary the voltage of external power source (V4) and measure the Fsc output (Pin 44) using a frequency counter. (5) Measure the free-run sensitivity β for the (V4 + 100 mV) near fsc. (3.58NTSC ; β3, 4.43 ; PAL ; 4β ; M-PAL ; βM)
C3	SECAM ID Output DC Level	80	80	80	81 or 83 or 84	80	B	—	—	(1) Connect the chroma input pin (Pin 6) to GND via a capacitor. (2) Change the sub address (03) data to (81h), (83h), and (84h) and measure the output DC level of the SECAM ID (Pin 46). 3.58 NTSC mode (81h) ; SEN 4.43 PAL mode (83h) ; SEP SECAM mode (84h) ; SES
C4	NTSC Ident Sensitivity	80	80 or 81	80	80	80	A	—	—	(1) Input 3.58-NTSC signal 1 rainbow signal (Burst : chroma = 1 : 1) to the chroma input (Pin 6). (2) While monitoring READ BUS “COLOR“, perform the following with BUS “P / N-ID“ data = 1 and 0. (3) Increase the amplitude of the input signal from 0 mV_{p-p} and measure the amplitude at mode change to 3.58 NTSC mode.(Normal (1) ; vNCL, High (0) ; vNCH) (4) Decrease the amplitude of the input signal from 100 mV_{p-p} and measure the amplitude at mode change to 3.58 NTSC mode. (Normal (1) ; vNBL, High (0) ; vNBH)

(Unless otherwise specified, SYNC / SW V_{CC} = 9 V, DAC / C V_{CC} = 5 V, preset bus data, Ta = 25°C ± 3°C)

NOTE	CHARACTERISTIC	TEST CONDITION								TEST METHOD
		SUB ADDRESS & DATA					SW MODE			
		00	01	02	03	05	SW1	—	—	
C5	PAL Ident Sensitivity	80	80 or 81	80	80	80	A	—	—	(1) Input 4.43 PAL signal 1 rainbow signal (Burst : chroma = 1 : 1) to the CHROMA input (Pin 6). (2) While monitoring the READ BUS “COLOR“, perform the following with BUS “P / N-ID“ data = 1 and 0. (3) Increase the amplitude of the input signal from 0 mV_{p-p} and measure the amplitude at mode change to 4.43 PAL mode. (Normal (1) ; vPCL, High (0) ; vPCH) (4) Decrease the amplitude of the input signal from 100 mV_{p-p} and measure the amplitude at mode change to 4.43 PAL mode. (Normal (1) ; vPBL, High (0) ; vPBH)
C6	TOF Characteristics	80	83	80	81 or 83	80	A	—	—	(1) Input f_{sc} signal to the chroma input (Pin 6).(signal amplitude = 10 mV_{p-p}, f01 = 3.579545 MHz,f02 = 4.433619 MHz) (2) Set sub address (01) data to (38h). With f01, set sub address (03) data to (81h) ; with f01, to (83h). Insert a 1.5 kΩ resistor between R-Y output (Pin 48) and V_{CC} (5 V). Monitor R-Y output (Pin 48) and perform the following. (3) Measure the output amplitude with f0 and calculate the gain from the input. (f01 ; GFC3, f02 ; GFC4) (4) Measure the output amplitude with f0 ± 500 kHz and calculate the gain from the input. (f01 + 500 kHz ; GFH3, f01 − 500 kHz ; GFL3, f02 + 500 kHz ; GFH4, f02 − 500 kHz ; GFL4)

Switching block (Unless otherwise specified, SYNC / SW V_{CC} = 9 V, DAC / C V_{CC} = 5 V, preset bus data, Ta = 25°C ± 3°C)

NOTE	CHARACTERISTIC	TEST CONDITION							TEST METHOD
		SUB ADDRESS & DATA			SW MODE				
		00	01	02					
S1	Y Gain (Through Mode)	80	80	80	SW2	SW6	SW8	SW9	(1) Input signal 2 to Yin2 input. (f0 = 100 kHz, picture period amplitude = 0.2 V_{p-p}) (2) Apply DC = 5 V to Ys input (Pin 32). (3) Input signal 2 to Y1 input (Pin 29). (4) Measure the output amplitude of Y / G output (Pin 20) and calculate the gain from the input. (5) Input signal 2 to Y2 input (Pin 25), set Ys input (Pin 32) DC = 0 V, and repeat (3) and (4) above. (Y1~Y / G ; GY1, Y2~Y / G ; GY2)
					A	B or A	—	A or B	
					SW10	SW11	SW14	SW16	
					B	B	A	—	
S2	Color Difference Gain (Through Mode)	80	80	81 or 82 or 83	SW2	SW6	SW8	SW9	(1) Same as (1) and (2) for S1 above. (2) Input signal 2 to B-Y1 input (Pin 30) and input +90° phase signal of signal 2 to R-Y1 input (Pin 30). (3) Measure the amplitude of the B-Y / B output and the R-Y / R output and calculate the gain from the input. (4) Input signal 2 to B-Y2 input (Pin 26) and input +90° phase signal of signal 2 to the R-Y2 input (Pin 27). (5) Set the Ys input pin DC = 0 V and repeat (4) above. (B-Y1~B-Y / B ; GBY1, R-Y1~R-Y / R ; GRY1 B-Y2~B-Y / B ; GBY2, R-Y2~R-Y / R ; GRY2)
					A	A or B	B or A	B or A	
					SW10	SW11	SW14	SW16	
					A or B	A or B	A	—	
S3	Y Gain (Matrix Mode)	80	80	81 or 82 or 83	SW2	SW6	SW8	SW9	(1) Same as (1) and (2) for S1 above. (2) Change the sub address (06) data to PAL (81h), NTSC1 (82h), and NTSC2 (83h), perform the following. (3) Input signal 2 to Y1 input (Pin 29), measure the amplitude of Y / G output, B-Y / B output, R-Y / R output, and calculate the gain from the input. (Y1~Y / G : PAL ; GY1GP, NTSC1 ; GY1GN1, NTSC2 ; GY1GN2 Y1~B-Y / B : PAL ; GY1BP, NTSC1 ; GY1BN1, NTSC2 ; GY1BN2 Y1~R-Y / B : PAL ; GY1RP, NTSC1 ; GY1RN1, NTSC2 ; GY1RN2)
					A	B or A	—	A or B	
					SW10	SW11	SW14	SW16	
					B	B	A	—	

(Unless otherwise specified, SYNC / SW V_{CC} = 9 V, DAC / C V_{CC} = 5 V, preset bus data, Ta = 25°C ± 3°C)

NOTE	CHARACTERISTIC	TEST CONDITION							TEST METHOD
		SUB ADDRESS & DATA			SW MODE				
		00	01	02					
S4	Color Difference Gain (Matrix Mode)	80	83	81 or 82 or 83	SW2	SW6	SW8	SW9	(1) Same as (1) and (2) for S2 above. (2) Change the sub address (05) data to PAL (81h), NTSC1 (82h), and NTSC2 (83h), perform the following. (3) Measure the amplitude of Y / G output, B-Y / B output, R-Y / R output, then calculate the gain from the input. (Y1~Y / G : PAL ; GGYP, NTSC1 ; GGYN1, NTSC2 ; GGYN2 Y1~B-Y / B : PAL ; GBYP, NTSC1 ; GBYN1, NTSC2 ; GBYN2 Y1~R-Y / R : PAL ; GRYP, NTSC1 ; GRYN1, NTSC2 ; GRYN2)
					A	A or B	B or A	B or A	
					SW10	SW11	SW14	SW16	
					A or B	A or B	A	—	
S5	Switch Output Offset Amount	80	80	80	SW2	SW6	SW7	SW8	(1) Input signal 2 to Yin2. (2) Apply DC = 5 V to Ys input (Pin 32). (3) Change the sub address (04) data from (80h) to (88h) and measure DC variation ΔVYO, ΔVBO, and ΔVRO of Y / G output, B-Y / B output, and R-Y / R output picture period.
					A	B	B	B	
					SW14	—	—	—	
					A	—	—	—	
S6	Y / G Output Black Level Range	Vari-able	80	80	SW2	SW6	SW7	SW8	(1) Same as (1) and (2) for S1 above. (2) Change the sub address (04) data from (80h) to (F0h) and measure the DC variation ΔVYB+ of the Y / G output (Pin 20) picture period. Also change the data from (80h) to (00h) and measure the DC variation ΔVYB−. (3) Change the sub address (04) data from (88h) to (F8h) and from (88h) to (08h), then measure ΔVYO+ and ΔVYO−.
					A	B	B	B	
					SW14	—	—	—	
					A	—	—	—	
S7	B-Y / B Output Black Level Range	80	80	Vari-able	SW2	SW6	SW7	SW8	(1) Same as (1) and (2) for S1 above. (2) Change the sub address (06) data from (80h) to (00h) and measure the DC variation ΔVBB+ of the B-Y / B output (Pin 21) picture period. Also change the data from (80h) to (F8h) and measure the DC variation ΔVBB−. (3) Change the sub address (04) data to (88h) and measure ΔVBO+ and ΔVBO− same as (2) above.
					A	B	B	B	
					SW14	—	—	—	
					A	—	—	—	
S8	R-Y / R Output Black Level Range	80	Vari-able	80	SW2	SW6	SW7	SW8	(1) Same as (1) and (2) for S1 above. (2) Change the sub address (05) data from (80h) to (00h) and measure the DC variation ΔVRB+ of the R-Y / R output (Pin 22) picture period. Also change the data from (80h) to (F8h) and measure the DC variation ΔVRB−. (3) Change the sub address (04) data to (88h) and measure ΔVRO+ and ΔVRO− same as (2) above.
					A	B	B	B	
					SW14	—	—	—	
					A	—	—	—	

(Unless otherwise specified, SYNC / SW V_{CC} = 9 V, DAC / C V_{CC} = 5 V, preset bus data, Ta = 25°C ± 3°C)

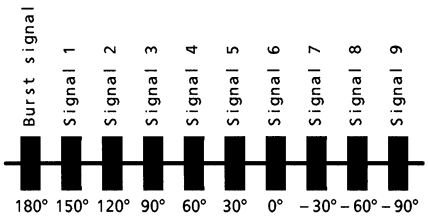
NOTE	CHARACTERISTIC	TEST CONDITION				
		SW MODE				TEST METHOD
		SW2	SW4	SW5	TP32	
D1	Horizontal Sync Phase	A	B	A	5V	(1) Input signal in the figure below from TG7 to Y2in. (2) Measure the pin 10 waveform phase difference Sph1 in relation to the TP8 waveform. (3) Set the sub address (05) D1 as 1 and measure Sph2 same as (1) above.
D2	Horizontal Blanking Start Phase Horizontal Blanking Pulse Width	A	B	A	5V	(1) Same as (1) for D1. (2) Measure phase differences HPs and HPw for pin 10 and pin 21, respectively
D3	Gate Pulse Start Phase Gate Pulse Width	A	B	A	5V	(1) Same as (1) for D1. (2) Measure the pin 15 waveform phase difference GPs in relation to the pin 10 waveform and measure pulse width GPw.
D4	Horizontal Blanking Pulse Start Phase Horizontal Blanking Pulse Width	A	B	A	5V	(1) Same as (1) for D1. (2) Measure HPs and HPw same as (2) for D3.
D5	HD Output Start Phase HD Output Pulse Width HD Output Amplitude	A	B	A	5V	(1) Same as (1) for D1. (2) Measure the pin 14 waveform phase difference HDs in relation to the pin 10 waveform and measure pulse width HDw and amplitude VHD.
D6	Vertical Blanking Pulse Start Phase Vertical Blanking Pulse Width	A	B	A	5V	(1) Input 50Hz CVBS signal to Y2in. (2) Measure the pin 15 waveform phase difference VP50s1 in relation to the pin 8 waveform and measure pulse width VP50s2. (3) Input 60Hz CVBS signal to Y2Yin. (4) Measure VP60s1 and VP60s2 same as (2) above.
D7	Vertical Pulse Width	A	B	A	5V	(1) Input 60Hz CVBS signal to Y2in. (2) Measure the delay Td of the pin 13 vertical pulse in relation to the pin 8 vertical signal and measure the pulse width Tw.

(Unless otherwise specified, SYNC / SW V_{CC} = 9 V, DAC / C V_{CC} = 5 V, preset bus data, Ta = 25°C ± 3°C)

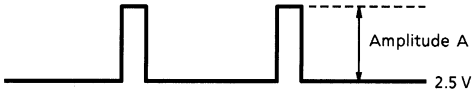
NOTE	CHARACTERISTIC	TEST CONDITION				
		SW MODE				TEST METHOD
		SW2	SW4	SW5	TP32	
D8	Vertical Pull-In Range (1)	A	B	A	5V	(1) Input 50 Hz CVBS signal to Y2in. (2) Change the input signal vertical frequency in 0.5 H steps and measure the pull-in ranges fPL1 and fPH1. (3) Set the sub address (04) D2 / D1 / D0 to (100) and measure fPL2 and fPH2 same as in (2). (4) Input 60 Hz CVBS signal to Y2in and set the sub address (04) D2 / D1 / D0 to (001). (5) Change the input signal vertical frequency in 0.5 H steps and measure the pull-in ranges fPL3 and fPH3. (6) Set the sub address (04) D2 / D1 / D0 to (101) and measure fPL4 and fPH4 same as (5).
	Vertical Pull-In Range (2)					
	Vertical Pull-In Range (3)					
	Vertical Pull-In Range (4)					

TEST SIGNALS

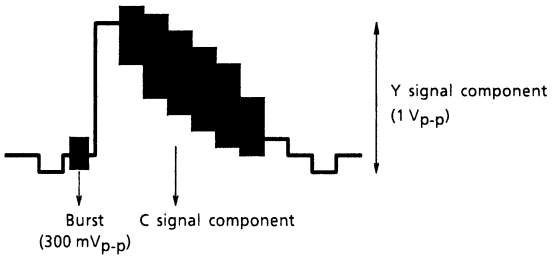
1) Signal 1 (Rainbow signal)



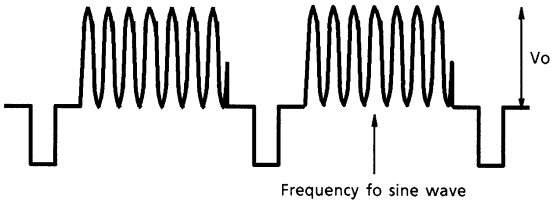
2) Signal 2



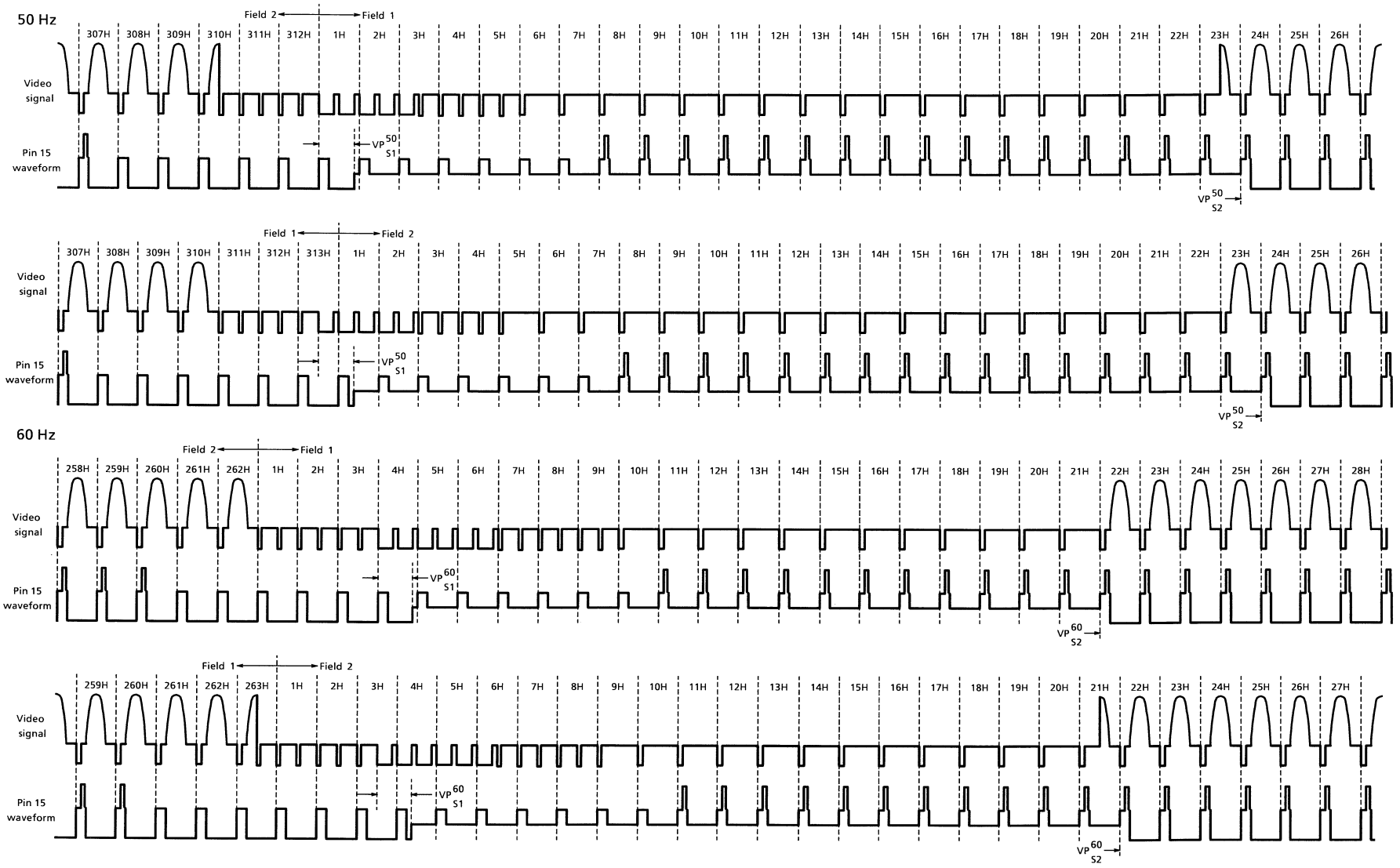
3) Signal 3



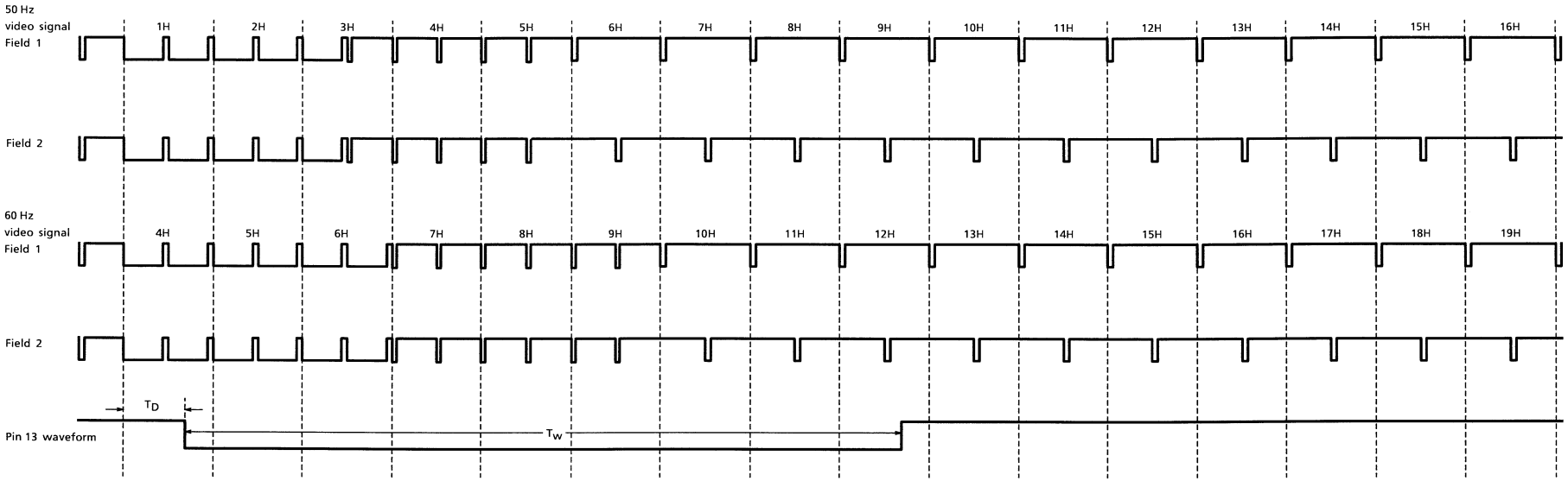
4) Signal 4



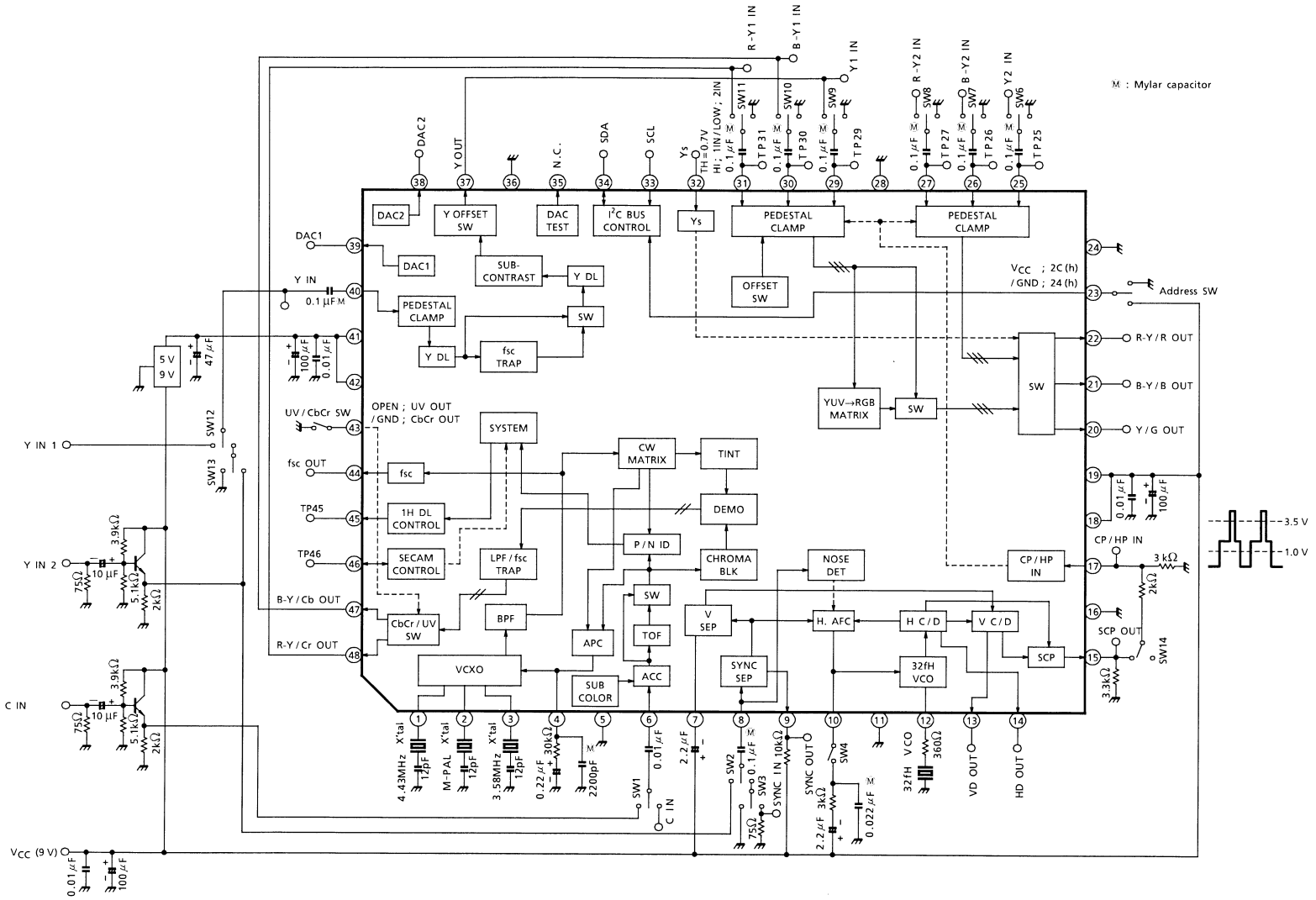
(Note D6) VERTICAL BLANKING PULSE



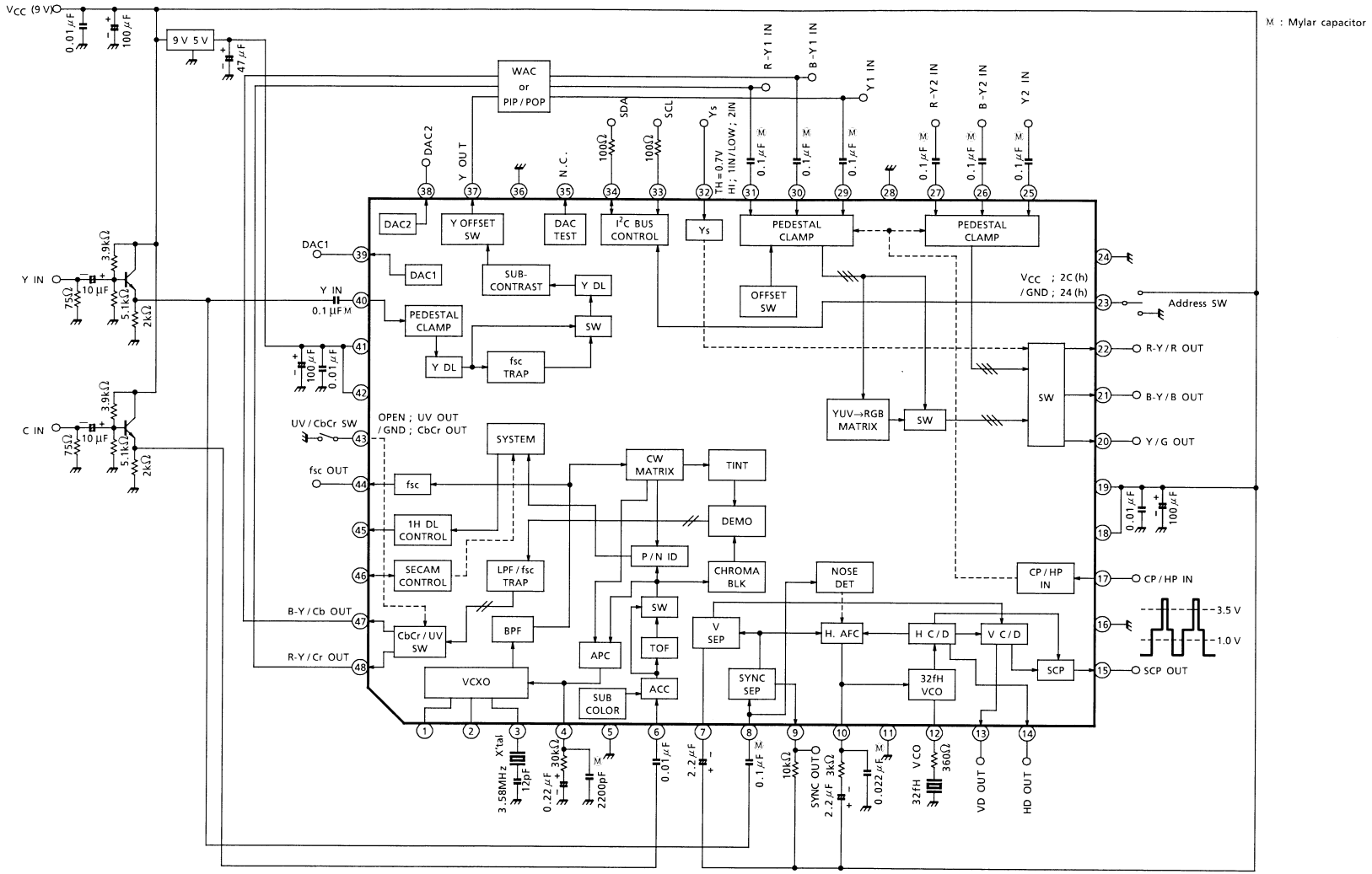
(Note D6) VERTICAL OUTPUT PULSE WIDTH



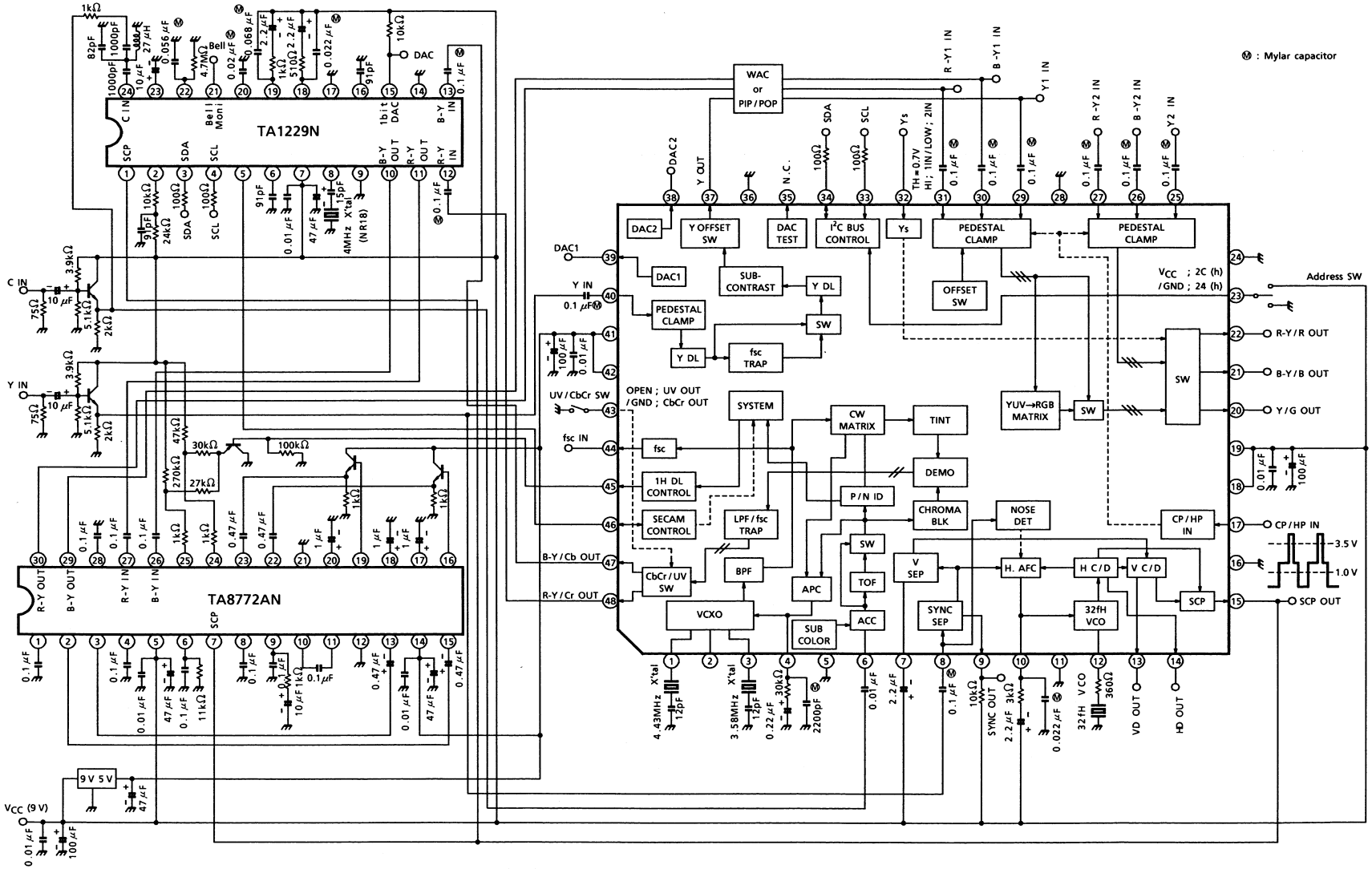
TEST CIRCUIT



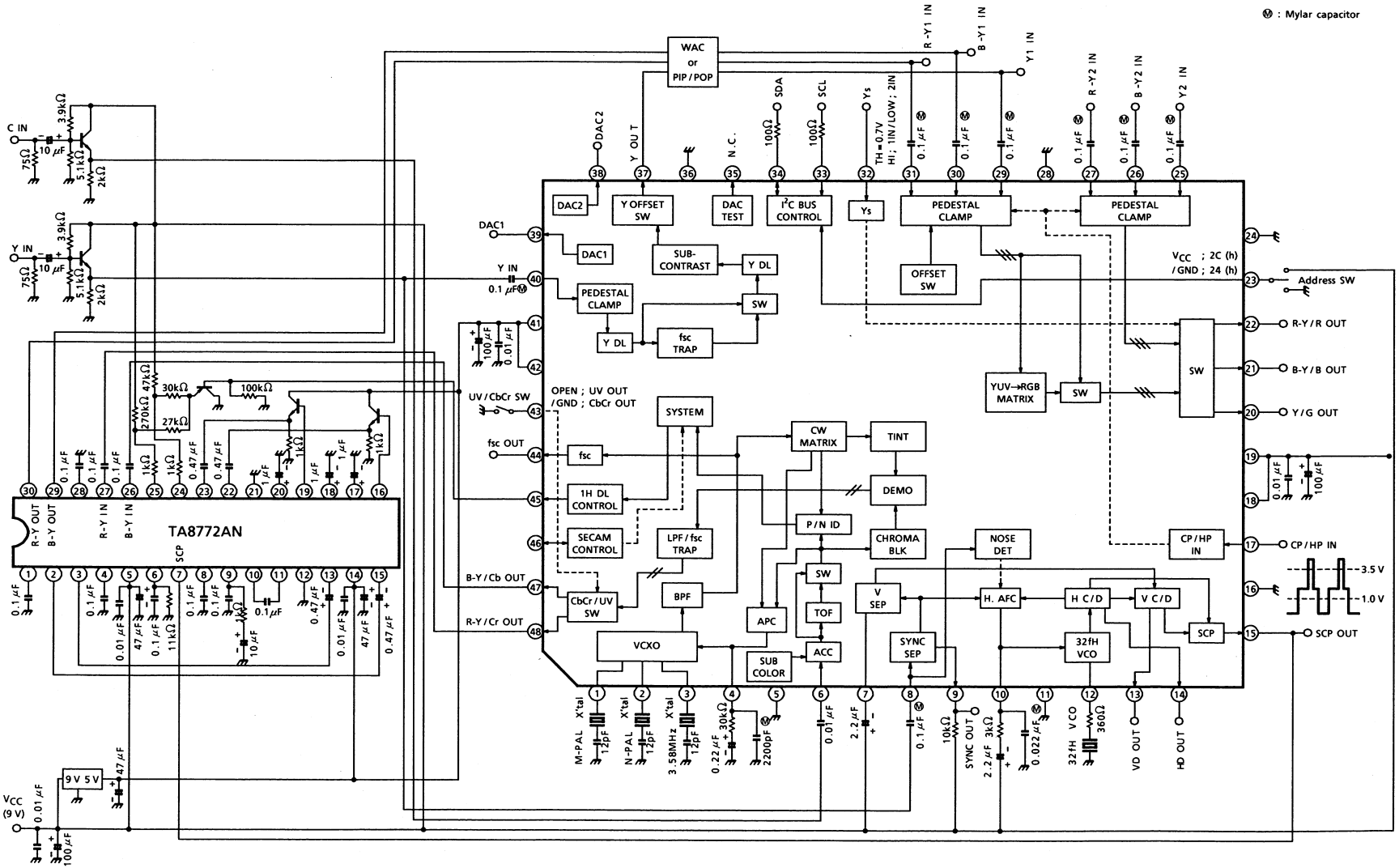
APPLICATION CIRCUIT 1 (NTSC)



APPLICATION CIRCUIT 2 (MULTI)

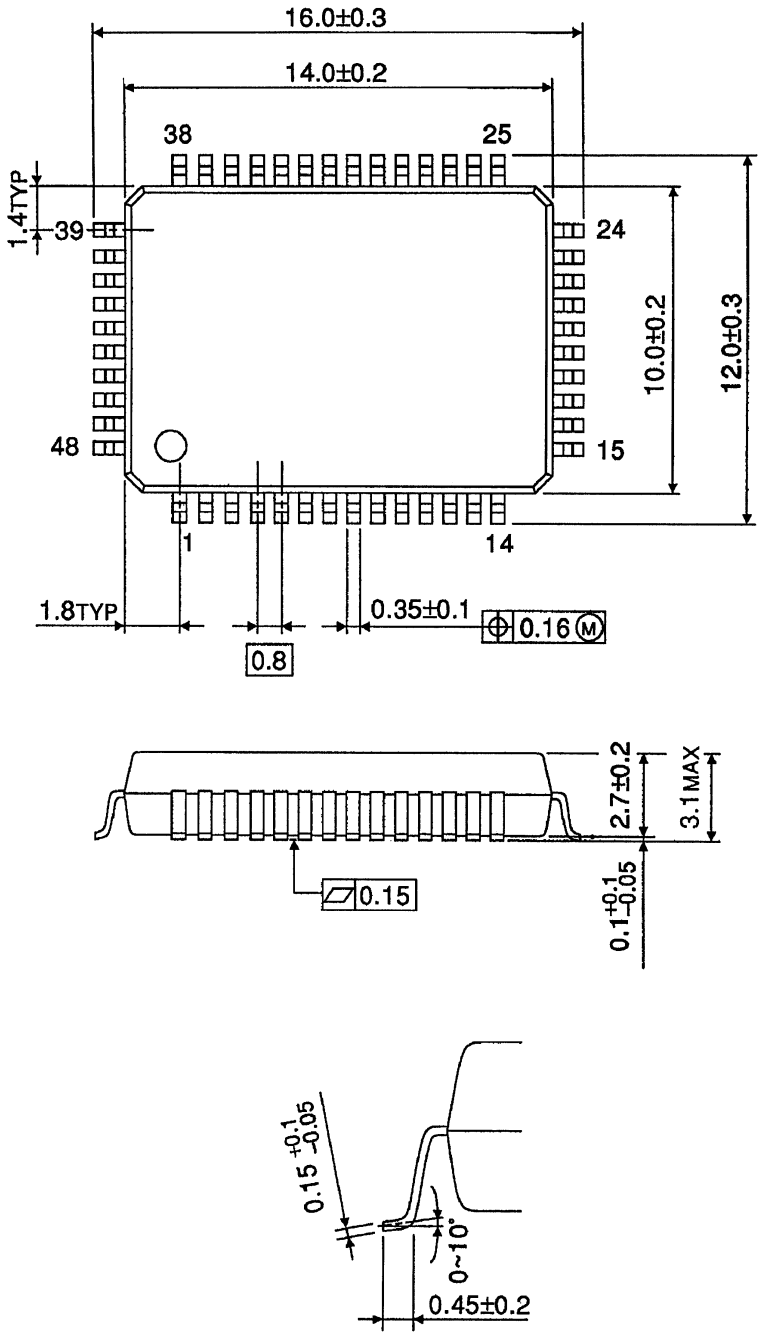


APPLICATION CIRCUIT 3 (South America)



PACKAGE DIMENSIONS

QFP48-P-1014-0.80 Unit: mm



Weight: 0.83g (Typ.)

About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-63Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

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030619EBA

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