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F75909

SMBus Level Shifter

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Release Date: Dec, 2011
Version: V0.11P

F75909 Datasheet Revision History

Version	Date	Page	Revision History
Data Brief	2011/10	-	Data Brief
V0.10P	2011/11	-	Made Clarification and Correction Add Application Circuit
V0.11P	2011/12	-	Add Electrical Characteristics
V0.12P	2011/12	--	Update Block Diagram / Application Circuit

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1 General Description

The F75909 is a I^2C-bus/SMBus level shifter that translating signal voltage level of standard I^2C-bus or SMBus. Port L allows a operating voltage range from 1.0 V to [$V_{CC(H)}$ -1.0 V]. The operating voltage of Port H is range from 3.0 V to 5.5 V. When F75909 is disabled, both port L and port H I/O pins are high-impedance.

The bus port H are compliant with SMBus I/O levels, while port L uses a current sensing mechanism to detect the input or output LOW signal which prevents bus lock-up. Port L uses a 1 mA current source for pull-up and a 200 . pull-down driver. This results in a LOW on the port L accommodating smaller voltage swings. The output pull-down on the port L internal buffer LOW is set for approximately 0.2 V, while the input threshold of the internal buffer is set about 50 mV lower than that of the output voltage LOW. When the port L I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the port H drives a hard LOW and the input level is set at 0.3 of SMBus or I^2C-bus voltage level which enables port H to connect to any other I^2C-bus devices or buffer.

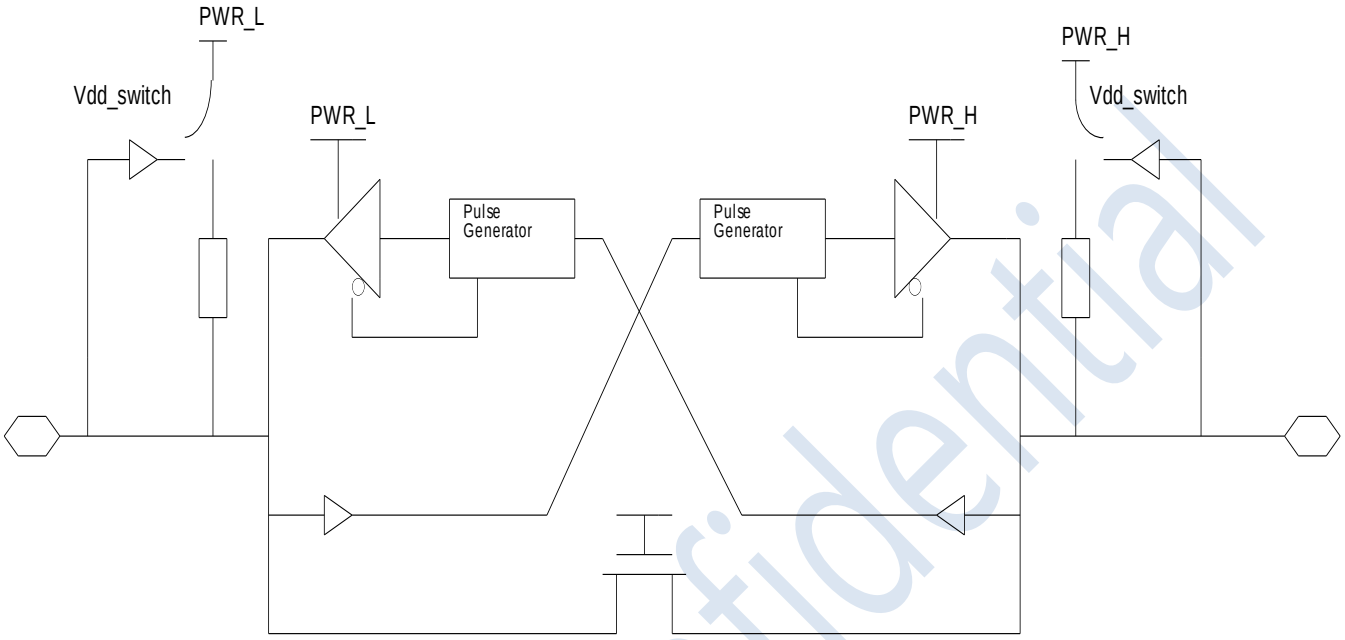
The F75909 is not enabled unless $V_{CC(L)}$ is above 0.8 V and $V_{CC(H)}$ is above 2.5 V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.

2 Feature List

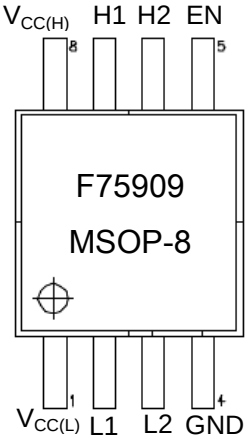
- Voltage level shifting from L-Port (1V to Vcc(H) -1.0V)
- No external pull-up resistors required on Port L
- Open-drain I/O
- Lock-up free operation
- High impedance bus pin when Power-off.

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3 Block Diagram



4 Pin Configuration



Pin Configuration of F75909

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5 Pin Description

IN - input pin with schmitt trigger.
OUT - Open-drain output pin
P -Power.

4.1. Pin Description

Pin No.	Pin Name	Type	Description
1	VCC (L)	P	Port L power supply
2	L1	Analog	Port L1 (lower voltage side)
3	L2	Analog	Port L2 (lower voltage side)
4	GND	Ground	Ground
5	EN	IN	Enable input
6	H2	Analog	Port H1 (I/O signal input Side)
7	H1	Analog	Port H2 (I/O signal input Side)
8	VCC (H)	P	Port H power supply

7 Electrical Characteristics

Limiting Values

In accordance with the Absolute Maximum Rating System

Symbol	Parameter	Conditions	Min	Max	Unit
$Vcc_{(H)}$	Supply voltage port High side		-0.5	+5.5	V
$Vcc_{(L)}$	Supply voltage port Low side		-0.5	+5.5	V
$V_{I/O}$	Voltage on an input/output pin	Port low side, enable pin (EN)	-0.5	+3.6	V
		Port high side;	-0.5	+5	V
I_O	output current			16	mA
P_{tot}	Total power dissipation				mW
T_{stg}	Storage temperature		-55	145	℃
T_{amb}	Ambient temperature	Operating in free air	0	70	℃

Static Characteristics

GND=0V; T_{amb}=-40℃ to +85℃; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ*1	Max	Unit
Supplies						
$Vcc_{(H)}$	Supply voltage port High side		2.5		3.6	V
$Vcc_{(L)}$	Supply voltage port Low side		1		$Vcc_{(B)}$	V
$Icc_{(L)}$	Supply current port Low side	All port low side static High				mA
		All port low side static Low				mA

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$Icc_{(H)}$	Supply current port High side	All port High side static High				mA
Input and output of port Low side (L1 to L2)						
V_{IH}	High-level input voltage	Port Low side	0.7 $Vcc_{(L)}$		$Vcc_{(L)}$	V
V_{IL}	Low-level input voltage	Port Low side	-0.5		0.3 $Vcc_{(L)}$	V
I_{IH}	Input leakage current	V_I=$Vcc_{(L)}$			1	uA
I_{IL}	Low-level input current					mA
I_{LOH}	output High leakage current	V_O=1.1V			15	uA
C_{iO}	Input/output capacitance			5		pF
Input and output of port High side (H1 to H2)						
V_{IH}	High-level input voltage	Port H	0.7 $Vcc_{(H)}$		5	V
V_{IL}	Low-level input voltage	Port H	-0.5		0.3 $Vcc_{(H)}$	V
I_{IH}	Input leakage current	V_I=3.6V			1	uA
I_{IL}	Low-level input current	V_I=0.2V			1	uA
I_{LOH}	output High leakage current	V_O=3.6V			120	uA
C_{iO}	Input/output capacitance			5		pF
Enable						
V_{IH}	Low-level input voltage		0.7 $Vcc_{(L)}$		$Vcc_{(H)}$	V
V_{IL}	High-level input voltage		-0.5		0.3 $Vcc_{(L)}$	V
I_{IH}	Low-level input current				1	uA
I_{IL}	Input leakage current				1	uA
C_i	Input capacitance	V_I=3.6V or 0V		4		pF

*1 Typical values with $Vcc_{(A)}$=1.1V, $Vcc_{(B)}$=3.3V

Dynamic Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Vcc_{(A)}$ = 1.1V ; $Vcc_{(B)}$ = 3.3V						
t_{PLH}	Low to High propagation delay	Port H to port L	*1	1.2		ns
t_{PHL}	High to Low propagation delay	Port H to port L	*1	4.9		ns
t_{TLH}	Low to High output transition time	Port L	*1	2.3		ns
t_{THL}	High to Low output transition time	Port L	*1	1.5		ns
t_{PLH}	Low to High propagation delay	Port L to port H	*1	4.8		ns
t_{PLH2}	Low to High propagation delay 2	Port L to port H; measured from the 50% of initial Low on port L to 1.5V rising on port H	*1			ns
t_{PHL}	High to Low propagation delay	Port L to port H	*1	3.8		ns
t_{TLH}	Low to High propagation delay	Port H	*1*2	2.4		
t_{THL}	High to Low output transition time	Port H	*1	3.9		ns
t_{su}	Set-up time	EN High before Start condition		2.7		ns
t_h	Hold time	En High after Stop condition		2.7		ns
$Vcc_{(A)}$ = 1.9V ; $Vcc_{(B)}$ = 5.0V						
t_{PLH}	Low to High propagation delay	Port H to port L	*1	1		ns
t_{PHL}	High to Low propagation delay	Port H to port L	*1	4.4		ns
t_{TLH}	Low to High output transition time	Port L	*1	2		ns
t_{THL}	High to Low output transition time	Port L	*1	2		ns
t_{PLH}	Low to High propagation delay	Port L to port H	*1	2.5		ns

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t_{PLH2}	Low to High propagation delay 2	Port L to port H; measured from the 50% of initial Low on port L to 1.5V rising on port H	*1			ns
t_{PHL}	High to Low propagation delay	Port L to port H	*1	1.8		ns
t_{TLH}	Low to High propagation delay	Port H	*1*2	2.5		
t_{THL}	High to Low output transition time	Port H	*1	2.7		ns
t_{su}	Set-up time	EN High before Start condition				ns
t_h	Hold time	En High after Stop condition				ns

*1 Load capacitance = 50 pF; load resistance on port B =1.35 kΩ.
*2 Value is determined by RC time constant of bus line.

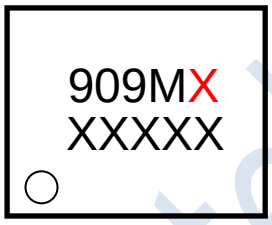
8 Ordering Information

Part Number	Package Type	Production Flow
F75909M	MSOP-8	Commercial, 0°C to +70°C

9 Top Marking Specification

The version identification is shown as the bold red characters. Please refer to below for detail:

MSOP-8



1st Line: Device Name + **IC Version (X)**

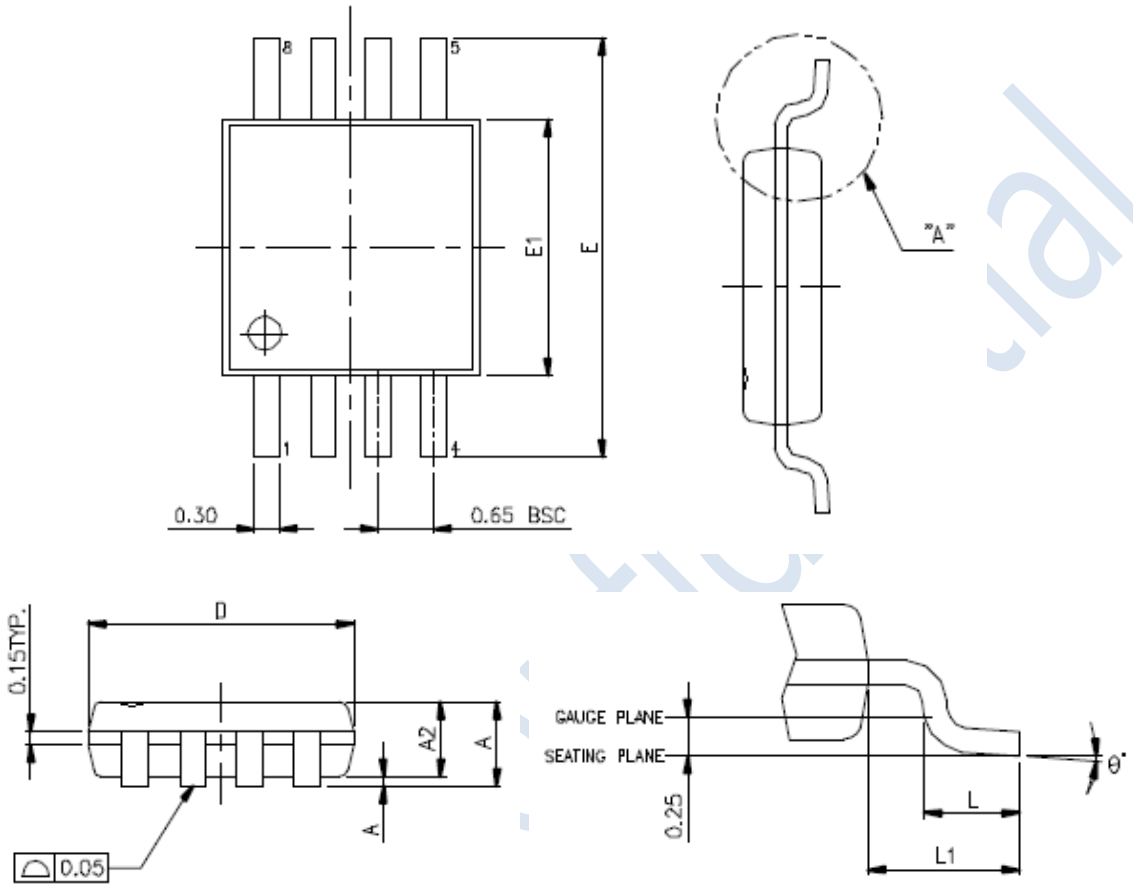
2nd Line: Assembly Code (X)+Date code(XXX)+Trace Code(X)

◯ : Pin 1 Identifier

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10 Package Spec.

MSOP-8 Package

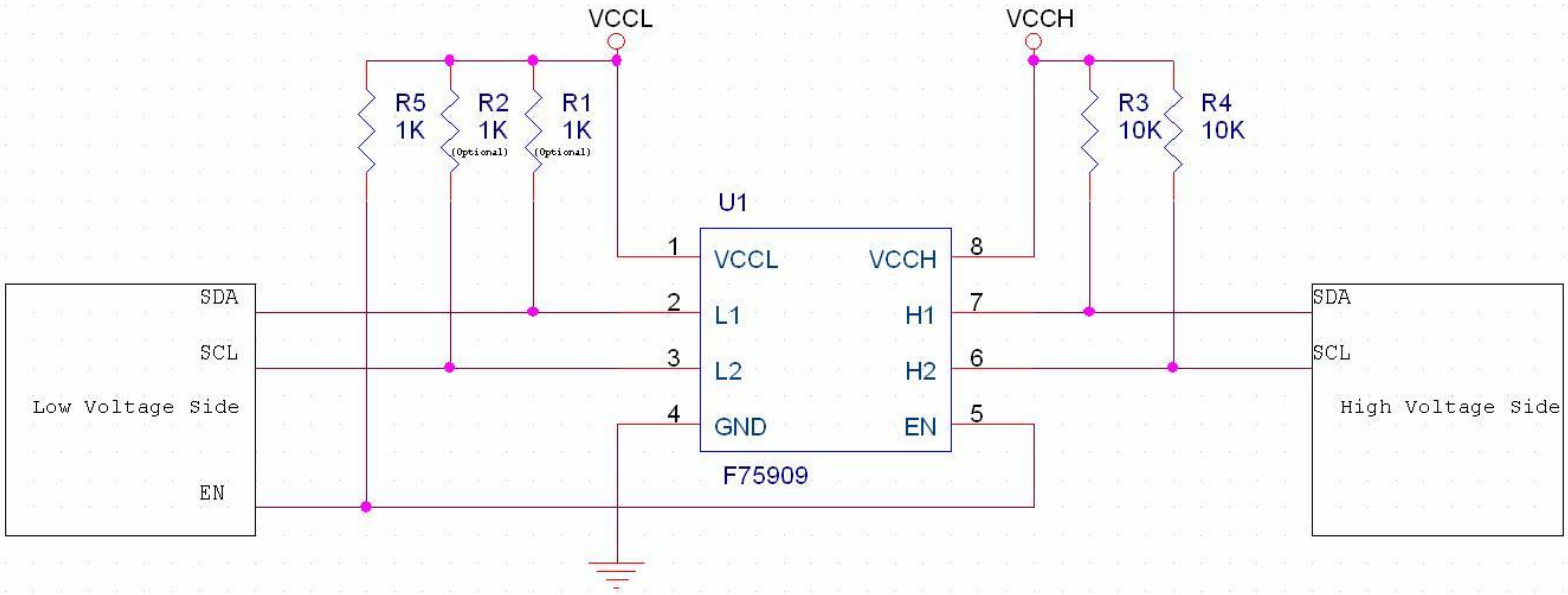


SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.10
A1	0.00	–	0.15
A2	0.75	0.85	0.95
D		3.00 BSC	
E		4.90 BSC	
E1		3.00 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
θ°	0	–	8

UNIT : MM

NOTES:
1.JEDEC OUTLINE : MO-187 AA
2.DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3.DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4.DIMENSION "0.22" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "0.22" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPAC BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5.DIMENSIONS "b" AND "E1" TO BE DETERMINED AT DATUM PLANE H .

11 Application Circuit



**Optional: If the master device has the loading, 1KΩ should be added.

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